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Adaptive Stabilization and Dynamic Performance Preservation of Cascaded DC-DC Systems by Incorporating Low Pass Filters

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Abstract: This paper proposes a method to stabilize and enhance the dynamic performance of a cascaded DC-DC system by adaptively reshaping the source output impedance. The method aims to reduce the ratio of the source output impedance to the load input impedance, referred to as the minor loop gain, to eliminate the interaction between the load and the source systems. This interaction can deteriorate the dynamic performance or might lead to instability. Thus, the bus current is used to improve the dynamic performance by reducing the magnitude of the source's output impedance adaptively according to the loading condition such that the dynamic performance is consistently improved. Utilizing the bus current facilitates the compatibility between the proposed controller and most widely used DC-DC converters controlled in voltage mode, including non-minimum phase converters. In addition to the flexibility the bus current provides to embed the proposed solution with conventional control schemes. Experimental results have validated the effectiveness of the proposed controller along with time-based simulation and theoretical analysis, for minimum and non-minimum phase converters.

Keywords: adaptive reshaping, cascaded systems, constant power load (CPL), dynamic performance improvement, loaded loop gain, minimum-phase converters, negative impedance, non-minimum phase converters, output Impedance

1. Introduction

Cascaded DC-DC systems have been widely used in aerospace, maritime, and automobile industries due to their attractive features such as modularity, scalability, high power density, and high reliability [1]. They provide a flexible environment to efficiently integrate renewable energy resources with the existing power systems [2,3]. Typically, a cascaded system consists of a line regulating converter (LRC) [4], which acts as the source, connected in series with a load subsystem, as shown in Figure 1. The load system might consist of DC-DC converters, inverters, or a combination connected in parallel [5]. Since most load converter modules are tightly regulated and supply a load with one-to-one characteristic of voltage-to-current or speed-to-torque relationships [6,7], these modules act as constant power loads (CPL). CPLs exhibit a negative incremental impedance seen by the LRC [8]. This characteristic is notorious for degrading the dynamic performance of cascaded systems and might lead to instability [9].

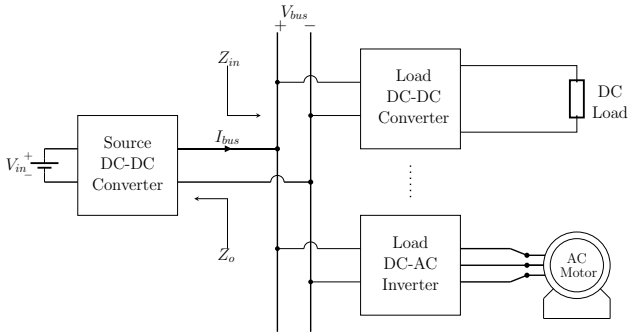

Figure 1. Cascaded DC-DC system.

Assessing the stability and the dynamic performance of cascaded DC-DC systems was initiated by R.D. Middlebrook in 1976, who studied the impact of the input filters on the stability and on the performance of regulated DC-DC converters [8]. His study resulted in the Middlebrook criterion, which ensures the stability and performance of cascaded systems. It is based on relating the ratio of the source output impedance to the load input impedance, which is called the minor loop gain ($T_m(s) = Z_o(s)/Z_{in}(s)$) in Figure 1), to system stability properties. The criterion is deemed to be very conservative [3], and requires infinite phase margin. Consequently, high capacitance is needed at the DC bus to achieve the required phase margin. Those requirements are impractical because they reduce the power density of cascaded systems, which is not desirable for most applications. To relax the conservativeness imposed by the Middlebrook criterion, other criteria have been proposed in the literature such as the Gain Margin Phase Margin (GMPM) [10], the Opposing Argument [11], and Energy Source Analysis Consortium (ESAC) [12], which in various ways confine the polar plot of T_m in a specific region of the complex plane to guarantee acceptable dynamic performance [2,13]. All these criteria assume that the load and the source converters are standalone stable. The Three-Steps criterion was introduced in [14] to assess the stability of cascaded systems even if the source converter was standalone unstable. In addition, the Passivity-Based criterion was introduced in [15] to further relax the artificial conservativeness of designing cascaded systems. It examines the stability of a cascaded system by injecting current into the DC bus to determine the passivity of the bus impedance. Bus impedance passivity would ensure stability. All of the above mentioned criteria provide sufficient conditions to ensure stability or dynamic performance, so their violation does not necessarily mean instability.

It is desirable to implement the system of Figure 1 in a modular and scalable manner, such that it can host various load and source subsystems from different vendors [2]. However, these miscellaneous components have different dynamic properties and ensuring stability with satisfactory performance of such an assorted system is a challenging task. Hence, passive damping methods have been proposed to preserve the stability and to improve the dynamic performance of such a system. Using passive components to damp out system oscillations incurs inevitable power loss that reduces the overall efficiency. In addition, passive damping reduces the power density of the system by including bulky passive components.

Active damping methods were introduced to overcome the passive damping disadvantages [1,9,16]. In this approach, stability is ensured by modifying the control loop of the LRC or the load system. However, in the existing active damping methods, little attention has been given to preservation or improvement of system dynamic behavior, and it is typically compromised in favor of ensuring system stability. The existing solutions for enhancing the dynamic performance are either applicable to a single load converter, or limited to a particular configuration of source (LRC) DC-DC converter. In [17], the stability of the system has been exclusively ensured for buck converters, as the LRC, via adding extra feedback loops to modify the inductor's series resistance. Although the system stability is guaranteed, the dynamic performance of the system is not improved because the system dynamics are

changed while the controller has not been modified to accommodate that. In [18], the Middlebrook criterion was partially fulfilled; the stability condition has been met by inserting a virtual resistance in series with the load via feeding back the bus current into the controller. The performance requirement of the Middlebrook criterion was neglected. Moreover, a second controller is required to compensate for the voltage drop across the DC bus, which may introduce other stability and performance issues. In [19], the magnitude or the phase of the load's input impedance is modified to prevent the interaction between the load and the source subsystems where the impedance overlap occurs using a band pass filter based on a method in [20]. It is achieved by inserting a virtual resistance either in series or in parallel with the load subsystem. The relative stability margins will be affected in that region, while the solution requires modifications for every converter that would be connected as a load.

In [21], an adaptive virtual capacitor connected to the DC bus is proposed to stabilize the system; the solution results in power density reduction because the virtual capacitor is implemented using an additional auxiliary converter, making it less desirable for density-sensitive applications. In reference [22], a method to improve the dynamic performance of a cascaded system that consists of a single DC-DC converter as the load was introduced. The proposed solution cannot handle multiple load converters operating in parallel. The authors of reference [23] proposed a method to design both source and load controllers simultaneously, such that their interaction is minimized. Similar to [22], the proposed method is solely valid for a single load DC-DC converter. The vast majority of the above mentioned active damping methods were introduced, and tested to stabilize minimum phase converters, e.g., buck converters, while the non-minimum phase converters have not received much attention in this sense.

To devise a method for ensuring stability and performance of cascaded DC-DC systems with multiple loads and to address the discussed issues, we propose a method that reshapes the output impedance of the LRC to stabilize the system and improve its dynamic performance. The proposed method is applicable to minimum and non-minimum phase converters, and it neither incurs additional power losses nor changes the LRC controller parameters. Additionally, it is applicable to linearized feedback control schemes, without changing the controller parameters. The method is based on adaptively reducing the magnitude of the source output impedance by feeding back the average value of the bus current. Consequently, the output impedance is reduced depending on the loading condition. Reducing the output impedance helps eliminate the interaction between load and source systems, and effectively decouples these two.

This paper first discusses the stability and performance issues of cascaded systems in Section 2. Then the proposed controller is explained in Section 3. The compatibility of the proposed controller with minimum and non-minimum phase converters is discussed in Sections 4 and 5, respectively. Finally, the conclusions are drawn in Section 6.

2. Stability and Performance of Cascaded DC-DC Systems

The stability and performance of cascaded DC-DC systems are deteriorated by the incremental negative impedance exhibited by the load subsystem. The negative impedance appears to be due to the active nature of the load subsystem, which tightly regulates its output voltage while delivering a constant amount of power despite the variation in the input voltage. The mathematical derivation of the negative input impedance [24,25], is

$$r = \frac{\partial V_{bus}}{\partial I_{bus}} = \frac{\partial}{\partial I_{bus}}\left(\frac{P_{bus}}{I_{bus}}\right) = -\frac{P_{bus}}{I_{bus}^2} = -\frac{V_{bus}}{I_{bus}} \quad (1)$$

where r is the load low frequency impedance, V_{bus} is the DC bus voltage, and I_{bus} is the DC bus current. Equation (1) can be related to the bus voltage and output power of each load converter (P_{oi}), assuming lossless converters [26], as

$$r = -\frac{V_{bus}^2}{\sum_1^n P_{oi}} \quad (2)$$

where n is the number of loads. Equations (1) and (2) are valid for the frequencies that are less than the cut-off frequency of the load converter (ω_c) [8], where the impedance is $|r|\angle 180°$. Beyond ω_c, the load input impedance resembles an inductor impedance. Typical plots of the source output impedance Z_o and the load input impedance Z_{in} are shown in Figure 2, [13,24,27]. The proposed stabilization method depends on the maximum frequency ($\omega_{i,max}$) of the interaction region, as illustrated in Figure 2.

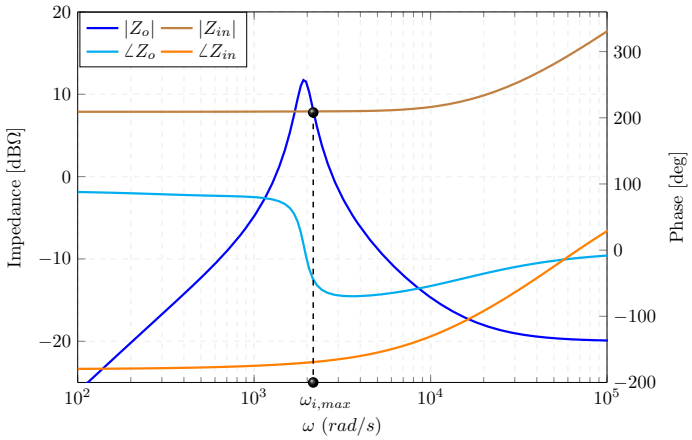

Figure 2. Typical source and load impedances of Figure 1, highlighting their interaction around $\omega_{i,max}$.

The roles of Z_o and Z_{in} in assessing the stability of cascaded systems can be visualized using the characteristic equation of distributed DC systems [10,27] as

$$\frac{v_{o,i}}{v_{in}} = \frac{G_{vds} G_{vdl,i}}{1 + T_m} \tag{3}$$

where $v_{o,i}$ is the ith load output voltage, v_{in} is the source converter input voltage, G_{vds} is the source converter control to output transfer function, and $G_{vdl,i}$ is the ith load converter control to output transfer function. For multiple loads, the input impedance of the load system is the parallel combination of each load module input impedance, i.e., $Z_{in} = Z_{i1} \parallel Z_{i2} \parallel Z_{i3} \parallel \cdots$.

To determine stability properties of the cascaded system, Nyquist criterion is used [13,16]. Stability is preserved if the polar plot of $T_m(s)$ does not encircle $(-1, j0)$. An impedance overlap in the low-frequency region ($\omega < \omega_c$) implies $|T_m| \geq 1$ and $\angle T_m(s) > 180°$, consequently the polar plot of $T_m(s)$ will encircle $(-1, j0)$.

Source and load subsystems interaction alters the dynamic performance of the overall system. As a result of this interaction, the source control loop gain (T_s) is altered [28,29] as

$$T_s^L = \frac{T_s}{1 + \underbrace{\frac{Z_o}{Z_{in}}}_{T_m}(1 + T_s)} \tag{4}$$

where T_s and T_s^L are the original and load affected control loop gain of the LRC, respectively. The LRC dynamic performance stays intact from the loading effect iff $Z_o \ll 1$, consequently $T_s^L \approx T_s$ in Equation (4). Moreover, if T_m encircles $(-1, j0)$, so does T_s^L [16,29]. On the other hand, the dynamic performance of the load is degraded by the source according to

$$T_L^S = T_L \frac{1 + T_m}{1 + \frac{Z_o}{Z_{in\_o}}} \tag{5}$$

where Z_{in_o} is the open-loop input impedance impedance of the load converter, T_L is the load converter control loop gain, and T_L^S is source affected control loop gain of the load. Similarly, the load dynamic performance will be preserved iff $Z_o \ll 1$, which implies $T_L^S \approx T_L$ in Equation (5). Since reducing Z_o helps decouple the dynamics of source and load systems, we propose to reduce the magnitude of the source output impedance based on

$$Z_o^{new} = \frac{Z_o}{1+\rho} \quad \rho > 0 \tag{6}$$

where ρ is a positive constant. Having $(1+\rho)$ as the divisor is justified in the next section. Using Equation (6) the minor loop gain can be re-expressed as

$$T_m = \frac{Z_o}{(1+\rho)Z_{in}} \tag{7}$$

Increasing ρ reduces the magnitude of Z_o^{new}, and consequently reduces $|T_m|$, which implies $T_s^L \approx T_s$ and $T_L^S \approx T_L$. Thus the source and the load systems are decoupled, and the Middlebrook criterion of ensuring stability and preserving the dynamic performance is satisfied without artificial conservativeness.

3. The Controller Design

The proposed controller aims to adaptively stabilize and preserve the dynamic performance of cascaded DC-DC converters without changing the LRC controller parameters. To do so, T_s must stay intact from the loading effect as discussed earlier, and Z_o must be reshaped adaptively according to the load conditions. In addition, the closed-loop transfer function of reference voltage to output voltage $(\widetilde{v}_o/\widetilde{v}_{ref})$ should stay as $(T_s/(1+T_s))$.

In references [30,31], a controller that preserves $(\widetilde{v}_o/\widetilde{v}_{ref})$ relationship, and reshapes the output impedance of single phase inverters or multi-input-dual-active-bridge DC-DC converters was introduced, as shown in Figure 3. We propose modifications to this controller such that the output impedance is adaptively shaped according to Equation (6). The small-signal output voltage $(\widetilde{v}_o)$ of a DC-DC converter equipped with the controller of Figure 3 is expressed as

$$\widetilde{v}_o = \widetilde{v}_{ref}\frac{T_s}{1+T_s} - \widetilde{i}_o\frac{Z_{o\_o}}{1+HG_{vd}G_{PWM}} + \widetilde{v}_g\frac{G_{vg}}{(1+T_s)(1+HG_{vd}G_{PWM})} \tag{8}$$

where $\widetilde{i}_o$, $\widetilde{v}_g$ are the variations in the output current and input voltage, respectively. The coefficient H is used to shape Z_o, G_{vg} is the input to output transfer function, $T_s = G_cG_{vd}G_{PWM}$, G_c is the original controller, Z_{o_o} is the open loop output impedance of the source, and $Z_o = Z_{o\_o}/(1+T_s)$. G_{PWM} is assumed unity hereinafter, for the sake of simplicity.

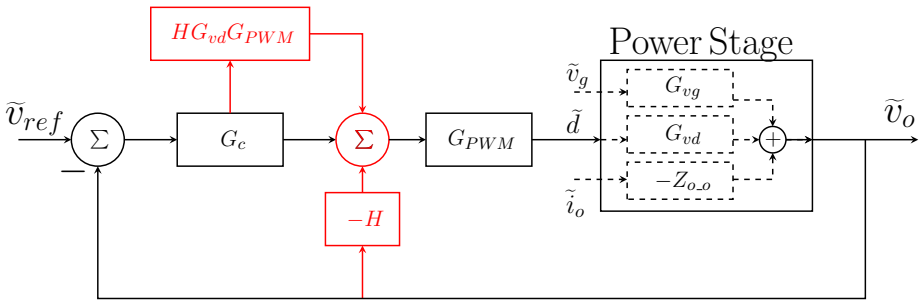

Figure 3. Closed-loop LRC using the proposed modifications in [30,31], where their additions to the original control are highlighted in red.

3.1. The Proposed Reshaping

To achieve the proposed reshaping of the output impedance according to Equation (6), the denominator $1 + HG_{vd}$ in Equation (8) should equal $1 + \rho$ [32]. Choosing H to be ρG_{vd}^{-1} is an obvious option, yet it is a non-realizable choice. G_{vd} is a strictly proper transfer function for DC-DC converters. Thus, G_{vd}^{-1} yields more zeros than poles, emulating an anticipatory system. We propose to realize G_{vd}^{-1} in a certain frequency range using the transfer function of a low pass filter with unity DC gain

$$G_{LPF} = \frac{\omega_x^p}{(s + \omega_x)^p} \tag{9}$$

where ω_x is the corner frequency in rad/s, and p specifies the order of the filter. G_{vd}^{-1} is practically realized as

$$G_R = G_{vd}^{-1} \frac{\omega_x^p}{(s + \omega_x)^p} \tag{10}$$

The coefficient p depends on LRC control-to-output transfer function and is selected such that Equation (10) is always realizable for DC-DC converters. Thus, Equation (6) is achieved by setting H equals to

$$H = \rho G_R \tag{11}$$

Consequently, $(1 + HG_{vd})$ in Equation (8) can be interpreted as $(1 + \rho)\ \forall\ \omega \leq \omega_x$. Hence, Z_o^{new} in Equation (6) can be practically realized as a function of ρ as

$$\begin{aligned} Z_p(\rho) &= \frac{Z_o}{1 + \rho G_R G_{vd}} \\ &= \frac{Z_o}{1 + \rho} \quad \forall\ \omega < \omega_x \end{aligned} \tag{12}$$

where $Z_p(\rho)$ is the output impedance of the LRC corresponding to the proposed controller, referred as the proposed output impedance hereinafter. $Z_p(\rho)$ does not require any change to the controller parameter while the desired response of $\widetilde{v}_o/\widetilde{v}_{ref}$ and the dynamic performance are preserved. In addition, it is applicable to linearized feedback control configuration, not limited to PI controllers only as in [30] or a specific converter as in [20]. The final shape of the source converter output impedance using (12) compared to Z_o, which corresponds to the original controller, is shown in Figure 4, where $\omega_x = 1 \times 10^5$ rad/s. Ultimately, substituting Equation (12) into Equation (8) expresses the output voltage of a DC-DC converter that utilizes the controller with the proposed modifications as

$$\widetilde{v}_o = \widetilde{v}_{ref} \frac{T_s}{1 + T_s} - \widetilde{i}_o \frac{Z_o}{1 + \rho} + \widetilde{v}_g \frac{G_{vg}}{(1 + T_s)(1 + HG_{vd})}\ \omega < \omega_x \tag{13}$$

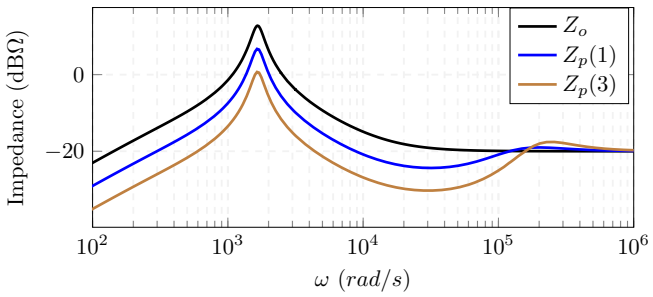

Figure 4. Reshaping of source output impedance, where Z_o represents that of the original controller, and $Z_p(\rho)$ is the reshaped impedance for the proposed controller with $\rho = 1, 3$ in equation (12) and $\omega_x = 1 \times 10^5$ rad/s.

3.2. The Adaptivity

Evidently, any $\rho > 0$ in Equation (12) will reduce the output impedance of the LRC. To make the proposed technique adaptive to load changes, we propose to use the average bus current

$$I_{bus} = \frac{1}{V_{bus}}(P_{o1} + P_{o2} + P_{o3} + ...) \tag{14}$$

in Equation (12) such that $\rho = I_{bus}$. The bus current is used because it makes the proposed control adaptive to load changes. In addition, it equips the controller with the flexibility required to integrate it with minimum and non-minimum phase DC-DC converters. Thus, replacing ρ by I_{bus} in Equation (12) reduces $Z_p(\rho)$ adaptively by a factor of $(1 + I_{bus})$ at various loading conditions. Figure 5 shows the practical implementation of the proposed controller.

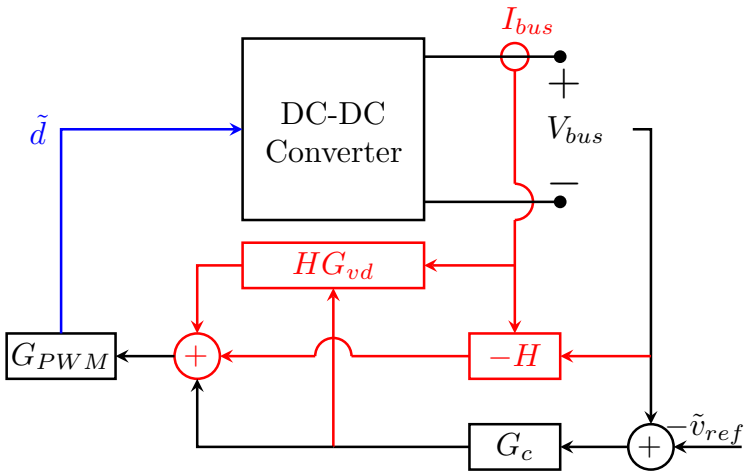

Figure 5. The proposed controller for the line regulating converter, where modifications to original controller are highlighted in red.

3.3. Determining the Low Pass Filter Corner Frequency

Selecting ω_x is vital in successfully implementing the proposed controller. The interaction between the source and the load subsystems tends to occur around the LRC peak output impedance [13,16,24]. Thus, ω_x should be selected as

$$\omega_x > \omega_{i,max} \tag{15}$$

where $\omega_{i,max}$ is shown in Figure 2. Selecting $\omega_x < \omega_{i,max}$ will neither stabilize the system nor preserve the dynamic performance because $Z_p(\rho) = Z_o$, $\forall\ \omega > \omega_x$, as shown in Figure 4.

3.4. Modification for Non-Minimum Phase Converters

Non-minimum phase converters are featuring right-half-plane (RHP) zero(s) in their control-to-output transfer functions (G_{vd}). Boost, buck-boost, fly-back and Cũk converters are typical examples of the non-minimum phase converter family. As a result, inverting their G_{vd} yields unstable poles in the proposed controller. Although Equation (12) implies that the unstable poles in $(G_{vd}^{-1}G_{vd})$ would be canceled by the RHP zeros, it is misleading. Unstable pole-zero cancellation violates the internal stability of the system [33], so the controller will still be unstable despite the cancellation.

The unstable poles impediment can be addressed by the proposed controller, which depends on the magnitude of G_{vd} to reshape the source output impedance. Hence, we propose to replace the RHP zeros of G_{vd} by their left-half-plane (LHP) mirrors to obtain the modified control-to-output transfer function (G_{vdm}) for non-minimum phase converters. The magnitudes of G_{vd} and G_{vdm} are the same [34].

G_{vdm} will have a different phase response compared to G_{vd}, which will not impact our scheme as it mainly depends on the magnitude. ρ is a DC value, so the phase response of H in Equation (11) would have no impact on the proposed impedance reduction method. It solely manipulates the magnitude of the output impedance. G_R in Equation (10) can be re-expressed for non-minimum phase converters as

$$G_R = G_{vdm}^{-1} \frac{\omega_x^p}{(s+\omega_x)^p} \tag{16}$$

while Equations (11)–(13) hold.

4. Minimum-Phase Cascaded System

4.1. Theoretical Analysis

A test system consisting of a buck converter, as the (LRC), and two loads has been designed to validate the performance of the proposed controller. Figure 6 shows the system schematic diagram, and Table 1 tabulates its parameters. The loads' controllers are described by Equation (A1) in the Appendix A.

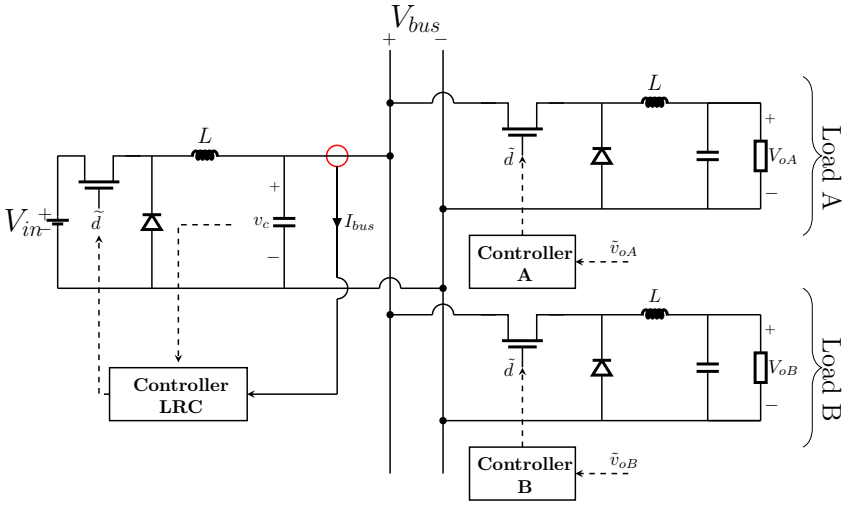

Figure 6. Experimental setup schematic diagram.

Table 1. Numerical parameters of the test system.

Parameter	Source	Load A	Load B
V_{in}	20	7	7
V_o	7	4	4
$L(uH)$	510	390	400
$r_L()$	0.05	0.01	0.04
$C(uF)$	697	697	697
$r_C(\Omega)$	0.1	0.1	0.1
$R_{load}(\Omega)$	...	2	2
$f_{switching}(KHz)$	100		
$V_{PWM}(V)$	1		
Source Controller			
Gc	$0.001 + \frac{18}{s}$		

The LRC was designed to supply two load converters, however, an impedance overlap occurs while supplying full load using the original controller, as shown in Figure 7. Supplying a single

converter (50% of the load) degraded the dynamic performance by lowering the gain margin of the LRC from 6.12 dB ($\approx 20\log_{10}(1/0.49)$) to 3.09 dB ($\approx 20\log_{10}(1/0.7)$), as depicted in Figure 8. Moreover, the system become completely unstable after adding the second load, when T_s^L encircles $(-1, j0)$.

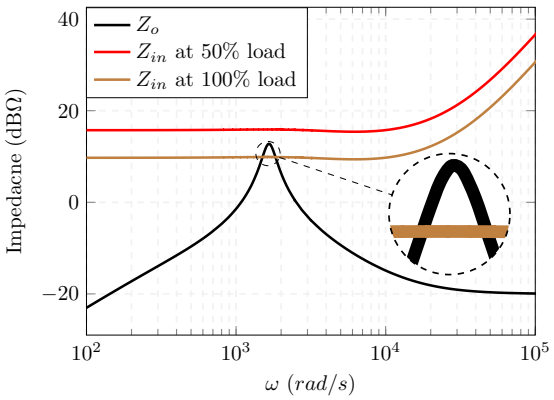

Figure 7. Impedance interaction for the experimental system, for the original controller, with two different loading conditions.

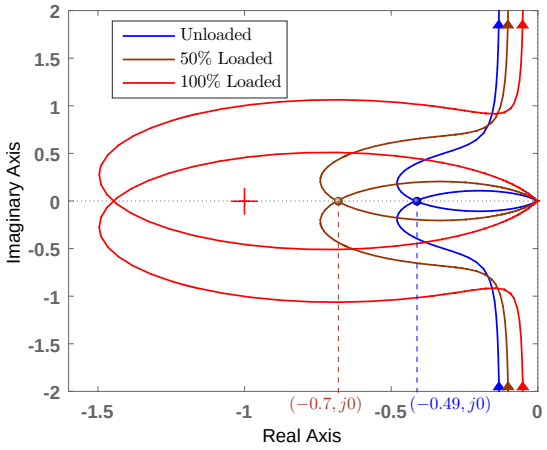

Figure 8. Nyquist diagram of the LRC loop gain (T_S) for the original controller for three loading conditions, where it encircles $(-1, j0)$ at 100% loading.

To validate the proposed controller, its corresponding LRC output impedance ($Z_p(\rho)$) is compared to the LRC impedance induced by using the original controller, Z_o, in Figure 9 at full load condition. ω_x was selected to be 1×10^5 rad/s. Z_o had a peak impedance of 12.7 dBΩ (4.32 Ω), while $Z_p(\rho)$ had 1.77 dBΩ (1.23 Ω). The difference between them is 10.93 dBΩ which corresponds to $(1 + I_{bus})$, where I_{bus} = 2.52 A.

As $Z_p(\rho)$ decreases while increasing the output power, the poles of the loaded system ($T_s^L/(1 + T_s^L)$) move towards the poles of the unloaded system ($T_s/(1 + T_s)$), as illustrated in Figure 10. Consequently, the loading impact is reduced. Hence, the dynamic performance is improved. Figure 11 compares the impact of loading on T_s using the original controller verses the proposed controller. The system was unstable while supplying 100% of the load using the original controller. In contrast, the proposed modifications not only stabilized the system, but also were able to improve the dynamic performance. The LRC gain margin improved to 4.42 dB using the proposed controller compared to −3.88 dB using the original controller, as displayed in Figure 11.

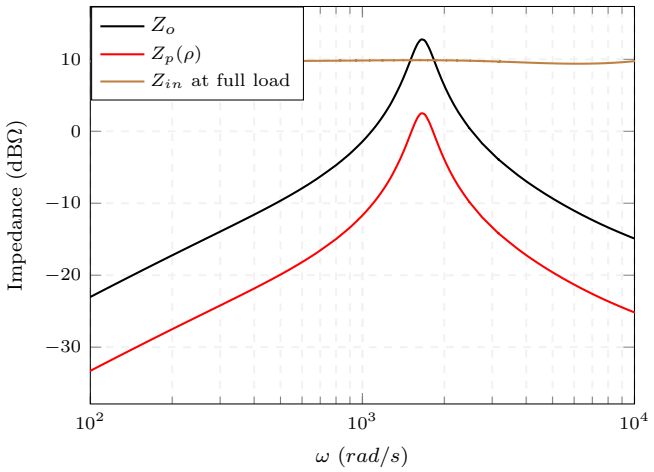

Figure 9. Comparison between original and proposed output impedances of the LRC, highlighting the capability of the proposed controller in removing the interaction.

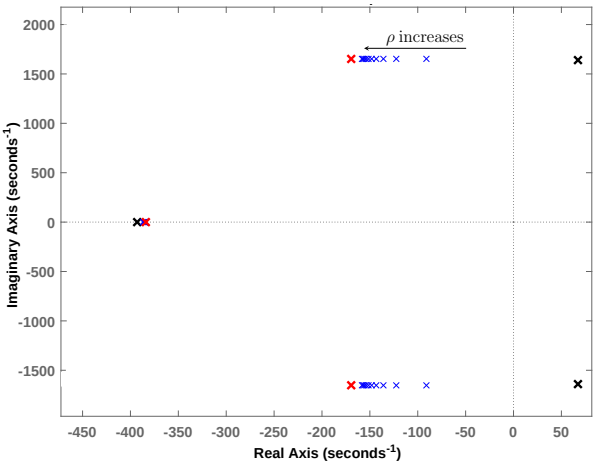

Figure 10. Pole loci of the closed loop LRC, for unstable system with the original control at full load (black poles), original control at no load (red poles), and proposed control (blue poles), highlighting the decoupling capability, as a function of ρ.

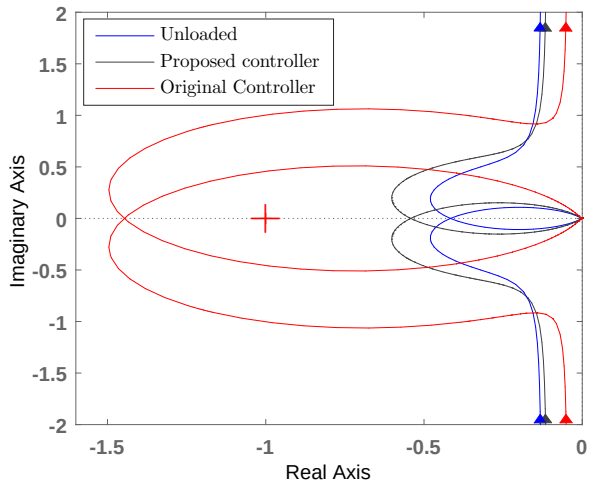

Figure 11. Comparing the Nyquist diagrams of LRC's loop gain at full load with and without the proposed controller, highlighting its stabilizing and performance preserving capability.

4.2. Simulation Case Studies

The system described in Figure 6 was simulated using PLECS Standalone software package (Plexim, Zürich, Switzerland) to verify the effectiveness of the proposed controller in order to adaptively reshape the source output impedance, and to improve the overall dynamic performance. The system with its original controller (depicted in Figure 3) was simulated to demonstrate the impact of loading on its stability. Figure 12a shows connecting Load_A caused substantial oscillations in the bus voltage due to the loss of 3.09 dB of gain margin, as expected from Figure 8. After 200 ms Load_B was connected, which completely destabilized the bus voltage. Despite the oscillations in the bus voltage, the output voltages of both loads were stable. Reference [35] explains this phenomena as every load controller was able to successfully track its input voltage due to their high bandwidth.

The performance of the proposed controller to stabilize and enhance the relative stability margins was then assessed. Load_A was connected first, and the dynamic response of the bus voltage was highly improved, as illustrated in Figure 12b. The settling time was substantially reduced from 100 ms, in Figure 12a, to 25 ms. Connecting load_B, after 200 ms, has neither destabilized the system nor degraded its dynamic performance.

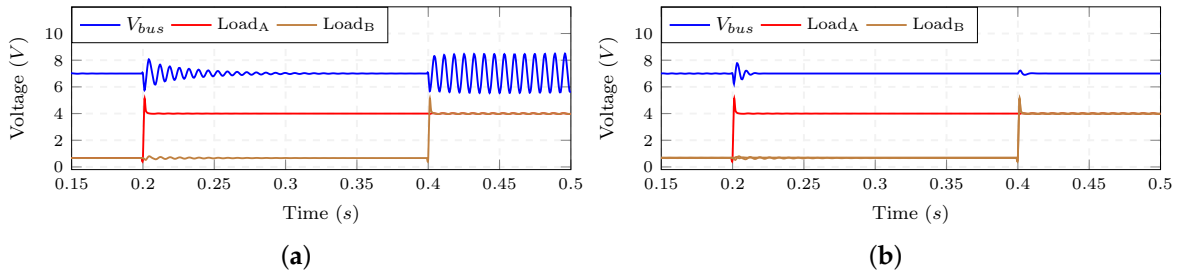

Figure 12. Simulation results for sequential switchings of Load_A (at t = 0.2 s) and Load_B (at t = 0.4 s): (**a**) without the proposed control; and (**b**) with the proposed control.

To further demonstrate the effectiveness of the proposed controller, both loads were connected simultaneously to the DC bus. The original controller was unable to handle both loads, as shown in Figure 13a. Figure 13b demonstrates the capability of our controller, which stabilized the system in 25 ms.

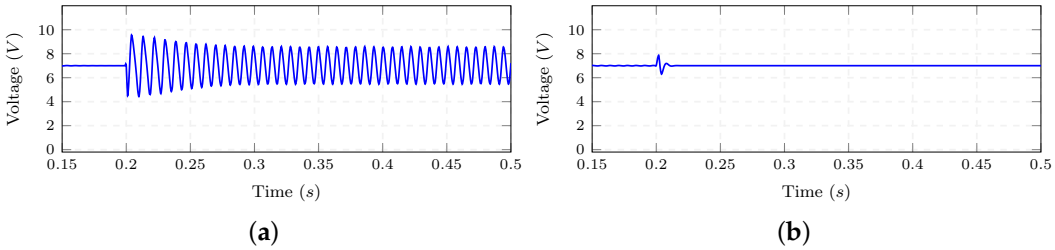

Figure 13. Simulation results for sequential switchings of Load_A and Load_B (at t = 0.2 s): (**a**) without the proposed control; and (**b**) with the proposed control.

4.3. Experiment

To validate the effectiveness of the proposed controller experimentally, the system in Figure 6 was built in the laboratory, as shown in Figure 14.

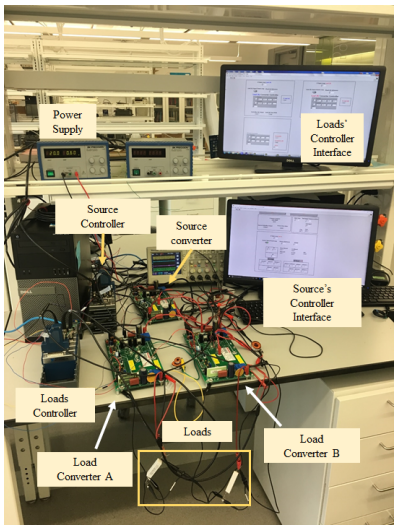

Figure 14. The experimental setup.

Two digital control platforms, using NI-cRIO systems (National Instruments, Austin, TX, USA), were employed. One NI-cRIO was used to implement the LRC controller including the proposed method and the other one realizes two voltage controllers for two load converters. The selected sampling rate was 30 kHz, and the discrete transfer functions such as

$$\frac{y(z)}{x(z)} = \frac{n_3 z^3 + n_2 z^2 + n_1 z + n_0}{z^3 + d_2 z^2 + d_1 z + d_0} \tag{17}$$

were realized using Normal Direct Form II (NDF-II) [36], as illustrated in Figure 15.

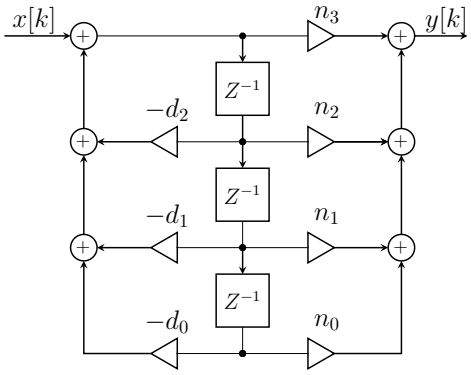

Figure 15. Normal Direct Form-II realization of the discrete transfer function of Equation (17).

Two tests were conducted to verify the effectiveness of the proposed controller. For the first test, the load converters were sequentially connected to the DC bus such that load_B connects to the system 200 ms after Load_A. For the second test, the load converters were simultaneously connected to the DC bus.

4.3.1. Sequential Connection

Figure 16a shows the response of the system with the original controller to show its inability to handle the entire load, where V_{oA} and V_{oB} denote the output voltages of loads A and B, respectively. Connecting Load_A caused a decaying oscillatory response for 100 ms. Then, integrating load_B totally destabilized the bus voltage. As discussed earlier, the output voltages of the loads were stable.

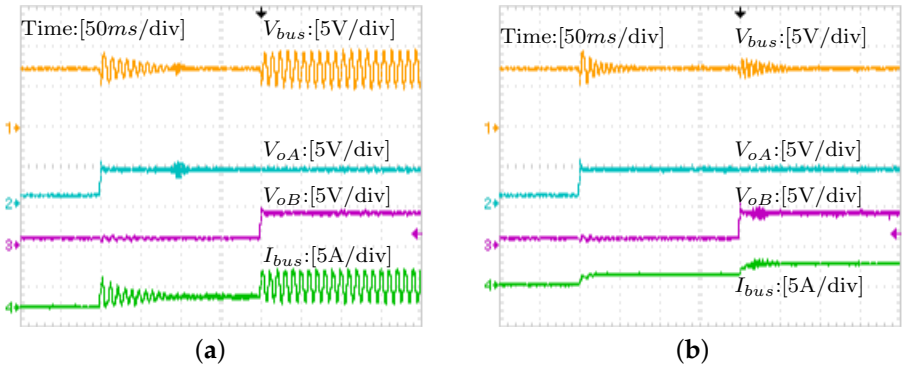

Figure 16. Experimental results of sequential switching of Load_A and Load_B: (**a**) without the proposed controller; and (**b**) with the proposed controller.

Figure 16b shows the enhancement in the dynamic performance accomplished by the proposed controller. Connecting Load_A created oscillations in the bus voltage for 40 ms, showing 60% improvement in the settling time compared to Figure 16a. The reduction in the settling time implies that the poles of the system have moved towards the original system's dominant poles, as shown in Figure 10. Then, connecting load_B caused negligible oscillations because the new gain margin is 4.2 dB compared to −3.88 dB, as shown in Figure 11.

4.3.2. Simultaneous Testing

The effectiveness of the proposed controller to stabilize and improve the dynamic performance while connecting the two loads simultaneously is verified in this case study. Figure 17a shows connecting the two loads without the proposed modification destabilizes the bus voltage. Then, the proposed controller was implemented, and it was able to stabilize the system in 50 ms, as shown in Figure 17b, which proves the ability of the introduced method to stabilize and enhance the dynamic performance.

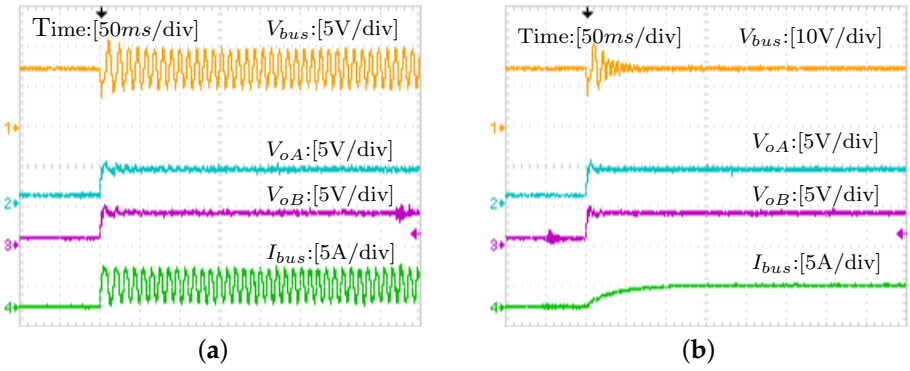

Figure 17. Experimental results of simultaneous switching of Load_A and Load_B: (**a**) without the proposed controller; and (**b**) with the proposed controller.

5. Non-Minimum Phase Cascaded System

5.1. Theoretical Analysis

Another prototype consisting of a boost converter, as the LRC, supplying a buck converter was designed, as shown in Figure 18. This prototype is studied to validate the capability of the proposed controller in controlling non-minimum phase converters. Table 2 tabulates the parameters of the system, where the source controller is (0.005 + 13.2/s) and the load controller is described by Equation (A2) in

the Appendix A. The load converter was designed to supply 9.25 W. However, an impedance overlap occurs, as seen in Figure 19, that destabilizes the bus voltage.

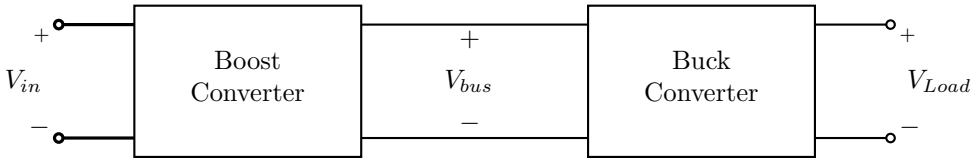

Figure 18. Cascaded system with a boost converter as the LRC.

Table 2. Numerical parameters of the test system in Figure 18.

Parameter	Boost	Buck
V_{in}	5	7
V_o	7	3.6
$L(uH)$	930	390
$r_L(\Omega)$	0.05	0.01
$C(uF)$	697	697
$r_C(\Omega)$	0.1	0.1
$R_{load}(\Omega)$	···	1.4
$f_{switching}(KHz)$	100	
$V_{PWM}(V)$	1	

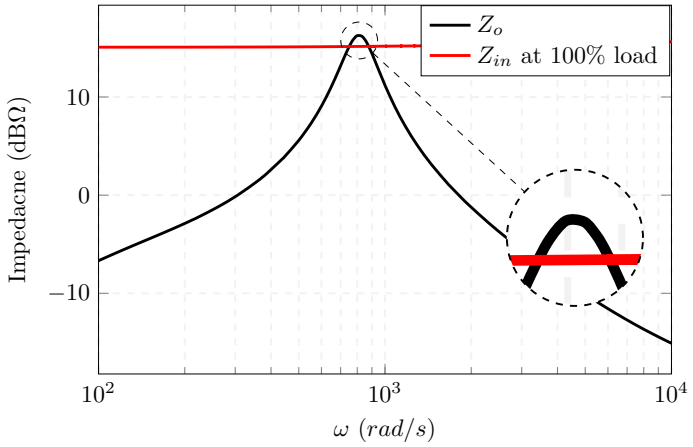

Figure 19. Impedance interaction between the boost and the buck converters.

The boost converter control-to-output transfer function is described by

$$G_{vd} = 0.56\frac{(s - 1.435 \times 10^4)(s + 657.9)}{s^2 + 339.5s + 7.871 \times 10^5} \tag{18}$$

which has a RHP zero, and is modified to

$$G_{vdm} = 0.56\frac{(s + 1.435 \times 10^4)(s + 657.9)}{s^2 + 339.5s + 7.871 \times 10^5} \tag{19}$$

G_{vdm} and Equation (16) were used to shape the output impedance of the boost converter. ω_x was chosen to be 10^5 rad/s because the impedance overlap occurred at $\omega = 10^3$ rad/s, as Figure 19 depicts. As a result, the reshaped output impedance of the boost converter, using Equation (19), is shown in Figure 20, which highlights the ability of the proposed method to reshape the output impedance of the non-minimum phase converters. In addition, Figure 21 shows the unloaded loop gain (T_S),

the unstable loop gain (T_S^L) due to the loading impact, and the improved loop gain using the proposed controller (T_I).

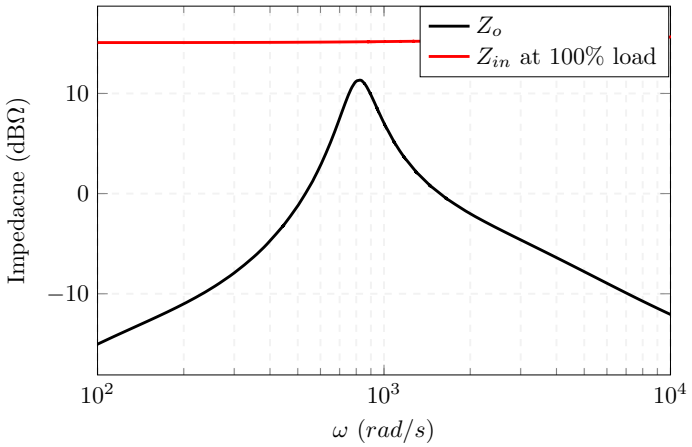

Figure 20. Impedance interaction decoupling between the boost and the buck converters using the proposed method.

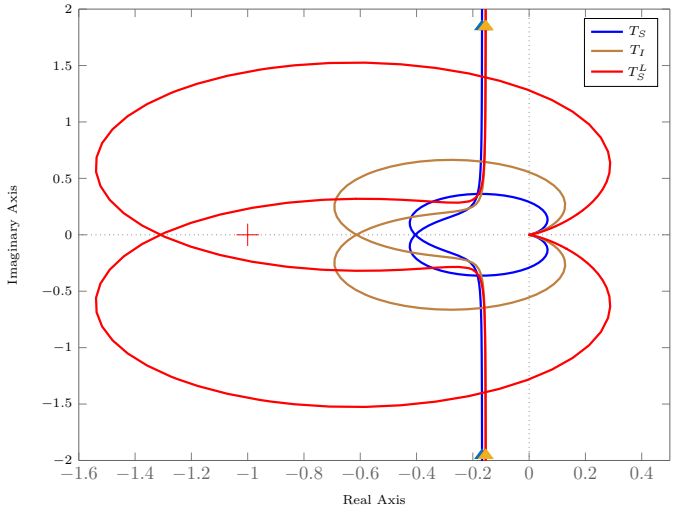

Figure 21. The unloaded, improved, and unstable loop gains of the source converter, depicting the ability of the proposed controller to stabilized the non-minimum phase systems.

5.2. Simulation Case Studies

The system described in Figure 18 along with its parameters in Table 2 was simulated to verify the effectiveness of the proposed controller to stabilize a non-minimum phase converter. The test was performed by supplying 70% of the load. Then, the remaining 30% was connected at t = 0.2 s. Figure 22a shows that the bus voltage has become unstable at the full load condition using the original controller.

Next the system was equipped with the proposed controller, and the test was preformed again. Adding the load at $t = 0.2s$ did not compromise the stability of the system. The bus voltage suffered from neither permanent oscillations nor a long settling time. Hence, the simulation validates the effectiveness of the proposed controller, and the proposed modification of G_{vd} to stabilize a non-minimum phase converter.

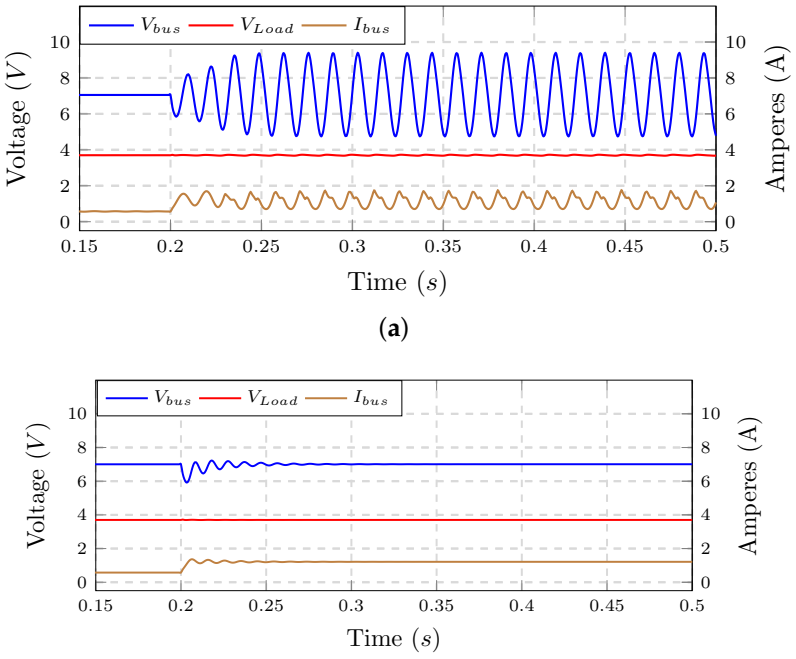

Figure 22. The dynamic performance of the boost-driven cascaded system: (**a**) without the proposed controller; and (**b**) with the proposed controller.

5.3. Experiment

The analytical and simulation results were further validated by experiments. A single NI-cRIO digital platform controller, with a sampling rate was of 30 kHz, was used to control the entire system of Figure 18. The digital transfer functions, such as Equation (17) were realized, as demonstrated in Figure 15.

The test was run first to demonstrate the inability of the original controller to preserve the bus voltage stability at full load condition, as shown in Figure 23a. The impact of the impedance overlap is evident. Thus, the proposed controller was implemented to decouple the impedance interaction, and the test was run again. The bus voltage stability was preserved, as Figure 23b depicts, so the experimental results are in agreement with the analytical and simulation outcomes. Collectively, these results validate the effectiveness of the proposed controller to stabilize and improve the dynamic performance of non-minimum phase converters.

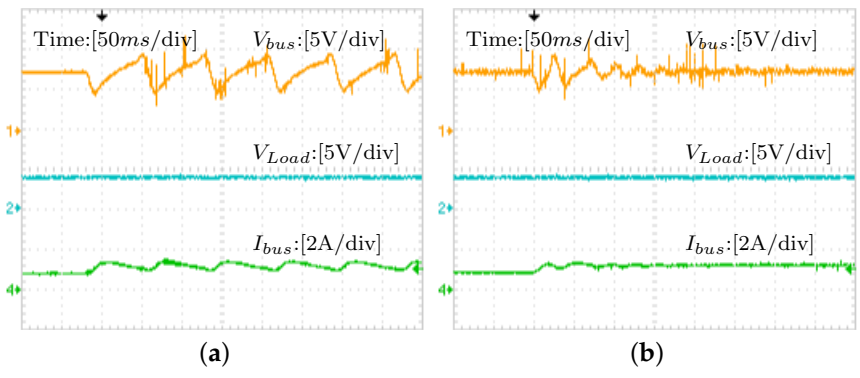

Figure 23. Experimental results the boost-driven cascaded system: (**a**) without the proposed controller; and (**b**) with the proposed controller.

6. Conclusions

This paper presents a method to stabilize and enhance the dynamic performance of cascaded DC-DC systems by reducing the magnitude of the source output impedance adaptively. The proposed controller is applicable to minimum and non-minimum phase converters that employ linearized feedback control schemes. In addition, the method can handle single or multiple loads. This flexibility is achieved by utilizing the average value of the bus current to reduce the magnitude of the source output impedance by the factor of $(1 + I_{bus})$. The problem of reciprocating the control-to-output transfer function of DC-DC converters is solved by utilizing a low pass filter in order to realize the inversion in a certain frequency range. However, the RHP zeros of non-minimum phase converters cause instability if the corresponding transfer function is reciprocated as a result of introducing unstable poles to the system, which has been solved by mirroring the RHP zeros about the imaginary-axis of the complex plane.

Assessing the effectiveness of the controller is carried out by mathematical analysis, simulation, and experiments. All of the analyses results are in agreement and validated the satisfactory performance of the proposed control. Implementing the proposed controller could improve the relative stability margins of the studied systems. It is noteworthy that filtering the bus current introduces delay, which might prolong the settling time if the introduced delay was substantial. In addition, the discrete transfer functions are implemented practically by NDF-II, which produces the closest experimental outcomes to the simulation and to the theoretical results.

Author Contributions: The authors have participated equally in this work. Analyses, simulations, and experiments were conducted and analyzed by both of the authors.

Conflicts of Interest: The authors declare no conflict of interest.

Appendix A

The loads' controllers for the system in Section 4 is

$$G_{cl} = \frac{6.1783 \times 10^6}{s} \left[\frac{s + 2439}{s + 1.012 \times 10^5} \right]^2 \tag{A1}$$

and the load controller of the system in Section 5 is

$$G_{cl} = \frac{6.6336 \times 10^6}{s} \left[\frac{s + 2321}{s + 1.063 \times 10^6} \right]^2 \tag{A2}$$

References

1. Luo, S. A review of distributed power systems part I: DC distributed power system. *IEEE Aerosp. Electron. Syst. Mag.* **2005**, *20*, 5–16.
2. Riccobono, A.; Santi, E. Comprehensive Review of Stability Criteria for DC Power Distribution Systems. *IEEE Trans. Ind. Appl.* **2014**, *50*, 3525–3535.
3. Yi, Z. Solar Photovoltaic (PV) Distributed Generation Systems—Control and Protection. Ph.D Thesis, The George Washington University, Washington, DC, USA, 2017.
4. Ahmadi, R. Dynamic Modeling, Stability Analysis, and Controller Design for DC Distribution Systems. Ph.D Thesis, Missouri University of Science and Technology, Rolla, MO, USA, 2013.
5. Muroyama, S.; Sakakibara, K.; Yamashita, T. Transient Voltage Analysis of DC Power Distribution Systems. In Proceedings of the Fifth International Telecommunications Energy Conference, 1983, INTELEC '83, Tokyo, Japan, 18–21 October 1983; pp. 315–321.
6. Emadi, A.; Ehsani, M.; Miller, J.M. *Vehicular Electric Power Systems: Land, Sea, Air, and Space Vehicles*; Marcel Dekker: New York, NY, USA, 2004.
7. Yi, Z.; Etemadi, A.H. Line-to-Line Fault Detection for Photovoltaic Arrays Based on Multiresolution Signal Decomposition and Two-Stage Support Vector Machine. *IEEE Trans. Ind. Electron.* **2017**, *64*, 8546–8556.

8. Middlebrook, R.D. Input Filter Considerations in Design and Application of Switching Regulators. *IEEE Ind. Appl. Soc. Annu. Meet.* **1976**, *11*, 366–382.
9. Dragicevic, T.; Lu, X.; Vasquez, J.C.; Guerrero, J.M. DC Microgrids-Part I: A Review of Control Strategies and Stabilization Techniques. *IEEE Trans. Power Electron.* **2016**, *31*, 4876–4891.
10. Wildrick, C.M.; Lee, F.C.; Cho, B.H.; Choi, B. A method of defining the load impedance specification for a stable distributed power system. In Proceedings of the 24th Annual IEEE Power Electronics Specialists Conference, 1993. PESC '93 Record, Seattle, WA, USA, 20–24 June 1993; pp. 826–832.
11. Feng, X.; Ye, Z.; Xing, K.; Lee, F.C.; Borojevic, D. Impedance specification and impedance improvement for DC distributed power system. In Proceedings of the 30th Annual IEEE, Power Electronics Specialists Conference (PESC 99), Charleston, SC, USA, 1 July 1999; Volume 2, pp. 889–894.
12. Sudhoff, S.D.; Glover, S.F.; Lamm, P.T.; Schmucker, D.H.; Delisle, D.E. Admittance space stability analysis of power electronic systems. *IEEE Trans. Aerosp. Electron. Syst.* **2000**, *36*, 965–973.
13. Suntio, T. *Dynamic Profile of Switched-Mode Converter: Modeling, Analysis and Control*; Wiley-VCH: Weinheim, Germany, 2009.
14. Wang, X.; Yao, R.; Rao, F. Three-step impedance criterion for small-signal stability analysis in two-stage DC distributed power systems. *IEEE Power Electron. Lett.* **2003**, *1*, 83–87.
15. Riccobono, A.; Santi, E. A novel Passivity-Based Stability Criterion (PBSC) for switching converter DC distribution systems. In Proceedings of the 2012 Twenty-Seventh Annual IEEE Applied Power Electronics Conference and Exposition (APEC), Orlando, FL, USA, 5–9 February 2012; pp. 2560–2567.
16. Hankaniemi, M. Dynamical Profile of Switched-Mode Converter—Fact or Fiction? Ph.D Thesis, Tampere University of Technology, Tampere, Finland, 2007.
17. Cai, W.; Yi, F.; Cosoroaba, E.; Fahimi, B. Stability Optimization Method Based on Virtual Resistor and Nonunity Voltage Feedback Loop for Cascaded DC DC Converters. *IEEE Trans. Ind. Appl.* **2015**, *51*, 4575–4583.
18. Wu, M.; Lu, D.D.C. A Novel Stabilization Method of LC Input Filter With Constant Power Loads Without Load Performance Compromise in DC Microgrids. *IEEE Trans. Ind. Electron.* **2015**, *62*, 4552–4562.
19. Zhang, X.; Ruan, X.; Zhong, Q.C. Improving the Stability of Cascaded DC/DC Converter Systems via Shaping the Input Impedance of the Load Converter With a Parallel or Series Virtual Impedance. *IEEE Trans. Ind. Electron.* **2015**, *62*, 7499–7512.
20. Zhang, X.; Ruan, X.; Kim, H.; Tse, C.K. Adaptive Active Capacitor Converter for Improving Stability of Cascaded DC Power Supply System. *IEEE Trans. Power Electron.* **2013**, *28*, 1807–1816.
21. Zhang, X.; Zhong, Q.C.; Ming, W.L. Stabilization of a Cascaded DC Converter System via Adding a Virtual Adaptive Parallel Impedance to the Input of the Load Converter. *IEEE Trans. Power Electron.* **2016**, *31*, 1826–1832.
22. Ahmadi, R.; Ferdowsi, M. Improving the Performance of a Line Regulating Converter in a Converter-Dominated DC Microgrid System. *IEEE Trans. Smart Grid* **2014**, *5*, 2553–2563.
23. Ahmadi, R.; Ferdowsi, M. Controller design method for a cascaded converter system comprised of two DC-DC converters considering the effects of mutual interactions. In Proceedings of the 2012 Twenty-Seventh Annual IEEE Applied Power Electronics Conference and Exposition (APEC), Orlando, FL, USA, 5–9 February 2012; pp. 1838–1844.
24. Erickson, R.W.; Dragan, M. *Fundamentals of Power Electronics*; Kluwer Academic: Norwell, MA, USA, 2001.
25. Basso, C.P. *Designing Control Loops for Linear and Switching Power Supplies: A Tutorial Guide*; Artech House: Norwood, MA, USA, 2012.
26. Ang, S.S. *Power-Switching Converters*; M. Dekker: New York, NY, USA, 1995.
27. Ahmadi, R.; Paschedag, D.; Ferdowsi, M. Analyzing stability issues in a cascaded converter system comprised of two voltage-mode controlled dc-dc converters. In Proceedings of the 2011 Twenty-Sixth Annual IEEE, Applied Power Electronics Conference and Exposition (APEC), Fort Worth, TX, USA, 6–11 March 2011; pp. 1769–1775.
28. Wildrick, C.M. Stability of Distributed Power Supply Systems. Ph.D Thesis, Virginia Polytechnic and State University, Blacksburg, VA, USA, 1993.
29. Pidaparthy, S.K.; Choi, B. Stability analysis of PWM converters connected to general load subsystems. In Proceedings of the 2015 9th International Conference on Power Electronics and ECCE Asia (ICPE-ECCE Asia), Seoul, Korea, 1–5 June 2015; pp. 1033–1040.

30. Cao, L.; Loo, K.H.; Lai, Y.M. Systematic Derivation of a Family of Output-Impedance Shaping Methods for Power Converters—A Case Study Using Fuel Cell-Battery-Powered Single-Phase Inverter System. *IEEE Trans. Power Electron.* **2015**, *30*, 5854–5869.
31. Cao, L.; Loo, K.H.; Lai, Y.M. Output-Impedance Shaping of Bidirectional DAB DC - DC Converter Using Double-Proportional-Integral Feedback for Near-Ripple-Free DC Bus Voltage Regulation in Renewable Energy Systems. *IEEE Trans. Power Electron.* **2016**, *31*, 2187–2199.
32. Aldhaheri, A.; Etemadi, A. Impedance Decoupling in DC Distributed Systems to Maintain Stability and Dynamic Performance. *Energies* **2017**, *10*, 470.
33. Braatz, R.D. On Internal Stability and Unstable Pole-Zero Cancellations [Feedback]. *IEEE Control Syst.* **2012**, *32*, 15–16.
34. Nise, N.S. *Control Systems Engineering, Binder Version*; John Wiley & Sons Inc.: Hoboken, NJ, USA, 2010.
35. Sudhoff, S.D.; Corzine, K.A.; Glover, S.F.; Hegner, H.J.; Robey, H.N. DC link stabilized field oriented control of electric propulsion systems. *IEEE Trans. Energy Conver.* **1998**, *13*, 27–33.
36. Manolakis, D.G.; Ingle, V.K. *Applied Digital Signal Processing: Theory and Practice*; Cambridge University Press: Cambridge, UK, 2011.