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Suppression of Switching Crosstalk and Voltage Oscillations in a SiC MOSFET Based Half-Bridge Converter

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Abstract: The silicon carbide (SiC) MOSFET is characterized by high operating voltage, temperature, switching frequency and efficiency which enables a converter to achieve high power density. However, at high switching frequency, the crosstalk phenomenon occurs when the gate voltage spike introduced by high dv/dt and voltage ringing forces false turn-on of SiC MOSFET which causes a crow-bar current thereby increasing switching losses. In order to increase the immunity against the crosstalk phenomenon in a half-bridge configuration, this paper presents a gate driver for SiC MOSFET capable of generating the negative turn-off voltage without using a negative power supply. In addition, the effect of parasitic inductances on the switching response is analyzed and an *RC* snubber is designed using high-frequency based circuit reduction technique to dampen the switching ringing. The performance of the proposed gate driver and the designed *RC* snubber is validated using simulation and experiment at the 1 MHz switching frequency. The results show that the proposed gate driver with *RC* snubber eliminates crosstalk by maintaining any spurious gate spike below the gate threshold voltage.

Keywords: SiC MOSFET; parasitic inductance; *RC* snubber; half-bridge converter

1. Introduction

The demand for fast-switching, high voltage, and high-temperature devices, capable of operating at elevated efficiency has enabled the trend towards WBG semiconductor materials [1,2]. Among the WBG, the SiC and GaN technologies have matured enough and devices up to 1.7 kV and 650 V voltage ratings respectively, are commercially available which have been proved as promising alternatives to the Si. Due to an almost identical gate drive requirements, the GaN cascode transistor can easily replace Si MOSFET [3]. However, due to features such as a restricted-range of gate voltage, low threshold voltage, and low parasitic capacitances the gate drive requirements of a SiC MOSFET are more stringent [4,5].

The recent research focuses on the gate driver design for SiC MOSFET to enable the high switching speed, also featuring the damping of parasitic resonance and crosstalk suppression [6,7]. The crosstalk phenomena in half-bridge configuration refer to the spurious triggering of the low-side SiC MOSFET during the turn-on transition of the high-side SiC MOSFET and vice versa [8]. Due to voltage rise across the device in off-state, a charging current flow through its parasitic gate-drain capacitance and induces a positive spike in its gate voltage. When this voltage spike exceeds the gate threshold voltage, it can falsely trigger the high-side MOSFET, which causes a crow-bar current and result in increased switching power losses. Therefore, it is essential to suppress the crosstalk phenomena for the high-frequency and reliable operation of the half-bridge converter [9].

The gate-impedance control technique reduces the gate voltage spike by adding external gate-source capacitance to provide a low-impedance path [10,11]. However, the crosstalk mitigation is vestigial as it results in a prolonged switching transition, increasing the switching losses [12]. The active suppression technique reported in [13], employed a transistor between the gate and source terminals to create a short when the gate-source voltage climb above the threshold voltage is detected. However, due to the high internal gate and source impedances, the gate voltage feedback for crosstalk detection lacks accuracy and degrades the effectiveness of active suppression system.

Another reported technique used a negatively biased gate voltage, which by level shifting the gate voltage spike prevents false turn-on and accelerates the SiC MOSFET's turn-off [14]. The negative turn-off voltage is commonly supplied using an additional negative voltage source, but, the level shifter circuits proposed in [15,16] used voltage divider circuit to get rid of the negative voltage source. However, due to increased circuit complexity, it is not a viable solution for volume optimized and cost-sensitive converters. In this paper, a gate driver is proposed for SiC MOSFET to suppress the crosstalk phenomena by a negative level shifting of the gate voltage using a parallel connected zener diode and a capacitor. Furthermore, the proposed driver circuit does not require a dedicated negative voltage source and voltage feedback and is realized using low-cost components.

The parasitic inductance and stray capacitance of SiC MOSFET at a high-switching frequency manifest resonance which introduces a voltage overshoot and ringing during turn-off transition [17]. The parasitic package inductances of the SiC MOSFET becomes further unpropitious when combined with the stray inductance of PCB interconnection [18]. The parasitic inductance reinforces voltage overshoot which deteriorates the total harmonic distortion (THD) performance, and as a result, the converter may require a higher-order filter to meet the desired performance. Therefore, it is necessary to suppress the parasitic resonance to enable improved THD of half-bridge dc-ac converter or otherwise; the high-frequency operation will be vestigial [19].

Optimization of package inductances for pushing higher the parasitic resonant frequency is becoming faltered, and therefore, the conspicuous solution is to maneuver the impedance of the switching circuit using an auxiliary network [20]. Several techniques aimed to suppress the voltage ringing, range in complexity from reducing the switching speed using high gate impedance to active gate control involving a feedback compensator [21,22]. The simplest approach advocates lowering the switching speed by raising the gate impedance, however, the prolonged switching transition enlarges switching losses [23]. Due to magnetic saturation caused by current escalation limits application of ferrite bead to restrain the parasitic inductance. Moreover, the suppression using dc-link capacitors [24] and magnetically coupled damping circuits [25] is not very convincing. The *RC* shunt snubber is the familiar and most effective technique which offers flexibility to achieve the desired level of suppression. However, the experience-based design commonly leads to inadequate damping [26]. In [27], the authors formulated a root-locus based *RC* snubber design for the double-pulse circuit by neglecting the parasitic source inductance of the SiC MOSFET. In this work, the same design procedure is adapted to optimize the suppression circuit for the half-bridge dc-ac converter while the SiC MOSFET embodies the parasitic source inductance.

The rest of this paper is organized as follows. The gate driver for SiC MOSFET is presented in Section 2. Effect of parasitic components on switching response is illustrated in Section 3. In Section 4, the snubber circuit design is proposed for mitigating the switching ringing. Simulation and experimental results are presented in Section 5, followed by the conclusion in Section 6.

2. Gate Driver for SiC MOSFET

2.1. Crosstalk Phenomenon in Half-Bridge dc-ac Converter

Due to fast-rising drain-source voltage, the parasitic capacitances of a MOSFET cause a gate voltage spike during switching transitions and may result in spurious turn-on if it exceeds the threshold voltage. The SiC MOSFET is more vulnerable to false triggering due to its low-threshold voltage as compared to Si counterpart. For instance, the typical threshold voltage of Si MOSFET IPW65R190CFD from Infineon Technologies is 4 V, while for SiC MOSFET C3M0120090J from Cree

Inc., the value is only 2.1 V. A detailed schematic of the half-bridge dc-ac converter, including the parasitic components of SiC MOSFET is shown in Figure 1a. The driving voltages v_{GH} and v_{GL} control the switching state of the high-side S_H and low-side S_L MOSFETs respectively. Further, the R_{GL} and $R_{GL(in)}$ are the external and internal gate resistances of low-side MOSFET S_L respectively, while C_{GSL}, C_{DGL}, and C_{DSL} are its parasitic gate-source, drain-gate, and drain-source capacitances respectively.

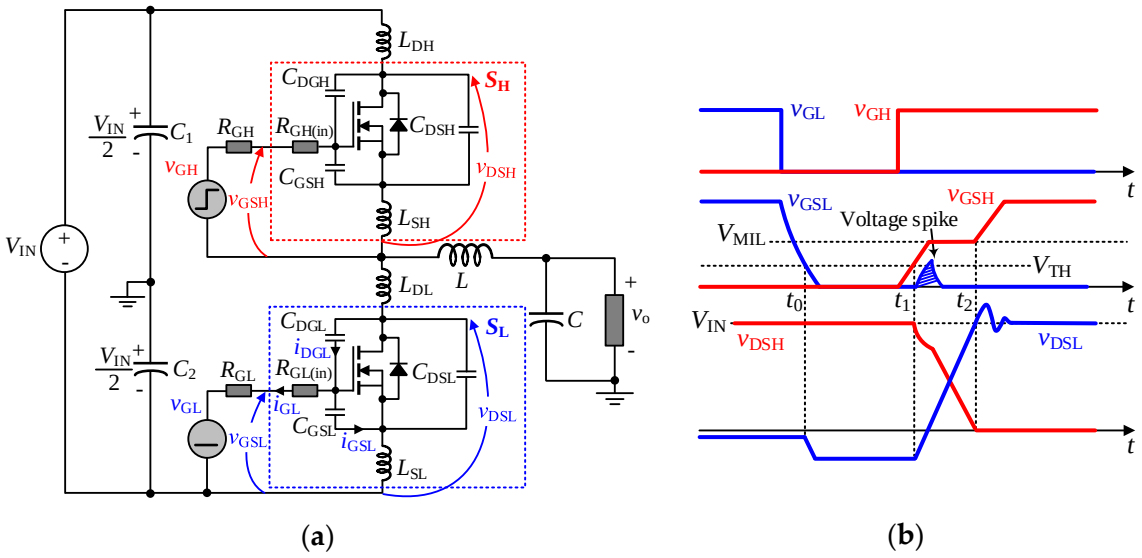


Figure 1. (**a**) Equivalent circuit of the SiC MOSFET based half-bridge dc-ac converter with the parasitic components (**b**) illustration of voltage spike during turn-on transition of high-side MOSFET.

It is assumed that S_L is in its blocking state, and the MOSFET S_H is tuning-on as shown in Figure 1b to illustrate the mechanism of spurious gate voltage spike. At time t_1, the v_{GSH} crosses the threshold voltage V_{TH}, which allows the drain-source voltage of the low-side MOSFET v_{DSL} to rise abruptly, producing a current i_{DGL} through parasitic capacitance C_{DGL}. This charging current i_{DGL} further flows through the parasitic capacitance C_{GSL} and the gate resistors $R_{GL(in)}$ and R_{GL}, respectively denoted as i_{GSL} and i_{GL}. The current i_{GL} introduces a spike in the gate voltage v_{GSL} with the peak determined by R_{GL}, C_{GSL}, and C_{DGL}. Consequently, a spurious turn-on of the low-side MOSFET occurs if the resulting voltage spike exceeds the threshold voltage V_{TH}. A likely method to reduce i_{GL} is by adding external gate-source capacitance, which not only shunts the i_{DGL} but also useful in suppressing the resonance due to the stray inductance and gate-source capacitance C_{GSL}. However, the external gate-source capacitance increases the rise time of the gate voltage and thereby results in increased switching losses. In this paper, the crosstalk suppression by level-shifting of the gate voltage is adopted using a gate driver that does not require a dedicated negative voltage source and voltage feedback while is realized only using passive components.

2.2. Previous Work on Gate Driver for SiC MOSFET with Level Shifter

To increase the immunity of SiC MOSFET against the crosstalk phenomenon in a half-bridge configuration, a gate driver capable of generating the negative turn-off voltage without using a negative power supply is trending. The reason is that the elimination of negative voltage supply significantly reduces the complexity in the converter's layout design. However, it is required that the level shifter circuit must be simple and effective to justify the replacement. Two of the recently reported gate drivers use RCD level shifter and voltage divider circuit.

The RCD level shifter [15] consists of two pairs of parallel connected resistor and capacitor and a diode as shown in Figure 2a. The diode D_P conducts when the driving voltage v_{GL} is high, otherwise it operates in the blocking mode. For C_P and $C_N >> C_{GSL}$, conduction of D_P sets the steady-state v_N as given by Equation (1). When v_{GL} flips back to the low-state, the D_P disconnects the

R_P-C_P and forcing the turn-off gate current to flow through R_N-C_N branch. Therefore, the applied gate voltage is level shifted by V_N.

A modified version of the RCD level shifter reported in [28] is shown in Figure 2b, in which the offset in the gate voltage is also given by Equation (1). During turn-on of SiC MOSFET, the gate current returns through resistor R_M which triggers the transistor Q by creating a positive emitter-base voltage. The capacitor C_P precharged by gate driving voltage, charges C_{GSL} to avoid delays in turning-on. During turn-off of SiC MOSFET, the current flows through diode D when the capacitor C_N acts as local voltage source to supply negative voltage.

$$V_N = \frac{R_N}{R_N + R_P} V_{GG} \tag{1}$$

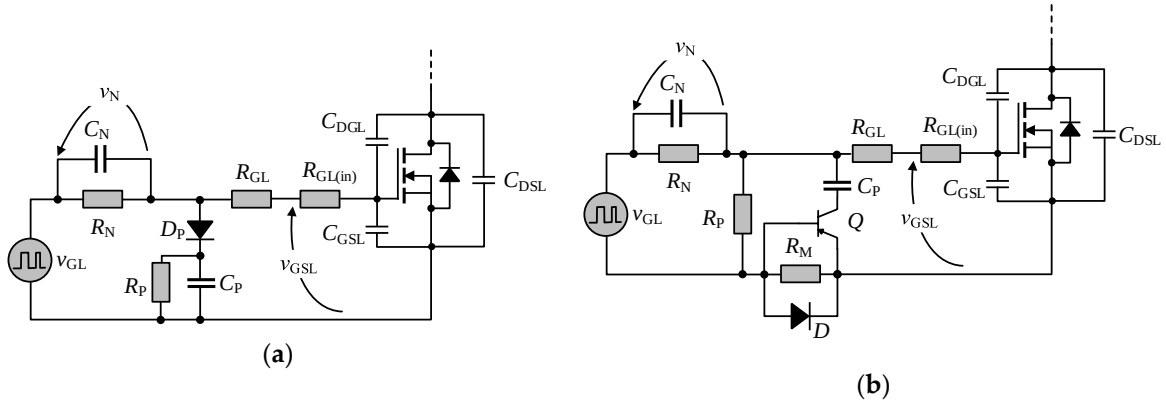


Figure 2. Gate driver for SiC MOSFET with (**a**) RCD level shifter [15] (**b**) voltage divider based level shifter [28].

2.3. Proposed Gate Driver for SiC MOSFET

The proposed gate driver is shown in Figure 3a only for low-side MOSFET, which is comprised of a capacitor C_{ZL}, an ultra-fast diode D_{OFL}, two resistors R_{1L} and R_{2L}, and three zener diodes D_{ZL}, D_{ZPL} and D_{ZNL}. The components of the high-side driver use similar notation, except their subscripts end with the letter "H" instead of letter "L". The parallel connected zener diode D_{ZL} and capacitor C_{ZL} generates a negative gate voltage and thus perform the voltage level shifting without using a negative voltage supply. Due to narrow operating gate voltage range, i.e., 8/18 V, two zener diodes are used as a voltage clipper between the gate and source terminals to protect the MOSFET against the gate breakdown. The diode D_{OFL} enables a lower impedance path for the turn-off gate current to accelerate the turn-off transition. When the diode D_{OFL} is forward biased, a lower turn-off gate resistance is realized by the parallel connection of resistors R_{1L} and R_{2L}.

The design criterion of the components is approached through the transient analysis of the proposed gate driver. Mathematical expressions are derived for gate-source voltage during turn-on and turn-off process.

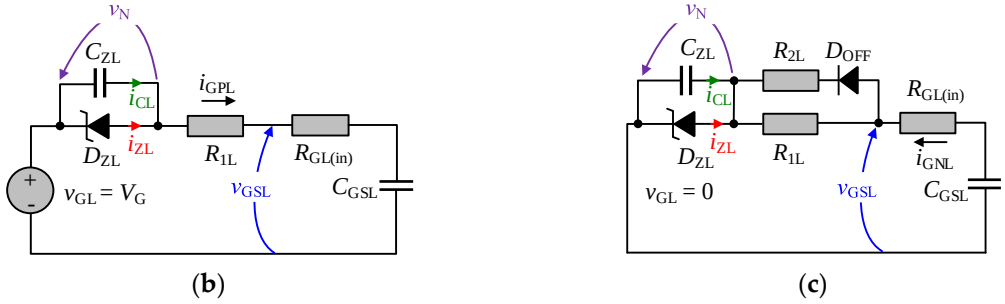


Figure 3. (**a**) The proposed gate driver for SiC MOSFET, and equivalent circuits during (**b**) turning-on transition and (**c**) turning-off.

2.3.1. Turn-on Process

An equivalent circuit of the gate driver when the gate drive voltage v_{GL} steps from 0 to V_G at time t_0 is shown in Figure 3b. The inceptive gate current i_{GPL} path comprises the components C_{ZL}, R_{1L}, $R_{GL(in)}$ and C_{GSL}, ramping up the voltage v_N to the zener voltage V_Z of the diode D_{ZL}. As a result, the current through the zener diode denoted as i_{ZL} rises and take over the capacitor current i_{CL} regulating v_N at V_Z. This indicates that i_{GPL} is the algebraic sum of the capacitor current i_{CL} and the current through the zener diode i_{ZL}. Kirchhoff voltage law (KVL) is applied to the equivalent circuit in Figure 3b which gives Equation (1) which is essential to derive the mathematical relation for i_{GPL}.

$$V_G = \begin{cases} \left(R_{1L} + R_{GL(in)}\right) i_{CL} + \dfrac{1}{\left(C_{ZL} + C_{GSL}\right)} \displaystyle\int i_{CL}\, dt & \text{when } v_N < V_Z \\ \left(R_{1L} + R_{GL(in)}\right) i_{ZL} + \dfrac{1}{C_{GSL}} \displaystyle\int i_{ZL}\, dt \;\; + V_Z & \text{when } v_N = V_Z \end{cases} \tag{2}$$

Using the Laplace transform, the solution of the integral equations in (2) are given in (3)

$$i_{GLP} = \begin{cases} i_{CL} = \dfrac{V_G}{\left(R_{1L} + R_{GL(in)}\right)} \exp\left(\dfrac{-t}{\tau_a}\right) & \text{when } v_N < V_Z \\ i_{ZL} = \dfrac{V_G - V_Z}{\left(R_{1L} + R_{GL(in)}\right)} \exp\left(\dfrac{-(t - t_1)}{\tau_b}\right) & \text{when } v_N = V_Z \end{cases} \tag{3}$$

where t_1 is the time required to charge C_{ZL} to voltage V_Z, and τ_a and τ_b are the time constants expressed in (4). Equation (3) indicates that the peak i_{GPL} is determined by the driving voltage V_G, and the external and intrinsic gate resistors, i.e., R_{1L} and $R_{GL(in)}$. Since $\tau_a > \tau_b$, the current i_{ZL} decays faster than i_{CL}. However, for the desired level shifting operation, the zener diode must not cease conduction until the v_{GL} step to 0 V.

$$\tau_a = \left(C_{ZL} + C_{GSL}\right)\left(R_{1L} + R_{GL(in)}\right) \;\text{ and }\; \tau_b = C_{GSL}\left(R_{1L} + R_{GL(in)}\right) \tag{4}$$

It is essential to observe v_{GSL} as gate-source voltage determines the MOSFET turn-on. Using KVL the voltage equation is given as

$$v_{GSL} = V_G - i_{GPL} R_{1L} - \left(\frac{1}{C_{ZL}} \int i_{GPL}\, dt \;\; + v_N\left(t = t_0\right)\right) \tag{5}$$

substituting i_{GPL} gives the v_{GSL} expressed in (6). It indicates that the decay rate of v_{GSL} can be controlled by tuning C_{ZL} and R_{1L}. To prevent the abrupt drop of v_{GSL} the criteria, i.e., $C_{ZL} >> C_{GSL}$, should be ensured.

$$v_{GSL} = \begin{cases} \dfrac{V_G}{\tau_b}\left(R_{GL(in)} C_{GSL} - \tau_a\right) \exp\left(\dfrac{-t}{\tau_a}\right) - v_N\left(t = t_0\right) & \text{when } v_N < V_Z \\ \left(V_G - V_Z\right)\left(1 - \dfrac{R_{1L}}{\left(R_{1L} + R_{GL(in)}\right)} \exp\left(\dfrac{-(t - t_1)}{\tau_b}\right)\right) & \text{when } v_N = V_Z \end{cases} \tag{6}$$

2.3.2. Turn-off Process

When v_{GL} steps to 0 V, the diode D_{OFL} provides a low impedance path for the gate drive current i_{GNL}, turning-off MOSFET as shown in Figure 3c. It is desirable to use low-valued external gate resistance as it shortens the turn-off time. The Kirchhoff voltage law applied to the equivalent circuit in Figure 3c gives the integral equation

$$\left(R_{TL} + R_{GL(in)}\right) i_{GNL} + \frac{1}{\left(C_{ZL} + C_{GSL}\right)} \int i_{GNL}\, dt \;\; = V_Z \tag{7}$$

where $R_{TL} = R_{1L} // R_{2L}$. Again, solving the Equation (7) using the Laplace Transform gives the gate loop current i_{GPL} and voltage-source v_{GSL} voltage as

$$\begin{cases} i_{\mathrm{GNL}} = \dfrac{V_{\mathrm{Z}}}{R_{\mathrm{TL}} + R_{\mathrm{GL(in)}}} \exp\left(\dfrac{-t}{\tau_{\mathrm{c}}}\right) \\ V_{\mathrm{GSL}} = -V_{\mathrm{Z}} \exp\left(\dfrac{-t}{\tau_{\mathrm{c}}}\right) \end{cases} \tag{8}$$

where τ_c is the time constant of the equivalent driver circuit during turn-off and is expressed by

$$\tau_{\mathrm{c}} = \left(C_{\mathrm{ZL}} + C_{\mathrm{GSL}}\right)\left(\frac{R_{1\mathrm{L}} R_{2\mathrm{L}}}{R_{1\mathrm{L}} + R_{2\mathrm{L}}} + R_{\mathrm{GL(in)}}\right) \tag{9}$$

The capacitor C_{ZL}, precharged up to voltage V_Z serves as a local storage and supplies a negative gate voltage during turn-off without using a dedicated negative voltage supply. Again, to maintain the negative gate voltage, the value of C_{ZL} must satisfy the condition

$$\left(C_{\mathrm{ZL}} + C_{\mathrm{GSL}}\right)\left(\frac{R_{1\mathrm{L}} R_{2\mathrm{L}}}{R_{1\mathrm{L}} + R_{2\mathrm{L}}} + R_{\mathrm{GL(in)}}\right) > D_{\mathrm{m}} T_{\mathrm{S}} \tag{10}$$

where D_m is the expected maximum duty-cycle, and T_S is the switching period.

Equations (6) and (8) indicate that the proposed gate driver level shift v_{GSL} by $-V_Z$ and thus toggles between $-V_Z$ and $V_G - V_Z$ voltage levels. The negative bias voltage has a negligible effect on the turn-on transient of the MOSFET, but accelerates the turn-off as illustrated by the waveforms of the proposed gate driver in Figure 4.

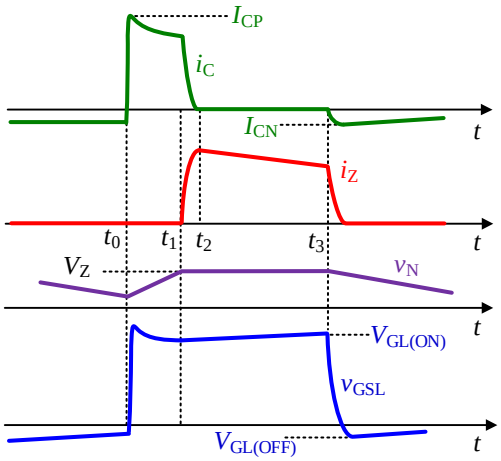


Figure 4. Switching waveforms of the proposed gate driver.

3. Effect of Parasitic Inductances on Switching Waveform of SiC MOSFET

The demand for miniaturized power converters pushes the semiconductor devices to operate at higher switching frequencies. However, the parasitic inductances from PCB interconnections and device packages together with the stray capacitances of the SiC MOSFET can influence switching operation due to high di/dt [29,30]. They causes parasitic resonances which increase electrical stress [31] and slow down the rise and fall of drain current [32]. Therefore, it is important to model effect of parasitic components on switching characteristics. For the study, a conduction overlap is assumed, followed by the low-side MOSFET turn-off transient.

3.1. Overlap Conduction

In the presence of interconnection inductances, an overlap in the conduction of two switches is first investigated to recognize the effect on the turn-off process. Figure 5a shows the half-bridge dc-ac converter with lumped package and interconnection inductances. The L_{DH} and L_{DL} represent the drain inductances, and L_{SH} and L_{SL} represent source inductances of S_H and S_L MOSFETs respectively. When the dead-time is too short, there is overlap conduction which allows a

momentary crow-bar current. It is assumed that switch S_L is initially conducting current I_o and before its transition to blocking state, the high-side MOSFET S_H turns-on creating a crow-bar current. Therefore, MOSFETs S_H and S_L are replaced with close switches with conduction resistance R_{ONH} and R_{ONL} respectively. The inductor current is assumed as a current source I in order to simplify the analysis. The voltage equations of the equivalent circuit during overlap conduction are given as

$$\begin{cases} V_{IN} = (L_{DH} + L_{SH})\dfrac{di_{DH}}{dt} + i_{DH}R_{ONH} + L_{DL}\dfrac{di_{DL}}{dt} + v_{DSL} \\ v_{DSL} = L_{SL}\dfrac{di_{DL}}{dt} + i_{DL}R_{ONL} \end{cases} \quad (11)$$

using $i_{DH} = I + i_{DL}$ in (11), and using Laplace transform to solve, the low-side drain current i_{DL} and drain voltage v_{DSL} are expressed as follows.

$$\begin{cases} i_{DL} = I_o \exp\left(\dfrac{-t}{\tau_d}\right) + \dfrac{(V_{IN} - I R_{ONH})}{(R_{ONL} + R_{ONH})}\left(1 - \exp\left(\dfrac{-t}{\tau_d}\right)\right) \quad \text{where } \tau_d = \dfrac{(R_{ONL} + R_{ONH})}{(L_{DL} + L_{SL} + L_{DH} + L_{SH})} \\ v_{DSL} = \dfrac{(L_{DL} + L_{SL})}{\tau_d}\left\{\dfrac{(V_{IN} - I R_{ONH})}{(R_{ONL} + R_{ONH})} - I_o\right\}\exp\left(\dfrac{-t}{\tau_d}\right) + (V_{IN} - I R_{ONH})\dfrac{R_{ONL}}{(R_{ONL} + R_{ONH})}\left(1 - \exp\left(\dfrac{-t}{\tau_d}\right)\right) \end{cases} \quad (12)$$

Assuming $R_{ONL} = R_{ONH}$, Equation (11) indicates that v_{DSL} will approach $0.5 \times (V_{IN} - IR_{ONH})$ during the overlap time of length T_{oc}, energizing the parasitic inductances.

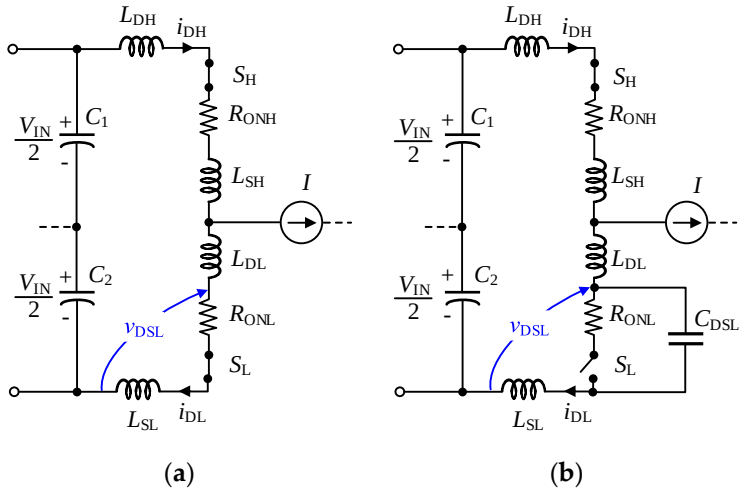


Figure 5. (**a**) Equivalent circuit of the half-bridge converter during overlap conduction (**b**) equivalent circuit when the S_L turn-off.

3.2. The S_L Turn-off Transient

Following the overlap conduction, the transition of low-side MOSFET from conduction to blocking state is shown in Figure 5b, with S_L replaced with an open switch. During this switching transition, the interconnection inductances release their previously stored energy. The drain-source capacitance C_{DSL} and inductances L_{DL} and L_{SL} of the low-side MOSFET realizes a resonant circuit which introduces oscillations in v_{DSL}. The circuit equation during S_L turn-off is given as

$$\begin{cases} V_{IN} = (L_{DH} + L_{SH})\dfrac{di_{DH}}{dt} + i_{DH}R_{ONH} + L_{DL}\dfrac{di_{DL}}{dt} + v_{DSL} \\ v_{DSL} = L_{SL}\dfrac{di_{DL}}{dt} + \dfrac{1}{C_{DS}}\displaystyle\int i_{DL}dt \end{cases} \quad (13)$$

Differentiation of (14) and using $i_{DH} = I + i_{DL}$, reduces the circuit equation to the following standard form

$$\frac{d^2 i_{DL}}{dt^2} + 2\omega_r \zeta \frac{di_{DL}}{dt} + \omega_r^2 i_{DL} = 0 \quad (14)$$

where the resonance frequency ω_r and damping factor ζ are related to the parasitic components as

$$\omega_r = \frac{1}{\sqrt{C_{DS}(L_{DH}+L_{SH}+L_{DL}+L_{SL})}} \text{ and } \zeta = \frac{R_{ONH}}{2}\sqrt{\frac{C_{DS}}{(L_{DH}+L_{SH}+L_{DL}+L_{SL})}} \quad (15)$$

Using the Laplace transform, the equation for drain current i_{DL} is expressed in (15)

$$i_{DL} = A\exp(-\zeta\omega_r t)\sin\left(\left(\omega_r\sqrt{1-\zeta^2}\right)t\right) + B\exp(-\zeta\omega_r t)\cos\left(\left(\omega_r\sqrt{1-\zeta^2}\right)t\right) \quad (16)$$

where the initial conditions determine the constants A and B. Due to the equivalent second-order circuit, i_{DL} exhibit underdamped oscillations as determined by the milliohm ranged conduction resistance R_{ONH}, forcing v_{DSL} to swing accordingly.

Figure 6 shows the waveform of i_{DL} for overlap conduction interval T_{oc} followed by turn-off of low side MOSFET S_L. Assuming an initial 1.2 A steady drain-source current through the body diode of S_L, during T_{oc} the cross-bar current forces i_{DL} to rise rapidly. Finally, elapse of T_{oc} results in underdamped oscillations. A significant reduction is noted in the average drain-source voltage which would result in a lower voltage gain of the dc-ac conversion.

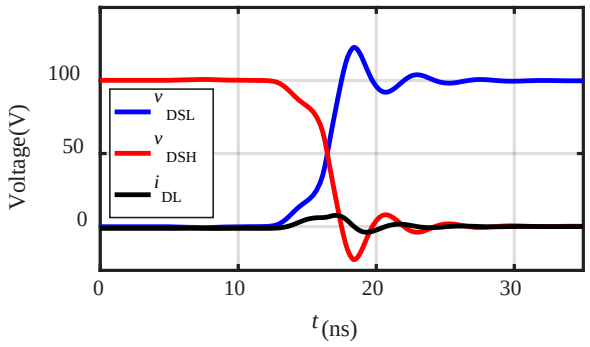


Figure 6. Effect of parasitic inductance on the drain current i_{DL} and gate-source and drain-source voltage waveforms.

3.3. PCB Guidelines

Besides, there is always inescapable intrinsic parasitic inductances of the device, but an adequate PCB layout can optimize the efficiency, enhances the input voltage operating range and reduces the noise among traces of converter [33]. Importantly, minimizing the high-frequency loop inductance enables higher switching frequencies and reduces the voltage overshoot and EMI. Besides improving the THD, it also relaxes the filter requirement. The input path carries the pulsating current and thereby needs special attention as high di/dt and parasitic inductance of a trace can generate voltage ringing [34]. Therefore, it is necessary to minimize the circumference of the high-frequency power-loop.

Conventionally, the power-loop is routed on a single layer known as the lateral power-loop, while the next inner layer is used as a shield plane [19], which reduces the impact of the field generated by high-frequency switching. Due to pulsating current, the power-loop induces a current in the shield layer which produces a magnetic field of its own, counteracting the field of the power-loop. Here the shortest loop has been achieved using the top and the next inner layer (power plane) for laying out the power-loop. Transistors have been placed on the topmost layer, while the internal power plane serves as the return path. Furthermore, the power inductor has been placed on the bottom layer and connected to the drain of MOSFET using vias. Several interleaved channels by assuming vias reduce the current density and thus the interconnection inductances. This results in a smaller power-loop with the field cancellation capability.

The soldering pad for the transistor's tab serves as the primary heat-sink, and thereby a larger copper area is assigned to spread out the heat. The vias used to connect the power plane, and drain of the high-side MOSFET not only reduces the parasitic inductance but also improves the thermal performance by facilitating heat conduction from top to bottom of the PCB [35]. Since the bottom is a

low-resistance path for heat flow, vias on the bottom side are connected to the large copper polygon. Heat sink soldered on the bottom-side is recommended to improve the thermal performance further.

4. *RC* Snubber for Suppression of Parasitic Ringing

The antecedent section discussed the negative influence of parasitic elements on the switching waveform of SiC MOSFET. The derived equation indicates that due to parasitic inductance and capacitance the drain current undergoes ringing, thereby forcing the drain-source voltage to oscillate [36,37]. Suppression of this obtruded ringing in the switching waveform is vital to ensure low distortion and stunted electromagnetic noise [38]. Here, the objective is to dampen the ringing in the drain-source voltage of the low-side MOSFET S_L during turn-off by employing an *RC* snubber across the S_L as shown in Figure 7a. The R_{SBR} and C_{SBR} represent snubber circuit resistance and capacitance respectively, while R_{C1} and R_{C2} are the equivalent series resistance (ESR) of dc-link capacitors.

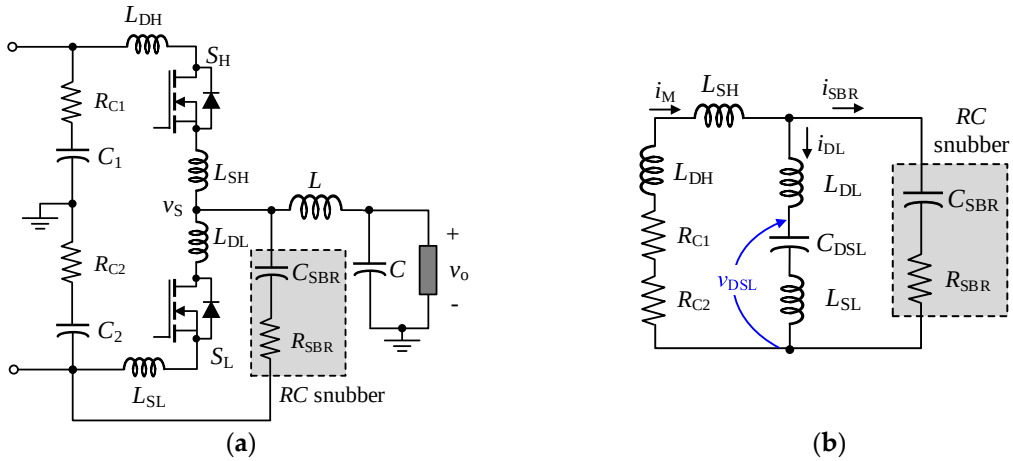


Figure 7. (**a**) half-bridge dc-ac converter with *RC* snubber (**b**) Equivalent circuit using high-frequency assumption.

The snubber design starts with deriving an equivalent circuit of Figure 7a using the high-frequency minimization [27]. It is supposed that initially, the low-side MOSFET S_L conducts current I_o. When the channel resistance increases during the turn-off process, a change in drain-source voltage v_{DSL} causes the drain-source capacitance C_{DS} of the MOSFET to conduct. Finally, neglecting body-diode conduction resistance, replacing large inductances such as L and interconnection inductance between source and converter with open, and replacing dc-link capacitances with short-circuit result in the equivalent circuit shown in Figure 7b. The notation i_{SBR}, i_D, and v_{DSL} represent current through snubber, drain current and drain-source voltage of S_L respectively. In [27], the authors ignored the parasitic source inductance L_{SL} and assumed v_{DSL} as the voltage across C_{DS}. On the contrary, v_{DSL} is exercised here as the sum of the voltage across C_{DS} and L_{SL} to achieve more accurate analysis.

The next step is to derive the expression for v_{DSL} as a function of initial drain current I_o using the equivalent circuit, which gives the rule for snubber components design. Applying KCL and KVL to the equivalent circuit gives the dynamics in (17).

$$\begin{cases} i_M = i_{DL} + i_{SBR} \\ v_{DSL} = \dfrac{1}{C_{DSL}} \displaystyle\int i_D dt \; + L_{SL} \dfrac{di_{DL}}{dt} \\ v_{DSL} = \dfrac{1}{C_{SBR}} \displaystyle\int i_{SBR} dt \; + i_{SBR} R_{SBR} - L_{DL} \dfrac{di_{DL}}{dt} \\ v_{DSL} = -i_M \left(R_{C1} + R_{C2}\right) - \left(L_{DH} + L_{SH}\right) \dfrac{di_M}{dt} - L_{DL} \dfrac{di_{DL}}{dt} \end{cases} \tag{17}$$

Applying Laplace transform and using I_{SBR}, I_{DL}, I_{M}, and V_{DSL} for the corresponding s-domain functions of i_{SBR}, i_{DL}, i_{M}, and v_{DSL}, respectively, gives Equation (18).

$$\begin{cases} I_M = I_{DL} + I_{SBR} \\ V_{DSL} = \dfrac{I_D}{sC_{DSL}} + L_{SL}\left(sI_D - I_o\right) \\ V_{DSL} = \dfrac{I_{SBR}}{sC_{SBR}} + I_{SBR}R_{SBR} - L_{DL}\left(sI_{DL} - I_o\right) \\ V_{DSL} = -I_M\left(R_{C1} + R_{C2}\right) - \left(L_{DH} + L_{SH}\right)\left(sI_M - I_o\right) - L_{DL}\left(sI_D - I_o\right) \end{cases} \tag{18}$$

Using (18a)–(18c) in (18d) and solving for V_{DSL} gives (19) in terms of initial drain current I_o.

$$V_{DSL} = \frac{N(s)}{\Delta(s)} I_o \tag{19}$$

where the numerator N and denominator Δ are expressed in (19) and (20) respectively.

$$\begin{aligned} N(s) = {} & s^2\left(C_{SBR}L_{DH}L_{DL} + C_{SBR}L_{SH}L_{DL} - C_{DSL}C_{SBR}L_{SL}R_{C1}R_{SBR} - C_{DSL}C_{SBR}L_{SL}R_{C2}R_{SBR}\right) \\ & + s\begin{pmatrix} C_{SBR}R_{SBR}L_{DL} + C_{SBR}R_{SBR}L_{SH} + C_{SBR}R_{SBR}L_{DH} + C_{SBR}R_{C1}L_{DL} + C_{SBR}R_{C2}L_{DL} \\ -C_{DSL}R_{C1}L_{SL} - C_{DSL}R_{C2}L_{SL} \end{pmatrix} \\ & + L_{DH} + L_{SH} + L_{DL} \end{aligned} \tag{20}$$

$$\begin{aligned} \Delta(s) = {} & s^4\left(C_{DSL}C_{SBR}L_{SL}L_{DH} + C_{DSL}C_{SBR}L_{SL}L_{SH} + C_{DSL}C_{SBR}L_{DL}L_{SH} + C_{DSL}C_{SBR}L_{DL}L_{DH}\right) \\ & + s^3\begin{pmatrix} C_{DSL}C_{SBR}L_{SL}R_{C1} + C_{DSL}C_{SBR}L_{SL}R_{C2} + C_{DSL}C_{SBR}L_{DL}R_{C1} + C_{DSL}C_{SBR}L_{DL}R_{C2} \\ + C_{DSL}C_{SBR}L_{DH}R_{SBR} + C_{DSL}C_{SBR}L_{SH}R_{SBR} + C_{DSL}C_{SBR}L_{SL}R_{SBR} + C_{DSL}C_{SBR}L_{DL}R_{SBR} \end{pmatrix} \\ & + s^2\begin{pmatrix} C_{DSL}C_{SBR}R_{C1}R_{SBR} + C_{DSL}C_{SBR}R_{C2}R_{SBR} + C_{DSL}L_{DH} + C_{DSL}L_{SH} + C_{SBR}L_{DH} + C_{SBR}L_{SH} \\ C_{DSL}L_{SL} + C_{DSL}L_{DL} \end{pmatrix} \\ & + s\left(C_{DSL}R_{C1} + C_{DSL}R_{C2} + C_{SBR}R_{C1} + C_{SBR}R_{C2} + C_{SBR}R_{SBR}\right) \\ & + 1 \end{aligned} \tag{21}$$

The response of v_{DSL} can be analyzed from the denominator Δ which give the rules to suppress the ringing. By choosing R_{SBR} and C_{SBR} such that all the roots of $\Delta(s)$ are real, ensures successful mitigation of oscillations in v_{DSL}. However, it is not a straightforward to comprehend in case of a fourth-order equation as there is a breakaway point due to the intersection of only two root loci with the real axis. Therefore, to reduce $\Delta(s)$ to a third-order polynomial equation, the drain-source inductances of high-side MOSFET are assumed negligibly small. Substitution of $L_{SH} = L_{DH} = 0$ in (21) and solving algebraic equations $\Delta(s) = 0$ and $d\Delta(s)/dt = 0$ for R_{SBR} and C_{SBR} gives

$$C_{SBR} = \frac{N_C(s)}{\Delta_C(s)} \text{ and } R_{SBR} = \frac{N_R(s)}{\Delta_R(s)} \tag{22}$$

where the $N_C(s)$, $\Delta_C(s)$, $N_R(s)$ and $\Delta_R(s)$ are explicity given in (23)

$$\begin{cases} N_C(s) = \Delta_R(s) = \left(sC_{DSL}R_{C1} + sC_{DSL}R_{C2} + s^2C_{DSL}L_{SL} + s^2C_{DSL}L_{DL} + 1\right)^2 \\ \Delta_C = s^2\begin{pmatrix} s^2\left(C_{DSL}^2L_{SL}R_{C2}^2 + C_{DSL}^2L_{DL}R_{C1}^2 + C_{DSL}^2L_{DL}R_{C2}^2 + C_{DSL}^2L_{SL}R_{C1}^2 + 2C_{DSL}^2L_{SL}R_{C1}R_{C2} + 2C_{DSL}^2L_{DL}R_{C1}R_{C2}\right) \\ -\left(C_{DSL}R_{C2}^2 + 2R_{C1}R_{C2} + C_{DSL}R_{C1}^2\right) \end{pmatrix} \\ N_R = -\left(R_{C1} + R_{C2}\right)\begin{pmatrix} s^4C_{DSL}^2\left(L_{SL}^2 + L_{DL}^2 + 2L_{SL}L_{DL}\right) + s^3\,2C_{DSL}^2\left(L_{SL}R_{C1} + L_{SL}R_{C2} + L_{DL}R_{C1} + L_{DL}R_{C2}\right) \\ + s^2\,2C_{DSL}\left(L_{SL} + L_{DL}\right) + 1 \end{pmatrix} \end{cases} \tag{23}$$

The final step is to draw R_{SBR} verses C_{SBR} parametric curve by sweeping the variable s in (22), which gives the boundary of the region where all the roots of $\Delta(s)$ are real. Since the solutions to $\Delta(s) = 0$ are negative for a stable operation, the parameter s is swept on the negative real axis of the complex plane. Figure 8 shows the resulting parametric curve with the snubber components chosen

in the shaded region ensures suppression of switching oscillations. In addition to dampen the voltage vibrations, the snubber must also ensure minimum power losses. Therefore, the lower part of the critically damped region is more suitable as the C_{SBR} significantly affects snubber losses as compared to R_{SBR}.

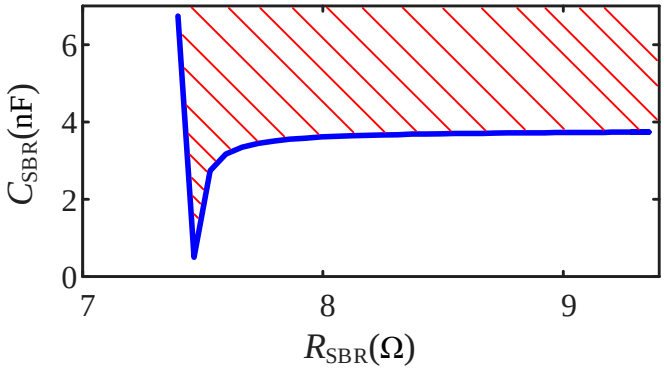


Figure 8. The parametric graph of snubber with the region where oscillation is suppressed.

5. Results and Discussion

In this section, the proposed gate driver performance is verified using computer simulation and experimental prototype of SiC half-bridge dc-ac converter. Specifications of the converter under study are given in Table 1. To simulate the Spice model of SiC MOSFET provided by Cree Inc., LTspice software is used with a step size of 1 ns. Parameters of SiC MOSFET, i.e., C3M0120090J related to the gate driving are listed in Table 2. For reduced conduction losses, 16 V turn-on gate-source voltage is recommended. Since the proposed circuit performs level shifting, therefore, a regulated 18.4 V gate driver source is applied to set +16 V and -2.4 V, as the on and off gate driving voltages respectively. Other specifications of the gate driver components based on its transient analysis are given in Table 3.

Table 1. Specifications of the SiC MOSFET based half-bridge dc-ac converter.

Parameter	Value
Source voltage (V_{IN})	100 V
Capacitor (C)	1.5 μF
Inductor (L)	33 μH
Load Resistance (R)	10 Ω
Switching frequency (f_s)	1 MHz

Table 2. Parameters of the C3M0120090J.

Parameter	Value
Threshold voltage	2.1 V
Intrinsic gate resistance	16 Ω
Maximum gate-source voltage	−8/+18
Input capacitance	350 pF
Output capacitance	40 pF
Reverse transfer capacitance	3 pF

Table 3. Parameters of the proposed gate driver.

Parameter	Value
R_{1L}	3 Ω
R_{2L}	3 Ω
D_{ZPL}	18 V
D_{ZNL}	5 V
C_{ZL}	1 μF

5.1. Simulation Results

The captured switching waveforms are shown in Figure 9, where the gate-source voltages are level shifted by 2.4 V. During the turn-on process of low-side MOSFET, the v_{GSL} rises to 16V in 5 ns thereby forcing drain-source voltage v_{DSL} to fall as shown in Figure 9a. Below 50 V, the change in v_{DSL} is high, i.e., 15 V/ns, and induces 1.7 V in v_{GSH}. A similar phenomenon is observed in the turning-off waveform shown in Figure 9b. However, due to the level shifted gate-source voltages, there is no spurious turn-on.

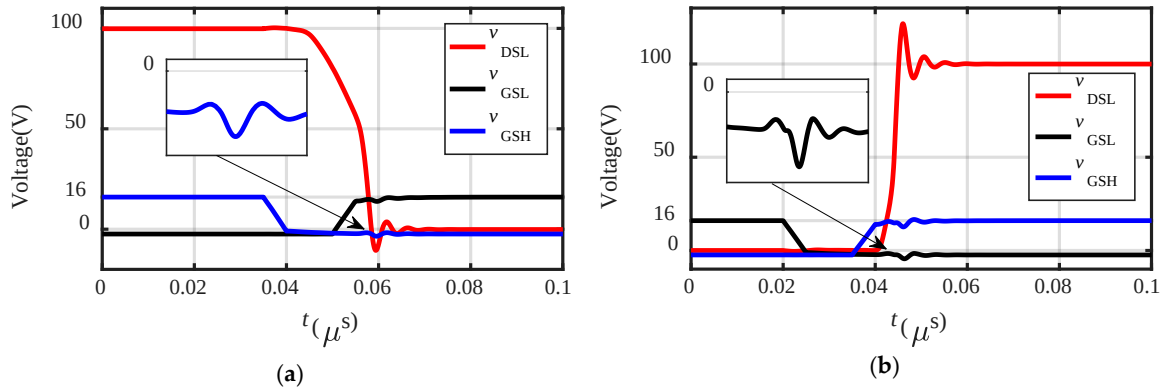


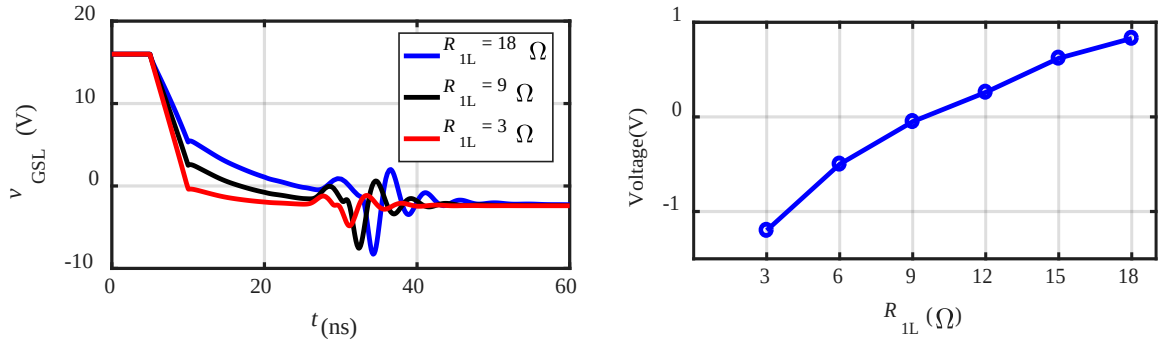
Figure 9. Switching waveform captured from simulation (**a**) during turn-on of low-side MOSFET (**b**) during turn-off of low-side MOSFET.

Moreover, using LTspice simulation the effect of gate resistance on the switching operation is investigated. Figure 10a shows the turning-off gate-source waveforms under 3 Ω, 9 Ω, and 18 Ω gate resistances. SiC MOSFET based half-bridge converter is simulated using the Spice model with inductances of 7.46 nH, 1.5 nH, and 7.06 nH added to the source, drain and gate terminals of each MOSFET respectively in order to verify the theoretically analyzed effects of parasitic elements. It is observed that the increase in gate resistance slows down the transition of gate-source voltage and results in higher spurious peaks, which can also be noted from the relationship between gate resistance R_{1L} and gate voltage spike, shown in Figure 10b. Thus, it is significantly important to choose a relatively lower R_{1L} to achieve the desired level shifting and protects the MOSFET from false turn-on. On the other hand, while choosing R_{2L} the high intrinsic gate resistance is particularly noteworthy as spurious turn-on can occur if the voltage drop across $R_{1L}//R_{2L}$ exceeds the gate threshold voltage. Therefore, R_{2L} is chosen same as R_{1L} to ensure the turning-off gate impedance as half of the turning-on counterpart.

Thus, it is concluded that the parasitic inductances negatively influence the switching response of SiC MOSFET, including voltage overshoot exceeding the steady-state drain-source voltage and high-frequency oscillations, thereby enlarging voltage stress and EMI noise. Moreover, since the source inductance couples the power and gate-loop, therefore, the ringing in drain-source voltage forces the gate-source voltage to oscillate accordingly.

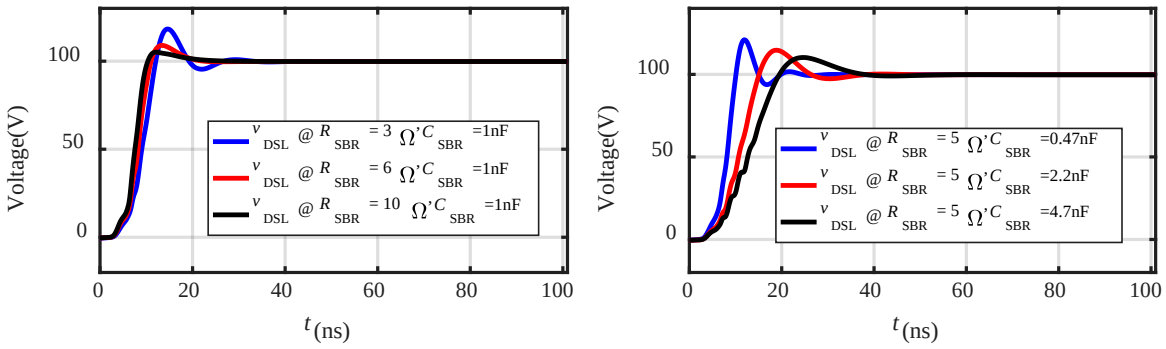
An *RC* snubber circuit is used to suppress such oscillations. Figure 11 shows the simulation results of voltage ringing using different snubber combinations. Figure 11a shows that raising the

R_{SBR} dampens the oscillations, while, the converter simulated for different C_{SBR} and R_{SBR} = 1 Ω is shown in Figure 11b, which indicates that raising C_{SBR} can also suppress the parasitic ringing. However, the power losses significantly increase by raising C_{SBR} [39]. Therefore, its minimum value is chosen for experimental implementation.



(**a**) (**b**)

Figure 10. (**a**) Gate-source voltage of low-side MOSFET under different R_{1L} values (**b**) relationship between R_{1L} and spurious peak voltage.



(**a**) (**b**)

Figure 11. Simulation results of voltage ringing for different snubber cases (**a**) C_{SBR} = 1 nF and R_{SBR} = 3, 6 and 10 Ω (**b**) R_{SBR} = 1 Ω and C_{SBR} = 0.47, 2.2 and 4.7 nF.

5.2. Experimental Results

Figure 12 shows the setup of a half-bridge dc-ac converter for experimental verification. An isolated driver IC (Si8234) from Silicon Labs incorporation is used, which can operate at elevated frequencies, source and sink high gate current, and show significant immunity to EMI. Since the driver circuit traces carry a high-frequency signal, therefore, they are routed on the same layer to prevent the propagation of noise to other layers. Furthermore, to ensure Equation (24) [18], the driver circuit is routed using wide (25 mil) and shortest possible traces.

$$L_G \frac{di_G}{dt} < I_R \frac{1}{g_{fs}} 10\% \tag{24}$$

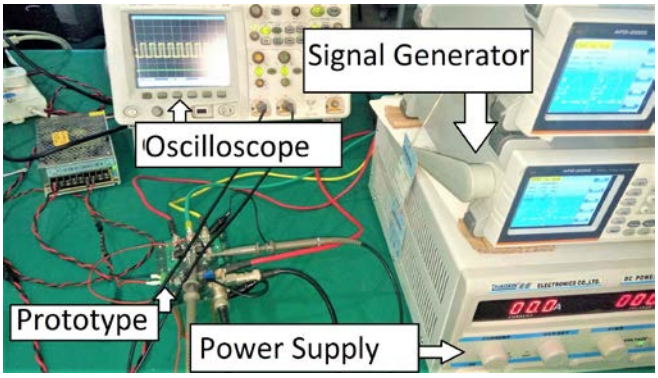


Figure 12. Experimental setup of the half-bridge dc-ac converter with the proposed gate driver.

The symbol I_R represents the rated current, g_{fs} is the transconductance of SiC MOSFET, and L_G is the parasitic gate inductance. Since the stray input capacitance is fixed, thereby, minimizing L_G is effective in improving the damping of gate voltage resonance. In addition, a 10 kΩ gate-source resistor is connected, which is also useful in suppressing gate voltage oscillations.

Figure 13 shows the experimental gate voltage waveform v_{GSL} generated using the proposed gate driver at the 1 MHz switching frequency. The driver sets the turn-on and turn-off voltage to 16.5 V and −2.4 V respectively. The −2.4 V offset in gate voltage validates the basic level shifting capability of the gate driver. Moreover, Figure 14a,b show the turn-off and turn-on transition of the low-side MOSFET, respectively. Although, the spurious spike in gate-source voltage introduced by the fast-rising v_{DSL} is below the gate threshold voltage, but the oscillations in v_{GSL} are alarming due to the higher peaks. The ringing in v_{DSL} due to circuit parasitics forces v_{GSL} to oscillate, which can cause the crosstalk as well as stressing the device by exceeding the negative gate voltage limit. Therefore, *RC* snubber is used to dampen the parasitic ringing and thus increase the immunity to the crosstalk phenomenon and the gate breakdown. Figure 15 shows the gate-source and drain-source voltage waveforms of low-side MOSFET for two different *RC* snubbers. The waveform in Figure 15a shows the measured v_{DSL} and v_{GSL} when C_{SBR} = 440 pF and R_{SBR} = 10 Ω, resulting in a voltage overshoot of 41 V and settling time of 90 ns. For measurement of Figure 15b, C_{SBR} has been raised to 1 nF, which reduces the voltage overshoot to 27 V and settling time to 54 ns. The results indicate that the assumption $L_{SH} = L_{DH} = 0$ leads to a mismatch between the experimental and mathematically derived parametric curves, and thus, the snubber selected using valley in the non-oscillatory region of Figure 8 is not viable. It is vital to choose high-valued R_{SBR} to improve damping rather than C_{SBR} to maintain relatively low power losses.

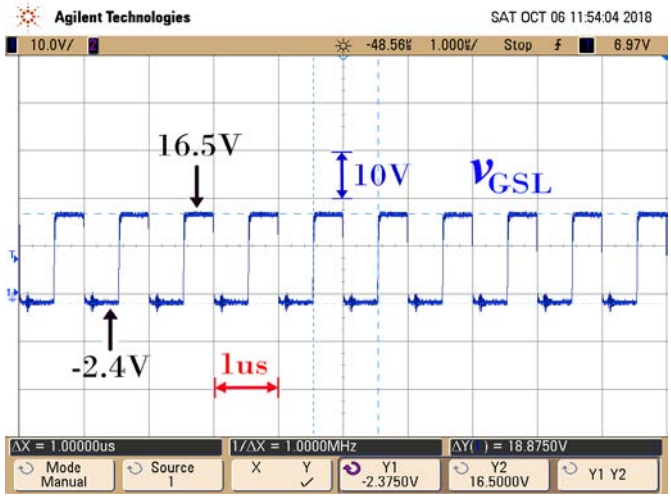
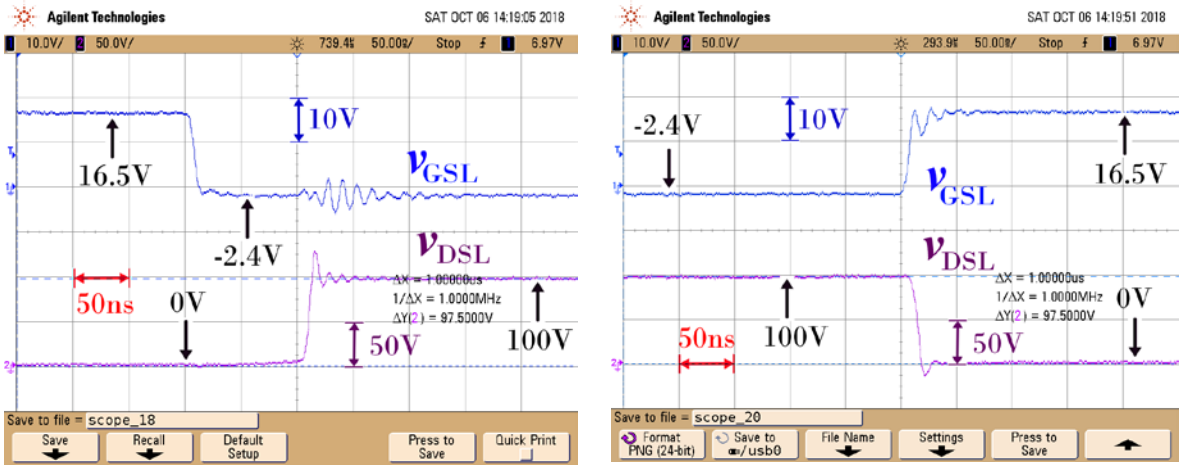
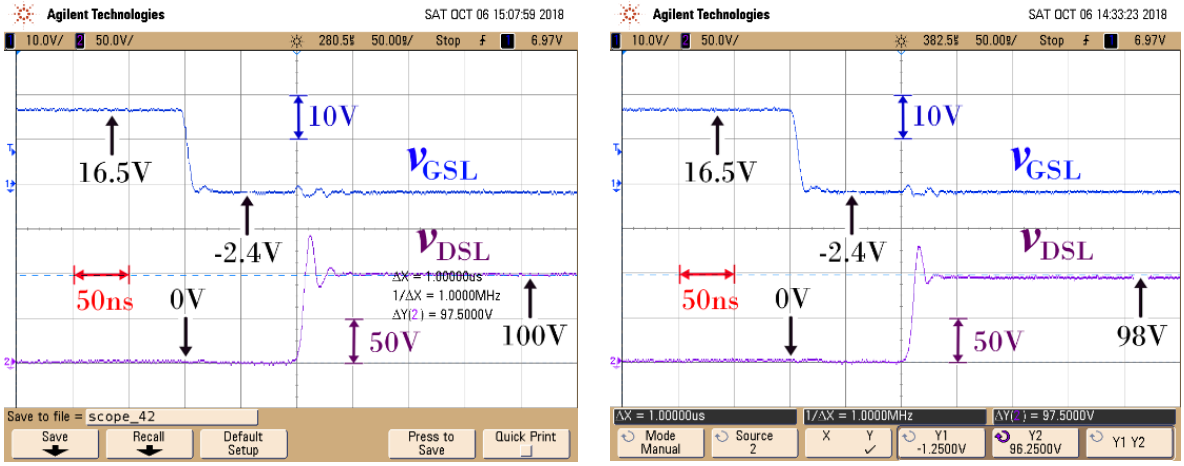


Figure 13. Experimental gate-source voltage waveform of low-side MOSFET.



(**a**) (**b**)

Figure 14. Experimental switching waveforms without snubber (**a**) turn-off, and (**b**) turn-on of low-side SiC MOSFET.



(**a**) (**b**)

Figure 15. Experimental turning-on waveforms with *RC* snubber using (**a**) C_{SBR} = 440 pF and R_{SBR} = 10 Ω, and (**b**) C_{SBR} = 1 nF and R_{SBR} = 10 Ω.

5.3. Limitations of the Proposed Gate Driver and the Snubber Design Technique

Although the proposed level shifter circuit relaxes the gate driver layout by getting rid of the additional negative voltage supply, but at the same time it relatively lowers the performance bar. The important concern is that the introduction of the capacitor C_{ZL} in the gate loop delays the turn-on transition of the SiC MOSFET. Moreover, v_N requires several switching cycles at the start-up to rise up to the zener voltage V_Z, and thus the negative turn-off voltage as determined by v_N gradually increases in magnitude V_Z. Finally, the negative voltage generated using the level shifter circuit is prone to parasitic oscillations, which can force gate voltage to exceed the negative limit, as a result overstressing the SiC MOSFET.

The snubber design technique presented in the paper predicts a region in the R_{SBR}-C_{SBR} plane where the switching ringing is suppressed. However, the accuracy of parasitic inductances and capacitances in the power loop determines the matching of the region derived using analytical equations with the experimental counterpart. Although, the manufacturer provides device specifications, but for computation of interconnection inductance, programs driven by the finite-element algorithm such as Maxwell 3D is required.

6. Conclusions

To improve the immunity against crosstalk phenomena, a gate driver has been proposed for SiC MOSFET capable of generating the negative turn-off voltage without using a negative power supply. Unlike the voltage divider based level shifters, the proposed circuit adds a negative offset to the gate-source voltage using reduced components with no additional resistor in the gate loop, thereby not affecting the efficiency. The effectiveness of the level shifter circuit has been validated by driving the SiC MOSFET in the half-bridge dc-ac converter at a switching frequency of 1 MHz which is 10 times higher than the RCD counterpart. Moreover, oscillation due to circuit parasitics are modeled, and guidelines for PCB layout to minimize the interconnection inductances are recommended. It is emphasized that due to unavoidable parasitic inductances, certain voltage ringing still exists which encourages passive damping. A procedure for the *RC* snubber design has been presented to avoid the trial and error based design. The snubber circuit has successfully lowered the gate voltage spike by 2.56 V and reduced the damping time by 63 ns.

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Conflicts of Interest: There is no conflict of interest.

Nomenclature

V_{IN}	Source voltage
C	Output stage capacitor filter
C_1/C_2	DC-link capacitors
L	Output stage inductor filter
R	Load resistance
f_s/T_s	Switching frequency/switching time period
V_{TH}	Threshold voltage
V_{MIL}	Miller voltage
S_L/S_H	Low-side/high-side MOSFET of half-bridge converter
R_{ONL}/R_{ONH}	Conduction resistance of low-side/high-side MOSFET
C_{GSL}/C_{GSH}	Parasitic gate-source capacitance of low-side/high-side MOSFET
C_{DGL}/C_{DGH}	Parasitic drain-gate capacitance of low-side/high-side MOSFET
C_{DSL}/C_{DSH}	Parasitic drain-source capacitance of low-side/high-side MOSFET
L_{DL}/L_{DH}	Parasitic drain inductance of low-side/high-side MOSFET
L_{SL}/L_{SH}	Parasitic source inductance of low-side/high-side MOSFET
$R_{GL(in)}/R_{GH(in)}$	Internal gate resistance of low-side/high-side MOSFET
R_{IL}/R_{TL}	External gate turn-on/turn-off resistance of low-side MOSFET
D_{ZPL}/D_{ZNL}	Zener diode for positive/negative overvoltage gate protection
C_{ZL}/D_{ZL}	Capacitor/zener diode of the Level shifter circuit
v_N/V_Z	Voltage across C_{ZL}/zener voltage of D_{ZL}
V_G	Gate driver supply voltage
L_G	Parasitic gate inductance
v_{GSL}/v_{GSH}	Gate-source voltage of low-side/high-side MOSFET
v_{DSL}/v_{DSH}	Drain-source voltage of low-side/high-side MOSFET
i_{DL}/i_{DH}	Drain-source current of low-side/high-side MOSFET
i_{GPL}/i_{GNL}	Low-side gate current in turning-on/turning-off of MOSFET
i_{CL}/i_{ZL}	Current through C_{ZL}/D_{ZL}
D_m	Maximum duty cycle
τ_a/τ_b	Time constant of gate loop during turn-on when ($v_N < V_Z$)/($v_N = V_Z$)
τ_c	Time constant of gate loop during turn-off
i_{SBR}/I_{SBR}	Snubber current in time-domain/s-domain
g_{fs}	transconductance of MOSFET

ω_r/ζ	Parasitic resonance frequency/damping factor
R_{SBR}/C_{SBR}	Snubber resistor/capacitor
R_{C1}/R_{C2}	Equivalent series resistance of C_1/C_2
WBG	Wide band-gap devices
GaN	Gallium Nitride
SiC	Silicon carbide
THD	Total harmonic distortion
PCB	Printed circuit board
EMI	Electromagnetic interference
RC	Resistor-capacitor

References

1. Li, K.; Evans, P.; Johnson, M. SiC/GaN power semiconductor devices: a theoretical comparison and experimental evaluation under different switching conditions. *IET Electr. Syst. Transp.* **2018**, 8, 3–11.
2. Jung, D.Y.; Park, Y. Design and Evaluation of Cascode GaN FET for Switching Power Conversion Systems. *ETRI J.* **2017**, 39, 62–68.
3. Logan, T.; McMahon, R.; N. Hari. Design considerations for 600 V GaN cascode based half-bridge converter systems for utility based applications. In Proceedings of the 2016 IET International Conference on Power Electronics, Machine and Drives, Glasgow, UK, 19–21 April 2016, pp. 1–6.
4. Yamaguchi, K.; Sasaki, Y.; Imakubo, T. Low loss and low noise gate driver for SiC-MOSFET with gate boost circuit. In Proceedings of the 2014 Annual Conference of the IEEE Industrial Electronics Society, Dallas, TX, USA, 29 October–1 November 2014, pp. 1594–1598.
5. Peftitsis, D.; Rabkowski, J. Gate and Base Drivers for Silicon Carbide Power Transistors: An Overview. *IEEE Trans. Power Electron.* **2016**, 31, 7194–7213.
6. Camacho, A.P.; Sala, V.; Ghorbani, H.; Martinez, J.L.R. A Novel Active Gate Driver for Improving SiC MOSFET Switching Trajectory. *IEEE Trans. Ind. Electron.* **2017**, 64, 9032–9042.
7. Zeng, Z.; Li, X. Comparative Study on Multiple Degrees of Freedom of Gate Drivers for Transient Behavior Regulation of SiC MOSFET. *IEEE Trans. Power Electron.* **2018**, 33, 8754–8763.
8. Wu, T. Cdv/dt induced turn-on in synchronous buck regulators. *Int. rectifier Tech. Rep.* **2007**, 2, 2–7.
9. Li, H.; Liao, X; Hu, Y.; Huang, Z.; Wang, K. Analysis of voltage variation in silicon carbide MOSFETs during turn-on and turn-off. *Energies* **2017**, 10, 1456.
10. Chen, H.; Divan, D. High speed switching issues of high power rated silicon-carbide devices and the mitigation methods. In Proceedings of the 2015 IEEE Energy Conversion Congress and Exposition, Montreal, QC, Canada, 20–24 September 2015, pp. 2254–2260.
11. Zaman, H.; Zheng, X.; Yang, M.; Ali, H.; Wu, X.; A SiC MOSFET based high efficiency interleaved boost converter for more electric aircraft. *J. Power Electron.* **2018**, 18, 23–33.
12. Liu, H.; Huang, X.; Lin, F.; Yang, Z. Loss Model and Efficiency Analysis of Tram Auxiliary Converter Based on a SiC Device. *Energies* **2017**, 10, 2018.
13. Zheyu, Z.; Wang, F. Active gate driver for fast switching and cross-talk suppression of SiC devices in a phase-leg configuration. In Proceedings of the 2015 IEEE Applied Power Electronics Conference and Exposition, Charlotte, NC, USA, 15–19 March 2015, pp. 774–781.
14. Abbatelli, L.; Brusca, C.; Catalisano, G. Application note: How to fine tune your SiC MOSFET gate driver to minimize losses. Available online: https://www.stmicroelectronics.com.cn/content/ccc/resource/technical/document/application_note/7d/2b/9d/f0/88/07/4b/6f/DM00170577.pdf/files/DM00170577.pdf/jcr:content/translations/en.DM00170577.pdf (accessed on 7 June 2017)
15. Wang, J.; Chung, H.S.H. A novel RCD level shifter for elimination of spurious turn-on in the bridge-leg configuration. *IEEE Trans. Power Electron.* **2015**, 30, 976–984.
16. Zhou, Q.; Gao, F.; Jiang, T. A gate driver of SiC MOSFET with passive triggered auxiliary transistor in a phase-leg configuration. In Proceedings of the 2015 Energy Conversion Congress and Exposition, Montreal, QC, Canada, 20–24 September 2015, pp. 7023–7030.
17. Noppakunkajorn, J.; Han, D.; Sarlioglu B. Analysis of high-speed PCB with SiC devices by investigating turn-off overvoltage and interconnection inductance influence. In Proceedings of the 2014 Applied Power Electronics Conference and Exposition, Fort Worth, TX, USA, 16–20 March 2014, pp. 2628–2634.

18. Qin, H.; Ma, C.; Zhu, Z.; Yan, Y. Influence of parasitic parameters on switching characteristics and layout design considerations of SiC MOSFETs. *J. Power Electron.* **2018**, 18, 1255–1267.
19. Chen, Z.; Yao, Y.; Boroyevich, D.; Ngo, K.; Mattavelli, P. Exploration of a switching loop snubber for parasitic ringing suppression. In Proceedings of the 2014 IEEE Energy Conversion Congress and Exposition, Pittsburgh, PA, USA, 14–18 September 2014, pp. 1605–1612.
20. Ren, Y.; Yang, X.; Zhang, F.; Tan, L.; Zeng X. Analysis of a low-inductance packaging layout for Full-SiC power module embedding split damping. In Proceedings of the 2016 IEEE Applied Power Electronics Conference and Exposition, Long Beach, CA, USA, 20–24 March, pp. 2102–2107.
21. Palmer, P.R.; Zhang, J.; Zhang, X. SiC MOSFETs Connected in Series with Active Voltage Control. In Proceedings of the 2015 IEEE 3rd Workshop on Wide Bandgap Power Devices and Applications, Blacksburg, VA, USA, 2–4 November 2015, pp. 60–65.
22. Huang, H.; Yang, X.; Wen, Y.; Long, Z. A switching ringing suppression scheme of SiC MOSFET by Active Gate Drive. In Proceedings of the 2016 IEEE 8th International Power Electronics and Motion Control Conference, Hefei, China, 22–26 May 2016, pp. 285–291.
23. Han, D.; Sarlioglu, B. Comprehensive Study of the Performance of SiC MOSFET-Based Automotive DC-DC Converter under the Influence of Parasitic Inductance. *IEEE Trans. Ind. Appl.***2016**, 52, 5100–5111.
24. Li, L.; Ning, P.; Duan, Z.; Zhang, D.; Wen, X.; Qiu, Z. A study on the effect of DC-link decoupling capacitors. In Proceedings of the 2017 IEEE Transportation Electrification Conference and Expo, Asia-Pacific, Harbin, China, 7–10 August 2017, pp. 4845–4850.
25. Kim, J.; Shin, D.; Sul, S. K. A Damping Scheme for Switching Ringing of Full SiC MOSFET by Air Core PCB Circuit. *IEEE Trans. Power Electron.* **2018**, 33, 4605–4615.
26. Vaculik, P. The Experience with SiC MOSFET and Buck Converter Snubber Design. *Int. J. Elect., Comput. Energ. Commun.* **2014**, 8, 49–54.
27. Yatsugi, K.; Nomura, K.; Hattori, Y. Analytical Technique for Designing an RC Snubber Circuit for Ringing Suppression in a Phase-Leg Configuration. *IEEE Trans. Power Electron.* **2018**, 33, 6, 4736–4745.
28. Gao, F.; Zhou, Q.; Wang, P.; Zhang, C. A Gate Driver of SiC MOSFET for Suppressing the Negative Voltage Spikes in a Bridge Circuit. *IEEE Trans. Power Electron.* **2018**, 33, 2339–2353.
29. Nayak, P.; Krishna, M. V.; Vasudevakrishna, K.; Hatua, K. Study of the effects of parasitic inductances and device capacitances on 1200 V, 35 A SiC MOSFET based voltage source inverter design. In Proceedings of the 2014 IEEE International Conference on Power Electronics, Drives and Energy Systems, Mumbai, India, 16–19 December 2014, pp. 1–6.
30. Wang, Z.; Zhang, J.; Wu, X.; Sheng, K. Analysis of stray inductance's influence on SiC MOSFET switching performance. In Proceedings of the 2014 IEEE Energy Conversion Congress and Exposition, Pittsburgh, PA, USA, 14–18 September 2014, pp. 2838–2843.
31. Han, D.; Lee, W.; Noppakunkajorn, J.; Sarlioglu, B. Investigating the influence of interconnection parasitic inductance on the performance of SiC Based DC-DC converters in hybrid vehicles. In Proceedings of the 2014 IEEE Transportation Electrification Conference and Expo, Dearborn, MI, USA, 15–18 June 2014, pp. 1–7.
32. Anthon, A.; Hernandez, J. C.; Zhang, Z.; Andersen M . A. E. Switching investigations on a SiC MOSFET in a TO-247 package. In Proceedings of the 2014 Conference of the IEEE Industrial Electronics Society, Dallas, TX, USA, 29 October–1 November 2014, pp. 1854–1860.
33. White Paper. Optimizing PCB Layout. 2014. Available online: https://epc-co.com/epc/Portals/0/epc/documents/papers/Optimizing%20PCB%20Layout%20with%20eGaN%20FETs.pdf (accessed on 7 June 2017)
34. Application Note. PCB layout considerations for non-isolated switching power supplies. Available online: https://www.analog.com/media/en/technical-documentation/application-notes/an136f.pdf (accessed on 7 June 2017)
35. Application Note. Thermal Considerations for a Class D Amplifier 2006. Available online: https://www.maximintegrated.com/en/app-notes/index.mvp/id/3879 (accessed on 7 June 2017)
36. Application Note. RC Snubber for Class-D Audio Amplifiers 2018. Available online: https://statics.cirrus.com/pubs/appNote/AN0454REV1.pdf (accessed on 7 June 2017)
37. Application Note. Snubber circuits for power electronics 2008. Available online: https://rudys.typepad.com/files/snubber-e-book-complete.pdf (accessed on 7 June 2017)

38. Wang, X.; Shi, J.; Li, T.; Sun, Y. Active closed-loop gate voltage control method to mitigate metal-oxide semiconductor field-effect transistor turn-off voltage overshoot and ring. *IET Power Electron.* 2013, 6, 1715–1722.
39. Torsaeter, B.N.; Tiwari, S.; Lund, R.; Midtgard,. M. Experimental evaluation of switching characteristics, switching losses and snubber design for a full SiC half-bridge power module. 2016 IEEE 7th International Symposium on Power Electronics for Distributed Generation Systems, Vancouver, BC, Canada, 27–30 June 2016, pp. 1–8.