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A Wide Load Current and Voltage Range Switched Capacitor DC–DC Converter with Load Dependent Configurability for Dynamic Voltage Implementation in Miniature Sensors

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Received: 19 October 2018; Accepted: 6 November 2018; Published: 8 November 2018

Abstract: Advancements in low power circuits and batteries have enabled the design of miniature sensors with tiny batteries. In such systems, implementing dynamic voltage scaling (DVS) is crucial for maximizing system lifetime. In this paper, a new switched capacitor (SC) converter that is capable of handling a wide range of load currents and output voltages is presented for on-chip DVS implementation. The proposed converter consists of multi-ratio multi-leaf SC stages and reconfigurable interconnect, enabling fine voltage resolution. The stage interconnect scheme enables cascaded or parallel connection of stages. The multi-leaf structure allows load-dependent switch size selection, offering a better trade-off between losses over a wide load range. A limited-voltage-swing switch-driving scheme allows efficient down-conversion from high battery voltage input. A prototype was fabricated in a 180 nm process, providing an output voltage with effective resolution of 16 mV over a load current range of 300 nA to 300 µA (1000×) from a 4 V battery. Efficiency greater than 62% and a peak efficiency of 77% are achieved under a light load (500 nA) over a voltage range of 400 mV to 1.6 V. Efficiency greater than 64% and a peak efficiency of 72% are achieved under a heavy load (200 µA) over a voltage range of 700 mV to 1.6 V.

Keywords: switched capacitor circuits; DC–DC converter; dynamic voltage scaling; internet of things; wireless sensor network; low power electronics

1. Introduction

With the recent advancements in low power circuit design, packaging and battery technologies, the volumes of computing systems have been significantly reduced. With such a trend, numerous mm-scale miniature sensors have been demonstrated over the last decade [1–3]. These miniature sensors have been drawing attention since they can make traditional sensor systems more effective and energy-efficient. At the same time they also enable new volume-constrained applications such as implanted medical diagnostic sensors and monitoring sensors for an access-limited environment. However, the biggest concern for such miniature systems is the operation lifetime. Therefore, optimizing the use of energy stored in a battery is a key design goal for battery powered miniature sensor systems [1].

Miniature sensor systems are typically designed to spend most of their time in standby mode to minimize power consumption and maximize battery lifetime [1,2] but are periodically activated for short periods of time to perform their designated functions. During standby mode, the current

consumption of such systems is on the order of sub-microamperes. On the other hand, the active mode current consumption ranges from a few microamperes to hundreds of microamperes depending on the task being performed [3]. Therefore, the power management unit in miniature sensor systems should be able to efficiently handle a load current ranging from sub-microamperes to hundreds of microamperes.

To minimize standby power, the supply voltage needs to be reduced to the minimum voltage level at which data can be retained in standby mode. Conversely, in active mode, the supply voltage should be increased for better performance and stable operation [4,5]. This implies that the power management unit in miniature sensor systems should also be capable of handling a wide voltage range.

Providing a wide range of voltage conversion ratios for DC–DC conversion is also an important feature for the power management unit in miniature sensors. To enable dynamic voltage scaling (DVS) for energy efficient operation, a range of output voltages should be generated from the fixed battery voltage. Moreover, since the battery voltage can also vary over time, various conversion ratios are also required to provide constant regulated voltage.

Switched capacitor (SC) DC–DC converters are good candidates for power management units in miniature systems. By utilizing integrated capacitors as passive elements, they can provide fully integrated solutions that are capable of handling microwatts of power. This enables a cost-effective small form factor, which typically cannot be offered with inductor-based buck converters, where one of the following is required: a bulky off-chip inductor [6–8]; an expensive on-chip inductor [9,10]; or a complicated post-fabrication process [11]. The large conversion ratio requirement also prohibits the use of low dropout regulators (LDOs) in such systems since the efficiency of an LDO is proportional to its conversion ratio [12–14].

However, some challenges must be overcome for SC converters to fulfill the aforementioned requirements. SC converters can provide only rational conversion ratios, which can be represented as

$$V_{OUT} = \frac{n}{m} \cdot V_{IN} \tag{1}$$

where 'n' and 'm' are integers determined by the converter topology. This implies that SC converters can only provide limited resolution on regulated voltage, which complicates the implementation of DVS for efficient operation. Moreover, maintaining efficient operation in both active and standby modes is also non-trivial: it requires efficient clock generation over a wide frequency range and driving switches with limited voltage swing may be required since the switching loss with full battery voltage swing can be significant in standby modes.

A number of SC DC–DC converter topologies applicable to miniature systems have been reported in recent years [15–22]. Many single-stage SC structures [15–19] have been introduced that provide very high efficiency but only at a few ratios, which limits their application to a narrow voltage range. A few multi-stage SC converters, such as successive approximation (SAR) [20], recursive-tertiary [21], and recursive-binary [22] DC–DC converters, have been reported that provide high efficiency over a wide output voltage range. However, these converters are only optimized for active operation state, and the minimum load current is on the order of a few microamperes. Therefore, the efficiency of these architectures in standby mode is low. For example, the efficiency of SAR [20] at near threshold voltage (0.4–0.7 V) degrades drastically to less than 40% when the load current reaches 1 µA or less. A reconfigurable SC structure presented in [21] achieves a higher number of conversion ratios with fewer SC stages, but with full input voltage (2.5 V) swing switch driving. Such full-swing switch-driving is acceptable with heavy load condition, since conduction loss is the dominant loss. However, with a light load condition in standby mode, which could be the dominant operating mode in heavy duty-cycled wireless sensor nodes (WSN) and IoT systems, switching loss become the dominant loss contributor and driving switches with voltages significantly higher than their threshold voltage can be a waste of power, resulting in inefficient operation in standby mode. Since the WSNs often

utilize high energy density batteries with high output voltage (~4 V), unnecessary loss with full-swing switch-driving can be significant.

In this paper, a multi-stage and multi-leaf reconfigurable SC converter with load-dependent reconfigurability and limited-swing switch-driving scheme [23] is presented. The proposed converter consists of multi-ratio multi-leaf SC stages and reconfigurable interconnect, enabling fine voltage resolution with switch width modulation, which is required for DVS over a broad load current range. The reconfigurable stage interconnect (RSI) scheme allows cascaded or parallel connection of stages depending on the output voltage and current demand. The multi-leaf structure allows load-dependent switch size selection, offering a better trade-off between conduction loss and switching loss over a broad current range. A symmetric leakage-based clock generator allows efficient clock generation over a wide frequency range with balanced duty cycle. As switching loss is proportional to the square of the driving voltage, the full input voltage swing driving scheme degrades efficiency at the voltage conversion from high battery voltage. The proposed SC converter switches are driven by a limited voltage swing driving scheme, which makes switching loss independent of input voltage, enabling efficient voltage conversion with high battery voltage.

Various types of batteries can be used for powering miniature systems. Depending upon the battery type, the output voltage may vary from 1.2 to 4.0 V [15–22]. This work uses a Li-ion battery where the voltage can vary from 3.6 to 4.2 V. This is typically the maximum voltage level used for stand-alone miniature systems and thus represents the worst case scenario. The same structure applied at a lower input voltage (e.g., 2.0 V) can result in improved efficiency.

For power electronics applications with at least a few milli-watts of power, electromagnetic interference (EMI) analysis, like that presented in [24–26] is essential to determine compliance to the EMI regulations for satisfactory operation of nearby circuits. However, the proposed SC converter is implemented for low power applications, where maximum power demand is less than 1 mW, and fully integrated implementation makes EMI negligible. Therefore, EMI analysis of the proposed SC converter has not been considered in this work.

The remainder of this paper is organized as follows: Section 2 provides a detailed analysis of the loss mechanisms in the SC converter at varying operating conditions. Then the detailed architecture of the proposed converter is presented in Section 3. In Section 4, the measurement results are shown to verify the effectiveness of the proposed approach, and Section 5 concludes the paper.

2. Loss Analysis and Power Delivery Capability of an SC Converter

In SC converters, there are two fundamental loss mechanisms, namely conduction loss and switching loss. As the output load current and voltage change, both of these losses can vary drastically; hence, careful balancing between these losses is required for optimized power delivery. Therefore, analyzing the trade-off between these losses is the first step in implementing an efficient SC converter suitable for operation over wide voltage and current ranges.

SC converters rely on energy and charge transfer between flying capacitors, which act as voltage sources. Since the voltage conversion is achieved by connecting flying capacitors in series or parallel, the voltage generated by an SC stage is determined by its topology and the summation or subtraction of flying capacitor voltages. Therefore, unlike the inductor-based converters where conversion ratios can be continuously adjusted by controlling the switching frequency or duty cycle, only discrete conversion ratios can be generated with SC converters.

The number of available conversion ratios in an SC stage is determined by the number of flying capacitors and charge transfer phases per operation cycle. For a given number of flying capacitors, more voltage conversion ratios can be implemented by increasing the number of charge transfer phases [21]. However, this limits the net conduction time of each transistor, resulting in reduced efficiency. For example, each phase lasts up to 50% in a 2-phase operation and up to 33% in a 3-phase operation. Therefore, assuming the same operation frequency, a 3-phase operation requires a larger switch to conduct the same amount of charge in a shorter conduction time, resulting in greater switching loss.

This work focuses on the efficient operation of an SC converter over varying load currents and voltages, including light load cases where the control and drivers are the dominant loss. A 2-phase clock is used owing to the simple drivers and control schemes.

To illustrate the basic tradeoff between switching and conduction loss, a simple 2:1 step-down SC converter, shown in Figure 1, was analyzed at light and heavy load conditions. Table 1 provides a list of the parameters used in analysis and their measurement units. The converter presented in Figure 1 operates with a 2-phase non-overlapping clock. During phase ϕ_1, the top and bottom terminals of C_{FLY1} are connected to the battery (V_{IN}) and output (V_{OUT}), respectively; thus, drawing charge from the battery as charges are taken at the output node. On the other hand, C_{FLY2} is connected between V_{OUT} and ground (V_{SS}), supplying charge to the output node. During phase ϕ_2, the flying capacitors switch their positions such that C_{FLY2} is charged, and C_{FLY1} is discharged. Periodic charging and discharging of the flying capacitors results in ripple voltage (ΔV) at the flying capacitors, which can be written as

$$\Delta V = \frac{I_{LOAD}}{2C_{FLY}f_{SW}} \tag{2}$$

where I_{LOAD} is the load current, and f_{SW} is the switching frequency. Such ripple incurs power loss, which can be categorized as conduction loss. This is an inevitable loss in SC converters because power is delivered through charge transfer via transistors, and a voltage difference between source and drain is required for charge transfer to be enabled. The conduction loss due to ripple voltage, as investigated in detail in [27,28], can be given as

$$P_{Cond.\Delta V} = I_{LOAD}.\frac{\Delta V}{2} = \frac{I^2{}_{LOAD}}{K_C C_{FLY} f_{SW}} \tag{3}$$

where K_C is the loss coefficient related to the converter topology. Ideally, switches in SC converters are assumed to have zero resistance, but real switches have finite resistance, which leads to additional conductance loss. Conduction loss due to switch resistance is given in [27] as

$$P_{Cond.Sw} = \frac{I^2{}_{LOAD} R_{ON} K_{SW}}{W_{SW}} \tag{4}$$

where R_{ON} is the switch resistance per unit width during the "on" state, W_{SW} is the total width of the switches, and K_{SW} is the topology-dependent loss coefficient. Therefore, the total conduction loss can be calculated by adding the loss due to voltage ripple and the switch conduction loss as follows:

$$\begin{aligned} P_{Cond} &= P_{Cond.\Delta V} + P_{Cond.Sw} \\ P_{Cond} &= \frac{I^2{}_{LOAD}}{K_C C_{FLY} f_{SW}} + \frac{I^2{}_{LOAD} R_{ON} f_{SW}}{W_{SW}} \end{aligned} \tag{5}$$

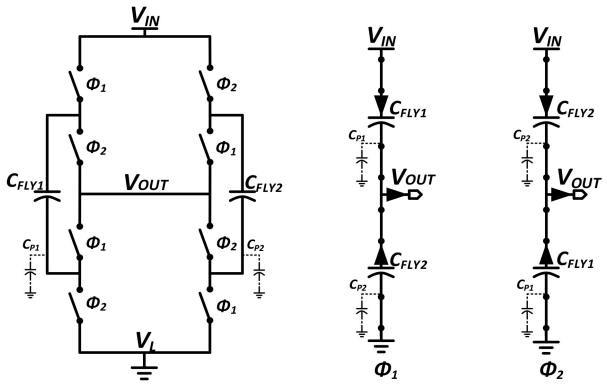

Figure 1. A 2-phase 2:1 step down switched capacitor (SC) converter.

Table 1. Parameters summary.

Abbreviation	Description	Unit
ΔV	Ripple voltage	mV
I_{LOAD}	Load current	A
f_{SW}	Switching frequency	Hz
C_{FLY}	Flying capacitors capacitance	F
K_C	Ripple conduction loss coefficient	Constant
R_{ON}	Switch resistance per unit width	Ω·m
K_{SW}	Switch resistance conduction loss coefficient	Constant
W_{SW}	Total width of switches	m
K_P	Capacitor parasitic loss coefficient	Constant
V_{OUT}	Output voltage	V
C_P	Flying capacitors bottom plate parasitic capacitance	F
V_{SW}	Gate drive voltage swing	V
C_{Gate}	Net switch gate capacitance	F
V_{drop}	Voltage deviation from ideal no load voltage	V
K_L	Net loss coefficient	Constant

The other type of loss in SC converters is switching loss. One of the major contributors to switching loss is the parasitic capacitance associated with flying capacitors. For on-chip capacitors, both the top and bottom plates have associated parasitic capacitances. For simplicity, the switching loss associated with the top and bottom plate parasitic capacitances is referred to as bottom plate switching loss ($P_{Sw.Bot}$) since the bottom plate parasitic capacitance is much larger than the top plate parasitic capacitance in most integrated capacitors. For the converter in Figure 1, the parasitic capacitor C_{P1} associated with C_{FLY1} is charged to the output voltage (V_{OUT}) during ϕ_1. During the following phase, ϕ_2, C_{P1} is discharged to ground, resulting in bottom plate switching loss defined as

$$P_{Sw.Bot} = K_P {V^2}_{OUT} C_P f_{SW} \tag{6}$$

where K_P is the topology-dependent loss coefficient.

Another type of switching loss is the power consumed for the driving gate capacitances of all of the switches. This loss can be written as

$$P_{Sw.Gate} = {V^2}_{SW} C_{Gate} f_{SW} \tag{7}$$

where V_{SW} is the voltage swing at the gate, and C_{Gate} is the total gate capacitance. Adding Equations (6) and (7) yields the total switching loss (P_{SW}):

$$P_{Sw} = [K_P {V^2}_{OUT} C_P f_{SW}] + \left[{V^2}_{Sw} C_{Gate} f_{SW}\right] \tag{8}$$

Therefore, adding Equations (5) and (8) provides the total loss in an SC converter (P_{LOSS}) as follows:

$$P_{LOSS} = \left[\left(\frac{{I^2}_{LOAD}}{K_C C_{FLY} f_{SW}}\right) + \left(\frac{{I^2}_{LOAD} R_{ON} K_{SW}}{W_{SW}}\right)\right] + \left[\left(K_P {V^2}_{OUT} C_P f_{SW}\right) + \left({V^2}_{SW} C_{Gate} f_{SW}\right)\right] \tag{9}$$

The above equation provides insight on the tradeoff between conduction loss and switching loss in an SC converter. For conduction loss, f_{SW} and W_{SW} are in the denominator, whereas for switching loss, f_{SW} and C_{Gate} are in the numerator. Both W_{SW} and C_{Gate} are proportional to the switch size. This implies that increasing the operation frequency and transistor width will reduce conduction loss and increase switching loss, whereas decreasing the frequency and transistor width will have the opposite effect.

Meanwhile, the power delivery capability (P_{LOAD}) of an SC converter can be defined as [16]

$$P_{LOAD} = K_L C_{FLY} V_{OUT} V_{drop} f_{SW} \quad (10)$$

where K_L is the loss coefficient that is dependent upon the SC converter topology, and V_{drop} is the deviation from the ideal no-load voltage (V_{NL}). Equation (10) indicates that a light load can be provided with a small V_{drop} at a low f_{SW}, resulting in an optimal operating voltage (V_{OPT}) near V_{NL}. In contrast, heavy load operation results in a large V_{drop} at a high f_{SW}, resulting in a V_{OPT} much lower than V_{NL}.

Figure 2 presents the simulation results for a 2:1 down-conversion with 2 V input (V_{NL} = 1 V) in a single stage of the SC converter shown in Figure 1. The required operation frequency and power losses expressed as percentages are plotted as functions of the output voltage. For simulation, the parasitic capacitances C_P are kept at 3% of the flying capacitance, which is a typical value for high metal layer metal–insulator–metal (MIM) capacitors.

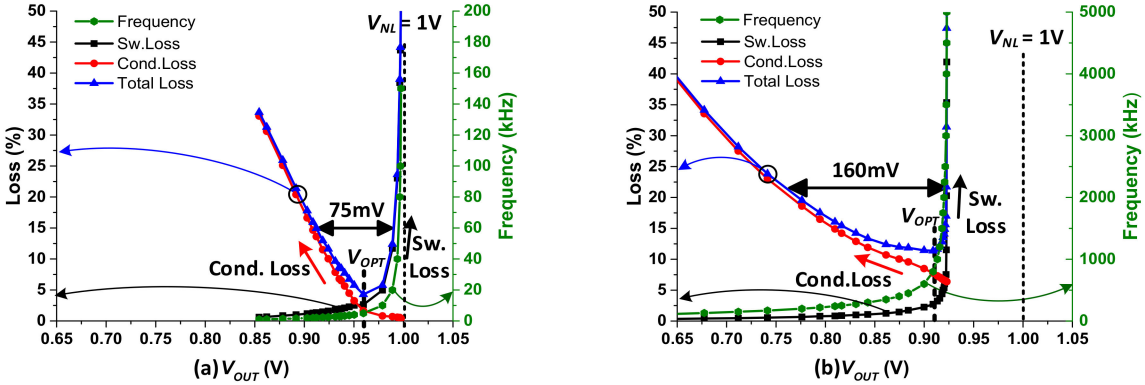

Figure 2. Loss contribution in single stage 2:1 SC converter from V_{IN} = 2.0 V (**a**) Light load (500 nA). (**b**) Heavy load (100 µA).

With a light load of 500 nA, the total loss is minimized at an output voltage of approximately 0.96 V (V_{OPT}), as shown in Figure 2a. To increase the output V_{OUT} above V_{OPT}, the frequency must be increased exponentially, which results in an exponential increase in switching loss. On other hand, to reduce V_{OUT} below V_{OPT}, the frequency must be decreased, lowering the corresponding switching loss. However, under light load conditions, the optimal operation is achieved at low frequency (~8 kHz in the presented case), where the output voltage ripple is sensitive to change in frequency. As the frequency is reduced, the voltage ripple increases drastically, resulting in a sharp increase in conduction loss, as can be found in Equation (2). These factors result in a narrow convex-shaped total loss curve whose V_{OPT} is close to V_{NL} for an SC converter under light load scenarios.

When a heavy load of 100 µA is applied to the identical SC converter, the switching and conduction losses change as shown in Figure 2b. The total loss is minimized at lower V_{OPT}, which is around 0.91 V with $f_{SW} \approx$ 830 kHz. To generate V_{OUT} higher than V_{OPT}, the frequency must be increased exponentially. This results in an exponential increase in switching loss, rendering the region between V_{OPT} and V_{NL} inefficient. However, under heavy load, the SC converter operates with a higher frequency (830 kHz vs. 8 kHz in this example), and the output ripple is less sensitive to change in frequency compared with the low load case. Therefore, as V_{OUT} is decreased with lower frequency, the voltage ripple and consequent conduction loss increase at a slower rate. The outcome is a wider convex-shaped loss curve, resulting in wider efficient region around V_{OPT} compared with the low load scenario.

The loss curves in Figure 2 can be translated into efficiency curves, as shown in Figure 3 with additional simulation results for intermediate load conditions. The following conclusions can be drawn from these simulation results.

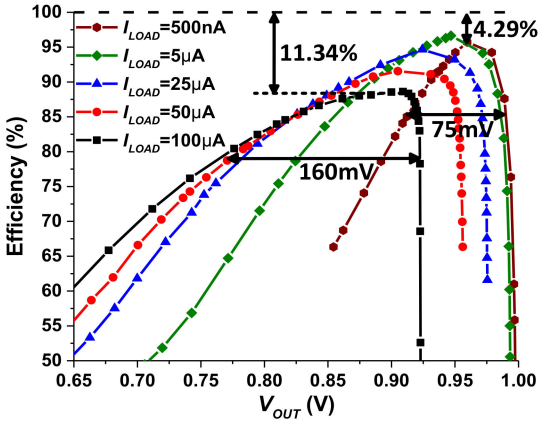

Figure 3. Efficiency of the 2:1 SC converter at varying load.

(1) The efficiency curves are narrower under light load conditions than under heavy load conditions. For example, the voltage range that keeps the efficiency within 10% of the peak efficiency is 75 mV for the 500 nA light load and 160 mV for the 100 μA heavy load. This implies that to maintain efficient operation over a given voltage range, more efficiency curves providing different V_{NL} are required for light load conditions. Since V_{NL} is determined by the conversion ratio, to maintain efficient operation for a given V_{OUT} range, more conversion ratios should be provided for light load conditions, and relatively fewer conversion ratios are required for heavy load conditions.

(2) The power loss at the optimum operation voltage (V_{OPT}) at a single stage of the SC converter is significantly higher (11.3%) with a heavy load (100 μA) and lower (4.3%) with a light load (500 nA). This implies that while cascading SC converter stages can provide finer voltage resolution, they result in significant loss under heavy load. Therefore, for heavy load conditions, the number of cascaded stages should be minimized.

Considering the efficiency trends stated above, the following operation strategies can be developed for an SC converter targeted for wide load current and voltage ranges:

(1) For light load conditions, each conversion ratio is efficient only over a very small voltage range. Therefore, providing many conversion ratios and fine resolution by cascading SC converter stages is preferred since stage loss is small.

(2) For heavy load conditions, each conversion ratio is efficient over a relatively wider voltage range. Therefore, fewer conversion ratios are required, and the number of cascaded stages can be reduced. Since the stage loss is larger, the number of cascaded stages should be minimized. In this case, the stages that are cascaded for providing fine voltage resolution under light load conditions can now operate in parallel configuration. This approach increases the effective flying capacitor and switch size and reduces conduction loss, which is the dominant loss factor under heavy load conditions.

(3) To minimize the number of cascaded stages, an SC stage structure that can provide multiple conversion ratios is preferred over an SC stage with a fixed 2:1 ratio. The maximum number of achievable conversion ratios using a 2-phase clock and two flying capacitors is three [29]. Therefore, an SC stage topology with three variable ratios is adopted, which can efficiently provide fine resolution with fewer SC stages by limiting conduction loss.

(4) To further optimize loss, especially with the light load conditions, it is desirable to adjust the switch size, i.e., the transistor width, of an SC converter, as shown in Equation (9). By adjusting W_{SW} and C_{Gate}, efficiency can be improved by balancing conduction and switching losses.

In Figure 3, where an identical switch size is used for various load currents, the peak efficiency at I_{LOAD} = 5 μA appears to be higher than at I_{LOAD} = 500 nA. This is because the switch size is too large for the 500 nA load, incurring unnecessary switching loss. Therefore, in addition to lowering the frequency for light load conditions, the switch size must also be reduced. Figure 4 shows the simulation results for the 2:1 converter with binary-sized switches with I_{LOAD} = 500 nA. With the

reduced switch size, peak efficiency improvement is observed under a light load by eliminating the excessive capacitance load of the power switch in Equation (7).

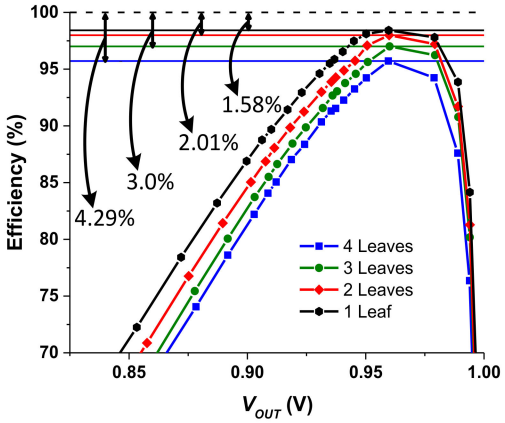

Figure 4. Effect of switch width modulation using leaf enable mechanism on efficiency of 2:1 converter at I_{LOAD} = 500 nA.

Since the switching loss for switch driving is proportional to the square of V_{SW} as shown in Equation (7), a switch driving scheme independent of input battery voltage V_{IN} is desirable and the optimal gate driving voltage depends upon the threshold voltage of switch. Figure 5 shows how efficiency changes with varying switch driving voltage swing for a 2:1 converter at I_{LOAD} of 500 nA and 100 µA respectively. With both low and high load conditions, driving switches with unnecessarily high V_{SW} of 2 V significantly drops the efficiency due to a large switching loss. However, with a high 100 µA load, utilizing too low V_{SW} could also be a problem since the insufficient overdriving voltage can make R_{ON} high, increasing conduction loss. Therefore, proper V_{SW}, which is technology dependent, should be carefully chosen to optimize both low and high load conditions.

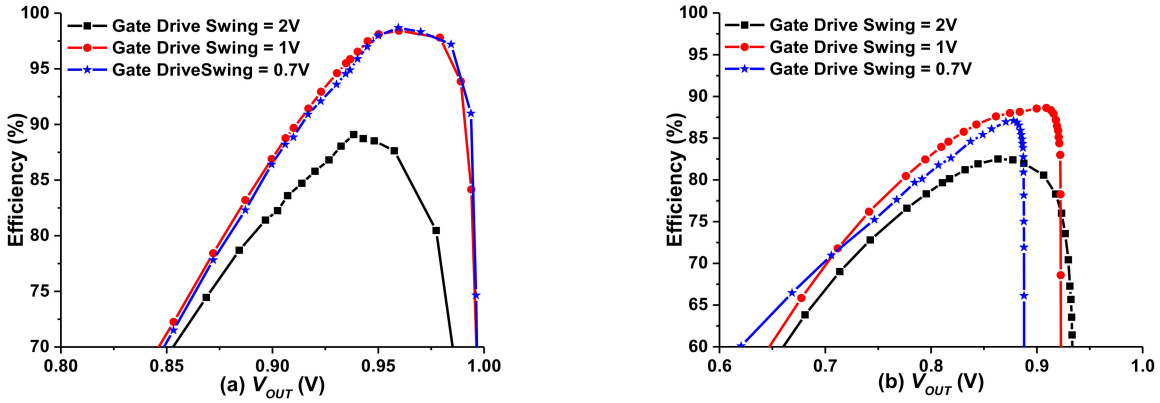

Figure 5. Effect of gate drive voltage swing variation V_{IN} = 2.0 V (**a**) Light load (500 nA). (**b**) Heavy load (100 µA).

3. Proposed SC Converter Architecture

Based on the four strategies discussed in the previous section, a reconfigurable SC converter suitable for wide load current and voltage ranges was proposed. The top level architecture of the proposed SC converter is presented in Figure 6a. To provide many voltage conversion ratios, five SC stages are utilized. The first SC stage has a fixed ratio of 2:1, whereas the following four SC stages are configurable to three different ratios, namely 1/3, 2/3, and 1/2. The multi-ratio SC stages are connected through reconfigurable stage interconnects (RSIs), which provide the flexibility of cascaded or parallel connections among stages, depending upon the load condition. With a light load, the SC stages can be connected in series, as shown in Figure 6b, whereas for a heavy load, the later four stages

can be connected in parallel, as shown in Figure 6c. Mixed series–parallel connections can be also employed for intermediate loads.

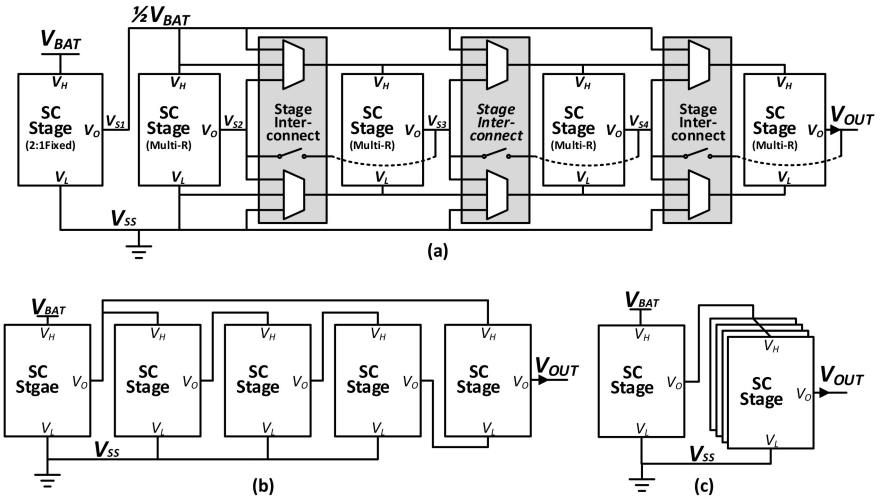

Figure 6. Multistage converter (**a**) Proposed reconfigurable SC topology. (**b**) Series connected. (**c**) Parallel connected.

3.1. Multi-Ratio and Multi-Leaf SC Stage Structure

Figure 7 illustrates the structure of multi-ratio and multi-leaf SC stages. Each SC stage consists of four switching leaves with binary-sized switches. Under light load conditions such as sub-µA, the switching loss is the major loss contributor; hence, only the minimum-sized leaf is activated to minimize the switching loss. As the load increases, leaves with larger switches can be activated to reduce conduction loss at the cost of additional switching loss. When only a subset of available leaves are activated, it is still better to operate with the maximum available flying capacitance to minimize conduction loss, as demonstrated in Equation (3). Therefore, flying capacitors are directly connected to the minimum leaf that is always active. Larger leaves are enabled/disabled by connecting switches to flying capacitors by controlling enable switches S_E with control signals (EN_{LX}, ENB_{LX}).

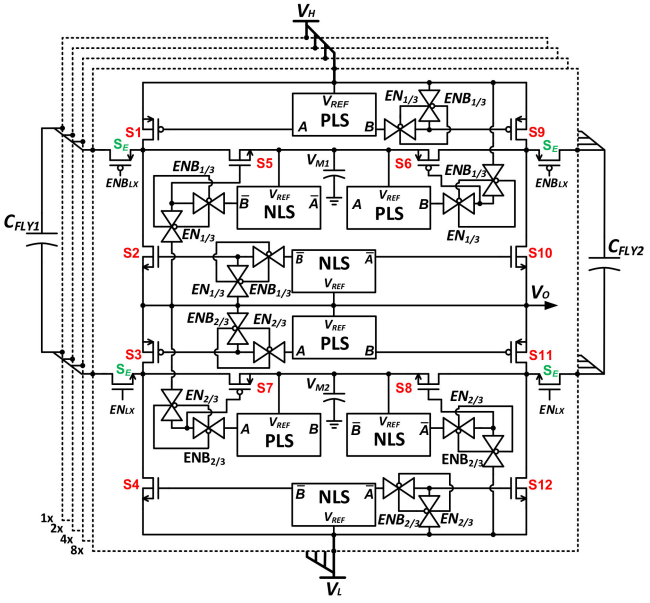

Figure 7. Multi-ratio, multi-leaf SC converter stage.

Each switching leaf consists of 12 power transistors (S1–S12) and the associated drivers with activation control to provide three discrete conversion ratios. To minimize switching overhead, instead of V_{IN}, limited clock swing is used for driving all switches. The P-channel MOSFET (PMOS) are driven by P-type level shifters (PLS), whereas the N-channel MOSFET (NMOS) are driven by N-type level shifters (NLS), as will be described in detail in subsection 3.4. A simplified diagram of a multi-ratio SC stage leaf is shown in Figure 8a. With the given structure, conversion ratios of 1/2, 1/3, and 2/3 can be achieved, as shown in Figure 8b–d, respectively, by driving eight power transistors with 2-phase-interleaved signals (red or blue switches in Figure 8) and disabling the rest of the four transistors (grey switches in Figure 8). Table 2 summarizes the enabled switches and phase sequence for each mode of operation. The enabled switches are closed in one phase and open during the alternate phase, e.g., switch S1 is closed during ϕ_1 and open during ϕ_2. Switches labeled as disabled are always open during the corresponding mode of operation, e.g., switch S2 is always open in 1/3 mode, but in 1/2 and 2/3 modes, it is closed during ϕ_2 and open during ϕ_1.

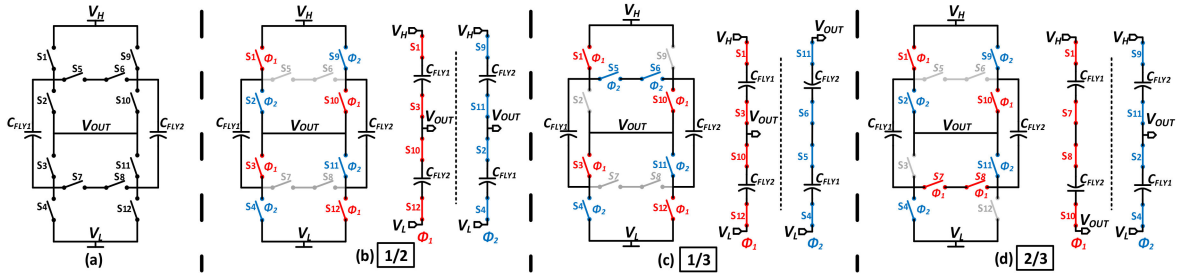

Figure 8. Multi-ratio, multi-leaf SC converter stage structure (**a**) Simplified diagram. (**b**) Operation scheme for 1/2 ratio. (**c**) 1/3 ratio. (**d**) 2/3 ratio.

Table 2. Switching sequence.

Ratio	$EN_{1/3}$	$EN_{2/3}$	Enabled (ϕ_1 or ϕ_2)	Disabled (Always off)	ϕ_1	ϕ_2
1/2	0	0	1,2,3,4,9,10,11,12	5, 6, 7, 8	1, 3, 10, 12	2, 4, 9, 11
1/3	1	0	1,3,4,5,6,10,11,12	2, 7, 8, 9	1, 3, 10, 12	4, 5, 6, 11
2/3	0	1	1,2,4,7,8,9,10,11	3, 5, 6, 12	1, 7, 8, 10	2, 4, 9, 11

The power switches in the SC stage's leaf can be categorized into the following two types depending on the availability of the stable source voltage:

I. Boundary switches (S1–S4, S9–S12)
II. Middle switches (S5, S8)

Boundary power switches have a stable voltage (V_H, V_L or V_{OUT}) at the transistor's source terminals. This stable source voltage is used as reference for generating limited voltage swing on/off control signal by the level shifters, which are described in more detail later. However, Middle switches lack such a topology-inherent stable voltage at the source terminals, which is required for level shifter drivers. To address this challenge, local capacitors C_{M1} and C_{M2} are placed to implement local reference voltages V_{M1} and V_{M2}, as shown in Figure 7. These voltages converge to deterministic voltages depending on the operating conversion ratio. Thus middle switches can be driven with limited voltage swing by using local reference for level shifter drivers.

Boundary switches can be disabled by shorting the gate with the source terminal through stage disable switches (EN_X, ENB_X in Figure 7). However, to disable Middle switches, local reference voltages (V_{M1} and V_{M2}) cannot be used since they are not deterministic when adjacent transistors are disabled (i.e., always off). Therefore, Middle switches are disabled by connecting the gate to the suitable stable power/ground rail, which is at a potential sufficient to keep the switches turned off. For example, when disabled, the gate terminal of S5 is connected to V_{OUT}, whereas the gate of S6 is connected to V_H.

Optimal capacitance allocation for flying capacitors amongst SC converter stages depends upon the conversion ratio configuration and interconnection scheme of the stages. Each configuration requires a unique optimal distribution of flying capacitors, which cannot be easily adjusted with a multi-stage structure. Thus the binary distribution of [21] with the smallest flying capacitor at the first and the largest at the last stage is opted for.

3.2. Reconfigurable Stage Interconnect

Figure 9 illustrates the implementation of the reconfigurable stage interconnection (RSI) scheme. RSI provides a differential input voltage ($V_H - V_L$) to each SC stage, which can be configured with 2-bit control signals A_n and B_n. Through RSI, the next stage's high input $V_{H(n)}$ can be connected to the previous stage's high $V_{H(n-1)}$ or intermediate power supply (first stage output $\frac{1}{2}V_{BAT}$) or the previous stage's output $V_{S(n-1)}$. Likewise, the next stage's low input $V_{L(n)}$ can be connected to the previous stage's low input $V_{L(n-1)}$ or ground node V_{SS} or the previous stage's output $V_{S(n-1)}$. By selecting the appropriate connection, RSI schemes operate in one of the modes illustrated in Figure 10, and the corresponding control bits are summarized in Table 3. In the first two modes shown in Figure 10, two adjacent stages are series connected to generate an output voltage whose value is between the earlier stage's output voltage [$V_{OUT(N-1)}$] and power/ground. On the other hand, in the last mode, two stages are parallel connected to increase the effective switch width and flying capacitance. Such a reconfigurable structure allows voltage generation with fine resolution for light loads and reduction of conduction loss for heavy loads as needed.

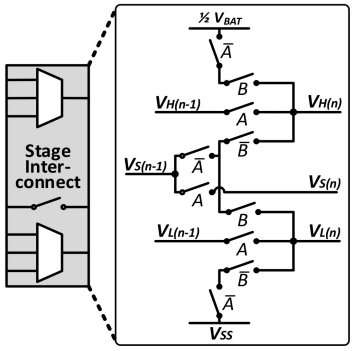

Figure 9. Switch level implementation of the Reconfigurable Stage Interconnection (RSI) scheme.

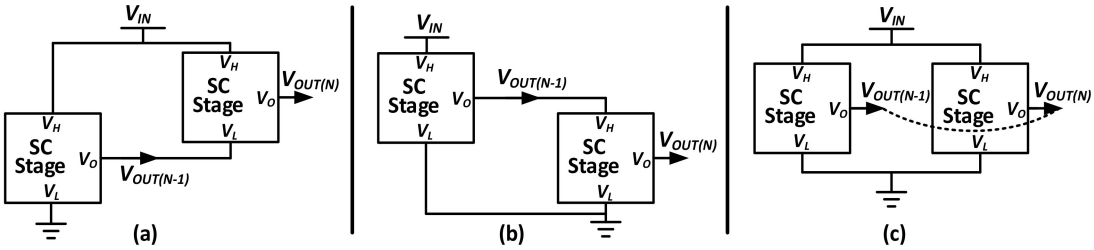

Figure 10. Figure 10. Three possible stage interconnect operation modes: (**a**) A_nB_n = 00. (**b**) A_nB_n = 01. (**c**) A_nB_n = 1X.

Table 3. Reconfigurable stage interconnect (RSI) control bits.

Control Bits		$V_{H(n)}$	$V_{L(n)}$	$V_{S(n)}$
A_n	B_n			
0	0	$V_{S(n-1)}$	V_{SS}	$\neq V_{S(n-1)}$
0	1	$\frac{1}{2}V_{BAT}$	$V_{S(n-1)}$	$\neq V_{S(n-1)}$
1	X	$V_{H(n-1)}$	$V_{L(n-1)}$	$=V_{S(n-1)}$ (parallel)

It must be noted that the output of the first stage ($V_{S1} = \frac{1}{2}V_{BAT}$) is kept as the power rail for the remainder of the stages since the target output voltage is <2 V. It is also worth noting that providing connection to power/ground recursively at each stage helps to reduce cascading loss due to direct charge transfer from power/ground rails [21]. Thick oxide devices are used for the first SC stage since it has to tolerate high V_{BAT}. However, the maximum voltage that the rest of the stages should handle is limited to 2 V, which allows for the use of thin oxide devices, significantly improving efficiency.

3.3. Load-Dependent Configurability

The use of a multi-ratio SC stage along with RSI results in ($3 \times 2 = 6$) conversion ratios per stage, excluding the parallel connection case. Therefore, in the presented topology, setting the first stage as a fixed 2:1 converter and the rest of the four stages as multi-ratio with three RSIs in between, results in $1 \times 6^3 \times 3 = 648$ possible configurations. Because many configurations provide duplicated conversion ratios, there are 125 discrete conversion ratios over the voltage range of 0–2 V, which translates into an average voltage resolution of 16 mV when the input battery voltage is 4 V. Such fine voltage resolution is vital for efficient operation under light load conditions where each configuration is efficient for only a very limited voltage range.

Figure 11 illustrates example operations of a reconfigurable SC converter. In Figure 11a, stage 1 provides a fixed $V_{S1} = 1/2$ conversion. Stage 2 is configured in 2/3 ratio with high input connected to stage 1 output ($V_{H2} = V_{S1}$) and low input to ground ($V_{L2} = V_{SS}$), which results in $V_{S2} = 1/3$. Then in the third stage, V_{H3} is connected to the previous stage output V_{S2}, and V_{L3} is connected to V_{SS} by applying a configuration code of '00' at the first RSI. The third stage converter is configured to 2/3 ratio, resulting in $V_{S3} = 2/9$. At the fourth stage, assigning $V_{H4} = V_{S3}$ and $V_{L4} = V_{SS}$ by applying a configuration code of '00' at the second RSI and using 1/3 ratio provides $V_{S4} = 2/27$. At the fifth stage, assigning $V_{H5} = V_{S1}$ and $V_{L5} = V_{S4}$ by applying an RSI configuration code of '01' and using 1/2 ratio results in $V_{OUT} = [V_{S4} + (V_{S1} - V_{S4})/2] = 31/108$. The overall conversion ratio of 31/108 provides a no load voltage of $V_{NL} = 1.148$ V when $V_{BAT} = 4.0$ V. Figure 11b presents the case of a conversion ratio of 7/24, which results in $V_{NL} = 1.167$ V. Since four stages are sufficient to generate this ratio, parallel connection can be applied to the third and fourth stages to reduce conduction loss.

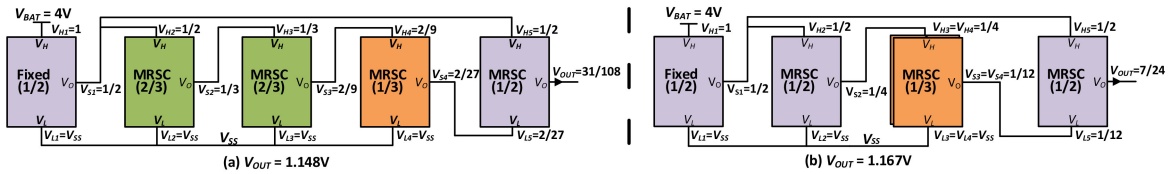

Figure 11. Figure 11. Operation of reconfigurable SC converter at no load (**a**) $V_{OUT} = 1.148$ V. (**b**) $V_{OUT} = 1.167$ V.

A multi-ratio multi-leaf SC converter with RSI provides load-dependent configurability for optimal voltage conversion operation. Depending on the system load condition, the conversion ratio and number of activated leaves in the proposed SC converter can be changed to provide an output voltage near V_{OPT} under new operating conditions. An example case is illustrated in Figure 12 where the target output voltage is $V_{OUT} = 0.725$ V from $V_{BAT} = 4.0$ V. Under 500 nA loading, only minimum-sized leaves are enabled, and the conversion ratio of 5/24 is used, which provides $V_{NL} = 0.833$ V. This requires a cascade length of four stages, as shown in Figure 12a, and 68.1% conversion efficiency could be obtained at target V_{OUT}. When the load is increased to 10 µA, a higher conversion ratio is required to provide the same V_{OUT} because the optimal operating point in a given conversion configuration moves away from V_{NL} as the load is increased (Equation (10)). Therefore, the conversion ratio should be increased to 2/9 in Figure 12b ($V_{NL} = 0.889$ V) with two leaves enabled, resulting in 66.3% efficiency. When the load is further increased to 200 µA, maximizing parallel connection and activation of all leaves are required. Therefore, the conversion ratio changes to 1/4 ($V_{NL} = 1.0$ V) with a cascade length of two stages, as shown in Figure 12c, achieving 64% efficiency.

It is worth mentioning that if the configuration optimized for 500 nA is used for 200 µA, efficiency drops to <27%, highlighting the effectiveness of reconfigurable SC topology.

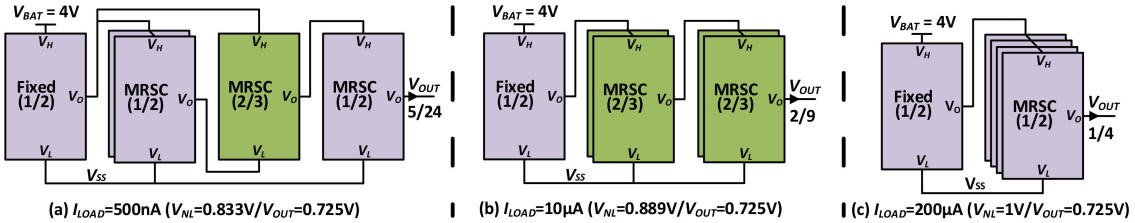

Figure 12. Optimal configuration for various load conditions when target V_{OUT} = 0.725 V from V_{BAT} = 4.0 V.

3.4. Switch Driver and Clock Voltage

As discussed in Section 2, the switching loss for the driving gate has quadratic dependence on the voltage swing, as shown in Equation (7). Therefore, to minimize switching loss, rather than using full input voltage swing (V_{BAT}), reduced clock swing is desired for driving switches. However, such reduced clock swing cannot be directly applied for driving MOSFETs, which are at a different potential, hence a cross-coupled level shifter scheme [20] is utilized. For driving PMOS, a P-type level shifter (PLS in Figure 7) is implemented, and for driving NMOS, an N-type level shifter (NLS in Figure 7) is implemented, as shown in Figure 13.

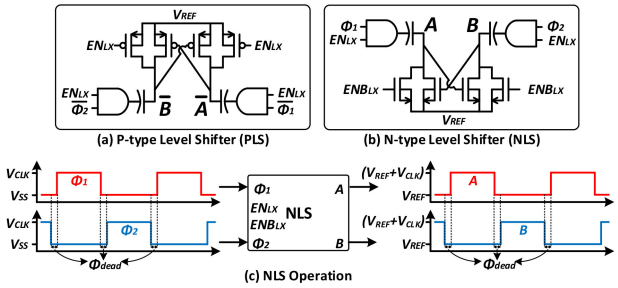

Figure 13. Cross coupled level shifter for gate diving (**a**) P-type level shifter (PLS). (**b**) N-type level shifter (NLS). (**c**) N-type level shifter operation.

For an N-type level shifter, when the clock is low, the gate driving voltage should be set to the source voltage to turn off the target NMOS. When the clock is set high, the potential at the gate terminal should be increased by a preset voltage swing with regard to the source voltage, thus turning on the target NMOS. Similarly, P-type level shifters drive PMOS by lowering the gate potential with regard to the source voltage when the clock phase is low. This operation is achieved by capacitive coupling. For triggering level shifters, 2-phase non-overlapping clocks (ϕ_1, ϕ_2) are utilized to eliminate the possibility of turning on transistors on opposite phase together. Clock swings applied to target NMOS/PMOS are identical to the swing of ϕ_1 and ϕ_2. To reduce switching loss, the output voltage of the second stage is used for generating ϕ_1 and ϕ_2. For the first stage where a thick oxide device is utilized, higher voltage ($\frac{1}{2}V_{BAT}$) is used for generating ϕ_1 and ϕ_2.

3.5. Leakage-Controlled Clock Generator

For efficient operation over a wide load current range, a wide clock frequency range from a few kHz to MHz is required. In addition, a balanced duty cycle is required for optimal utilization of the capacitor. This is because an unequal duty cycle results in unequal charge distribution among flying capacitors, which eventually results in larger ripple at stage outputs and corresponding higher conduction loss.

In this work, a leakage-controlled delay cell-based clock generator is presented for achieving a wide frequency range with an even duty cycle. A leakage-controlled delay cell structure was proposed earlier in [30,31] for energy-efficient clock generation over a wide frequency range. This clock

generator controls its output frequency by controlling the amount of leakage current injected to accelerate oscillation by adjusting the control voltage (V_{CONT}). However, as shown in Figure 14a, leakage control was only provided between IN and OUTB branch, whereas no control was applied to the other branch (INB–OUT). This asymmetry in delay cell structure results in uneven duty cycle.

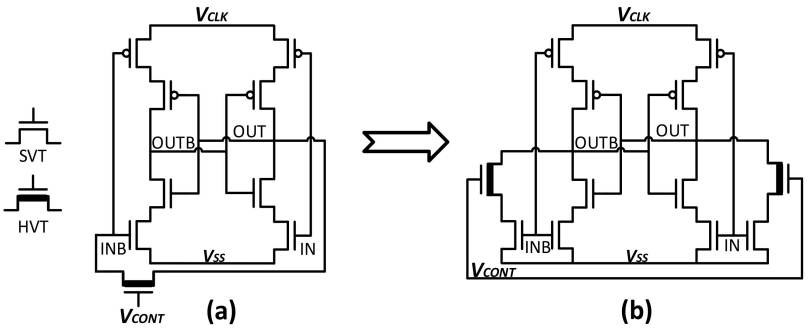

Figure 14. Leakage-controlled delay cell (**a**) Conventional single branch. (**b**) Modified two leakage control Branches.

To address this issue, a symmetric leakage-controlled delay cell structure was proposed as shown in Figure 14b. The modified structure consists of two symmetric leakage control paths, one for each flipping branch. By series connecting these delay cells as shown in Figure 15, an energy-efficient clock generator with even duty and a wide frequency range could be designed. The proposed structure generates a clock with approximately 50% duty over the frequency range from 100 s of Hz to a few MHz. Note that high threshold voltage devices are used in the leakage control path to provide fine control over the leakage current, resulting in fine frequency steps.

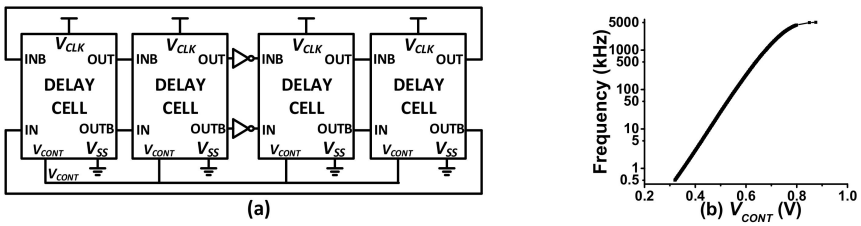

Figure 15. (**a**) Block diagram of leakage-based clock generator. (**b**) Frequency vs. control voltage (V_{CONT}).

In the proposed SC converter, leakage control voltage (V_{CONT}), which is used for clock generator frequency control, can be also used for controlling the number of activated leaves in the SC converter stages. As load current increases, V_{CONT} and the corresponding frequency should be increased, as shown in Figure 15b. Therefore, V_{CONT} indirectly represents the amount of load current the SC converter is currently handling. By comparing V_{CONT} with preset reference voltages, the appropriate number of leaves can be activated. Figure 16 shows the reference comparison circuitry for leaf control. Reference voltages are generated from a diode stack and made tunable to account for variations. As V_{CONT} increases, additional leaves are gradually added.

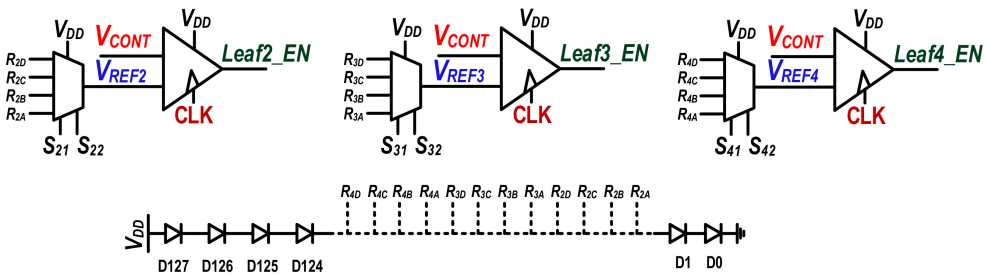

Figure 16. Reference comparison circuit for leaf control with V_{CONT}.

4. Measurement Results

A prototype test chip was fabricated in a 180 nm complimentary metal-oxide-semiconductor (CMOS) process. An effective die area of 1.525 mm^2 was utilized by the converter, which is dominantly occupied by 2.09 nF of on-chip MIM capacitors. The micrograph for the fabricated test chip is presented in Figure 17.

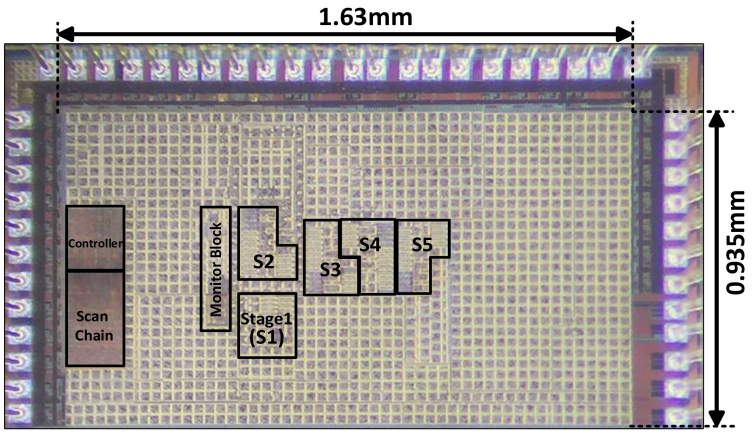

Figure 17. Chip micrograph.

The prototype SC converter was examined over a wide load current and voltage range. The experimental results presented in Figures 18 and 19 illustrate the importance of switch width modulation using multi-leaf structure under light load conditions. In these figures, the load current is fixed, and the operation frequency is swept for each conversion ratio configuration to measure the corresponding output voltage and efficiency. Colored curves represent the efficiency trend for configurations whose efficiency is the highest at least for one output voltage. Gray curves represent efficiency trends for configurations whose efficiency is never the optimal at any given output voltage and hence can be ignored. Under a light load (500 nA), minimum activation of switches is desired to minimize switching loss. Therefore, enabling only the smallest leaf is optimal (Figure 18a) and delivers output with approximately 13–20% higher efficiency compared with enabling all of the leaves (Figure 18b). However, under a higher load of 5 µA, two leaves are required to be activated to achieve comparable efficiency (Figure 19a) since enabling only the smallest leaf now incurs significant conduction loss. If too many leaves are activated, the efficiency drops again due to a large switching loss, as shown in Figure 19b, where all leaves are activated.

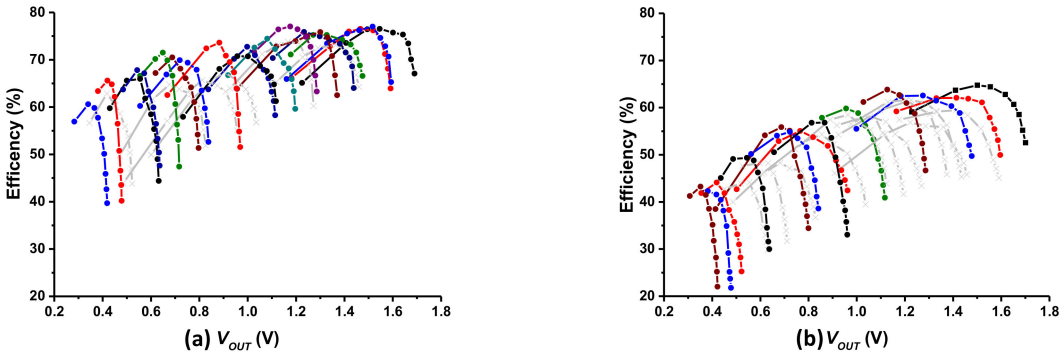

Figure 18. Efficiency vs. V_{OUT} at I_{LOAD} = 500 nA (**a**) Only 1 (smallest) leaf enable (Min. switch size). (**b**) All leaves enabled (Max. switch size).

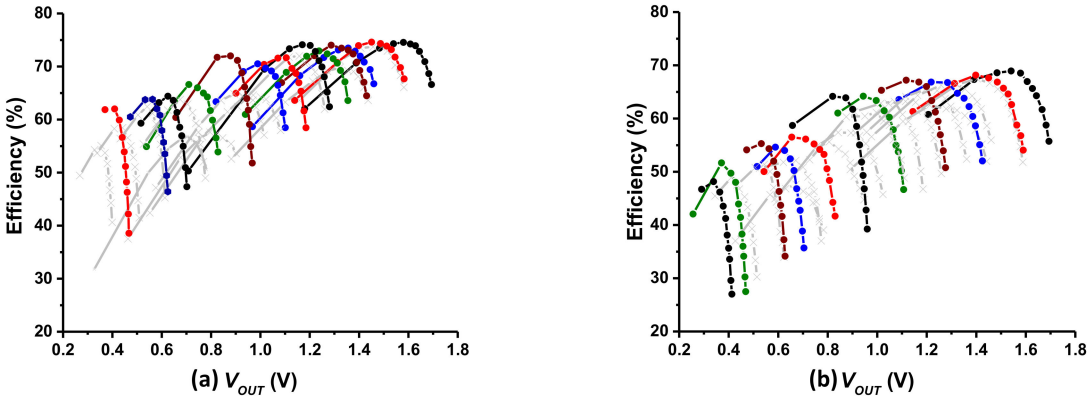

Figure 19. Efficiency vs. V_{OUT} at I_{LOAD} = 5 µA (**a**) Leaf 1 and 2 enabled. (**b**) All leaves enabled (Max. switch size).

The effectiveness of switch width modulation by using multiple leaf structures is summarized in Figure 20, where V_{OUT} = 1.2 V is generated from V_{BAT} = 4.0 V. For each load current point ranging from 300 nA to 300 µA (1000×), the optimal conversion ratio, operating frequency and number of active leaves are selected, and the corresponding efficiency and operating frequency are plotted. As load current increases, the optimal operating frequency also increases, and additional leaves should be gradually added to compensate for the increasing conduction loss.

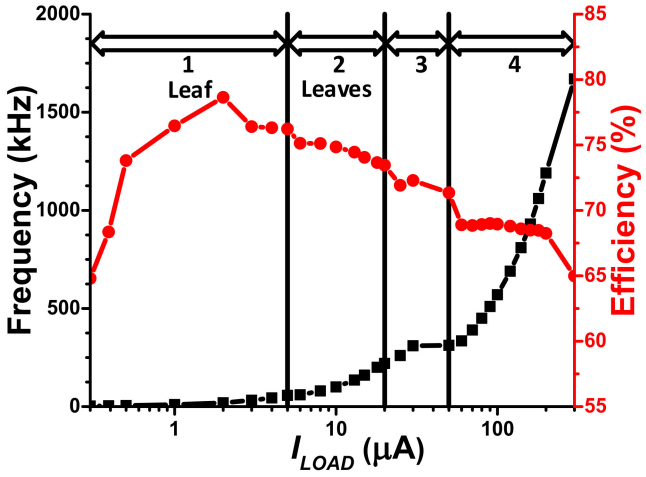

Figure 20. Frequency, efficiency and active leaves vs. I_{LOAD}.

Figure 21a shows the experimental results for regulated output voltage levels when targeted for 0.78 V, 1.2 V, and 1.45 V with load current ranging from 300 nA to 300 µA. The optimal configuration is identified and measured for each load current point. The maximum regulation error was kept under ±16 mV thanks to the fine resolution provided with multi-ratio multi-stage topology. Figure 21b shows the corresponding efficiency trends. The proposed SC converter could operate with peak efficiencies of 73.9%, 77.96%, and 77.5% and minimum efficiencies of 63.58%, 64.79%, and 65.98% for target output voltages of 0.78 V, 1.2 V, and 1.45 V, respectively.

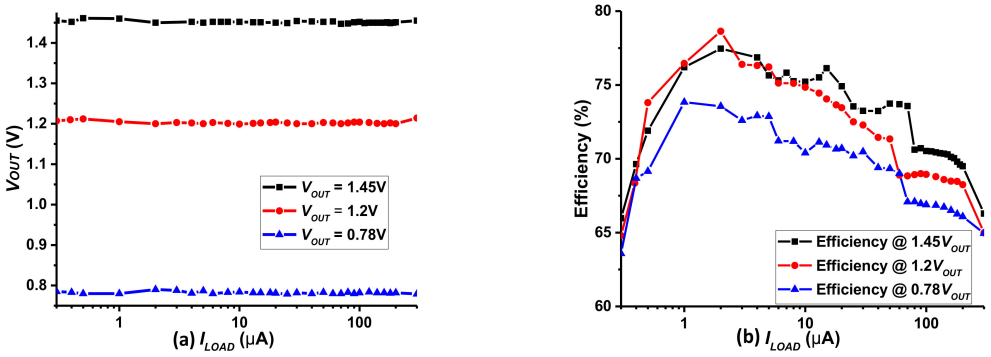

Figure 21. (**a**) Regulated output voltage vs. I_{LOAD}. (**b**) Corresponding efficiencies.

To verify the effectiveness of the proposed SC converter in providing dynamic voltage scalability in miniature sensors, the efficiency was measured over a target output voltage range of 0.4–1.6 V under various load conditions. The efficiency plots in Figure 22 show the efficiency trend for each conversion ratio configuration. The same color/grey notation in Figures 18 and 19 is used in these plots.

Under the light load condition of 500 nA, each configuration is only effective for a narrow output voltage range, resulting in narrow efficiency curves. This implies that many conversion ratio configurations are required to maintain high efficiency over a wide DVS range, validating the loss analysis discussion presented in Section 2. With the fine voltage resolution, 18 configurations were required to keep conversion efficiency above 60% for the target voltage range, and the peak efficiency was >77% at V_{OUT} of 1.176 V and 1.517 V. Only the smallest leaf was enabled to deal with the light load. Efficient operation under such light load conditions is essential for efficient miniature system operation during typically long standby.

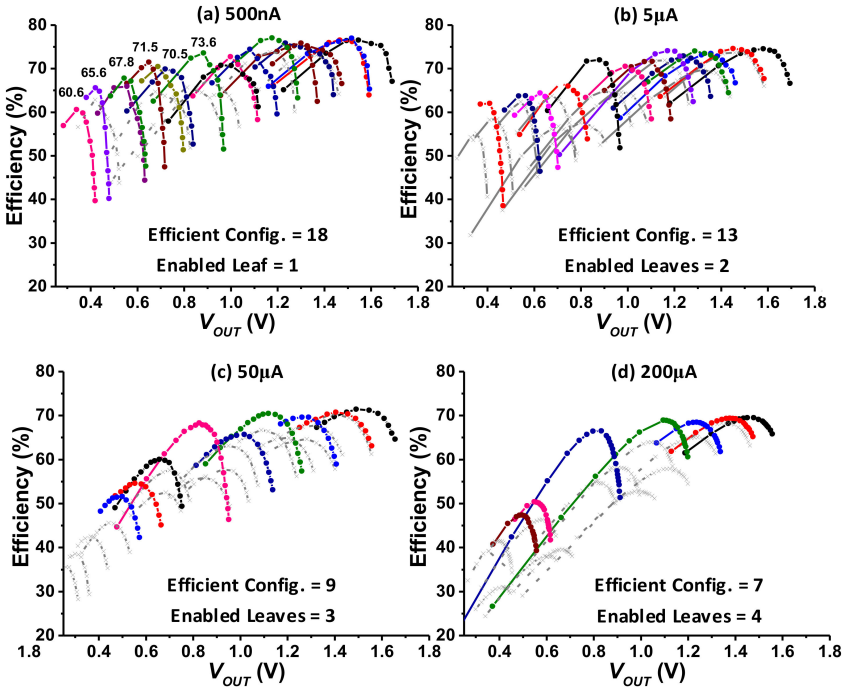

Figure 22. Multi-ratio, multi-leaf SC converter's efficiency curves at I_{LOAD} (**a**) 500 nA. (**b**) 5 µA. (**c**) 50 µA. (**d**) 200 µA.

When the load current is increased to 5 µA, the efficiency curves become slightly wider, and the number of required ratio configurations is reduced to 13. A second binary sized leaf is enabled to balance conduction and switching losses. The minimum efficiency for the entire output range was 62%, and the peak efficiency was 74.1%, as shown in Figure 22b.

As the load is further increased to 50 µA, three leaves need to be activated. Since the efficiency curves become even wider, fewer conversion ratios are required. This means less cascaded stages are required, and more stages can be parallel-connected to improve efficiency. Such parallelism facilitates high efficiency at high output voltages. However, for low output voltages, where many cascaded stages are required to form small conversion ratios, efficiency drops due to increased conduction loss. For a miniature sensor system, this is not a critical drawback since digital circuits with DVS tend to operate at high voltage when there is large current demand, i.e., computation demand. As shown in Figure 22c, the proposed SC converter could operate with >64% efficiency for an output range of 0.7–1.6 V with 50 µA load. When the voltage drops to 0.4 V, the efficiency drops to 47%, which is still high compared with the state-of-the-art systems [20,21] thanks to multi-leaves stage structure, stage configurability and cascading SC stages or parallel interconnect control.

With a heavy load current of 200 µA, all available leaves are activated, and only a few configurations inheriting parallel interconnection of SC stages are used to cover the entire output range, as shown in Figure 22d. From the detailed efficiency trend analysis for wide load current and voltage ranges, the observation made earlier in the loss analysis section that, "cascading SC stages are required for efficient operation under light loads, whereas parallelism is required for heavy loads" is confirmed.

A performance comparison of the proposed architecture with state-of-the-art structures including successive approximation (SAR) [20], recursive tertiary (RTC) [21], and recursive binary (RBC) [22] converters is summarized in Table 4. The proposed SC converter provides finer 16 mV effective voltage resolution as compared to the SAR with fewer stages, resulting in more efficient operation by limiting conduction loss. The peak efficiency of the proposed converter is lower than recursive architectures (RTC, RBC), but finer granularity and V_{IN} independent driving scheme results in significant efficiency improvement for light load conditions, which is crucial for duty-cycled miniature sensor systems. The proposed converter maintains efficient operation for very low output voltages even at higher V_{IN} level, which is the major contribution of this work. Other SC converters in [15–17] are efficient SC converter designs but are based upon a single SC stage. Therefore, only few conversion ratios can be provided, making them unsuitable for DVS implementation.

Table 4. Performance comparison with prior SC down-converters.

Parameters	This Work	[20]	[21]	[22]	[15]	[16]	[17]
Topology	Reconfigurable Multi-Stage	Successive Approximation	Recursive Tertiary	Recursive Binary	Single Stage Reconfigurable	Voltage Scalable	Single Ratio SC
Technology	180n	180n	250n	250n	130n	180n	45n
V_{IN} (V)	4	3.4–4.3	2.5	2.5	1.5	1.2	1.8
V_{OUT} (V)	0.4–1.6	>0.45	0.1–2.24	0.1–2.2	0.4–1.1	0.3–1.1	0.8–1
Number of Conversion Ratios	75 for 0.4 V–1.6 V 250 for 0 V–4.0 V (V_{BAT} = 4.0 V)	20 for 0.9 V–1.5 V 128 for 0 V–4.0 V (V_{BAT} = 4.0 V)	45	15	4	5	1
Voltage Step Resolution	16 mV @ 4.0 V_{BAT}	31 mV @ 4.0 V_{BAT}	55 mV @ 2.5 V_{BAT}	167 mV @ 2.5 V_{BAT}	-	-	-
Number of Stages	1 + 4	1 + 5	3	4	1	1	1
Capacitor Type	MIM Cap	On chip	MIM Cap	MIM cap	Ferroelectric	Gate Oxide	Gate Oxide
Output Load Range	300 nA–300 µA (1000×)	1 µA–300 µA (300×)	<1.86 mA	<2 mA	20 µA–1 mA (50×)	5 µW–1 mW (200×)	100 µA–8 mA (80×)
Capacitance	2.09 nF	2.24 nF	2.8 nF	3 nF	8 nF	2.4 nF	1.234 nF
Frequency	2 k–2.3 M	80 k–2.7 M	-	-	-	<15 M	<30 M
Area (mm^2)	1.525	1.69	4.3	4.645	0.366	0.57	0.16
η_{MAX} (%)	77	72	86	85	93	~77	69
η @ Heavy Load	69% @ 300 µA (1.2 V) (ratio = 3/10)	54% @ 300 µA (1.2 V) (ratio = 3/10)	74% @ 1.86 mA (1.2 V) (ratio = 4.8/10)	73% @ 2 mA (1.2 V) (ratio=4.8/10)	93% @ 500 µA (0.96 V) (ratio = 6.4/10)	73% @ 100 µW (0.8 V) (ratio = 2/3)	65% @ 8 mA @ (0.90 V) (ratio = 1/2)
η @ Light Load	76% @ 500 nA (1.2 V) 64% @ 300 nA (1.2 V)	64% @ 4 µA (1.2 V)	-	-	73% @ 20 µA (0.96 V)	-	48% @ 100 µA (0.90 V)
η @ Light Load & Low Voltage	64% @ 500 nA (0.4 V) 48% @ 300 nA (0.4 V)	45% @ 2 µA (0.9 V)	-	-	-	74% @ 5 µW @ 0.5 V	-

5. Conclusions

A fully integrated SC converter is proposed for DVS implementation in ultra-low power miniature sensor systems. For efficient DVS operation, the SC converter should be able to efficiently provide a wide range of output voltage over a wide range of load current to handle both standby and active mode operation. With light load current, an SC converter configured for a given ratio can operate efficiently only within a narrow voltage range. Therefore, multi-ratio, multi-stage architecture with RSI was utilized for the proposed SC converter to provide numerous conversion ratios and hence fine voltage resolution. Switch width modulation using binary sized leaves was also implemented to balance switching and conduction losses over wide load ranges. A limited-swing switch-driving scheme allowed conversion from higher voltage battery without increase in switching overhead. RSI also enabled parallel connection of stages so that efficiency at heavy load could be improved by increasing the effective stage capacitance and switch size, reducing conduction loss.

The experimental results verify that the proposed SC converter operates with greater than 64% efficiency for load currents ranging from 300 nA to 300 μA (1000×) with 1.2 V, and greater than 48% efficiency at ultra-light load and low voltage conditions of 300 nA/0.4 V. Amongst all prior architectures, ref. [20] provides a maximum load current range of 1 μA to 300 μA (300×). Thus, the proposed SC converter not only provides efficient operation at different loading and voltage levels during active mode but also maintains efficient operation during standby mode, which can be the dominant operation mode in miniature systems. We believe this efficient SC converter enables efficient implementation of DVS, which can lead to significant improvement in battery lifetime for miniature systems.

Author Contributions: Y.L. (Yoonmyung Lee) guided and directed the authors for this work. H.S. proposed and designed the overall architecture of proposed SC converter and wrote the paper. Y.L. (Yongmin Lee), H.L., M.K., and M.B.K. contributed in prototype test chip design and layout. J.-H.C. advised on concept development and helped in writing the paper.

Funding: This work was supported by the Basic Research Lab Program through the National Research Foundation of Korea (NRF) funded by the Ministry of Science and ICT (2017R1A4A1015400) and 'the Competency Development Program for Industry Specialists' of the Korean Ministry of Trade, Industry and Energy (MOTIE), operated by Korea Institute for Advancement of Technology (KIAT) (No. N0001883, HRD program for Intelligent Semiconductor Industry). The EDA tool was supported by the IC Design Education Center (IDEC), Korea.

Conflicts of Interest: The authors declare no conflict of interest.

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