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Modular Multi-Port Ultra-High Power Level Power Converter Integrated with Energy Storage for High Voltage Direct Current (HVDC) Transmission

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Received: 20 August 2018; Accepted: 8 October 2018; Published: 11 October 2018

Abstract: To connect renewable energy sources (RESs) with a unity-grid, energy storage (ES) systems are essential to eliminate the weather fluctuation effect, and high voltage direct current (HVDC) transmission is preferred for large-scale RESs power plants due to the merits of low cost and high efficiency. This paper proposes a multi-port bidirectional DC/DC converter consisting of multiple modules that can integrate ES system and HVDC transmission. Thanks to the adoption of three-port converters as submodules (SMs), ES devices, for example, batteries, can be decentralized into SMs and controlled directly by the SMs. Additionally, SMs are connected in a scalable matrix topology, presenting the advantages of flexible power flows, high voltage step-up ratios and low voltage/current ratings of components to satisfy the requirements of HVDC transmission. Furthermore, the control flexibility and fault tolerance capability are increased due to the matrix topology. In this paper, the analysis of the novel modular multi-port converter is introduced, and its functions are verified by the simulation results in PSIM.

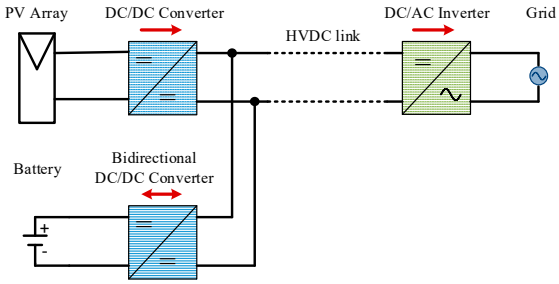
Keywords: DC/DC converter; multi-port; high voltage direct current (HVDC); high voltage gain; modular

1. Introduction

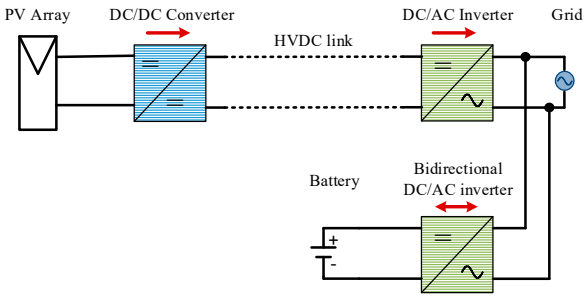
Solar and wind power are the dominant renewable energy sources (RESs) nowadays, whose average levelised cost of electricity (LCOE) falls within the fossil fuel-fired cost range as USD 0.05~0.17/kWh [1]. For example, the global weighted average LCOE of utility-scale solar power has decreased by 73% since 2010, to USD 0.10/kWh for new projects commissioned in 2017 [1]. However, the variability of RESs caused by the weather fluctuation is a challenge to connecting RESs with grid-tie systems. For example, passing clouds can affect up to 70% of daytime solar capacity, and 100% of wind capacity is reduced in calm days for individual generation assets, which have a negative impact on the stability and power quality of electric power systems [2]. To address this issue, energy storage (ES) systems with the ability to store and dispatch electricity are connected to compensate for the generation fluctuations of RESs. The battery has become a candidate of grid-tie large scale RESs power plants with its increasing deployable capability and reducing cost [3]. Additionally, the high voltage direct current (HVDC) transmission method is preferred for large-scale renewable power plants that have a large output power scale and long-distance transmission because HVDC transmission has the advantages of low cost and high transfer efficiency [4–6] compared with the conventional high voltage alternating current (HVAC) transmission. Therefore, RESs such as solar and wind power are delivered

to the unity grid through HVDC transmission in conjunction with ES systems to improve the reliability, power quality, and efficiency of the overall system.

Four dominant configurations illustrated in Figure 1 show the integration of battery (ES system) with HVDC transmission, where the red arrow indicates the power flow direction. As illustrated in Figure 1a,b, the battery is either connected to DC link through an additional bidirectional DC/DC converter [7,8] or integrated into the grid side using a separate bidirectional inverter [9,10]. Both configurations use a large number of components. Additionally, for the configuration illustrated in Figure 1b, due to the direct connection with the unity grid, extra circuit protection for the battery port is demanded and the power rate of the bidirectional inverter connected with the battery is as high as that of the inverter connected with the grid, which leads to a high cost. Thanks to the application of multi-port converters (MPCs), the configuration in Figure 1c solves the problems caused by the configurations in Figure 1a,b. Additionally, it has a reduced component count, fewer conversion stages, higher compactness, and improved reliability because the power conversion between any two of the source-battery outputs can be completed within one stage [11,12].



(**a**)



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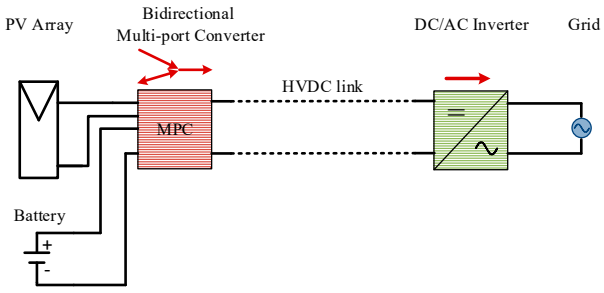


(**c**)

Figure 1. Main configurations for integrating energy storage (ES) system and high voltage direct current (HVDC) system: (**a**) dual-converter architecture; (**b**) dual-inverter architecture; (**c**) multi-port converter architecture.

The MPC design is a technical challenge to meet the HVDC requirement due to the required high DC voltage, e.g., ±800 kV [13] and the large power scale, which requires a large amount of battery cells connected in series. Battery management systems (BMS) are necessary to monitor and balance the state of charge (SOC) of each battery cell for safe operation. To design an MPC suitable for the grid-tie system, isolated, partially-isolated, and non-isolated MPCs are extensively studied.

The representative isolated MPCs install two transformers or one tri-winding transformer to extend the output ports of conventional dual-active-bridge (DAB) converters, which can achieve high DC/DC voltage conversion ratios [14–16]. However, the voltage stress on their semiconductor components is high. [17] eliminates the active switches that are connected with the output port by series-connecting the secondary sides of two transformers, whose primary sides are linked with two DC power sources, while the converter is only suitable for unidirectional power flow. Non-isolated MPCs use modules in parallel connection to obtain the multi-port configurations, which reduce the volume due to the elimination of bulky transformers [18–20]. However, they are mainly applied for the stand-alone systems such as electric vehicles (EVs) because galvanic isolation is preferred for the grid-tie systems for the safety reason. The partially-isolated MPCs reduce the switch count by sharing the switches of DAB converters, full bridge (FB), half-bridge (HB), or phase-shift converters [21–23]. In [24], an interleaved HB three-port converter can achieve free power flows among the RES–ES-output loop. Nevertheless, its output voltage has been determined at the design stage according to the characteristics of the installed capacitors, inductors and transformers, which causes low control flexibility. Furthermore, the voltage and current ratings of their semiconductor components are high in the scenario of HVDC transmission. By adding submodules (SMs), modular multilevel converters (MMCs) can achieve high voltage conversion ratio without increasing the voltage stress of components. Additionally, for MMCs [25,26], the high voltage and large size batteries can be distributed into several relatively smaller ones by connecting them with SMs. However, the battery cells are series connected to achieve a high voltage level, which requires BMS for them, resulting in high complexity [27]. Alternatively, the batteries cells can be decentralized into each submodule of multi-module converters [28,29] so that the distributed control of battery cells is achieved, and the BMS among isolated battery modules can be eliminated.

In this paper, based on the multi-module converter in [28], a novel bidirectional MPC is developed and adopted as the SM. The desired advantages such as power stage integration, low voltage stress of semiconductor components, expandable output voltage and power remain. Additionally, the power flow control of PV-battery output is more flexible because battery cells are controlled individually by each power cells with phase-shift (PS) as well as pulse width modulation (PWM) control. Moreover, the fault tolerant capability is improved to increase the reliability.

The paper is organised as follows: the basic cell is analysed in Section 2; the scalable topology design, operation and the fault tolerance strategy are discussed in Section 3; then, Section 4 presents the simulation results to verify the operation of the converter; finally, Section 5 concludes the main points of this paper.

2. Analysis of the Basic Cell

2.1. Topology of the Basic Cell

The topology of the basic power cell with PV panel is shown in Figure 2, consisting of the primary circuit, the battery side circuit, and the single-phase bridge rectifier linked through a transformer with four windings. The components in the primary circuit contains two main switches S_{M1}–S_{M2}, three clamp switches S_{C0}–S_{C1}, one clamp capacitor C_c, one input inductor L_1, and one input diode D_{in}. The battery side circuit is formed by two phase legs consisting of switches S_1, S_4 and S_2, S_3, and the inductor L_2. The output is in series connection with the single-phase bridge rectifier consisting of four diodes D_1–D_4. The transformer has the turns ratio as N_{p1}:N_{p2}:N_{s1}:N_{s2} = 1:1:1:n, and the leakage inductance connected with the output side is L_k.

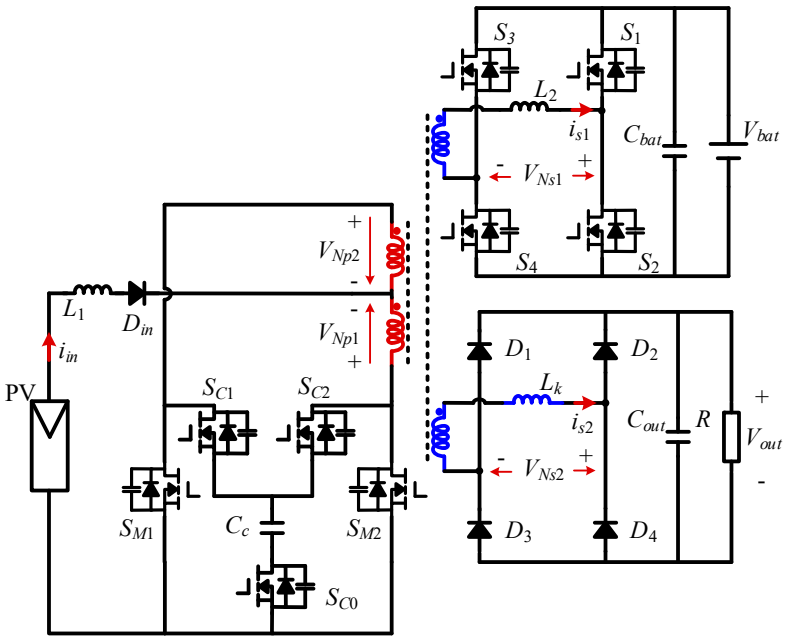
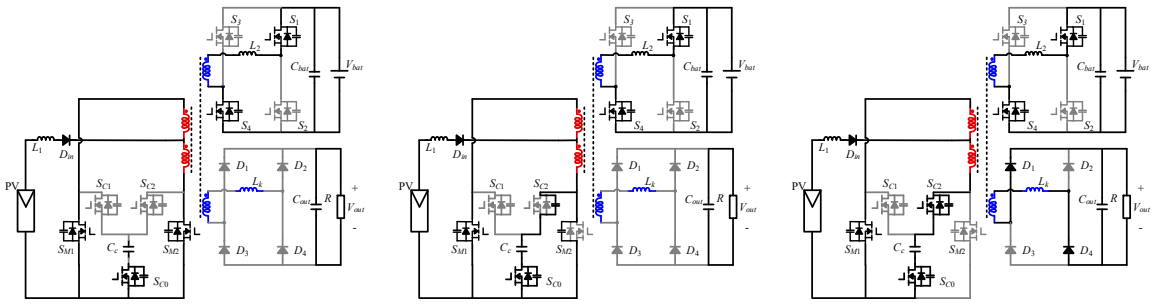


Figure 2. Topology of the basic cell.

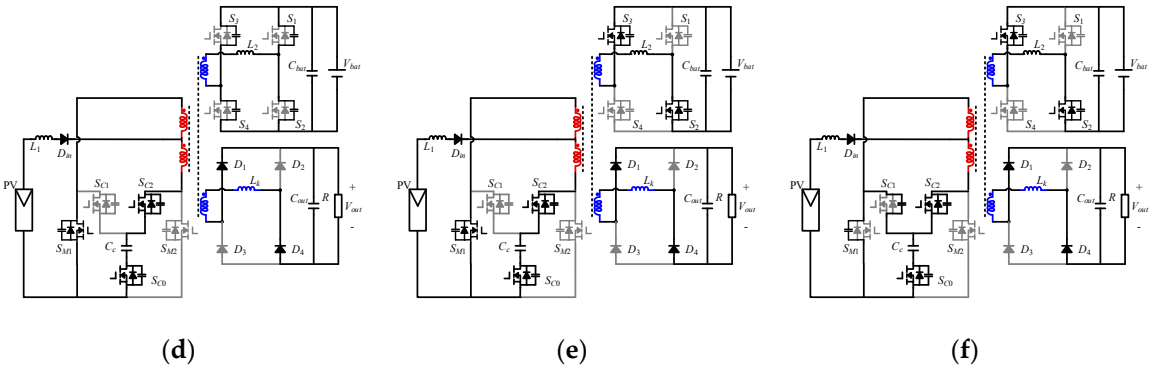
2.2. Operation of the Basic Cell with PV Source

The equivalent circuits of different operation modes and the steady-state waveforms for the basic cell with PV source are illustrated in Figures 3 and 4. V_{gsM1}–V_{gsM2} are the control signals with the duty cycle D_p for the two main switches S_{M1}–S_{M2}, which have a 180° phase shift angle. V_{gsc1}–V_{gsc2} are the control signals for the two clamp switches S_{C1}–S_{C2}, which are complementary to V_{gsM1}–V_{gsM2}, respectively. V_{gs1}–V_{gs4} are the control signals for switches S_1–S_4, which are set as $V_{gs1} = V_{gs4}$, and $V_{gs2} = V_{gs3}$. V_{gs1} and V_{gs3} have the same duty cycle D_b. V_{dsM1}–V_{dsM2}, V_{dsc1}–V_{dsc2}, and V_{ds1}–V_{ds4} are the drain–source voltages of switches S_{M1}–S_{M2}, S_{C1}–S_{C2}, and S_1–S_4. When there is the PV source, the switch S_{C0} is on permanently and $D_b = 0.5$. The PWM control for CFPP and the phase shift angle θ_1 between the V_{CFPP} and V_{FB} regulates the voltage level and power of the battery and output. To simplify the analysis, all switches and diodes are assumed to be identical, and the clamp capacitor is large enough so that the voltage ripple can be ignored.



(**a**) (**b**) (**c**)

Figure 3. *Cont.*



(**d**) (**e**) (**f**)

Figure 3. Equivalent circuits of the operation modes with PV source: (**a**) *Mode* 1 (t_0–t_1); (**b**) *Mode* 2 (t_1–t_2); (**c**) *Mode* 3 (t_2–t_3); (**d**) *Mode* 4 (t_3–t_4); (**e**) *Mode* 5 (t_4–t_5); (**f**) *Mode* 6 (t_5–t_6).

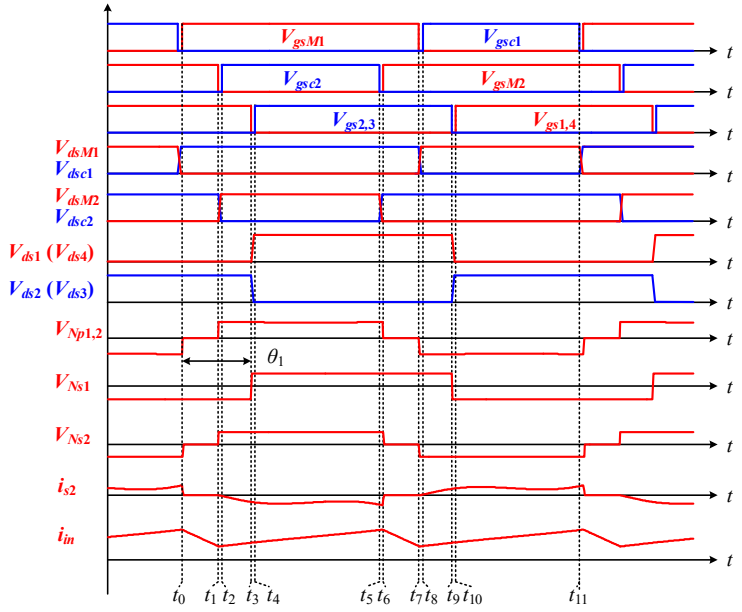


Figure 4. Operating waveforms of the basic cell with PV source.

In this example, the battery is charged. Only the operation of the basic cell during t_0–t_6 is introduced in this part because of the symmetrical operation.

Mode 1 (t_0~t_1): In this mode, the main switches S_{M1} and S_{M2} are on. The primary sides N_{p1}, N_{p2} are short-circuited. All the four diodes are reverse biased. At the same time, S_1 and S_4 are on. The voltage of the battery side N_{s1} is negative.

Mode 2 (t_1~t_2): At t_1, the main switch S_{M2} is turned off. The primary-side referred inductance resonates with the parasitic capacitances of S_{M2} and S_{C2}. The voltage across S_{C2} drops to zero at t_3 so that ZVS turn-on of S_{C2} is obtained.

Mode 3 (t_2~t_3): At t_2, the clamping switch S_{C2} is turned on with zero voltage. The energy is transferred from the PV and input inductor L_1 to the output. The diodes D_1 and D_3 are forward biased, and the current i_s increases.

Mode 4 (t_3~t_4): At t_3, switches S_1 and S_4 are turned off. The voltage V_{FB} becomes positive. The inductor L_2 resonates with the parasitic capacitances of S_1–S_4. The voltage across S_2 and S_3 drops to zero at t_5 so that ZVS turn-on of S_2 and S_3 is obtained.

Mode 5 (t_4~t_5): At t_4, switches S_2 and S_3 are turned on with zero-voltage. The power starts to be delivered into the FB circuit.

Mode 6 (t_5~t_6): At t_5, the clamp switch S_{C2} is turned off. The primary-side referred inductance resonates with the parasitic capacitances of S_{M2} and S_{C2}. The voltage across S_{M2} drops to zero at t_6 so that ZVS turn-on of S_{M2} is obtained.

Altering the duty cycle D_p, the three-level voltage waveforms $V_{Np1,2}$ and V_{Ns2} are generated in the primary side and the rectifier bridge. According to the flux balance of the input inductor L_1, the clamp voltage can be derived as

$$V_{in}(D_p - 0.5) + (V_{in} - 0.5V_{Cc})(1 - D_p) = 0 \tag{1}$$

$$V_{Cc} = \frac{V_{in}}{(1 - D_p)} \tag{2}$$

The output voltage can be determined as

$$\frac{V_{out}}{n} - \frac{V_{out}D_p}{n} - V_{in} + V_{in}D_p - V_{in}D_p + \frac{V_{in}}{2} = 0 \tag{3}$$

$$V_{out} = \frac{n}{2}\frac{V_{in}}{(1 - D_p)} \tag{4}$$

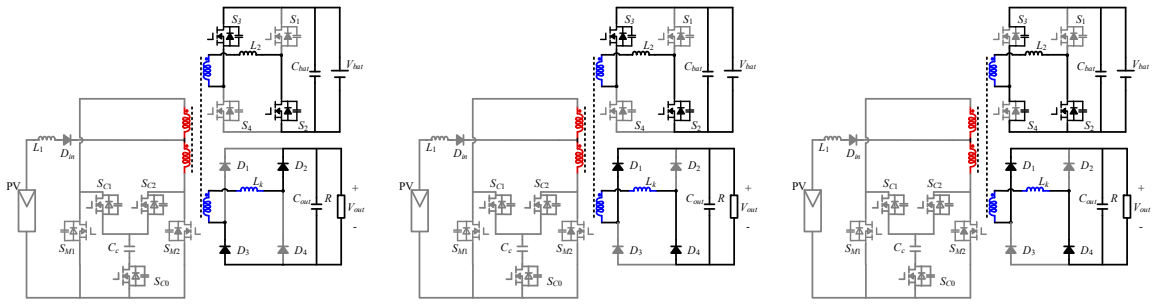
Additionally, based on the average power flow calculation of bidirectional power converters [30,31], the power transfer between P_{in} and P_{bat} with the switching frequency f_s is obtained in Equation (5). A specific phase shift θ_1 controls the power delivered to the battery. When $0 < \theta_1 < \pi$, the power can be transferred from the PV to battery and vice versa. Additionally, the power transfer between P_{in} and P_{bat} with the switching frequency f_s is obtained as

$$P_{in\leftrightarrow bat} = \frac{1}{T}\int_0^T v_p(t)i_L(t) = \frac{V_{in}V_{bat}}{\omega L_2}(2(1 - D_p)\theta_1 - \frac{\theta_1^2}{\pi} - 2(1 - D_p)^2\pi + (1 - D_p)\pi) \quad D_p \geq 0.5 \tag{5}$$

where $\omega = 2\pi f_s$.

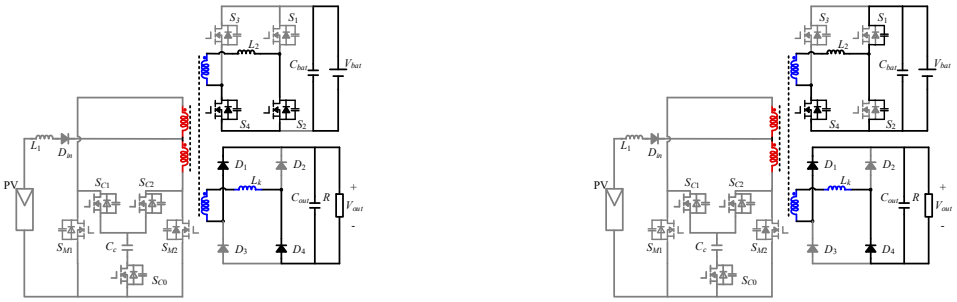
2.3. Operation of the Basic Cell without PV Source

When there is no PV source, the equivalent circuits of different modes and the steady-state waveforms for the basic cell are illustrated in Figures 5 and 6. V_{gs1} and V_{gs3} have a 180° phase shift angle with the duty cycle $D_b \leq 0.5$. V_{gs2}, V_{gs4} are complementary to V_{gs1}, V_{gs3} respectively. Additionally, the primary circuits are blocked to reduce the conduction losses. Because the operation is symmetrical, only the operation during t_0–t_5 is introduced in this part.



(**a**) (**b**) (**c**)

Figure 5. *Cont.*



(**d**) (**e**)

Figure 5. Equivalent circuits of the operation modes without PV source: (**a**) *Mode* 1 (t_0–t_1); (**b**) *Mode* 2 (t_1–t_2); (**c**) *Mode* 3 (t_2–t_3); (**d**) *Mode* 4 (t_3–t_4); (**e**) *Mode* 5 (t_4–t_5).

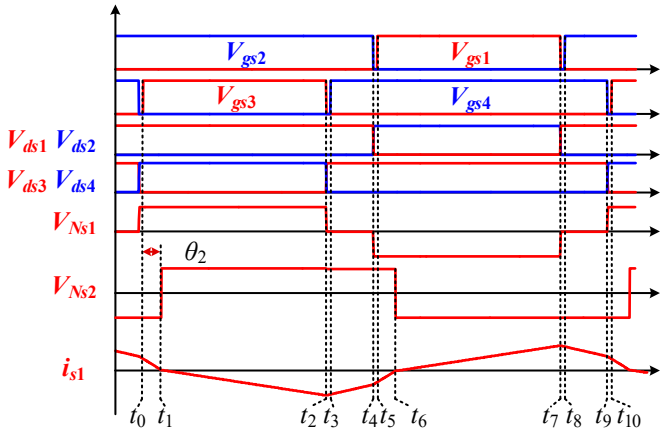


Figure 6. Operating waveform of the basic cell without PV source.

Mode 1 (t_0–t_1): At t_0, switch S_3 is turned on. There is a phase shift θ_2 between V_{Ns1} and V_{Ns2}, which is dependent on the inductance L_2, L_k and the output load. The battery-side current i_{s1} recovers to zero at t_1. The current i_{s1} as a function of $\beta = \omega t$ is derived as

$$i(\beta) = (\frac{V_{bat} + V'_o}{\omega L'_{bat}})\beta + i(0) \tag{6}$$

where V'_o is the battery-side referred output voltage, which equals to V_{out}/n; L'_{bat} is the battery-side referred inductance and $L'_{bat} = L_2 + L_{out}/n^2$.

Mode 2 (t_1–t_2): At t_2, i_{s1} starts to decrease. The voltage of V_{Ns2} becomes positive. In this mode, i_{s1} is determined as

$$i(\beta) = (\frac{V_{bat} - V'_o}{\omega L'_{bat}})(\beta - \theta_2) + i(\theta_2) \tag{7}$$

Mode 3 (t_2–t_3): At t_2, switch S_3 is turned off. The voltage V_{Ns1} drops to zero. The battery-side referred inductance resonates with the parasitic capacitances of switches S_3 and S_4. The parasitic capacitor of S_4 is discharged to zero. Therefore, ZVS turn-on of S_4 is obtained at t_3.

Mode 4 (t_3–t_4): At t_4, switch S_4 is turned on with zero voltage. The current i_{s1} starts to increase as shown in Equation (8):

$$i(\beta) = (\frac{-V'_o}{\omega L'_{bat}})(\beta - (D_b + t_{ds}) \cdot 2\pi) + i((D_b + t_{ds}) \cdot 2\pi) \tag{8}$$

where t_{ds} is the dead time between switches S_1–S_2 and S_3–S_4.

Mode 5 (t_4–t_5): At t_4, switch S_2 is turned off. The voltage V_{Ns1} drops to negative. The battery-side referred inductance resonates with the parasitic capacitances of switches S_1 and S_2. The voltage across S_1 is discharged to zero so that ZVS turn-on of S_1 can be achieved at t_5.

Because the dead time t_{ds} is relatively short, modes 3, 5 can be neglected in the calculation and the phase shift between voltage V_{Ns1} and V_{Ns2} defined as θ_2. Therefore, Equation (9) is derived according to Equation (8).

$$i(\beta) = (\frac{-V_o'}{\omega L_{bat}'})(\beta - D_b \cdot 2\pi) + i(D_b \cdot 2\pi) \tag{9}$$

At t_5, $i(t_5) = -i(t_0)$ since it is the end of half cycle. Additionally, $i(\theta_2) = 0$. Then, θ_2 can be derived as shown in Equation (10):

$$\theta_2 = \frac{1}{2}(D_b \cdot \pi - d\pi) \tag{10}$$

where d is defined as ${V_o}'/V_{bat}$. The power transfer is obtained as

$$P_{bat \to out} = \frac{1}{T}\int_0^T v_{bat}(t) i_{s1}(t) = \frac{V_{bat} V_{out}}{4\omega L_{bat}' \cdot n}(2D_b \cdot \pi - \pi d^2 - D_b^2 \cdot \pi) \tag{11}$$

3. Analysis of the Proposed Converter with Scalable Topology

As shown in Figure 7, the proposed modular multi-port bidirectional converter is composed of the basic cell illustrated in Figure 2 The primary sides are in parallel connection with the PV source V_{in}. The battery cells are decentralized into each basic cell to obtain individual control. Additionally, the output-side windings N_{s2} of transformers are connected in an $s \times p$ matrix configuration, where s is the row number, and p is the column number. The matrix configuration of the converter can be easily expanded to achieve high output voltage and power rating by increasing its row number and column number respectively. Therefore, the converter can satisfy the RESs applications demanding high voltage step-up ratios and high power scales.

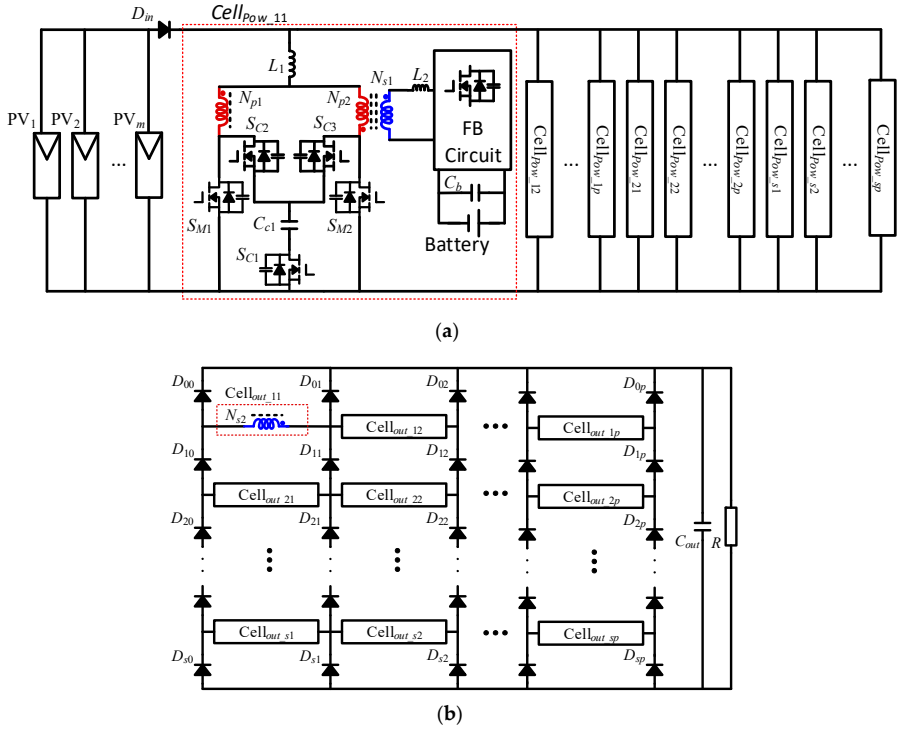


Figure 7. Topology of the proposed converter with s rows and p columns: (**a**) primary circuits with ES system; (**b**) secondary circuits connecting.

3.1. Operation Principle of the Scalable Topology

Cells of the scalable topology have similar operations with those for one basic cell except that the drive signals of switches in adjacent cells have a 180° phase shift. For example, cells 12, 21, 23, and 32 have the same drive signals, whose phases are shifted by 180° from the corresponding drive signals of cell 22. Hence, the polarities of output voltages V_{s2} and currents i_{s2} for adjacent cells are opposite. Then, the column interleaved working strategy of matrix topology is shown in Figure 8.

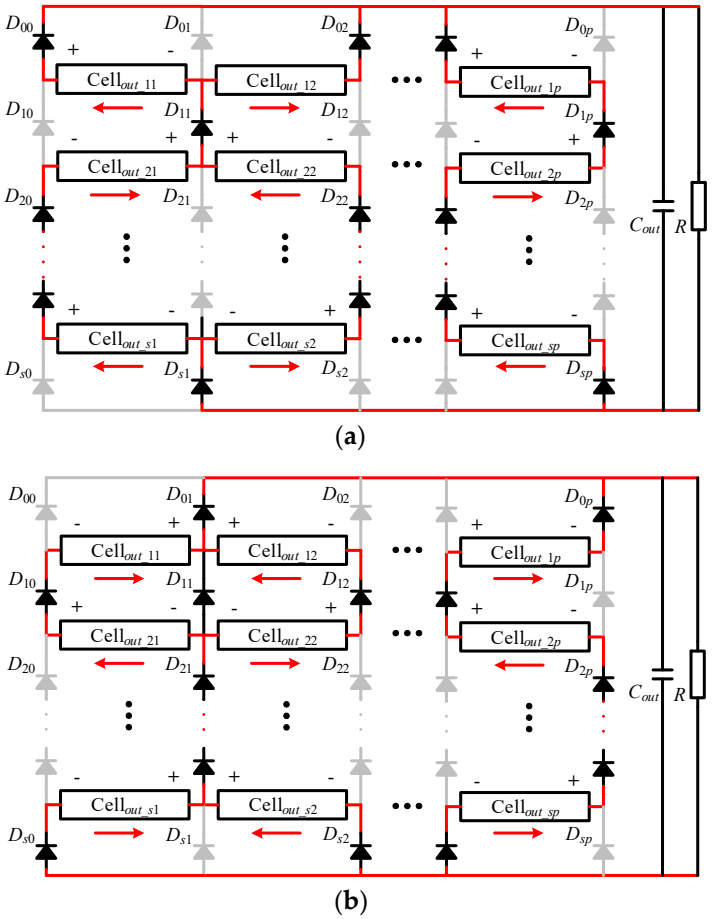


Figure 8. Equivalent secondary circuits of the $s \times p$ topology in the column interleaved strategy: (**a**) column interleaved mode 1; (**b**) column interleaved mode 2.

The output voltage is the sum of the voltages V_{s2} of cells in the same column, and the output current is the sum of the currents i_{s2} in every column, which are shown in Equation (12) with the assumption that every cell has the identical output voltage and current. Therefore, the high output voltage and power rating can be easily obtained by increasing the row and column number of the matrix topology.

$$\begin{cases} V_{o,s\times p} = s \times V_{s2} = \frac{s\times n}{2(1-D_p)} V_{in} \\ I_{o,s\times p} = p \times I_{s2} \end{cases} \tag{12}$$

Due to the parallel connection of primary-side circuit and individual battery-side circuit, all switches have the low voltage rating with high output voltage. The voltage ratings of switches in basic cells are derived as shown in Equation (13).

$$\begin{cases} V_{ds\_Np} = V_{Cc} = \frac{V_{in}}{1-D_p} \\ V_{ds\_Ns1} = V_{bat} \end{cases} \tag{13}$$

The current stress of diodes in columns 0 and p has half the value of I_{s2}, which is the average output current of the basic cell. Nevertheless, the diodes in columns 1 to $p-1$ have twice the current stress higher than that of other diodes, since they are connected with two basic cells. The sum of average currents of diodes in all columns equals the output current as shown in Equation (14), and the current stress of diodes is derived in Equation (15). Similarly, the voltage stress of diodes is obtained in Equation (16). For diodes in rows 1 to $s-1$, the voltage stress has twice the value larger than that of the diodes in rows 0 and s.

$$\sum_{j=0}^{p} I(D_{ij}) = I_{o,s\times p} \tag{14}$$

$$I(D_{ij}) = \frac{1}{2} I_{s2} = \begin{cases} \frac{1}{2p} I_{o,s\times p} & j = 0, p \\ \frac{1}{p} I_{o,s\times p} & j = 1, 2, \cdots, (p-1) \end{cases} \tag{15}$$

$$V(D_{ij}) = \begin{cases} \frac{n}{2(1-D_p)} V_{in} & i = 0, s \\ \frac{n}{(1-D_p)} V_{in} & i = 1, 2, \cdots, (s-1) \end{cases} \tag{16}$$

The maximum current and voltage stress of diodes in the $s \times p$ topology are only twice larger than that of one single cell, which is much lower than the average output voltage $V_{o,s\times p}$ and current $I_{o,s\times p}$. Therefore, the low voltage/current rating semiconductor components such as switches and diodes can be used to achieve a high voltage step-up ratio and output power.

3.2. Control Scheme

Since the number of working rows determines the value of output voltage and that of working columns determines the output current, the variable output power can be obtained. As shown in Figure 9, power control is achieved by controlling the working columns according to the input current and battery charged/discharged power value. The voltage control is mandatory to meet the system operation requirements by the PS–PWM control of switches in the primary-side and battery-side circuits.

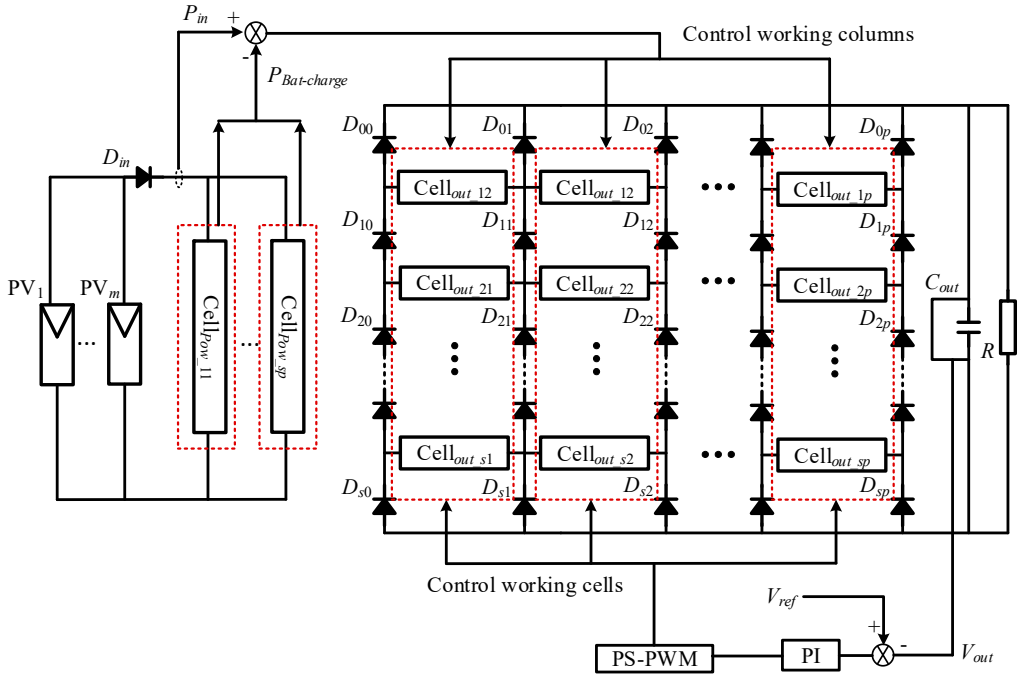


Figure 9. Control scheme of the $s \times p$ topology.

3.3. Fault Tolerance

For power electronics systems, semiconductor components are vulnerable devices [32]. With unexpectedly damaged devices, the whole system has to stop and wait for maintenance, resulting in high cost and loss. Figure 10 shows the fault tolerant operation with redundancy. In normal operation, the redundant cells in columns $p1$ and $p2$ are inactive, and the converter is working with the column interleaved strategy as shown in Figure 8. When there are failed cells, the converter can maintain normal operation by replacing the faulty column with one redundant column. For the damaged diodes in columns 1 to $p-1$, two redundant columns are necessary. For example, when cell 11 fails, the column in the red dotted rectangle is replaced by the redundancy in another red dotted box. For the defective diode D_{11}, columns 1 and 2 in the blue dotted box are idle, and the redundant columns $p1$ and $p2$ are applied.

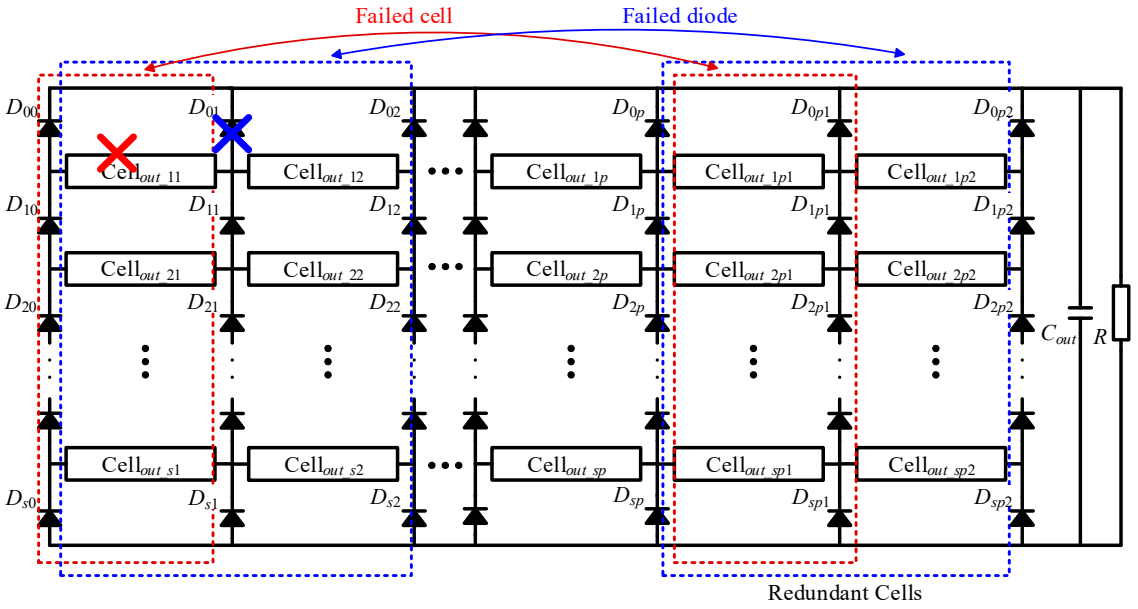


Figure 10. Fault tolerance with redundancy.

Additionally, owing to the matrix configuration and flexible control, the converter can still obtain fault tolerance of cells and diodes without redundancy as depicted in Figure 11. When there are failed cells or short-circuited diodes, the converter can still work as in Figure 11a,b. When diode D_{11} is short-circuited, its connecting rows 1 and 2 are inactive to block the damaged devices. The other cells still operate with the column interleaved strategy and the duty cycle D_p of them is increased to obtain the normal output voltage with fewer working rows. The fault tolerance of the open-circuited diode can be achieved as shown in Figure 11b,c. The fault tolerance operating group consists of the adjacent columns of the failed diode D_{11}, where the drive signals of cells in adjacent rows have a 180° phase shift and the cells in the same row have the same signals. Then, the adjacent rows have opposite polarities, and the cells in the same rows have the same polarity. Therefore, all cells in the faulty group are connected in series to block the damaged diode. To achieve the same terminal voltage, the output voltages of cells in the faulty group is half of that in the normal operation groups since the number of cells series-connected in the faulty group is twice larger than that in the normal operation group.

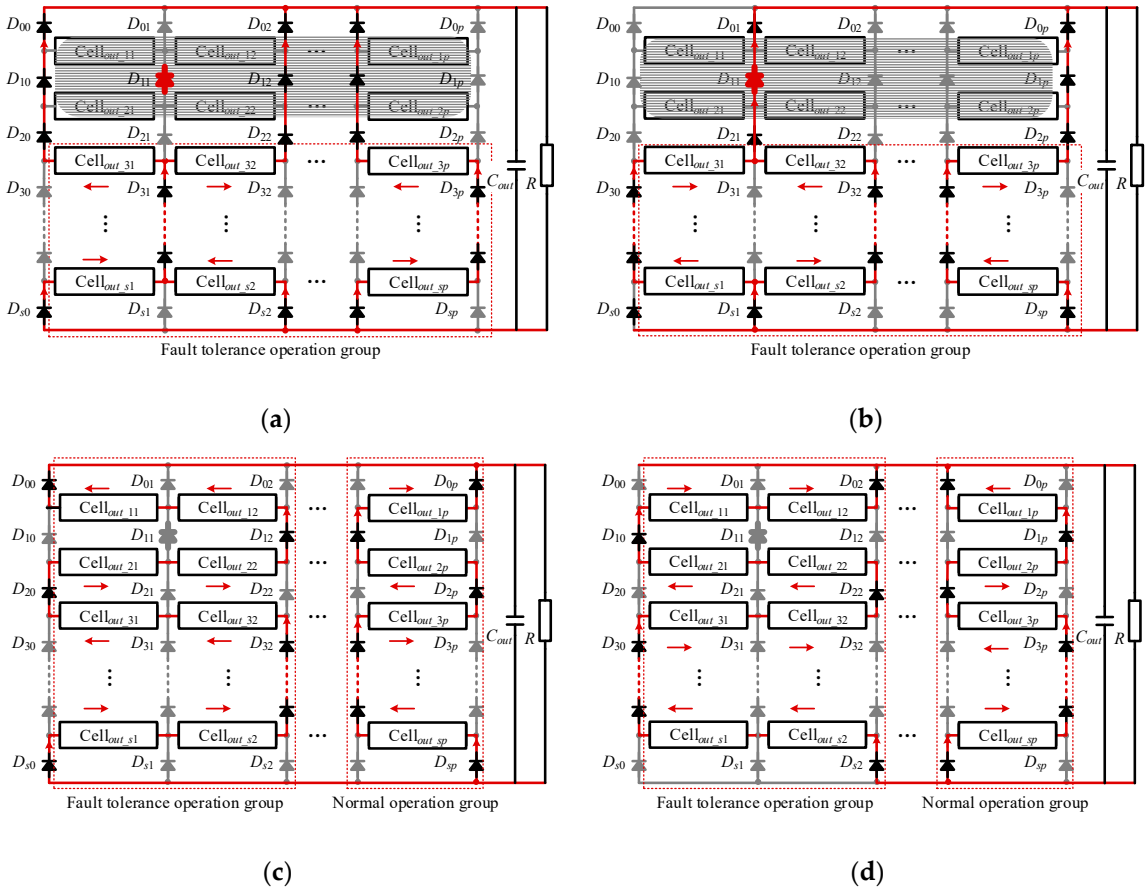


Figure 11. Fault tolerance without redundancy: (**a**) Working mode 1 under diode short-circuit; (**b**) Working mode 2 under diode short-circuit; (**c**) Working mode 1 under diode open-circuit; (**d**) Working mode 2 under diode open-circuit.

Furthermore, as illustrated in Figure 12, the diodes in the secondary circuits can be prevented from damage under DC fault condition, which is similar to the MMC converter by adding thyristors because they have a higher I^2t capacity compared with diodes.

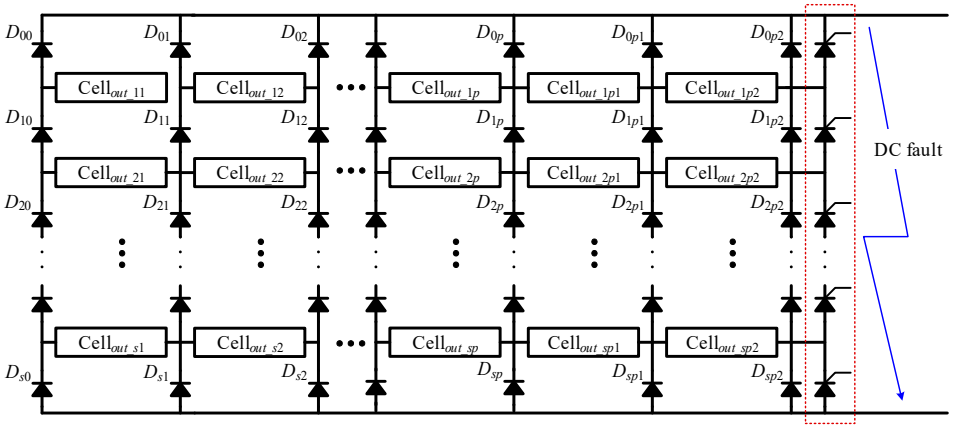


Figure 12. Addition of thyristors to protect secondary diodes under DC fault.

4. Simulation Results and Discussion

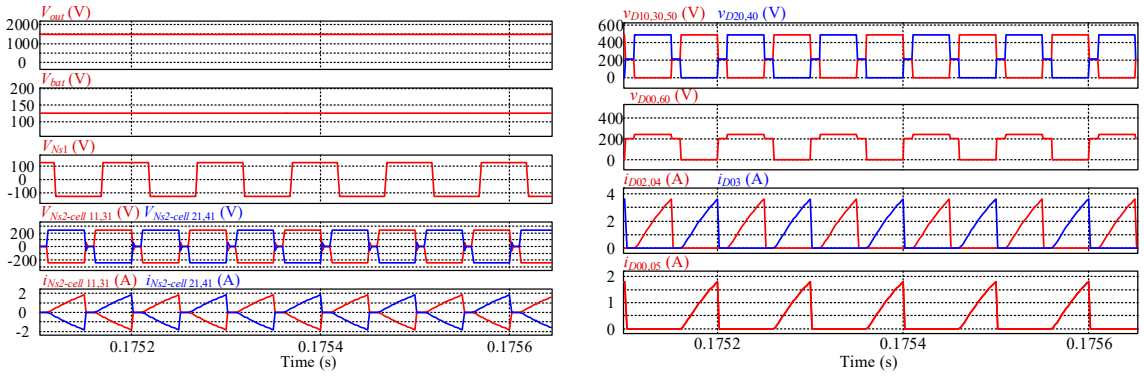
To verify the functionality of the proposed converter, a simulation model consisting of six rows×six columns that is similar to the one shown in Figure 7 is built in the software PSIM.

For the six columns, columns 1–4 are active, while columns 5–6 are redundant. Table 1 presents the simulation parameters

Table 1. Simulation parameters.

System Parameters	Values	Components	Values
Input Voltage	100 V	Turns ratio 1:1:1:n	1:1:1:2
Output Voltage	1500 V	Leakage inductance L_k	60 µH
Battery	125 V	Input inductor L_1	5 mH
Switching Frequency	10 kHz	Inductor L_2	2 mH
Output Power	5 kW	Clamp capacitor C_c	20 µF

The steady-state waveforms of the converter are shown in Figures 13 and 14. All cells in columns 1–4 work with the column interleaved strategy. The adjacent cells have the opposite voltage and current polarities. With six rows in the matrix structure, the power switches have low voltage stress, which is 1/6 of the output voltage, and the voltage and current ratings of all diodes are as low as 1/6 or 1/3 of the output voltage and current respectively.



(**a**) (**b**)

Figure 13. Steady-state waveforms with PV source: (**a**) voltage/current of basic cells; (**b**) voltage/current of diodes.

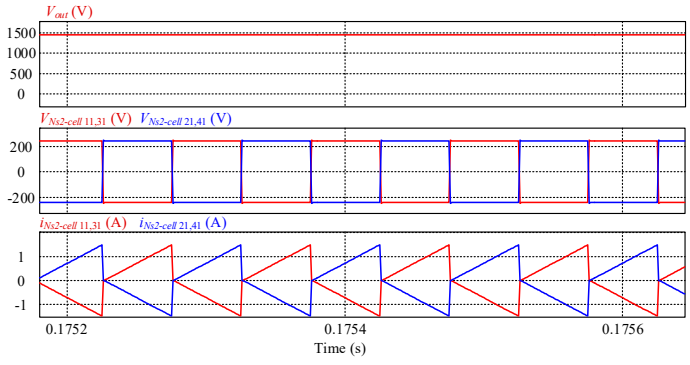


Figure 14. Steady-state waveforms of voltage/current of basic cells without PV source.

As illustrated in Figure 15, before turning on switch S_{M1} or S_{C1} in the primary circuits, the drain-source currents of both switches, i_{dsM1} and i_{dsC1}, are negative which shows the currents flow through their parasitic diodes so that zero-voltage turn-on is achieved for S_{M1} or S_{C1}. Similarly, the switches S_{M2} and S_{C2} can also obtain ZVS due to symmetrical operation.

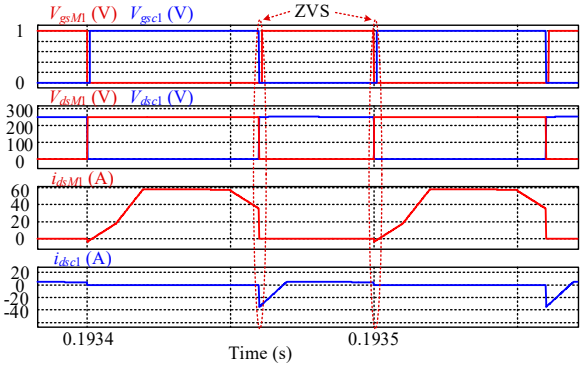
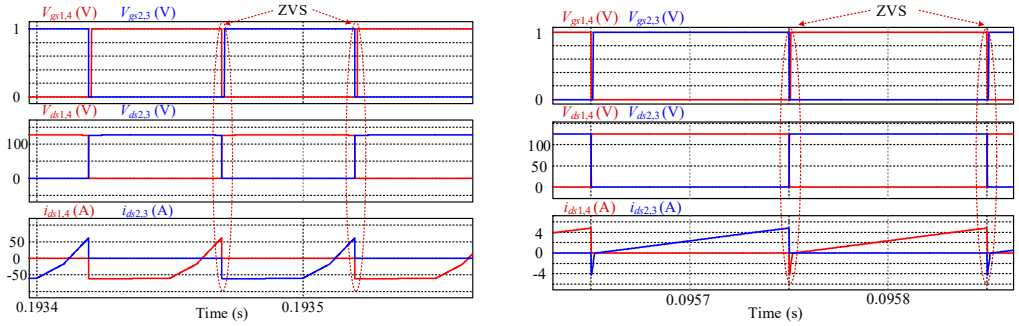


Figure 15. Zero voltage switching (ZVS) of switches in the primary circuit.

The voltage–current waveforms for switches S_1–S_4 are depicted in Figure 16 where D_b is set as 0.5. As shown in Figure 16a, when the battery is charged, the currents flow through the parasitic diodes of the corresponding switch before the switch is turned on so that ZVS is achieved. When the battery is discharged in Figure 16b, four switches still can be turned on with zero voltage due to the resonance between the inductance L_2 and the parasitic capacitance of switches. Therefore, all switches can achieve ZVS turn-on, which significantly reduces the switching loss.



(**a**) (**b**)

Figure 16. Zero voltage switching (ZVS) of switches in the battery side circuit: (**a**) battery is charged; (**b**) battery is discharged.

Figure 17 illustrates the fault tolerance capability with redundancy. At 0.1 s, columns 1–2 are inactive in the case that there are fault cells in columns 1–2 or diodes in columns 0–1. Then the redundant columns 5–4 start to work to guarantee the normal operation.

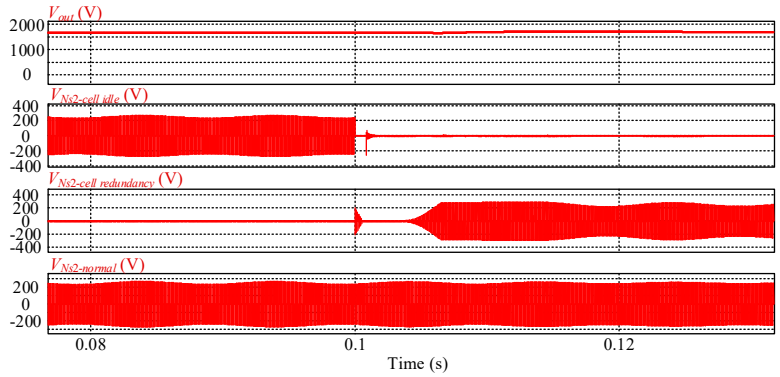
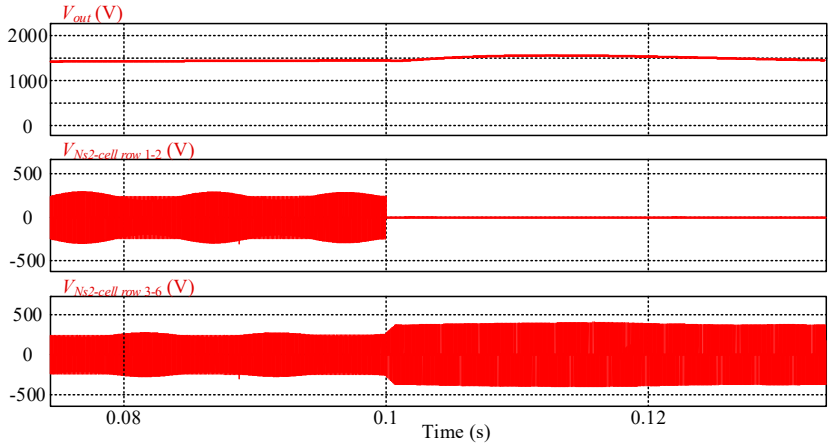
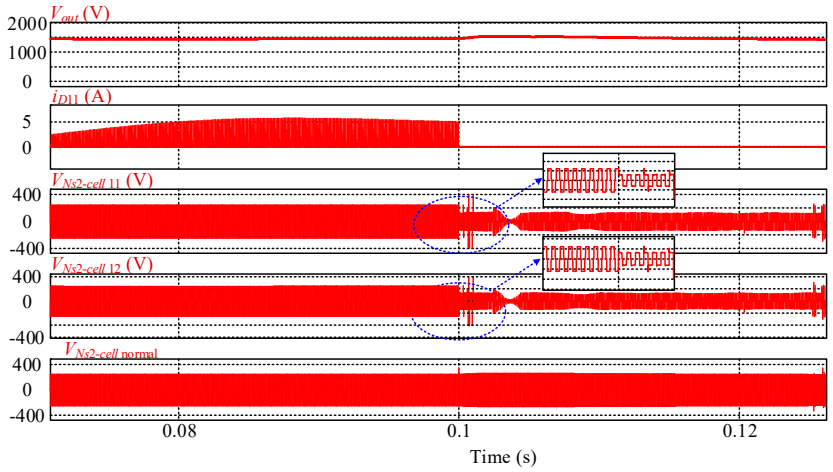


Figure 17. Fault tolerance operation with redundancy.

Figure 18 presents the fault tolerance operation without redundancy, where only columns 1–4 are active. In Figure 18a, when diode D_{11} is short-circuited, the cells in rows 1–2 are inactive at 0.1 s to block the defective component. The duty cycle of switches in primary circuits is modified according to Equation (9) to maintain the normal output voltage. In Figure 18b, diode D_{11} is open-circuited at 0.1 s. To block the failed components, the cells in the columns adjacent to D_{11} are all in series-connection by changing the voltage polarities of the cells in column 1. Furthermore, the voltages of cells in the faulty group are reduced to half of that in the normal operation group to obtain the same terminal voltage.



(**a**)



(**b**)

Figure 18. Fault tolerance operation without redundancy: (**a**) Without redundancy for D_{11} short-circuit; (**b**) Without redundancy for D_{11} open-circuit.

5. Conclusions

A modular multi-port bidirectional high power level DC/DC power converter applied for HVDC transmission of RESs is proposed in this paper. Thanks to the three-port basic cell, ES can be integrated with HVDC system with low component count as well as high compactness, and the power is transferred within one conversion stage. Additionally, due to the modularity, the proposed converter can achieve high output voltage and power by adding SMs.

The performances of isolated MPCs, partial-isolated MPCs, MMCs with ES system, and the proposed converter are compared. The proposed model appears to be more efficient and reliable, presenting the features of low switching loss, high DC voltage conversion ratio, high control flexibility, and high reliability.

The simulation results verify the advantages of the proposed converter such as the low voltage and current ratings of semiconductor components, ZVS turn-on of power switches, flexible control and improved fault tolerance operation.

Author Contributions: Conceptualization, Y.H.; Formal analysis, S.S. and Y.H.; Investigation, S.S.; Methodology, S.S. and Y.H.; Software, S.S.; Supervision, Y.H.; Validation, S.S.; Writing—original draft, S.S.; Writing—review and editing, W.L., K.N., H.X., and J.S.

Funding: This research received no external funding.

Conflicts of Interest: The authors declare no conflict of interest.

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