


Article

Bidirectional Interleaved PWM Converter with High Voltage-Conversion Ratio and Automatic Current Balancing Capability for Single-Cell Battery Power System in Small Scientific Satellites

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Abstract: Single-cell battery power systems are a promising bus architecture for small scientific satellites. However, to bridge the huge voltage gap between a single-cell battery and power bus, bidirectional converters with a high voltage conversion ratio and a large current capability for the low-voltage side are necessary. This article proposes a bidirectional interleaved pulse width modulation (PWM) converter with a high voltage conversion ratio and an automatic current balancing capability. By adding capacitors to conventional interleaved PWM converters, not only are inductor currents automatically balanced without feedback control or current sensors, but also voltage conversion ratios at a given duty cycle can be enhanced. Furthermore, the added capacitors can reduce voltage stresses of switches and charged-discharged energies of inductors, realizing more efficient power conversion and reduced circuit volume in comparison with conventional converters. A 100-W prototype was built for experimental verification, and results demonstrated the fundamental characteristics and efficacy of the proposed converter.

Keywords: bidirectional converter; current balancing; interleaved converter; high voltage-conversion ratio; scientific satellite; single-cell battery

1. Introduction

Vigorous research and development efforts for small scientific satellites are underway to realize frequent and low-cost scientific space missions. Traditional power systems in scientific satellites employ an unregulated bus architecture, where a rechargeable battery and load are directly connected, as illustrated in Figure 1a. The unregulated bus architecture (see Figure 1a) is advantageous over regulated bus architectures (see Figure 1b) from the viewpoint of the system simplicity, as no dedicated converter for battery regulation is necessary. However, since the battery is directly connected to the load in the unregulated bus architectures, the number of battery cells connected in a series is determined by the load voltage requirement—e.g., eight and twelve cells for 28-V and 50-V bus systems, respectively. The energy capacity of the battery in watt-hours should be adjusted by selecting or manufacturing cells with a proper capacity, hence impairing the design flexibility. The poor design flexibility is quite unfavorable for small satellites, to provide frequent scientific mission opportunities.

Although the converter count is doubled, the regulated bus architecture (see Figure 1b) is attractive from the viewpoint of battery design flexibility. The number of battery cells connected in series can be arbitrarily changed to meet the energy capacity demand, and even a single-cell battery system is theoretically feasible, as shown in Figure 1c [1]. Despite the cost penalty of the additional bidirectional

converter for batteries, the regulated bus system would be a promising choice to realize frequent scientific space missions demanding a wide range of power requirements.

In general, voltages of series-connected cells are gradually imbalanced due to a minor mismatch in individual cell characteristics, such as capacity, self-discharge rate, and internal impedance. Some cells with higher/lower voltages might be over-charged/discharged, likely accelerating irreversible deterioration and increasing risks of fire or, in the worst case, an explosion. To ensure years of safe operation of batteries consisting of multiple cells connected in series, a cell equalizer is indispensable to mitigate or even eliminate cell voltage imbalance. Cell equalizers are essentially a switching power converter, such as nonisolated bidirectional converters [2–5], single-input multi-output converters [6–9], etc. [10], and these add complexity to spacecraft power systems.

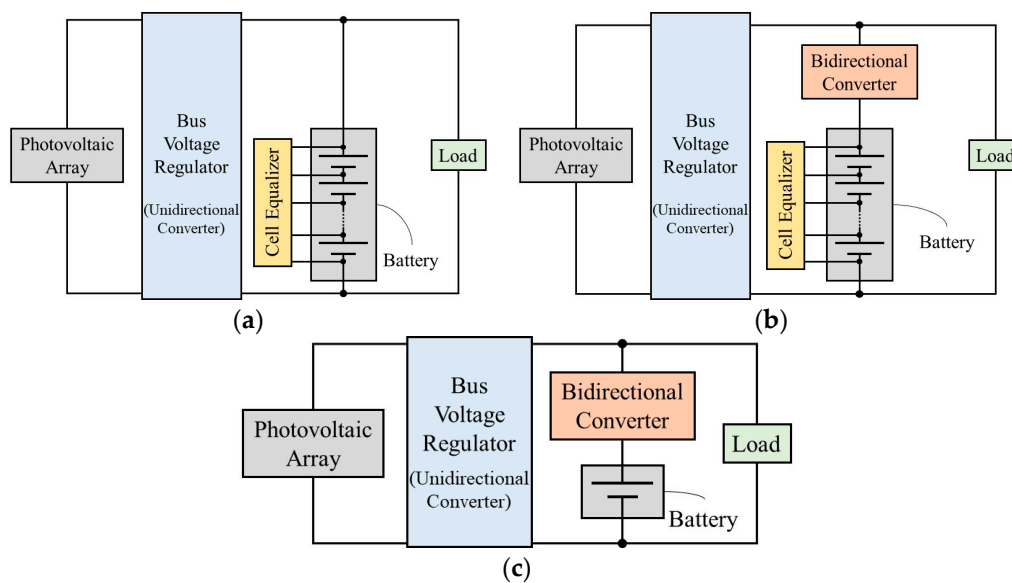


Figure 1. Spacecraft power systems: (a) Conventional unregulated bus architecture; (b) conventional regulated bus architecture; (c) Regulated bus architecture with single-cell battery.

In the single-cell battery system, cell voltage mismatch is no longer an issue because there is only one single cell. Hence, no cell equalizer is necessary, allowing the simplified system configuration, as shown in Figure 1c. Although the single-cell battery system offers flexible battery design and a simplified system, two major challenges concerning bidirectional converters arise.

The first issue is an extreme duty cycle operation. To bridge the huge voltage gap between the power bus (50 V) and single-cell battery (3.0–4.2 V for lithium-ion cells), a conventional nonisolated pulse width modulation (PWM) converter [Figure 2a] must operate with extremely high duty cycles (e.g., duty cycle greater than 0.9). However, conventional converters with such extreme duty cycles are exposed to high voltage and current stresses, and are known to suffer from increased losses and reduced controllability [11]. Coupled- or tapped-inductors [11–14] and switched-capacitor structures [15–17] are often employed to achieve high voltage conversion ratios at a given duty cycle. The coupled- or tapped-inductors behave as a voltage divider whose voltage conversion ratios are adjustable with the turns ratio. Although these magnetic components realize high voltage conversion ratios with relatively simple structures, the increased magnetic design difficulty is often cited as a top concern. Switched capacitors can arbitrarily increase voltage conversion ratios by adding capacitors and switches, but numerous switches are necessary to enhance its voltage gain, likely increasing the circuit complexity.

The second issue is a large current at the low-voltage battery side. A current of the low-voltage side is more than ten times greater than that of the high-voltage side, increasing current stress as well as associated Joule losses. Interleaved PWM converters, which equivalently consist of parallel-connected multiple PWM converters operating out of phase, are a favorable solution to mitigate current stresses

of switches and inductors. The topology shown in Figure 2b is a conventional three-phase interleaved PWM converter, and current stresses of inductors and switches are one-third those of the traditional converter shown in Figure 2a. However, all inductor currents need to be measured using current sensors to achieve active current balancing among multiple phases [18], increasing the cost and control complexity. Otherwise, inductor currents are likely to be unbalanced, due to minor mismatches in resistive components and duty cycles, and current stresses and power conversion losses are likely to soar, due to current concentration [19].

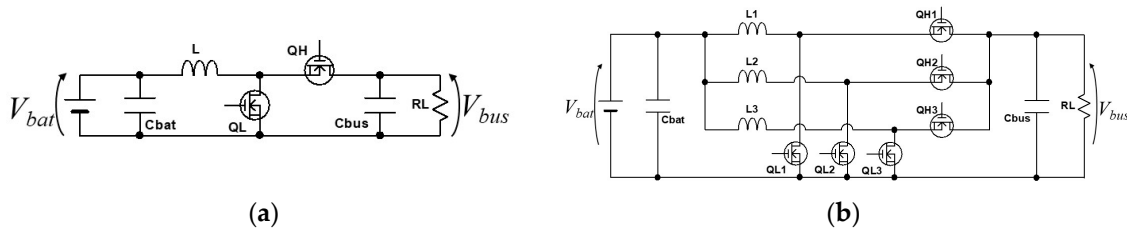


Figure 2. Conventional bidirectional interleaved pulse width modulation (PWM) converters: (a) Single-phase PWM converter; (b) Interleaved three-phase bidirectional PWM converter.

This article presents a bidirectional interleaved PWM converter with high voltage conversion-ratio and automatic current balancing capability for single-cell battery power systems in small scientific satellites. By adding only two capacitors to the conventional interleaved three-phase PWM converter (Figure 2b), the voltage conversion ratio at a given duty cycle is tripled, hence preventing extreme duty cycle operations. Inductor currents can be automatically balanced thanks to the added capacitors, and no current sensor is necessary for inductor current balancing. Furthermore, the added capacitors reduce voltage stresses of switches and charged-discharged energies of inductors, contributing to efficient power conversion and reduced circuit volume.

The rest of this article is organized as follows. Section 2 describes the proposed bidirectional converter topology. The detailed operation analysis, including the derivation for voltage conversion ratio and discussion about automatic current balancing, will be discussed in Section 3. Section 4 presents the quantitative comparison between proposed and conventional converters from the viewpoint of total device power rating (TDPR) and normalized charged-discharged energies in passive components—these can be metrics to quantitatively compare efficiencies and circuit volumes of different converter topologies. Experimental results of a 100-W prototype will be shown to demonstrate the proposed converter in Section 5.

2. Interleaved Bidirectional PWM Converter with High Voltage-Conversion Ratio and Automatic Current Balancing Capability

The proposed bidirectional interleaved PWM converter is shown in Figure 3. Three inductors, L_1 – L_3 , are connected to the battery and share the input current. Currents of these inductors are automatically balanced without feedback control, and therefore, no current sensors nor feedback control loops are necessary. The high- and low-side switches (Q_{Li} and Q_{Hi} , respectively, where $i = 1, \dots, 3$) operate in a complementary mode. Three pairs of switches (Q_{L1} – Q_{H1} , Q_{L2} – Q_{H2} , Q_{L3} – Q_{H3}) and inductors operate in the interleaving manner 120° out of phase, and thus, this converter can be regarded as a three-phase interleaved converter when viewed from the battery side. Capacitors, C_1 and C_2 , play two roles of a high voltage-conversion ratio and automatic current balancing, as will be discussed in the next section.

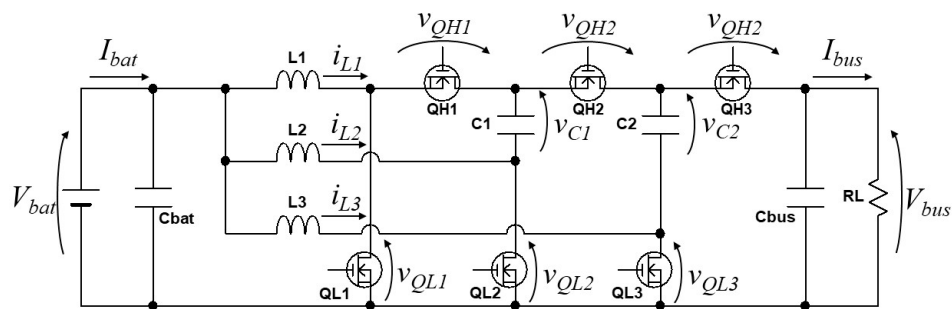


Figure 3. Proposed interleaved PWM converter with high voltage conversion ratio.

3. Operation Analysis

The presented converter operates as step-up and -down converters when a battery is being discharged and charged, respectively. This section deals only with the step-up operation or battery discharging for the sake of brevity. However, the step-down operation or battery charging can be analyzed similarly. The analysis is performed with the premise that all circuit elements are ideal, with no parasitic components and that all capacitors are large enough so that their voltages are constant.

3.1. Operation Modes and Voltage Conversion Ratio

The theoretical key operation waveforms and current flow directions are shown in Figures 4 and 5, respectively. Gating signals for Q_{L1} – Q_{L3} , v_{gsL1} – v_{gsL3} , are applied so that at least two of three switches are simultaneously on. v_{gsL1} – v_{gsL3} are 120° out of phase for the interleaving operation. One switching cycle can be divided into six operation modes, but three of them are Mode 1, during which all low-side switches are simultaneously turned on.

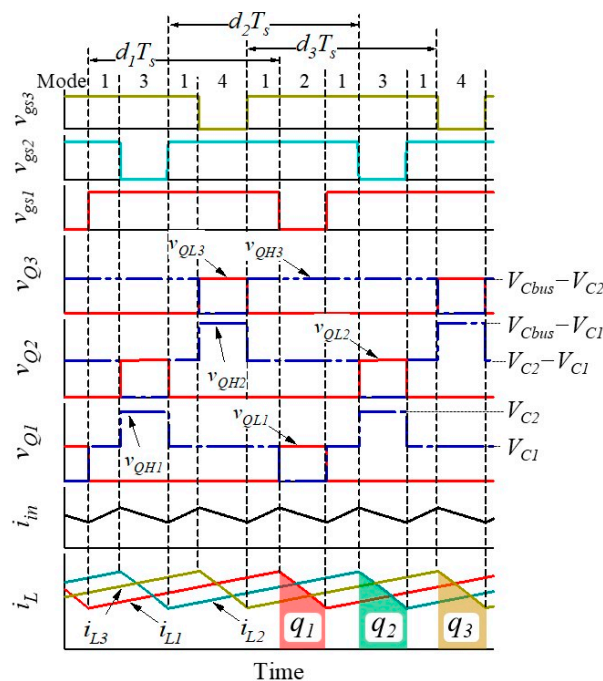


Figure 4. Theoretical key operation waveforms.

Mode 1 (Figure 5a): v_{gsL1} – v_{gsL3} are applied. All the low-side switches are on and their drain-source voltages, v_{QL1} – v_{QL3} , are zero. Inductor currents, i_{L1} – i_{L3} , linearly increase as V_{bat} is applied to L₁–L₃. The input current i_{in} , which is the sum of i_{L1} – i_{L3} , also increases.

Mode 2 (Figure 5b): v_{gsL1} is removed to turn off Q_{L1} . i_{L1} linearly decreases and flows through a channel or body diode of Q_{H1} . Since one of the inductor currents decreases, i_{in} also decreases. C_1 is charged by i_{L1} , and the volt-sec balance on L_1 yields the voltage of C_1 , V_{C1} , as

$$V_{C1} = \frac{1}{1-d_1} V_{bat} \quad (1)$$

where d_1 is the duty cycle of Q_{L1} as designated in Figure 4.

Mode 3 (Figure 5c): v_{gsL2} is at a low level to turn off Q_{L2} . A channel or body diode of Q_{H2} starts to conduct. At the same time, L_2 discharges and its current i_{L2} decreases. Similar to Mode 2, i_{in} decreases due to the decrease in i_{L2} . i_{L2} , together with C_1 , charges C_2 , and the voltage of C_2 , V_{C2} , can be yielded from the volt-sec balance on L_2 , as

$$V_{C2} = V_{C1} + \frac{1}{1-d_2} V_{bat} = \left(\frac{1}{1-d_1} + \frac{1}{1-d_2} \right) V_{bat} \quad (2)$$

where d_2 is the duty cycle of Q_{L2} .

Mode 4 (Figure 5d): Q_{L3} is turned off, and Q_{H3} conducts. L_3 and C_2 charge C_{bus} . i_{L3} discharges, and C_{bus} is charged by i_{L3} and C_2 . From volt-sec balance on L_3 , the voltage of C_{bus} , V_{bus} , is obtained as

$$V_{Cbus} = V_{C2} + \frac{1}{1-d_3} V_{bat} = \left(\frac{1}{1-d_1} + \frac{1}{1-d_2} + \frac{1}{1-d_3} \right) V_{bat} \quad (3)$$

where d_3 is the duty cycle of Q_{L3} . This equation dictates the step-up voltage conversion ratio of the proposed interleaved converter.

Given that all the duty cycles are identical as $d_1 = d_2 = d_3 = d$, (3) can be rewritten as

$$\frac{V_{Cbus}}{V_{bat}} = \frac{3}{1-d} \quad (4)$$

Thus, the voltage conversion ratio of the proposed three-phase interleaved converter is three times greater than that of traditional PWM boost converters.

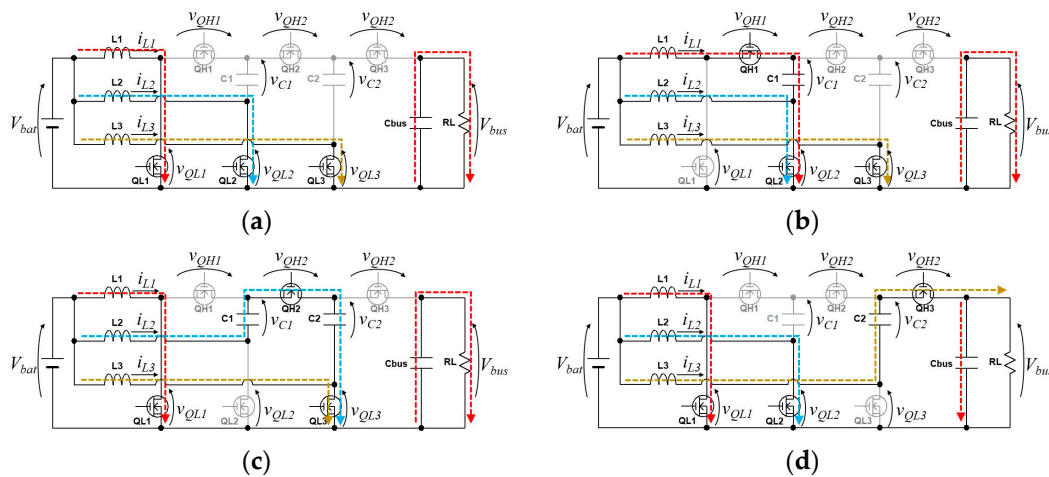


Figure 5. Operation modes in battery discharging: (a) Mode 1; (b) Mode 2; (c) Mode 3; (d) Mode 4.

In order to ensure the operation discussed above, all the low-side switches must be simultaneously on in every switching cycle, and more than two of them must be always on. To this end, d_1-d_3 must be greater than 0.667. Otherwise, inductor currents are no longer balanced.

The voltage conversion ratios of the proposed and conventional converters are compared in Figure 6. For the 50-V bus system, the required voltage conversion ratio is 12.5–16.7 for a lithium-ion

single cell with 3.0–4.2 V. Conventional converters need to operate with an extremely high duty cycle of $d > 0.92$. The duty cycle range of the proposed converter, on the other hand, is reduced to around 0.8, avoiding extreme duty cycle operations.

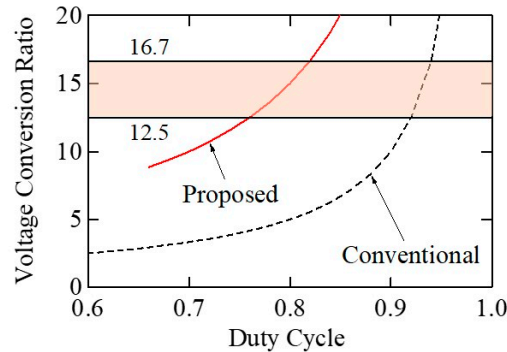


Figure 6. Theoretical step-up voltage conversion ratios of conventional and proposed converters.

3.2. Current Balancing Mechanism

C_1 is charged by i_{L1} during Mode 2 (Figure 5b) and its amount of charge stored corresponds to q_1 in Figure 4. During Mode 3, C_1 is discharged by i_{L2} , and a released charge amount is q_2 . Meanwhile, C_2 receives q_2 as i_{L2} flows through it. In Mode 4, C_2 is discharged by i_{L3} , and its released charge amount is q_3 that is transferred to the bus. The charge balance on C_2 and C_3 yields

$$q_1 = q_2 = q_3 = I_{bus}T_s \quad (5)$$

where I_{bus} is the bus current designated in Figure 3. Since q_1 – q_3 are equal to respective average inductor current I_{L1} – I_{L3} multiplied by mode length, Equation (5) can be rewritten as

$$(1 - d_1)I_{L1} = (1 - d_2)I_{L2} = (1 - d_3)I_{L3} = I_{bus} \quad (6)$$

This equation suggests that the balance among I_{L1} – I_{L3} is dependent on d_1 – d_3 . If d_1 – d_3 are identical, the charge conservation law for C_2 and C_3 ensures complete current balancing for all inductors. This balancing mechanism does not rely on any active control nor current sensing, and therefore, all inductor currents are automatically balanced.

Now consider the non-ideal case that d_1 – d_3 are slightly mismatched as $d_1 = d - \Delta d$ and $d_2 = d_3 = d$, due to non-ideality of microcontrollers and gate drivers. I_{L2} and I_{L3} can be balanced to be I_L , and Equation (6) can be rewritten as

$$(1 - d + \Delta d)I_{L1} = (1 - d)I_L \quad (7)$$

Rearrangement of Equation (7) yields

$$\frac{I_L - I_{L1}}{I_{L1}} = \frac{\Delta d}{1 - d} \quad (8)$$

This equation represents the degree of current imbalance due to duty cycle mismatch. For instance, even if d_1 severely deviates from others as $\Delta d = 0.01$, the inductor current imbalance is merely 5% with $d = 0.8$. Thus, the inductor current imbalance due to the non-ideality of microcontrollers and gate drives would be very minor.

4. Quantitative Comparison

4.1. Total Device Power Rating

Total device power rating (TDPR) is often introduced as a metric to quantitatively compare different topologies from the viewpoint of semiconductor volt-amp stresses [20,21]. TDPR is the sum of the theoretical volt-amp stress of all semiconductor devices normalized by input or output power and is defined as

$$TDPR = \sum_{All\ MOSFETs} \frac{V_{max} I_{max}}{V_{bat} I_{bat}} \quad (9)$$

where V_{max} and I_{max} are the theoretical maximum voltage and current stresses of a metal-oxide-semiconductor field-effect transistor (MOSFET). The lower the value of TDPR, the better the converter's performance will be, as power conversion loss reportedly increases with a sum of volt-ampere (V-A) products of switches [22]. In this paper, ripple components are not taken into consideration for the sake of simplicity.

The theoretical voltage and current stresses of MOSFETs in the proposed converter are summarized in Table 1. All duty cycles d_1 – d_3 and average inductor currents I_{L1} – I_{L3} are assumed equal to d and I_L , respectively. Voltage stresses can be determined from the operation modes shown in Figure 5 or values designated in Figure 4 with (1)–(3). The current stresses of Q_{L2} and Q_{L3} are double those of others as can be seen in Figure 5—two out of three inductor currents flow through Q_{L2} and Q_{L3} as shown in Figure 5b,c.

Table 1. Voltage and current stresses of metal-oxide-semiconductor field-effect transistors (MOSFETs) in the proposed interleaved converter.

Component	Voltage	Current
Q_{L1}	$V_{bat}/(1-d)$	I_L
Q_{H1}	$2V_{bat}/(1-d)$	I_L
Q_{L2}	$V_{bat}/(1-d)$	$2I_L$
Q_{H2}	$2V_{bat}/(1-d)$	I_L
Q_{L3}	$V_{bat}/(1-d)$	$2I_L$
Q_{H3}	$V_{bat}/(1-d)$	I_L

TDPRs of the proposed interleaved converter, conventional single-phase converter (Figure 2a), and conventional interleaved three-phase converter (Figure 2c) are compared in Figure 7. At a given conversion ratio higher than 9.0, the proposed converter achieves the lowest TDPR. At the voltage conversion ratio of 12.5, for example, the TDPR values of the conventional and proposed interleaved converters are 25.0 and 11.1, respectively, corresponding to 56% reduction. The lower TDPR tendency is attributable to the reduced voltage stresses, due to C_1 and C_2 . Switches in the conventional converters, on the other hand, must endure the full output voltage or the bus voltage V_{bus} , resulting in a higher TDPR trend.

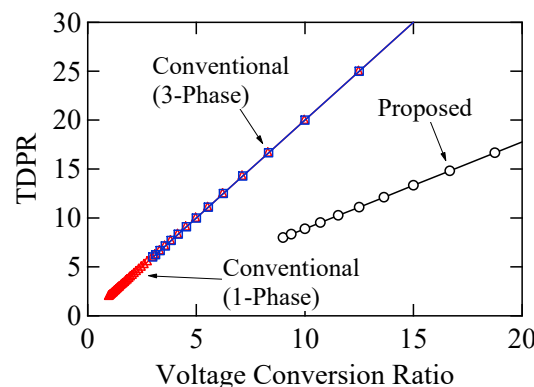


Figure 7. Total device power rating (TDPR) as a function of voltage step-up conversion ratio.

4.2. Normalized Charged-Discharged Energies in Passive Components

Inductors and capacitors occupy a significant portion of the total volume of converters. Volumes of passive components of inductors and capacitors are generally proportional to their stored energies. In this section, the proposed and conventional converters are quantitatively compared on the basis of total charged-discharged energies in inductors and capacitors normalized by input energy in a single switching cycle $E_{in} = V_{bat}I_{bat}T_s$.

To fairly compare various topologies, volume metrics S is introduced and is defined as

$$S = \frac{1}{E_{in}} \left(\sum_{Inductors} \frac{\beta E_L}{\alpha_L} + \sum_{Capacitors} \frac{E_C}{\alpha_C} \right) \quad (10)$$

where α_L and α_C are the ripple factors of inductor current and capacitor voltage, respectively, and β is the energy density ratio of capacitors to inductors. E_L and E_C are the charged-discharged energies of inductors and capacitors. Mathematical expressions of E_L and E_C for passive components in the proposed converter are listed in Table 2.

In general, α_L is chosen in the range of 0.2–0.4 for ordinary PWM converters. To tightly regulate input and output voltages, input and output smoothing capacitors (i.e., C_{bat} and C_{bus}) should be selected so that their ripple voltage α_C is in the range of 0.03–0.05. Meanwhile, ripple factors of flying capacitors (C_1 and C_2) can be around 0.1 [23]. Energy densities of discrete capacitors are in the range of more than three orders of magnitude greater than those of similarly scaled inductors [23–25]. In the following, the comparison on S was performed with $\alpha_L = 0.3$, $\alpha_C = 0.03$ and 0.1 for smoothing and flying capacitors, respectively, and $\beta = 100$.

Table 2. Charged-discharged energies in inductors and capacitors in the proposed converter.

Component	Charged-Discharged Energy
L_1 – L_3	$V_{bat}I_LdT_s$
C_1	$V_{bat}I_LT_s$
C_2	$2V_{bat}I_LT_s$
C_{bus}	$3V_{bat}I_Ld(1-d)T_s$
C_{bat}	$\alpha I_L V_{bat}(3d-2)T_s/24d$

Calculated tendencies of S are shown in Figure 8. Inductors took the largest portion in all the converters. The portions taken by smoothing capacitors (C_{bat} and C_{bus}) were substantial in the conventional single-phase converter and proposed interleaved converter, because C_{bus} must be large to absorb large pulsating current at the bus side. Meanwhile, C_{bus} in the conventional three-phase converter can be designed smaller, owing to the interleaving operation at the bus side. Although the proposed converter also operates in the interleaving manner at the battery side, the operation at the bus side is not in an interleaving manner, as can be seen in Figure 5.

Despite the increased portion of capacitors, the proposed converter exhibits the lowest S tendency. At the voltage conversion ratio of 12.5, the S values of the conventional 1-phase, 3-phase, and proposed converters were 339, 310, and 289, respectively, implying the volume of passive components would be reduced by greater than 7%. The lowest S tendency was chiefly because charged-discharged energies of inductors are significantly reduced by C_1 and C_2 . As shown in Figure 5, inductors together with capacitors contribute to power transfer, mitigating the energy storage burden of inductors. Since capacitors are far more compact than inductors (as characterized by β), reducing the burden of inductors by using capacitors translates into a reduction in total volume.

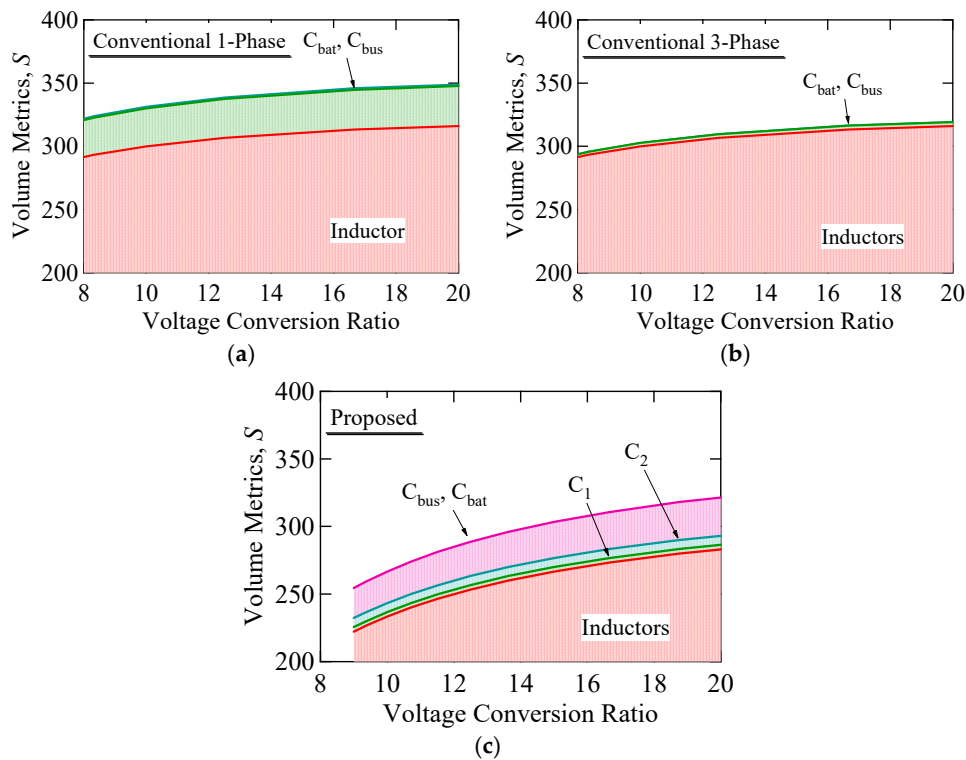


Figure 8. Normalized charged-discharged energies as a function of step-up voltage conversion ratio. (a) Conventional single-phase converter; (b) conventional three-phase interleaved converter; (c) proposed converter.

5. Experimental Results

A 100-W prototype of the proposed converter was built, as shown in Figure 9. Component values are listed in Table 3. The prototype operated with $V_{bat} = 4.0$ V and $V_{bus} = 50$ V at the switching frequency of 100 kHz. Gate drivers were powered by an external power supply (neither by V_{bus} nor V_{bat}). Gating signals were generated using a TMS320F28335 control card (Texas Instruments, Dallas, TX, USA).

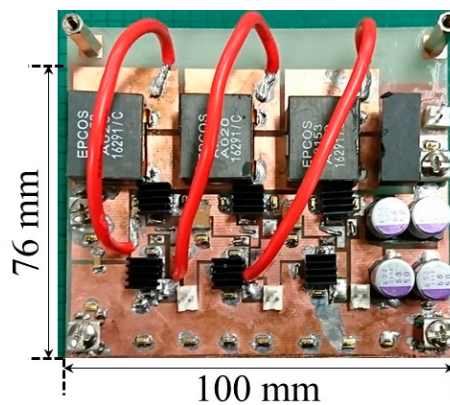


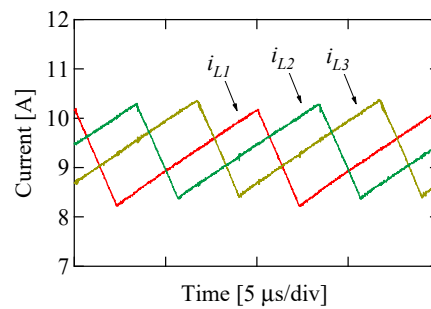
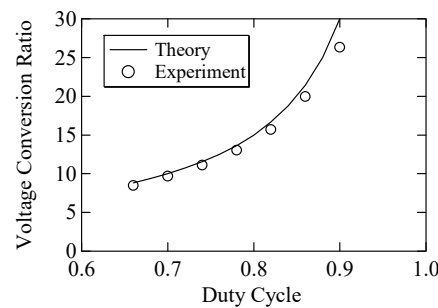
Figure 9. A photograph of 100-W prototype.

Measured key operation waveforms at full load in the step-up mode are shown in Figure 10. $v_{QL1}-v_{QL3}$ and $i_{L1}-i_{L3}$ were 120° out of phase, and inductor average currents were identical, verifying the passive automatic current balancing capability.

The measured step-up voltage conversion ratio is shown and compared with the theoretical one in Figure 11. The experimental result matched satisfactorily with the theoretical one. The error was considered due to the power conversion loss in the prototype.

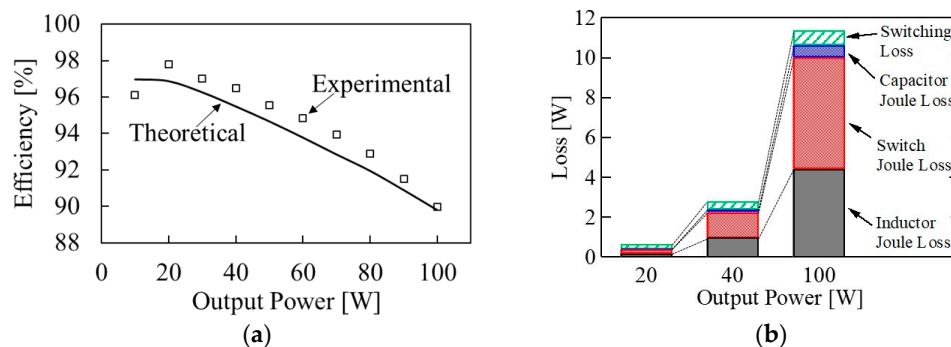
Table 3. Components used for prototype.

Component	Value
L_1 – L_3	15 μ H, 16.9 m Ω
C_{bat}	Ceramic Capacitor, 220 μ F, 3.1 m Ω
C_{bus}	Al Electrolytic Capacitor, 272 μ F, 5.0 m Ω
C_1, C_2	Ceramic Capacitor, 22 μ F, 6.0 m Ω
Q_{L1} – Q_{L3}, Q_{H1} – Q_{H3}	N-Channel MOSFET, TPCA8050-H, $R_{on} = 14.2$ m Ω

**Figure 10.** Measured key operation waveforms at full load.**Figure 11.** Experimental and theoretical step-up voltage conversion ratios.

The measured power conversion efficiency in the step-up mode is shown in Figure 12a. The efficiency steadily decreased as the output power increased. The efficiency at the full load of 100 W was as high as 90%.

The calculated loss breakdown is shown in Figure 12b. Joule losses of inductors and switches were dominant in medium to heavy load regions. Meanwhile, switching losses were insignificant in all power range, probably due to reduced voltage stresses of switches, as discussed in Section 4.1. The result suggests that the use of inductors and switches with low resistive components is a key to improving power conversion efficiency.

**Figure 12.** (a) Measured power conversion efficiencies; (b) Calculated loss breakdown.

6. Conclusions

A bidirectional interleaved PWM converter with high voltage conversion ratio and passive automatic current balancing capability has been proposed for single-cell battery power systems in small scientific satellites. The proposed converter operates in an interleaving manner, and the added capacitors realize not only voltage conversion ratios three times greater than those of conventional bidirectional converters, but also automatic current balancing. A quantitative comparison of TDPR and volume metrics S was performed for the proposed and conventional converters. The comparative results revealed that TDPR and S of the proposed converter could be reduced by 56% and >7%, respectively, in comparison with conventional converters, suggesting higher power conversion efficiencies and more compact circuit design. The 100-W prototype with $V_{bat} = 4.0$ V and $V_{bus} = 50$ V was built for experimental verification. The average inductor currents were automatically balanced due to the added capacitors, and the measured power conversion efficiency was higher than 90% in the entire range, demonstrating the fundamental characteristics of the proposed converter.

Author Contributions: The research study was carried out successfully with contribution from all authors. The main research idea, simulation works, manuscript preparation and revision were contributed by M.U.; M.I. contributed to the analysis, prototyping and experimental verification. Y.S. and H.N. contributed to the operation analysis and quantitative comparison.

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Nomenclature

α_C, α_L	Ripple factor of capacitor voltage and inductor current
β	Energy density ratio of capacitors to inductors
d_1, d_2, d_3	Duty cycle of Q_{L1}, Q_{L2}, Q_{L3}
E_C, E_L	Charged-discharged energy of capacitors and inductors
I_{bus} (A)	Average bus current
I_L (A)	Balanced average inductor current
i_{L1}, i_{L2}, i_{L3} (A)	Instantaneous inductor current of L_1, L_2, L_3
I_{L1}, I_{L2}, I_{L3} (A)	Average inductor current of L_1, L_2, L_3
I_{max} (A)	Theoretical maximum current stress of MOSFETs
q_1, q_2, q_3 (C)	Amount of charge released by i_{L1}, i_{L2}, i_{L3}
S	Size metrics
T_s [s]	Switching period
TDPR	Total device power rating
V_{C1}, V_{C2} (V)	Voltage of C_1, C_2
V_{bat} (V)	Battery voltage
V_{Cbus} (V)	Bus voltage
V_{max} (V)	Theoretical maximum voltage stress of MOSFETs

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