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# A New Bridgeless High Step-up Voltage Gain PFC Converter with Reduced Conduction Losses and Low Voltage Stress

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**Abstract:** Bridgeless power factor correction (PFC) converters have a reduced number of semiconductors in the current flowing path, contributing to low conduction losses. In this paper, a new bridgeless high step-up voltage gain PFC converter is proposed, analyzed and validated for high voltage applications. Compared to its conventional counterpart, the input rectifier bridge in the proposed bridgeless PFC converter is completely eliminated. As a result, its conduction losses are reduced. Also, the current flowing through the power switches in the proposed bridgeless PFC converter is only half of the current flowing through the rectifier diodes in its conventional counterpart, therefore, the conduction losses can be further improved. Moreover, in the proposed bridgeless PFC converter, not only the voltage stress of power switches is lower than the output voltage, but the voltage stress of the output diodes is lower than the conventional counterpart. In addition, this proposed bridgeless PFC converter features a simple circuit structure and high PFC performance. Finally, the proposed bridgeless PFC converter is analyzed and designed in the discontinuous conduction mode (DCM). The simulation results are presented to verify the effectiveness of the proposed bridgeless PFC converter.

**Keywords:** bridgeless converter; discontinuous conduction mode (DCM); high step-up voltage gain; power factor correction (PFC)

## 1. Introduction

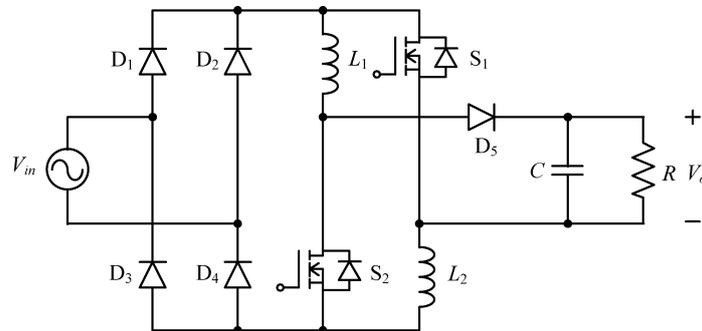
In the past decades, AC-DC converters have been widely used in numerous power electronic equipment supplied by the power grid in order to obtain the DC voltage. For the passive AC-DC rectifier, the input current harmonics are large, which is very harmful for the power grid and other power electronic equipment. In order to alleviate the input current harmonics and satisfy the rigorous input current harmonic standards, for instance, the IEC 61000-3-2 criterion, the active power factor correction (PFC) converter has become a popular and effective method to shape the input current waveform and achieve the near unity power factor (PF) in the power supplies. For single-phase power supplies, the boost topology is the most popular option as the PFC pre-regulator, by reason of its simple circuit structure and high PFC performance [1–3]. Unfortunately, the boost topology cannot achieve a very high voltage gain in practical applications, because the extremely high duty cycle is unpractical. Therefore, in some high voltage applications, for example, X-ray medical/industry equipment, HVDC system insulator testing, electrostatic precipitators and high voltage battery charger, the boost PFC converter is a poor candidate, especially for the universal line [4,5].

For outputting high voltage, many conventional high step-up voltage gain PFC converters have been studied in the past decade [6–16]. Based on the Cockcroft–Walton (CW) structure, some high step-up voltage gain PFC converters were proposed in [6–10]. In [6], a three-stage CW PFC converter was proposed. This converter can achieve a high output voltage and a high PFC performance. In [7], a transformerless hybrid boost and CW PFC converter was presented. By adding the CW voltage multiplier (VM) stages, high output voltage and high power factor are obtained. A single-phase single-stage high step-up matrix PFC converter using CW-VM was proposed in [8]. By combining a four bidirectional-switch matrix converter and the CW-VM, a high step-up voltage gain is achieved. Based on [6], a more comprehensive analysis and validation were presented in [9]. Based on [9], an improved high step-up voltage gain PFC converter with soft-switching characteristic was introduced in [10]. Besides the CW structure, some efforts focused on the switched-capacitor PFC topology to produce the high output voltage [11–13]. In [11], a family of high-voltage gain hybrid switched-capacitor PFC converters were proposed and validated, which can achieve a high output voltage and good PFC performance. A high voltage gain PFC converter based on a hybrid boost DC-DC converter was presented in [12]. By integrating boost topology and the switched-capacitor voltage doubler, a high output voltage and nearly unity PF are produced. In [13], a hybrid single ended primary inductor converter (SEPIC) PFC converter using switched-capacitor voltage doubler was proposed, which also owns a high voltage gain and a good PFC performance. Other new PFC converters can also achieve a high voltage gain [14–16]. In [14], a single-stage boost PFC converter with zero current switching (ZCS) characteristic was proposed and studied, which has a high voltage gain. In [15], a modified SEPIC PFC converter with a high voltage gain was proposed. A family of ZCS isolated high voltage gain PFC converters were proposed in [16]. Also, many high step-up voltage gain DC-DC converters have been studied in [17–24]. These DC-DC topologies can also be applied as the PFC converters for the high voltage applications. However, all the PFC converters, as mentioned above [6–24], are the conventional PFC type. The rectifier bridge is necessary for them, and their topology structures are more complex.

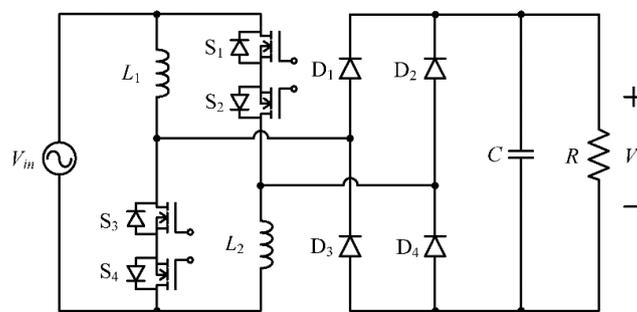
Compared to the conventional PFC converters, the bridgeless PFC converters possess the merits of low conduction losses and higher efficiency. That is because the input rectifier diodes of the bridgeless PFC converters are reduced, leading to a less number of semiconductors in the current-flowing path [2]. In order to improve efficiency, some bridgeless PFC converters with high output voltage are proposed in [25–27]. In [25], a bridgeless Cuk PFC converter was proposed for high voltage battery charger. In [26], a bridgeless modified SEPIC PFC converter was proposed with extended voltage gain. Two bridgeless hybrid boost PFC converters using the switched-capacitor structure were presented in [27]. All these bridgeless PFC converters can be applied for the high voltage applications, and their efficiency are improved compared to their conventional counterparts.

Based on the conventional high step-up voltage gain PFC converter shown in Figure 1, which was first proposed in [18] as the DC-DC converter, a new bridgeless high step-up voltage gain PFC converter with improved efficiency shown in Figure 2 is proposed for high voltage applications. By reducing the number of semiconductors in the current-flowing path and reducing the current stress of semiconductors, the proposed bridgeless PFC converter can achieve a reduced conduction losses and a higher efficiency compared to its conventional counterpart. Besides, the proposed bridgeless PFC converter owns a lower voltage stress of output diodes than the conventional one. The high PF and low total harmonic distortion (THD) are also obtained in the proposed bridgeless PFC converter. In addition, the proposed bridgeless PFC converter features a very simple circuit structure, contributing to cost and power density. The discontinuous conduction mode (DCM) is utilized with the merits of zero current turned on in the power switches, zero current turned off in the diodes, nature current-sharpening ability and a simple control method. As a result, the proposed bridgeless PFC converter is more suitable for the high voltage applications than its conventional counterpart.

The operation principle of the proposed bridgeless PFC converter is discussed in Section 2. A detailed theoretical analysis and design guideline is presented in Section 3. The validation by the simulated results is shown in Section 4, followed by the conclusions in Section 5.



**Figure 1.** The conventional high step-up voltage gain PFC converter.



**Figure 2.** The proposed bridgeless high step-up voltage gain PFC converter.

## 2. Operation Principle

This proposed bridgeless high step-up voltage gain PFC converter uses two bidirectional switches in series with two same level inductors. Each bidirectional switch is constructed by two anti-series power switches. It should be noted that the two power switches in one bidirectional switch have the common source terminal, which can simplify the drive circuit. Simultaneously, an output bridge including  $D_1, D_2, D_3$  and  $D_4$  which are fast-recovery diodes is used to obtain a high DC output voltage in the proposed bridgeless PFC converter, while only  $D_5$  is the fast-recovery diode in its conventional counterpart. The proposed bridgeless PFC converter is designed to operate in DCM. Thereby, it has three operation modes during one switching period. The detailed operation modes of one switching period in the positive line cycle are presented in Figure 3. Since the proposed bridgeless PFC converter is symmetrical, the operation modes in negative line cycle are similar to the modes in positive line cycle. Its key time-domain waveforms are exhibited in Figure 4.

Mode I shown in Figure 3a: when the power switches  $S_1$  and  $S_3$  are turned on, the input sinusoidal source  $v_{in}$  charges the two inductors  $L_1$  and  $L_2$ , simultaneously, through the power switches  $S_2$  and  $S_4$ . The output bulk capacitor maintains the output voltage  $v_o$ . In each branch of the proposed bridgeless PFC converter, only two semiconductors consisting by two power switches are active, while three semiconductors are active in one branch of the conventional counterpart. In this mode, the inductor currents satisfy:

$$v_{in} = L_1 \frac{di_{L1}}{dt} = L_2 \frac{di_{L2}}{dt} \quad (1)$$

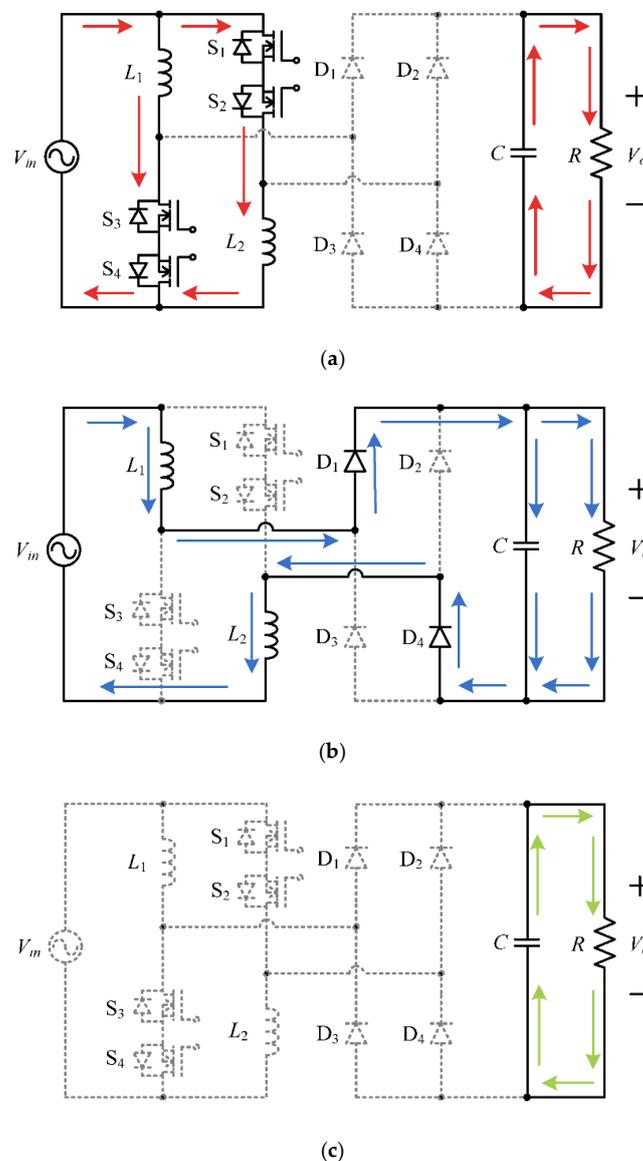
Mode II shown in Figure 3b: when all the power switches are turned off, the input source and the two inductors releases energies to the load. Only two output fast-recovery diodes conduct in this

mode, while three semiconductors including two slow-recovery diodes and one fast-recovery diode conduct in the corresponding conventional counterpart. In this mode, the inductor currents satisfy:

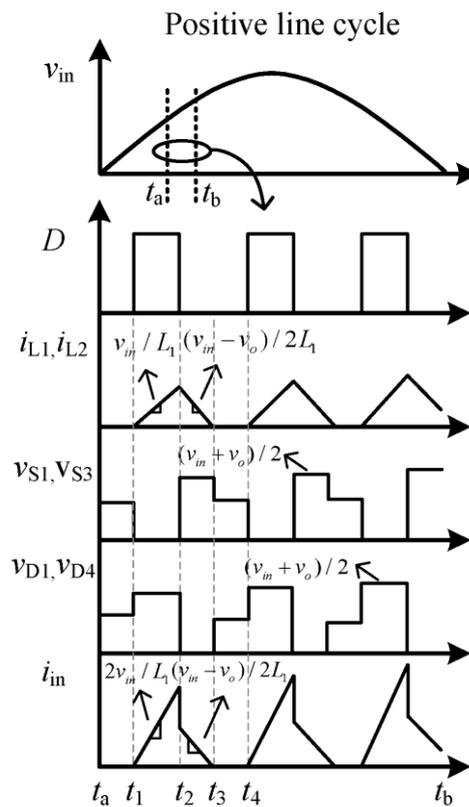
$$\frac{v_{in} - v_o}{2} = L_1 \frac{di_{L1}}{dt} = L_2 \frac{di_{L2}}{dt} \quad (2)$$

Mode III shown in Figure 3c: all the semiconductors are in the off state. The inductor currents are zero. The output bulk capacitor  $C$  maintains the output voltage.

Figure 4 presents the key waveforms of duty cycle  $D$ , inductor current  $i_{L1}$ ,  $i_{L2}$ , input current  $i_{in}$ , and the voltage  $v_{S1}$ ,  $v_{S3}$ ,  $v_{D1}$ ,  $v_{D4}$  across the semiconductors in the positive line cycle. From this figure, the inductor current  $i_{L1}$ ,  $i_{L2}$  are equal to each other. When the power switches are turned on, the inductor current are half of the input current  $i_{in}$ . When the power switches are turned off, the inductor current are same with the input current. The maximum voltage across the power switches and the output diodes are  $(v_{in} + v_o)/2$  in the positive line cycle. It should be noted that the duty cycle  $D$  equals to  $(t_2 - t_1)/T_S$ , where  $T_S$  is the switching period.



**Figure 3.** The operation modes of the proposed bridgeless high step-up voltage gain PFC converter in the positive line cycle: (a) mode I; (b) mode II and (c) mode III.



**Figure 4.** The key time-domain waveforms of the proposed bridgeless high step-up voltage gain PFC converter.

### 3. Theoretical Analysis

The detailed theoretical analysis and designed consideration in DCM are presented in this subsection. First of all, some ideal assumptions are provided to simplify the analysis. Notably, the theoretical analysis is made in one positive line cycle. These assumptions are shown as follows:

- The switching frequency  $f_s$  is much higher than the line frequency. Thus, the input voltage is constant during one switching period.
- The capacitance of the bulk capacitor is large enough. Thereby, the output voltage is ideal constant.
- All the components are ideal without losses.
- The input voltage is ideally sinusoidal.

#### 3.1. The Voltage Conversion Ratio $M$

Applying the voltage-second balance principle to the inductor  $L_1$ , the voltage conversion ratio  $M$  is derived as follows:

$$M = \frac{v_o}{v_m} = \frac{2D + D_x}{D_x} \times \sin \theta \tag{3}$$

where  $v_m$  is the amplitude of the sinusoidal input voltage  $v_{in}$ ,  $\theta$  is the angle of the input voltage  $v_{in}$ , and  $D_x$  is equal to  $(t_3 - t_2)/T_S$ .

Based on (3), the relationship between the duty cycle  $D$  and  $D_x$  can be expressed as:

$$D_x = 2D \times \frac{\sin \theta}{M - \sin \theta} \tag{4}$$

In addition, the peak inductor current  $i_{L1-peak}$  in one switching period is:

$$i_{L1-peak} = \frac{DT_S}{L_1} \times v_m \sin \theta \quad (5)$$

Due to the power balance between input power and output power, we can get:

$$\frac{1}{\pi} \int_0^\pi \frac{1}{2} \times i_{L1-peak} \times (2D + D_x) \times v_{in} d\theta = \frac{v_o^2}{R} \quad (6)$$

Substituting (4) and (5) into (6), the relationship of the voltage conversion ratio  $M$  and duty cycle  $D$  is derived as follows:

$$M = D \times \sqrt{\frac{\beta}{\pi K}} \quad (7)$$

where the dimensionless conduction parameter  $K$  is:

$$K = \frac{2L_1}{RT_S} \quad (8)$$

and the parameter  $\beta$  is

$$\beta = \int_0^\pi \left( \frac{2M}{M - \sin \theta} \right) \times \sin^2 \theta d\theta \quad (9)$$

The relationship of the voltage conversion ratio  $M$  and duty cycle  $D$  is presented in Figure 5. From this figure, one can see that the voltage conversion ratio  $M$  increases with the lower parameter  $K$ . Compared to the conventional boost PFC converter, the voltage conversion ratio  $M$  of the proposed bridgeless PFC converter is much higher. Therefore, the proposed bridgeless PFC converter is more suitable for the high voltage applications.

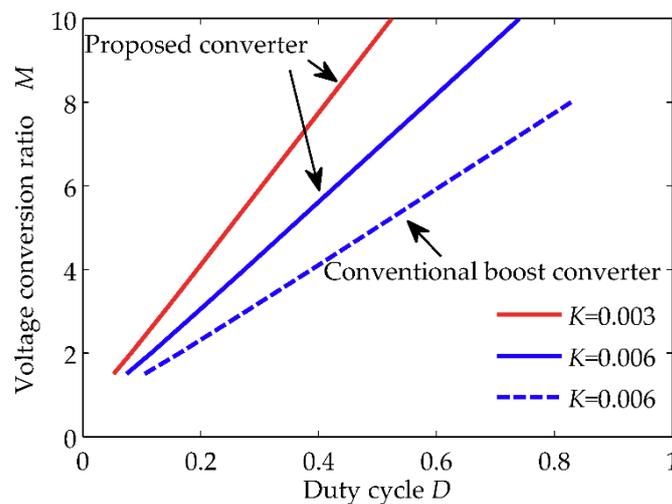


Figure 5. The relationship of the voltage conversion ratio  $M$  and duty cycle  $D$ .

### 3.2. The Operation Condition for DCM

In order to operate in DCM, the operation condition must satisfy as follows:

$$D + D_x < 1 \quad (10)$$

Substituting (3) and (7) into (10), the operation condition for DCM is derived as:

$$K < \frac{\beta}{\pi} \times \frac{1}{M^2} \times \left( \frac{M - \sin \theta}{M + \sin \theta} \right)^2 \quad (11)$$

The proposed bridgeless PFC converter is designed to operate in DCM totally. Therefore, the inductor currents should be discontinuous at the peak point in the line cycle. Thus, the simplified operation condition for DCM is:

$$K < \frac{\beta}{\pi} \times \frac{1}{M^2} \times \left( \frac{M-1}{M+1} \right)^2 \tag{12}$$

Figure 6 draws the operation boundary between the DCM and the continuous conduction mode (CCM). From this figure, the operation boundary is higher at the low voltage conversion ratio. However, for the universal line, the voltage conversion ratio is different under different input voltage. Hence, the key parameter  $K$  must be designed at the lowest input voltage.

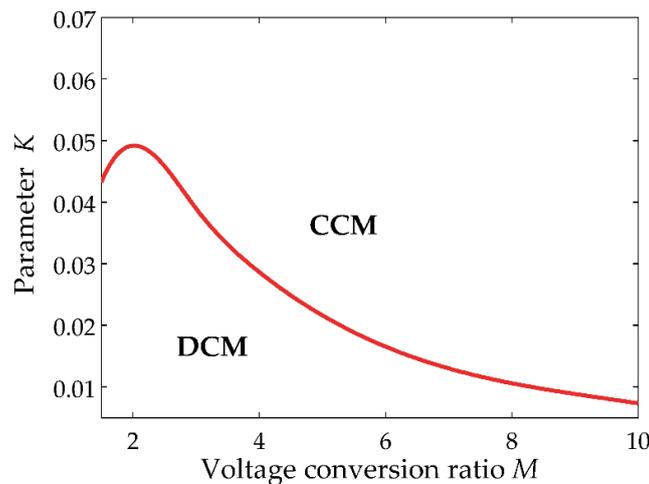


Figure 6. The operation boundary between DCM and CCM.

### 3.3. The Voltage Stress and Current Stress

The voltage stress of semiconductors in the proposed bridgeless PFC converter and in its conventional bridge counterpart are shown in Table 1. From this table, the voltage stress of power switch in the proposed bridgeless PFC converter is same with its conventional bridge converter, and it is lower than the output voltage. The voltage stress of fast-recovery diode in the proposed bridgeless PFC converter is lower than that in the conventional bridge converter. Therefore, the lower rated diode can be used in the proposed bridgeless PFC converter. It is beneficial to improve cost and losses. In addition, no slow-recovery diode is used in the proposed bridgeless PFC converter, while four slow-recovery diodes as the input bridge are used in its conventional bridge counterpart, and their voltage stress is  $v_m$ .

Table 1. The voltage stress of semiconductors.

	Proposed Bridgeless PFC Converter	Conventional Bridge PFC Converter
Power switch	$(v_m + v_o)/2$	$(v_m + v_o)/2$
Fast-recovery diode	$v_o$	$v_m + v_o$
Slow-recovery diode	-	$v_m$

The root-mean-square (RMS) current  $i_{S1-rms}$  of power switch in one switching period is shown as follows:

$$i_{S1-rms} = \frac{v_{in}DT_S}{L_1} \sqrt{\frac{D}{3}} \tag{13}$$

The averaged current  $i_{D1-avg}$  of output diode in one switching period is derived as follows:

$$i_{D1-avg} = \frac{v_{in}DD_xT_S}{2L_1} \quad (14)$$

### 3.4. The Conduction Losses

In this subsection, the conduction losses of semiconductors are calculated. The detail derivations in one positive line cycle are exhibited as follows:

$$P_{S1} = \frac{1}{\pi} \int_0^\pi \left( \frac{v_{in}DT_S}{L_1} \right)^2 \times \frac{D}{3} \times R_{on} d\theta \quad (15)$$

$$P_{D1} = \frac{1}{\pi} \int_0^\pi \frac{v_{in}DD_xT_S}{2L_1} \times V_F d\theta \quad (16)$$

where  $R_{on}$  is the conduction resistance of the power switch and  $V_F$  is the forward voltage of diodes.

Under the operation condition  $v_{in} = 220 \text{ V}_{rms}/50 \text{ Hz}$ ,  $v_o = 800 \text{ V}$ ,  $f_s = 30 \text{ kHz}$  and  $P_o = 500 \text{ W}$ , the conduction losses of semiconductors are calculated. It should be noted that the parameters  $R_{on}$  and  $V_F$  are chosen from the datasheet of the selected components. The conduction losses of semiconductors of the proposed bridgeless PFC converter and its conventional counterpart are presented in Figure 7. From this figure, it can be found that the total conduction losses of semiconductors in the proposed bridgeless PFC converter is much lower than its conventional bridge counterpart. The conduction losses of power switches in the proposed bridgeless PFC converter are higher, while it has no conduction losses of input rectifier diodes.

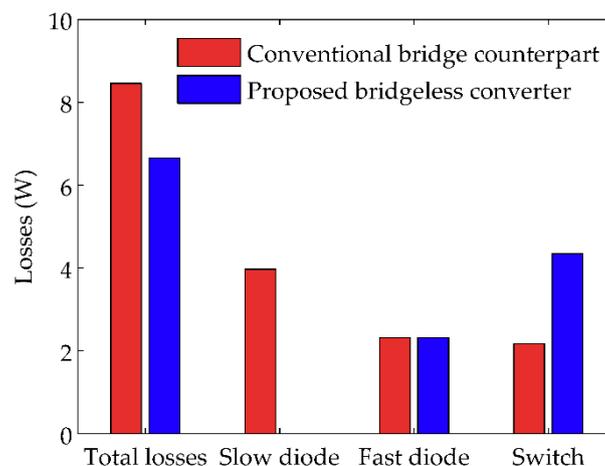
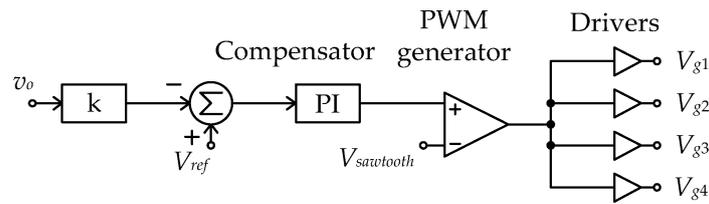


Figure 7. The calculated conduction losses of semiconductors.

### 3.5. The Control Principle

This proposed bridgeless PFC converter is designed in DCM. The DCM possesses the merit of a naturally current-sharpening ability, which contributes to a simple control method. Thereby, the voltage control loop is applied in order to obtain the constant DC output voltage. The control principle is displayed in Figure 8. From this figure, the controller mainly contains one compensator, one PWM generator and four drivers. It should be noted that the four power switches in the proposed bridgeless PFC converter can be driven by one same control signal, which simplifies the controller, significantly. Notably, the signal  $V_{g1}$ ,  $V_{g2}$ ,  $V_{g3}$  and  $V_{g4}$  drive the power switches  $S_1$ ,  $S_2$ ,  $S_3$  and  $S_4$ , respectively.



**Figure 8.** The control diagram of the proposed bridgeless high step-up voltage gain PFC converter.

#### 4. Simulation Results

The effectiveness of the proposed bridgeless PFC converter is validated in the SIMetrix/SIMPLIS (version 8.00, company SIMetrix Technologies Ltd., Thatcham, UK) environment. The simulation program with integrated circuit emphasis (SPICE) models of practical components are employed in this simulation. The key operation parameters of the proposed bridgeless PFC converter is  $v_{in}$  = universal line 95–265 V<sub>rms</sub>,  $v_o$  = 800 V,  $f_s$  = 30 kHz and  $P_o$  = 500 W. The selected components are shown in Table 2. Considering the voltage stress, current stress and safety margin, the SPP17N80C3 (company Infineon, GER) with  $R_{on}$  = 0.29  $\Omega$  and  $V_{DS}$  = 800 V is chosen as the power switches. The MUR490 (company On Semiconductor, Phoenix, AZ, USA) with  $V_F$  = 1.85 V and  $V_D$  = 900 V is chosen as the fast-recovery diodes in the proposed bridgeless PFC converter. Since the voltage stress of the fast-recovery diode in the conventional bridge counterpart is up to around 1200 V, which is much larger than the voltage stress 800 V of the fast-recovery diode in the proposed bridgeless PFC converter, we have to choose two series MUR490 as the fast-recovery diode in the conventional bridge counterpart. In the conventional bridge converter, 8EWS08 (company International Rectifier, El Segundo, CA, USA) with  $V_F$  = 1 V is used as the input rectifier diodes.

**Table 2.** The selected components.

	Proposed Bridgeless PFC Converter	Conventional Bridge PFC Converter
Power switches	SPP17N80C3	SPP17N80C3
Fast-recovery diodes	MUR490	MUR490
Slow-recovery diodes	—	8EWS08
Output capacitor	200 $\mu$ F	200 $\mu$ F
Inductors	200 $\mu$ H	200 $\mu$ H

The input current after the input LC filter at the typical input line is displayed in Figure 9. From this figure, the input current is shaped to be almost sinusoidal at the typical low line 110 V<sub>rms</sub> and the typical high line 220 V<sub>rms</sub>. Thereby, it is validated that the proposed bridgeless PFC converter owns a good current-shaping ability. Figure 10 presents the key time-domain waveforms of the proposed bridgeless PFC converter. It can be figure out that the simulated waveforms are in agreement with the theoretical analysis. The key waveforms also validate that the proposed bridgeless PFC converter operates in DCM.

Figure 11 presents the simulated PF and THD under the universal line. From this figure, one can see that nearly unity PF is achieved and the THD is low under the universal line. The high PF and low THD validate that the proposed bridgeless PFC converter owns a good PFC performance.

The simulated efficiency of the proposed bridgeless PFC converter and its conventional bridge counterpart under the universal line is shown in Figure 12. From this figure, it is clear that the efficiency of the proposed bridgeless PFC converter is higher than its conventional bridge counterpart, due to the reduced semiconductors and the reduced current. Also, the efficiency of other state of the art high step-up voltage gain converter in [12] is simulated. Under the same operation parameters and components, the efficiency of the converter in [12] is 97.42% at the typical line  $V_{in}$  = 220 V<sub>rms</sub>, while the efficiency of the proposed bridgeless PFC converter can reach up to 98.78% at the typical line  $V_{in}$  = 220 V<sub>rms</sub>. Therefore, the proposed bridgeless PFC converter is more suitable for the practical application.

Figure 13 displays the simulated input current harmonics compared with the IEC 61000-3-2 class D limits. From this figure, the input current harmonics of the proposed bridgeless PFC converter are much lower than the IEC 61000-3-2 class D limits under both the typical low line and high line. Namely, the proposed bridgeless PFC converter can easily satisfy the international harmonic standards, which is very beneficial to practical application.

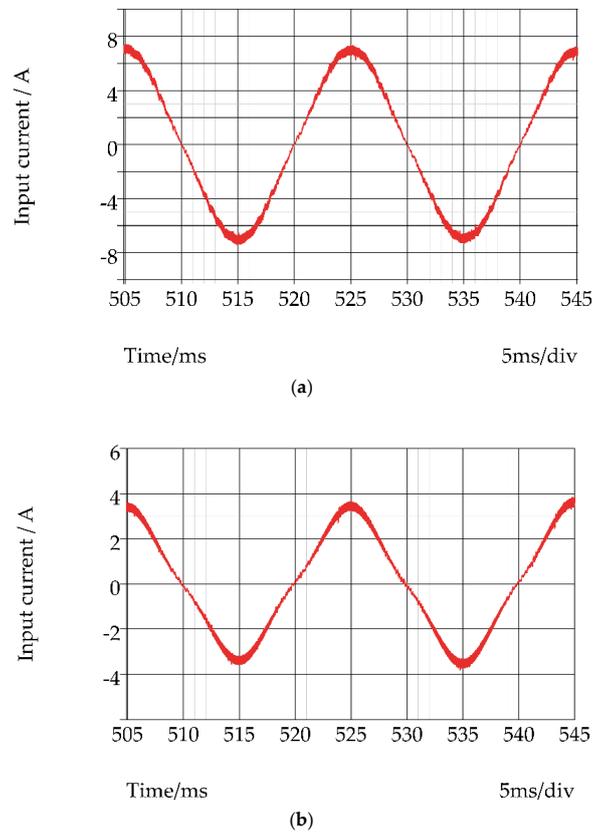


Figure 9. The input current waveforms after the input LC filter: (a)  $v_{in} = 110 V_{rms}$ ; (b)  $v_{in} = 220 V_{rms}$ .

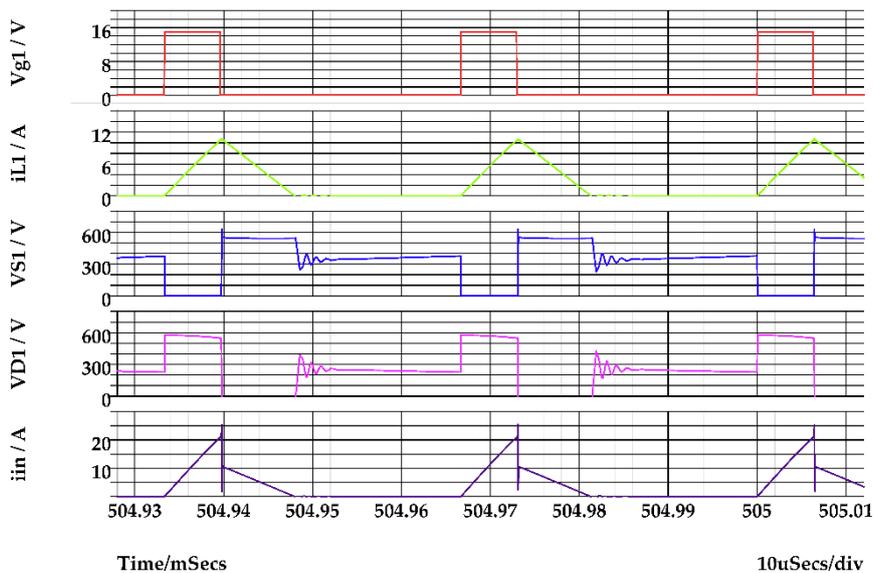


Figure 10. The key time-domain waveforms at  $v_{in} = 220 V_{rms}$ .

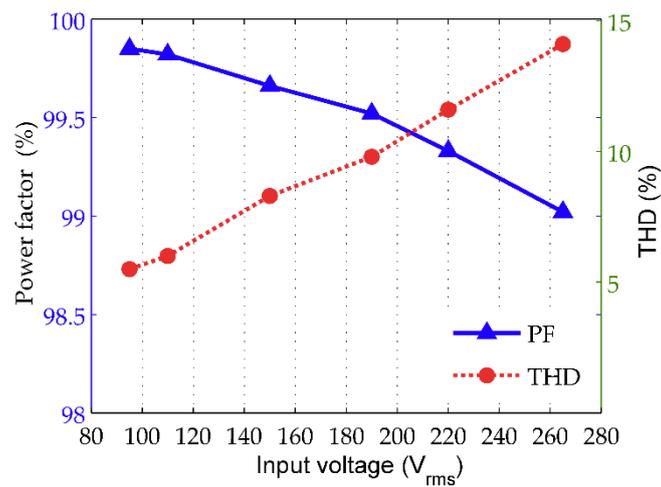


Figure 11. The simulated PF and THD of the proposed bridgeless high step-up gain PFC converter.

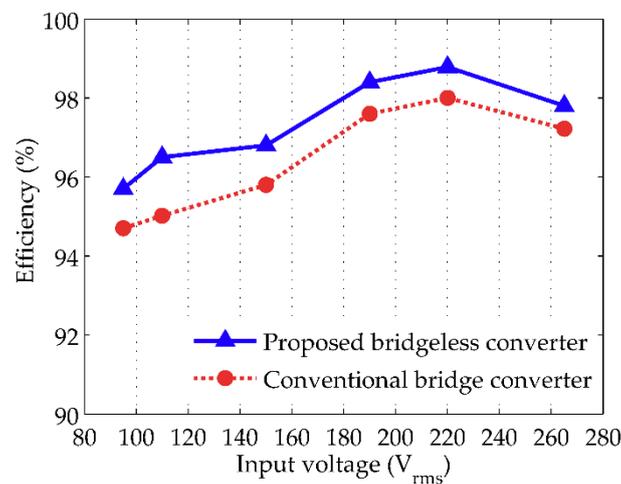
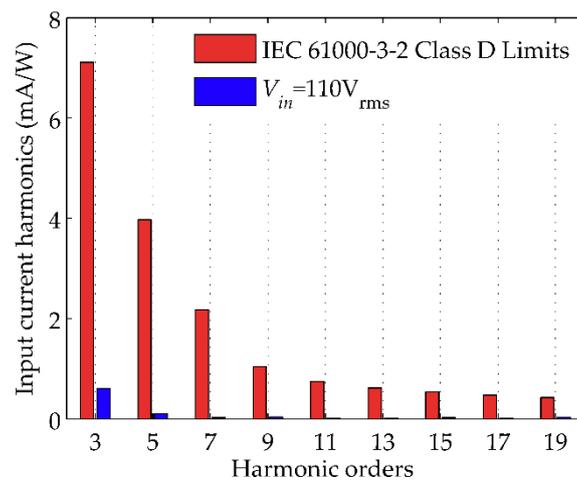
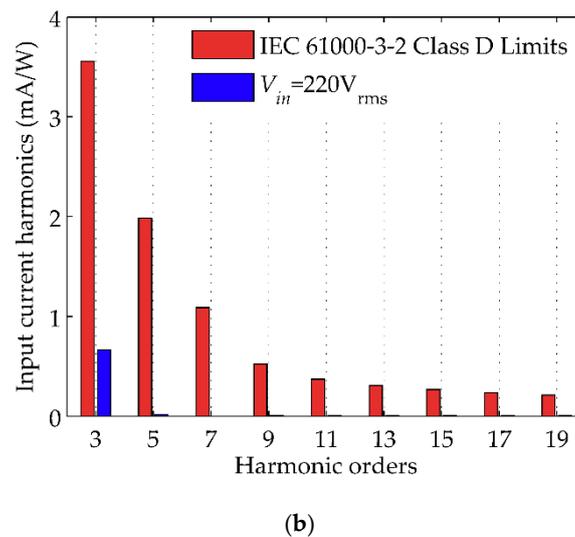


Figure 12. The simulated efficiency of the proposed bridgeless high step-up voltage gain PFC converter and its conventional bridge counterpart.



(a)

Figure 13. Cont.



**Figure 13.** The simulated input current harmonics of the proposed bridgeless high step-up voltage gain PFC converter compared with the IEC 61000-3-2 class D limits: (a)  $v_{in} = 110 V_{rms}$ ; (b)  $v_{in} = 220 V_{rms}$ .

## 5. Conclusions

A new bridgeless high step-up voltage gain PFC converter with low conduction losses and low voltage stresses for high voltage applications is proposed, analyzed and verified in this paper. The theoretical analysis and design consideration in DCM are presented. The simulated results validate that the proposed bridgeless PFC converter has a higher efficiency than its conventional bridge counterpart. Moreover, the proposed bridgeless PFC converter can achieve a very high PF and low THD, and it can easily satisfy the IEC 61000-3-2 class D limits, thereby, the proposed bridgeless PFC converter is a competitive option for the high voltage applications.

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**Conflicts of Interest:** The authors declare no conflict of interest.

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