



Article A Bilateral Zero-Voltage Switching Bidirectional DC-DC Converter with Low Switching Noise

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Abstract: This paper proposes a novel bilateral zero-voltage switching (ZVS) bidirectional converter with synchronous rectification. By controlling the direction and timing of excessive current injection, the main power switches can achieve bilateral ZVS under various loads and output voltages. Compared with the common soft-switching power converter with only zero-voltage turn-on, the proposed bilateral ZVS bidirectional converter can achieve both zero-voltage switching on and off in every switching cycle. This feature can alleviate the output switching noise due to the controlled rising and falling slope of the switch voltage. Furthermore, the voltage slopes almost remain unchanged over a wide range of output voltages and load levels. The most important feature of bilateral ZVS is to reduce the output switching noise. Experimental results based on a 1 kW prototype are presented to demonstrate the performance of the proposed converter. From experimental results on the proposed scheme, the switching noise reduction is about 75%.

Keywords: switching noise; zero-voltage switching; bidirectional converter

1. Introduction

With the increasingly stringent requirements on the output quality of instrument power supplies, the switching noise imposed on the output voltage should be minimized. Conventional linear regulators have excellent performance in terms of the noise concern, but cannot handle high power due to efficiency problems and the inability to process bidirectional power flow. Switching power converters, on the contrary, are capable of improving efficiency at high power outputs; the switching actions induce switching noise on the output and degrade the power quality of the load. The high-frequency switching noise usually ranges over a few hundred kHz to several MHz. The voltage perturbation is illustrated as in Figure 1.



Figure 1. Output voltage ripple ($V_{p-p,ripple}$) and switching noise ($V_{p-p,noise}$).

There are two factors influencing the switching noise in a switching power supply: one is the non-ideal characteristic of the output filter, and the other is the high-frequency component spectra of the voltage waveform injecting into the filter. Firstly, dealing with the non-ideal characteristics of the filter, take a buck converter as an example. The output inductor and capacitor are not only used

to store energy, but also behave as a filter to reduce the output ripple. An ideal LC low-pass filter, as shown in Figure 2a, can completely filter out the high-frequency component well above the designed cut-off frequency. However, practical inductors and capacitors contain parasitic elements. The parasitic elements in an inductor contains the capacitance between the windings as well as between the winding conductor and the core, denoted as lumped capacitance, C_p . In addition, there is winding equivalent resistance, R_s , as shown in Figure 2b. As for the capacitor counterpart, it contains the equivalent series inductance, L_c , and equivalent series resistance, R_c . These parasitic elements alter the transfer function of the filter and deteriorate the capability to filter out high frequency signals. Figure 3 shows the bode plots of ideal, semi-ideal and non-ideal filters. The component parameters used in the figure are as follows: $L_o = 42 \ \mu H$, $R_s = 0 \ \Omega$, $C_p = 10 \ pF$, $C_o = 1.36 \ mF$, $R_c = 1 \ m\Omega$, $L_c = 6 \ \mu H$, $R_o = 10 \ \Omega$. Where C_o is the filter capacitor, L_o is the filter only considers the capacitor's equivalent series resistance (*ESR*), the extra zero brings about +20 dB/dec; on the other hand, the non-ideal filter considers all the parasitic components; even a +40 dB/dec slope is present at extremely high-frequency regions. In other words, the high-frequency components of the input signal will be detected at the output terminals.



Figure 2. LC low-pass filter (a) ideal model; (b) non-ideal model.



Figure 3. Bode plots of ideal and non-ideal filters.

Clearly, it is very difficult to reduce the parasitic components on the filter; practically, it is impossible to eradicate them. Elsewise, in order to counteract the high-frequency current generated by the parasitic capacitance on the inductor, the literature [1] proposes an external circuit. The inductor is connected in parallel to a transformer or a secondary side winding, and a compensating capacitor is connected in series to the secondary side. By adjusting the transformer turns ratio to produce an appropriate compensating current, the transient current evoked from the parasitic capacitance is neutralized. Although the method claims limited extra circuitry components or volume/weight required to depress the switching noise, its performance will be seriously impaired due to the inevitable leakage inductance accompanying the additionally coupled winding, which is not accounted for in the theory. Another paper [2] proposed a different improved compensation circuit to reduce the effect of leakage inductance. In this external circuit, the compensation capacitor is connected to both sides of

the extra coupled inductor, and the effect of leakage inductance will be greatly reduced. For both of the above methods, an accurate inductor parasitic capacitance value is indispensable. However, this itself is a difficult task. Many researchers endeavor to construct inductor parasitic capacitance models and several parameter assignments have been proposed [1–3], even though the thickness, pitch or tightness deviation of the winding under realistic industrial mass production will affect the parasitic capacitance. Neither way is appropriate to reliably compensate for all the products under mass production.

On the other hand, elimination of parasitic inductance on the output capacitor is another remedy for reducing the high-frequency voltage noise. Reference [3] proposes a technique for eliminating the capacitor's equivalent series inductance (*ESL*) and *ESR*.

As shown in Figure 4, the two non-ideal capacitors are connected in diagonal form. From circuit theorem, if the compensation impedance Z_1 is equal to that of *ESL* and *ESR*, there is an equivalent pure capacitance located in the middle point. For high-frequency signals, the inductor exhibits high impedance while the capacitor exhibits low impedance. Therefore, the high-frequency noise can no longer pass through to the output. Although the compensation impedance Z_1 in this method is of limited value and can be implemented by using printed circuit board (PCB) trace, the internal parasitic elements inside capacitors are divergent due to several reasons. Therefore, there are still many difficulties to solve before mass production is possible. Nevertheless, the tolerance allowed for this method is wider than the compensation of inductor parasitic capacitance methods.



Figure 4. The equivalent series inductance (*ESL*) and equivalent series resistance (*ESR*) elimination concept for capacitors [3]. Z_1 = compensation impedance. Z_2 = non-ideal capacitor equivalent circuit.

Since the elimination of parasitic components in a filter circuit is very difficult, the remnant prescription is to reduce the voltage transient across the inductor. The commonly developed ZVS techniques indeed reduce the voltage transient since the inductor voltage transits over a longer commutation time as the switch voltage falls to zero. This simple idea just launches a much wider possibility for switching noise alleviation.

A synchronous rectified step-down converter operated in the triangular-current mode (TCM) [4–6] is a common way to achieve ZVS without introduction of auxiliary resonant components. For TCM operation, the inductor current is usually designed to operate in boundary conduction mode (BCM) at full load; therefore, TCM can be assured under the entire load range. However, this means that the inductance should be small so that the peak inductor current doubles the output current at full load. This seriously impairs the converter efficiency, especially at light load.

There are many proposed ZVT converters with auxiliary switches or resonant circuitry to achieve ZVS benefits [7–11]. However, the ZVS feature cannot be maintained within the overall load and voltage range. In recent years, the literature [12–15] lists many novel bidirectional converters applying various methods to achieve soft switching. However, most of them suffer from the range limitation of ZVS, i.e., ZVS is only achievable within a small range of load level, or even output voltage in some applications. A method proposed in [16] is capable of retaining ZVS switching at any load and wide output voltage range while reducing the switching losses of the auxiliary switch by a coupled inductor. However, from the detailed discussion in the next section, it is clear that the output switching noise could be further reduced if soft switching of switching-off is considered. Unfortunately, the aforementioned papers only focus on ZVS turn-on; i.e., those methods only alleviate the rising slope

of the filter input voltage, but without solving the sharp noise of the falling edge. In this paper, a new circuit architecture is proposed to achieve bilateral ZVS over a wide load range and wide output voltage. This architecture can reduce the output switching noise by controlling the resonant capacitor to simultaneously adjust the rise and fall slope of the voltage across the main switch. The voltage change rate of these is the same and does not change with the output voltage and the output current. It is not necessary to detect the voltage signal to determine the opening timing of the main switch, which is beneficial to the application of high-frequency switching. This architecture is especially suitable for instrument power which characterizes the low switching noise trait over wide load/voltage range.

The remaining arrangement of this paper is as follows: Section 2 discusses the Fourier analysis of the filter's input voltage. Section 3 shows the structure and operation principle of the proposed circuit. Detailed analyses of the circuit and the requirement for ZVS are described in Section 4. Section 5 is about the design consideration and equations of this architecture. Section 6 presents the simulation and measured results to verify the correctness and feasibility. Finally, the conclusion follows.

2. Fourier Analysis on Filter Input Voltage Waveforms

As for the discussion on the influence of frequency spectra of the input voltage waveform, take a buck converter as an example again. Ideally, the voltage at the LC filter's input port is a rectangular waveform. From the definition of the Fourier series, the Fourier series expansion of a rectangular waveform, $f_{rect}(t)$ is:

$$f_{rect}(t) = V_{in}D + \sum_{1}^{\infty} C_{n,rect} \cos\left(\frac{2\pi nt}{T_s}\right)$$
(1)

where

$$C_{n,rect} = \frac{2V_{in}\sin(n\pi D)}{n\pi}$$
(2)

Practically, there is always a small rise/fall time in the waveform. To simplify the analysis, let us assume an identical rise and fall time, t_r/t_f . Then we have a trapezoidal waveform. By dissecting the waveform into a rectangle and two triangles, the Fourier series expansion of a trapezoidal waveform, $f_{trap}(t)$ is:

$$f_{trap}(t) = C_0 + \sum_{1}^{\infty} 2|C_n| \cos(n\omega_s t + \angle C_n)$$
(3)

where

$$C_0 = \frac{1}{T_s} \int_{-DT_s/2 - t_r/2}^{T_s - DT_s/2 - t_r/2} f_{trap}(t) dt$$
(4)

$$C_n = \frac{1}{T_s} \int_{-DT_s/2 - t_r/2}^{T_s - DT_s/2 - t_r/2} f_{trap}(t) e^{-jn\omega_s t} dt$$
(5)

$$\omega_s = \frac{2\pi}{T_s} \tag{6}$$

Figure 5 is the Fourier spectrum of a rectangular and two trapezoidal waveforms. "Rect. Wave" represents a rectangular waveform, "Trap. Wave-1" represents a trapezoidal waveform of $t_r = t_f = 500$ ns, and "Trap. Wave-2" represents a trapezoidal wave of $t_r = 500$ ns, $t_f = 50$ ns. The amplitudes of the three waveforms are all 300 V, the equivalent duty ratio is 0.2, and the switching frequency is 200 kHz. The rectangular wave's spectrum turning point is the switching frequency. After the switching frequency, the maximum value of each harmonic decreases with a slope of -20 dB/dec. However, there are two turning points in the trapezoidal waveform's spectrum: one is the switching frequency $(f_{r*} = 1/\pi \sqrt{t_r t_f})$, the maximum value of each harmonic decreases with a slope of -40 dB/dec. If the slope of the rising and falling of a trapezoidal wave can be properly designed, the high frequency components will be rapidly attenuated after a suitable frequency. Even with non-ideal LC filters, the high-frequency components of the output voltage can still be properly attenuated.



Figure 5. Fourier spectrum of a rectangular and trapezoidal waveform. Rect. Wave = a rectangular waveform; Trap. Wave-1 = a trapezoidal waveform of $t_r = t_f = 500$ ns; Trap. Wave-2 = a trapezoidal wave of $t_r = 500$ ns; $t_f = 50$ ns; $f_s =$ switching frequency; $f_{r^*} =$ control by the trapezoidal wave.

From the time-domain analysis, slowing down the voltage variation slope also reduces the instantaneous charging current i_{Cp} of the parasitic capacitance C_p of the non-ideal LC filter in Figure 2b. Figure 6 shows the simulation results for the three kinds of input voltage waveforms used in Figure 5 fed into the non-ideal LC filter respectively. The results show that the rectangular waveform generates the maximum switching noise in both root mean square (rms) and peak–peak values. A trapezoidal waveform with alleviated rising slope did prove attenuated switching noise; however, high switching noise was still present due to the steep falling edge. The bilateral trapezoidal one that slows down both the rising and falling slopes has the smallest switching noise.



Figure 6. Simulation result of switching noise under different input voltage waveforms. pk-pk = peak-peak; $V_{rms} = rms$ value of voltage ripple.

3. Circuit Topology and Operation Principle

Figure 7 shows the proposed bilateral ZVS synchronous rectified step-down converter. The main switches Q_{sr1} and Q_{sr2} cooperate with the output inductor L_0 and the output capacitor C_0 to form a conventional synchronous rectified step-down converter. In order for the high-side switch to achieve ZVS, $C_{ossQsr1}$ must be completely discharged before Q_{sr1} is turned on. To achieve this purpose, a resonant inductor L_r is added to supply the discharging current at suitable timing. The bidirectional switch Q_{aux} is turned on shortly before the turn-off of Q_{sr1}/Q_{sr2} , and is turned off after Q_{sr1}/Q_{sr2} is turned on. The turn-on of Q_{aux} will create a charging path for L_r to generate the current required for ZVS operation. C_{ossD1}/C_{ossD2} represents the sum of the applied capacitance of the diode D_1/D_2 and its own parasitic capacitance. C_{r1} is the sum of C_{ossD1} and $C_{ossQsr1}$, and C_{r2} is the sum of C_{ossD2} and $C_{ossQsr2}$. C_{ossD1} and C_{ossD2} are much larger than the parasitic output capacitance of Q_{sr1} , Q_{sr2} , Q_1 and Q_2 . By adjusting C_{r1} , C_{r2} and the resonant inductor L_r , the voltage transition rate across the switches, Q_{sr1} and Q_{sr2} , as well as the resonant current magnitude can be adjusted.



Figure 7. Bilateral zero-voltage switching (ZVS) synchronous rectified step-down converter.

This architecture can be a bidirectional topology that uses the same switching signal to achieve natural commutation, and forward and reverse operation has similar behavior. This paper gives a detailed explanation of the forward operation, and the reverse part is presented with an action timing diagram. The complete circuit operation can be divided into 10 intervals as described later. The theoretical waveforms of forward mode are depicted in Figure 8, while the corresponding circuit operation diagrams are illustrated in Figure 9. Due to the length limitation, this paper does not elaborate on the action intervals of the reverse power flow operation. A timing diagram, Figure 10, is attached to illustrate the reverse power flow operation as a reference. For the convenience of analysis, the resonant capacitors C_{r1} and C_{r2} are assumed to be identical, i.e., $C_{r1} = C_{r2} = C_r$.



Figure 8. Bilateral ZVS synchronous rectified step-down converter operation waveform (forward mode).

Interval 1 (t_0-t_1): Before t_0 , switches Q_2 and Q_{sr2} are conducting. The output inductor current keeps flowing through Q_{sr2} , and the resonant current i_{Lr} freewheels through D_2 . Therefore, the voltage across Q_{aux} is zero, and $v_{GS}Q_{aux}$ can be pulled high at t_0 to turn on Q_{aux} at zero voltage. Shortly following the turn-on of Q_{aux} , Q_2 is turned off. After Q_2 is turned off, the resonant current detours to the body diode of Q_1 . Since the voltage across the resonant inductor is V_{in} , the resonant inductor current rises linearly. Q_1 can be turned on during this interval to achieve ZVS.

Interval 2 (t_1 – t_2): At t_1 , i_{Lr} is equal to the output inductor current i_L , such that both the body diode of Q_{sr2} and diode D_2 turn off. Since voltage v_{DS_Qsr2} is no longer clamped at zero, resonant inductor L_r begins to resonate with C_{r1} and C_{r2} . The resonance continues until v_{DS_Qsr1} drops to zero.

Interval 3 (t_2 – t_3): At t_2 , both the body diode of Q_{sr1} and diode D_1 are forward biased. The resonant inductor is then short-circuited since Q_1 also conducts. Because of the zero voltage across Q_{sr1} , it is ready for ZVS. Herein, i_{Lr} just freewheels during this interval, while the resonant inductor current continues to circulate in this interval. The power is passed from the input source to the output, and the output inductor current rises linearly.

Interval 4 (t_3 – t_4): At t_3 , switch Q_{aux} cuts off. Since the voltage across switch Q_{aux} is still kept at zero after the cutoff, the turn-off loss is trivial. Although it seems unnecessary to turn off Q_{aux} during this operation interval, in order to ease the gating signal generation for future bidirectional operations and natural commutation characteristics, the gating sequence is set to be the current form.

Interval 5 (t_4 – t_5): At t_4 , Q_{aux} is re-conducted. Again, Q_{aux} turns on at zero voltage and with ignorable switching loss. Immediately after the turn-off of Q_{aux} , switch Q_1 is turned off, and the resonant current i_{Lr} begins to discharge C_{ossQ2} .

Interval 6 (t_5-t_6): Since the voltage on the C_{ossQ2} resonates to zero, finally the body diode of Q_2 is forward biased. Thereafter, the voltage across L_r is $-V_{in}$, and the current through it rapidly drops linearly. Meanwhile, switch Q_2 can be turned on during this interval to reach ZVS.

Interval 7 (t_6-t_7): The resonant current is equal to the output current at t_6 , and the body diode of Q_{sr1} and diode D_1 are reverse-biased. Due to the reverse-recovery of the diodes, i_{Lr} will drop too much and be less than i_L , which forces C_{r1} to get charged and C_{r2} discharged to compensate for the current difference.

Interval 8 (t_7 – t_8): At t_7 , the voltage on C_{r2} drops to zero and forward-biases the body diode of Q_{sr2} and diode D_2 . Again, voltage across L_r is zero and i_{Lr} flows constantly. Since the body diode of the switch Q_{sr2} is already forward-biased, Q_{sr2} can readily reach ZVS during this interval.

Interval 9 (t_8 – t_9): At t_8 , switch Q_{aux} is turned off; accordingly, i_{Lr} discharges C_{r1} and charges C_{r2} . The voltage across C_{r1} finally drops to zero and forward biases diode D_1 . However, since the voltage applies on L_r negatively, i_{Lr} declines linearly.

Interval 10 (t_9-t_{10}): At $t = t_9$, diode D_1 naturally turns off because the resonant inductor current is zero. Similarly, due to reverse-recovery, the overshoot current triggers the resonant oscillation between C_{r1} , C_{r2} and L_r . At t_{10} , v_{DS_Q2} drops to zero, and resonant current freewheels between Q_2 and D_2 .





Figure 9. Topology operation intervals of the proposed converter.



Figure 10. Bilateral ZVS synchronous rectified step-down converter operation waveform (reverse mode).

4. Circuit Analysis

For the simplicity of analysis, some assumptions are made as follows:

- 1. Because the switch Q_{aux} is a series of two switches, its overall parasitic capacitance is much smaller than C_r and C_{ossD} . The switch's parasitic capacitance is omitted to simplify the analysis.
- 2. Since the focus of this paper is on the input waveform improvement, parasitic capacitance or inductance of the output filter is not discussed.
- 3. The on-resistance of the switch and the impedance on the trace are not considered.

4.1. ZVS on Main Switches at Wide Load Range

The ZVS energy requirement over full-load current range can be satisfied by designing the resonant inductor. Figure 11 shows the equivalent circuit of the resonant period (t_1-t_2) . At t_1 , the initial condition of the circuit is: $i_{Lr}(t_1) = i_L$ and $v_{Cr2}(t_1) = 0$.



Figure 11. Equivalent circuit of the resonant period (t_1-t_2) .

The capacitor voltage v_{Cr2} can be obtained as:

$$v_{Cr2} = \frac{(L_r V_o + L_o V_{in})(1 - \cos \omega_{Cr} t)}{L_o + L_r}$$
(7)

where $\omega_{Cr} = \sqrt{\frac{L_o + L_r}{2C_r L_o L_r}}$. To meet ZVS energy requirements over the complete load current range, without considering the diode clamping effect, the peak voltage of v_{Cr2} needs to be higher than V_{in} to satisfy ZVS at $t = \pi / \omega_{Cr}$. Thus:

$$\frac{2(L_r V_o + L_o V_{in})}{L_o + L_r} \ge V_{in} \tag{8}$$

Equation (9) can be derived from (8); in addition, a wide range of output voltage is considered:

$$L_r \le L_o \frac{V_{in}}{V_{in} - 2V_{o\max}} \tag{9}$$

From the equations, the conditions for achieving ZVS depend on the design of L_r and L_0 , regardless of the output load. So, this circuit can be ZVS from no load to full load.

4.2. Robust Control

In the literature [16,17], the ZVS timing requirement is satisfied over the full load range by using the variable zero-voltage detection timing control. Zero-voltage detection timing is influenced by signal detection and signal synthesis time. Therefore, not only is the switching frequency of the application limited, but the detection circuit is also susceptible to the switching noise and diminishes the reliability of the control.

For the operation proposed in this paper, once the body diode of switch Q_{sr1} is forward-biased, the resonant inductor current passes through the body diode of Q_{sr1} as during (t_1-t_3) in Figure 8. Due to the conduction of Q_1 , the voltage drop in this circulation loop consists only of the conduction voltages of the diode and Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET); basically, the resonant inductor current, i_{Lr} , changes quite little. In other words, the ZVS turn-on window for Q_{sr1} is generously wide. This feature allows Q_{sr1} to turn on at a fixed timing without employing any detection circuitry, making the control simpler and more robust.

4.3. ZVS on All Switches

Ideally, the hard-switching happening on the auxiliary switches Q_1 and Q_2 would not interfere with the output voltage at all. However, in the real-circuit operation, additional switching noise induced by the hard-switching of Q_1 and Q_2 is observed. In that case, additional snubber circuitry must be added to suppress the voltage noise. This deployment, however, increases unnecessary loss. In this paper, Q_1 and Q_2 can also achieve ZVS under certain load conditions as illustrated during (t_0-t_1) and (t_5-t_6) in Figure 8, which further reduces the switching noise.

Referring to Figure 8, we can observe that there are two platforms on the resonant inductor current, i.e., I_{Lr_PP} and I_{Lr_NP} . The value of I_{Lr_PP} is $(I_{L_Max} - \triangle i_{Lr})$, where I_{L_Max} is the peak value of the output inductor current, and Δi_{Lr} is the amplitude of the resonant inductor current designed by us. In other words, the value of I_{Lr_PP} will change with the load current. The value of I_{Lr_PP} results in two different operation cases, which in turn affects the value of I_{Lr_NP} , since I_{Lr_NP} is closely related to the ZVS of Q_1 . It turns out that the value of I_{Lr_NP} directly determines whether Q_1 can reach ZVS.

For the first case, $I_{Lr_PP} \ge I_{Lr_D1_ON}$, where $I_{Lr_D1_ON}$ is the critical current that would forward-bias D_1 , and it can be expressed as:

$$I_{Lr_D1_ON} = V_{in} \sqrt{\frac{2 \cdot C_{ossD}}{L_r}}$$
(10)

While I_{Lr_PP} is greater than $I_{Lr_D1_ON}$, D_1 turns on and then asserts $-V_{in}$ across L_r , forcing i_{Lr} to linearly decline to zero. Afterwards, i_{Lr} flows reversely via D_2 . Finally, i_{Lr} completely discharges C_{ossD2} and is locked to $-I_{Lr_NP}$. The value of I_{Lr_NP} is converted into the form of inductor current by the energy stored on C_{ossD2} . Since C_{ossD1} and C_{ossD2} have equal capacitance and are equivalently paralleled together as before, the value of I_{Lr_NP} , in this case, is equivalent to $I_{Lr_D1_ON}$. In other words, I_{Lr_NP} has a constant negative value and does not change with load.

From the time interval (t_1-t_2) , the minimum resonant inductor current value $-I_{Lr_Q1_ZV}$ required for zero-voltage switching of the Q_1 switch can be derived. Its value can be expressed by the following formula:

$$I_{Lr_Q1_ZV} = V_{in} \sqrt{\frac{2 \cdot C_{ossQ}}{L_r}}$$
(11)

Because C_{ossD} is greater than C_{ossQ} , according to Equations (10) and (11), $I_{Lr_D1_ON}$ is larger than $I_{Lr_Q1_ZV}$. When I_{Lr_PP} is greater than $I_{Lr_D1_ON}$, I_{Lr_NP} is fixed to $-I_{Lr_D1_ON}$, so we can see that when I_{Lr_PP} is greater than $I_{Lr_D1_ON}$, all the switches in the converter can achieve ZVS.

For the second case $I_{Lr_PP} \leq I_{Lr_D1_ON}$, i_{Lr} is insufficient to forward-bias D_1 during the interval (t_9-t_{10}) . In this case, the value of I_{Lr_NP} will be equal to I_{Lr_PP} , and the ZVS achievement depends on the value of I_{Lr_NP} . If $I_{Lr_NP} \geq I_{Lr_Q1_ZV}$, all switches in this converter still work with zero-voltage switching.

5. Design Considerations

For the main switch to achieve ZVS, the maximum inductance for L_r is given in Equation (9). However, besides satisfying Equation (9), dead time between switches Q_{sr1} and Q_{sr2} should also be considered. Figure 12 is a magnified timing diagram to narrate the switching operation. As seen in the figure, there are three main parts within the dead time zone. They are distinguished according to the value of i_{Lr} . Among them, only t_B is directly affected by the resonant inductor. After determining t_B , the resonant inductor L_r is designed according to Equation (9).



Figure 12. Detailed timing diagram of the switching operation.

The resonant capacitance affecting the ZVS of the main switches Q_{sr1} and Q_{sr2} includes two parts, C_{ossQsr} and C_{ossD} ; their sum is defined as C_r in previous section. There are two criteria to be considered on design of C_r : the change rate of v_{DS_Osr2} and the overshoot Δi_{Lr} .

From Equation (7), the time required for v_{DS_Qsr2} to rise from zero to V_{in} , defined as t_C in Figure 12, can be deduced. t_C can be expressed as the following equation:

$$t_{C} = \frac{\sqrt{2}\cos^{-1}\left[1 - \frac{V_{in}(L_{o} + L_{r})}{L_{o}V_{o} + L_{o}V_{in}}\right]}{\sqrt{\frac{L_{o} + L_{r}}{C_{r}L_{o}L_{r}}}}$$
(12)

To keep a suitable voltage stress and elapsed time, we first determine the time required for t_C , which is, say t_{C_design} . t_{C_design} is then used to calculate the desired value of C_r . The design rule of C_r can be deduced by Equation (13):

$$C_{r} = \frac{t_{C_design}(L_{o} + L_{r})}{2L_{o}L_{r}\cos^{-1}\left[1 - \frac{V_{in}(L_{o} + L_{r})}{L_{r}V_{o} + L_{o}V_{in}}\right]^{2}}$$
(13)

The value of C_r concurrently affects the overshoot of i_{Lr} . The overshoot Δi_{Lr} is depicted as follows:

$$\Delta i_{Lr} = \frac{\sqrt{2}C_r L_o \sqrt{\frac{L_o + L_r}{C_r L_o L_r}}}{\left(L_o + L_r\right)^2} \left\{ -L_r (V_{in} - V_o) \cos^{-1} \left(\frac{L_r V_o - L_r V_{in}}{L_r V_o + L_o V_{in}}\right) - (L_r V_o + L_o V_{in}) \sqrt{\frac{V_{in} (L_o + L_r) [2L_r V_o + V_{in} (L_o - L_r)]}{\left(L_r V_o + L_o V_{in}\right)^2}} \right\}$$
(14)

Since the overshoot of i_{Lr} must be greater than the ripple of the output inductor current, the voltage v_{DS_Qsr2} can be slowly reduced from V_{in} to zero volts when the Q_{sr1} switch is turned off. Consider the forward bias V_F of the circulating current diode D_1 . The minimum value of the Δi_{Lr} to make sure the end value of i_{Lr} is larger than i_L when Q_1 cuts off in the worst case scenario is:

$$\Delta i_{Lr_Min} = \Delta i_{L_Max} + \frac{D_{\Delta i_{L_Max}} V_F T_s}{L_r}$$
(15)

The Δi_{L_Max} represents the maximum output inductor current ripple of the converter. In the case of the step-down converter, it occurs when duty = 0.5. While $D_{\Delta i_{L_Max}}T_s$ represents the time when the actual resonant inductor current is clamped by the D_1 diode, this time can be approximated as the duty cycle time of the step-down converter. However, too large Δi_{L_r} will increase the circuit's unnecessary conduction loss. It is generally recommended that the final design value be close to the minimum value, taking only necessary margins for some component uncertainties. After C_r is determined, C_{ossD} is obtained by subtracting the parasitic capacitance of C_{ossQsr} from the value of C_r . As a matter of general design, the value of C_{ossD} requires additional shunt capacitance in addition to the parasitic capacitance of the diode itself. Although the parasitic capacitance of semiconductor devices changes with the voltage across it, the designed value of C_r is higher than the parasitic capacitance of the diodes and MOSFETs. In other words, the externally paralleled capacitors determine the criteria of ZVS, while the effect from the parasitic capacitances can be ignored. After the C_r design is completed, the minimum value of I_{Lr_NP} is known from Equation (10), i.e., $I_{Lr_D1_ON}$ can be obtained. Then t_A can be approximated as:

$$t_A = \frac{I_{Lr_D1_ON}L_r}{V_{in}} \tag{16}$$

The overall minimum dead time is $t_A + t_B + t_C$. The actual dead time must be greater than this minimum value to ensure that the circuit can properly achieve ZVS.

6. Simulation and Experimental Results

For verification that the topology has the ability to naturally transform the power flow, and the switch Q_{sr1}/Q_{sr2} can achieve bilateral zero voltage switching under any load conditions, the results of the simulation analysis are as follows. The key simulation parameters are listed in Table 1.

The simulation conditions are input voltage = 330 V, output voltage = 50 V, and output current = 20 A to -20 A. Figures 13–15 show the simulation results of forwarding output = 20 A, output = 0 A, and reverse output = -20 A. Respectively, it can be seen that under any load conditions, both Q_{sr1} and Q_{sr2} can achieve bilateral zero-voltage switching and slow down the rate of voltage change. The auxiliary switch Q_{aux} can also achieve full-range zero voltage switching, and the switches Q_1 and Q_2 can achieve zero voltage switching after a certain load, reducing switching losses.

Parameter	Symbol	Specification
Switching frequency	fsw	200 kHz
Dead time between Q_{sr1} and Q_{sr2}	-	500 nS
Resonant inductor	L_r	2.3 μH
Output inductor	Lo	82.5 μH
Output capacitor	C_o	1.36 mF
Switching parasitic capacitance	$C_{ossO*}/C_{ossOsr*}$	150 pF
Diode parallel capacitor	C_{ossD^*}	40 + 1160 pF

Table 1. The key simulation parameters.



Figure 13. Simulation results: v_{GS} and v_{DS} waveforms of each switch, resonant inductor and output inductor current waveform at V_O = 50 V, I_O = 20 A.



Figure 14. Simulation results: v_{GS} and v_{DS} waveforms of each switch, resonant inductor and output inductor current waveform at V_O = 50 V, Io = 0 A.



Figure 15. Simulation results: v_{GS} and v_{DS} waveforms of each switch, resonant inductor and output inductor current waveform at $V_O = 50$ V, $I_O = -20$ A.

Figure 16 shows the simulation results for an extreme forward-to-reverse conversion. At t = 0.5 ms, the output current is converted from 20 A to -20 A. The ripple, Δi_{Lr} , is designed to be 10 A. It can be seen from the figure that the output inductor current i_L follows the behavior of the output current i_O and the current changes from forward to reverse. Under each switching cycle, the resonant inductor current i_{Lr} automatically follows the output inductor current i_L to achieve the Q_{sr1} and Q_{sr2} bilateral zero voltage switching function. After the zero-voltage switching action, the resonant inductor current i_{Lr} resets to the initial current value cycle by cycle. It can also be seen from the observation of switch signal that the switching signals of the auxiliary switches Q_{aux} , Q_{sr1} , and Q_{sr2} are the same regardless of the forward or reverse operation. It represents the function of naturally transforming the power flow without adding additional detection circuits and changing different control modes.



Figure 16. Simulation results: v_{GS} waveforms of each switch, resonant inductor, output inductor current and output current waveform at $V_O = 50$ V, Io = 20 A to -20 A.

In order to verify the theoretical analysis, a prototype circuit of input voltage V_{in} = 330 V, output voltage V_O = 50–250 V and output power P_o = 1 kW is implemented.

Figure 17 shows the switch's v_{GS} signal waveform of Q_1 , Q_{sr1} , Q_{sr2} and Q_{aux} under the test conditions (output voltage = 250 V and output current = 4 A). In addition to verifying the relative position between the switching signals, it can be seen that all v_{GS} signals have no Miller platform, and it can be seen that all switches have zero voltage switching.



Figure 17. Switch gating signals (scale v_{GS_Q1} (Ch1): 20 V/div; v_{GS_Qsr1} (Ch2): 20 V/div; v_{GS_Qsr2} (Ch3): 20 V/div; v_{GS_aux} (Ch4): 20 V/div; time: 1 μ s/div).

Figure 18 shows the Q_{sr1} switch's v_{GS} signal, Q_{sr2} switch's v_{DS} voltage, resonant inductor current and output inductor current waveform under the test conditions (output voltage = 50 V and output current = 20 A). The converter operates in continuous current mode. It can be seen that the waveform rise and fall speeds of v_{DS} $_{Osr2}$ are simultaneously controlled and have the same slope of change.



Figure 18. Resonant inductor current and output inductor current waveform, Q_{sr1} switch's v_{GS} signal and Q_{sr2} switch's v_{DS} voltage at $V_O = 50$ V, Io = 20 A (scale i_L (Ch1): 20 A/div; i_{Lr} (Ch2): 20 A/div; v_{GS_Qsr1} (Ch3): 20 V/div; v_{DS_Qsr2} (Ch4): 500 V/div; time: 1 µs/div).

Figure 19 shows the Q_{sr1} switch's v_{GS} signal, Q_{sr2} switch's v_{DS} voltage, resonant inductor current and output inductor current waveform under the test conditions (output voltage = 250 V and output current = 4 A). The converter operates in continuous current mode. It can be seen that the waveform rise and fall speeds of v_{DS_Qsr2} are simultaneously controlled and have the same slope of change. Figure 20a,b show the output voltage ripple with and without the enabling of the auxiliary switching circuit; that is, Q_{sr1} is hard/soft switching. Test conditions are output voltage = 250 V and output power = 1 kW. The switching noise observed in Figure 20a is 266 mV, while it is 66 mV in Figure 20b. Under the same operation conditions, the output voltage switching noise is greatly reduced by the proposed circuit.



Figure 19. Resonant inductor current and output inductor current waveform, Q_{sr1} switch's v_{GS} signal and Q_{sr2} switch's v_{DS} voltage at $V_O = 250$ V, Io = 4 A (scale i_L (Ch1): 10 A/div; i_{Lr} (Ch2): 10 A/div; $v_{GS Osr1}$ (Ch3): 20 V/div; $v_{DS Osr2}$ (Ch4): 500 V/div; time: 1 µs/div).



Figure 20. Switching noise performance: output voltage ripple, output inductor current waveform, Q_{sr1} switch's v_{GS} signal and Q_{sr2} switch's v_{DS} voltage at $V_O = 250$ V, $I_O = 4$ A (**a**) without peration of auxiliary circuit (**b**) with peration of auxiliary circuit (scale $v_{o\ ripple}$ (Ch1): 200mV/div; i_L (Ch2): 20 A/div; v_{GS_Qsr1} (Ch3): 20 V/div; v_{DS_Qsr2} (Ch4): 500 V/div; time: 1 µs/div).

Figure 21a,b represents similar comparisons on switching noise, except that the output voltage = 50 V in this case. The switching noise measured in Figure 21a is 200 mV, compared to 144 mV in Figure 21b. Again, switching noise can also be greatly reduced by the proposed scheme. From the experimental results, it is verified that the proposed auxiliary switching circuit can improve the switching noise under adjustable output voltage and current level. This feature is particularly useful for instrument power supplies.



Figure 21. Switching noise performance: output voltage ripple, output inductor current waveform, Q_{sr1} switch's v_{GS} signal and Q_{sr2} switch's v_{DS} voltage at $V_O = 50$ V, Io = 20 A (**a**) without peration of auxiliary circuit (**b**) with peration of auxiliary circuit (scale $v_{o\ ripple}$ (Ch1): 200 mV/div; i_L (Ch2): 20 A/div; v_{GS_Qsr1} (Ch3): 20 V/div; v_{DS_Qsr2} (Ch4): 500 V/div; time: 1 µs/div).

7. Conclusions

This paper proposed a bidirectional converter operating at wide output voltages and load variation applications. By the auxiliary circuit, the main switches can achieve bilateral zero-voltage switching and the switching noise on the output voltage can be effectively reduced. Through the simulation and implementation results, the feasibility of the proposed architecture can be verified. A prototype of 1 kW with an output voltage of 50 V to 250 V has been implemented. Since the higher output voltage and higher load level will cause a higher voltage feeding into the output filter, the proposed method benefits even more from reducing the voltage slopes during both rising and falling. In the measured results, the best noise reduction is in the 250 V/1 kW output test condition. The switching noise of the output voltage is reduced from 266 mV to 66 mV; the reduction rate reaches about 75.18%.

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