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Design and Control of a 13.2 kV/10 kVA Single-Phase Solid-State-Transformer with 1.7 kV SiC Devices

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Abstract: This paper describes the power stage design, control, and performance evaluation of a 13.2 kV/10 kVA solid-state-transformer (SST) for a power distribution system. The proposed SST consists of 10 modules where each individual module contains a unidirectional three-level power factor correction (PFC) converter for the active-front-end (AFE) stage and an LLC resonant converter for the isolated DC-DC stage. The operating principles of the converters are analyzed and the modulation and the control schemes for the entire module are described in detail. The DC-link voltage imbalance is also less than other SST topologies due to the low number of uncontrollable switching states. In order to simplify the control of the power stage, a modulation strategy for the AFE stage is proposed, and the modulation frequency of the LLC converter is also fixed. In addition, a compensation algorithm is suggested to eliminate the current measurement offset in the AFE stage. The proposed SST achieves the unity power factor at the input AC current regardless of the reactive or nonlinear load and a low voltage regulation at the AC output. In order to verify the effectiveness of the SST, the 13.2 kV/10 kV SST prototype is built and tested. Both the simulation and the experimental results under actual 13.2 kV line show the excellent performance of the proposed SST scheme.

Keywords: solid-state-transformer (SST); three-level power factor correction (PFC) converter; LLC converter; multi-level converter

1. Introduction

Recently, solid-state-transformers (SSTs) have emerged in the electricity industries where new technologies such as the smart grid, the renewable energies, and the DC distribution systems are adopted [1–6]. A SST is a power transformer, which is based on power electronics technology, so that the voltage and the current of the primary and the secondary sides can be actively compensated or controlled which cannot be realized in traditional power transformers. Among various stages in a power system including the generation, the transmission and the substation, and the distribution systems, the power transformers in distribution stages are good candidates to be replaced with SSTs because they are directly connected to the loads, and have relatively lower input voltage compared to the one in the other stages.

Figure 1 compares the structures of a traditional distribution power transformer and a SST configuration. In the Republic of Korea, the primary and the secondary voltages of power distribution stages are standardized as 13.2 kV and 220 V in root-mean-square (rms) value. It means a SST in the distribution stage should be able to operate in the input and the output voltage ranges. Unlike the traditional transformers, the SST consists of three individual power stages, the active-front-end (AFE), the isolated DC-DC, and the load inverter stages. The main roles of each stage are described as follows. First, the AFE converter performs the input power factor correction (PFC) with low total harmonic distortion (THD) as well as regulating the input DC voltage of the isolated DC-DC stage. It means

that the utility grid can treat the SST as a purely resistive load, which does not produce harmonics. Since the unity power factor (PF) can be achieved, only a real power is transferred from the power system to the load regardless of the characteristics of the load. This is an important merit of the SST regarding the power system, because no reactive power is supplied. In fact, it is also possible to supply a reactive power according to the topology selection of the SST. Second, the load inverter stage exists to supply a regulated output voltage. The load inverter employs the DC-link capacitors so that a voltage sag or a short period of an under-voltage fault on the primary sides does not degrade the quality of the output voltage. Furthermore, the load voltage can be easily adjusted when the utility grid is necessary the feature. If a DC distribution is required in the utility grid, the load inverter can be omitted or replaced with a DC-DC converter. Third, the isolated DC-DC stage is employed to offer electrical isolations between the power grid and the load stages. Its input and output voltages are 25 kV and 500 V in this paper, respectively. By combining all three power stages, the SST features very attractive functions as summarized in Table 1.

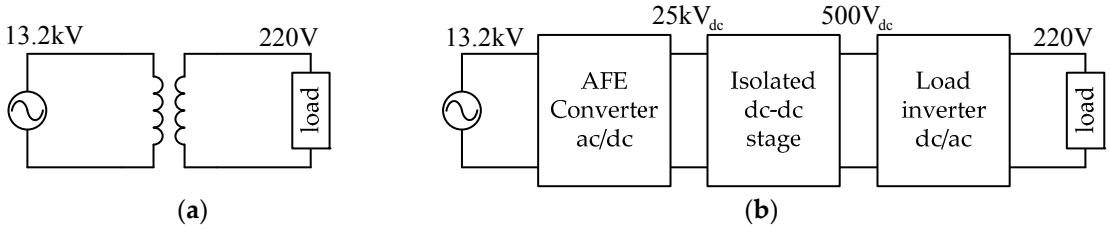

Figure 1. Distribution Transformer (**a**) Traditional distribution transformer (**b**) the solid-state-transformer (SST) configuration. AFE: active-front-end.

Table 1. Comparison between a traditional distribution transformer and the solid-state-transformer.

Traditional Transformers	Solid-State-Transformers
AC distribution only	either DC or AC distribution
Limited steps of voltage conversion ratio	Wide voltage conversion ratio
No power quality compensation	Power quality compensation available
Heavy	Relatively light
Without DC-link	With DC-link (easily interfaced with other power conversion systems)
Mature technology	New technology

Regarding SSTs, many research has been conducted. In [7–12], SSTs named intelligent universal transformer (IUT), smart transformer (ST), and power electronics transformer (PET), for the medium voltage systems were proposed and tested. In the documents, the neutral point clamp (NPC) type AFE and isolated DC-DC converters were implemented for 2.4 kV AC line. The excellent performance of the SST under the voltage sag and the nonlinear load conditions were demonstrated [8]. In [9], the frequency adaptive repetitive controller is studied for the solid state transformer to interface medium voltage (MV) to low voltage (LV) distribution line, where the operating frequency is varied. The voltage and power balance control methods were presented in [13–15] where the cascaded AFE and dual-active-bridge (DAB) converters with all H-bridge modules were employed. Reference [16] discussed the design strategy of the efficient and reliable silicon carbide (SiC) based DC-DC converter for ST. The design of PETs for electric traction applications are dealt in [17,18]. The SSTs for the DC distribution system were described in [4,19]. In [4], the DC droop control strategy was presented, so that the usefulness of the SST in the DC distribution system could be advanced. The 3D space modulation technique of the cascaded converter was proposed in [2]. By using the method, the current and the voltage control performances of the AFE stage could be improved. Reference [20] presented a 15-kV class SST. In the paper, the authors have employed 1.2 kV SiC metal oxide semiconductor field effect transistors (MOSFETs) to the individual power stage to secure high efficiency. Some papers [21–25] have dealt with the SSTs using high voltage switching devices whose voltage rating is over 10 kV.

If such high voltage devices become more common, it is expected that the use of SSTs in the power grid can be dramatically increased.

In this paper, a single-phase 10 kVA SST is proposed for the 13.2 kV/220 V power distribution system with 1.7 kV SiC MOSFETs. The proposed SST consists of 10 modules whose voltage rating is 1.32 kV. Each module is composed of a unidirectional three-level PFC converter for the AFE stage and an LLC resonant converter for the isolated DC-DC stage. Compared to other SSTs, where a bidirectional three-level inverter is employed, the proposed AFE stage is simple and reliable. The DC-link voltage imbalance is less than others, because the uncontrollable switching states are much less than them, and no significant power imbalance problem has occurred. The control and modulation are also simple in the proposed AFE and LLC stages. The operations of the individual and total power stage are described in detail. Furthermore, the current offset compensation algorithm for the current measurement offset in the AFE stage is proposed. By using the proposed offset compensation algorithm, the input current offset can be effectively compensated. The simulation and the experimental results show that the excellent current and voltage regulation performance of the proposed SST in practical 13.2 kV power distribution system.

2. Solid-State-Transformer for Electric Power Distribution System

2.1. Power Stage Configuration

Figure 2 illustrates the entire power stage configuration of the SST dealt in this paper. In the Republic of Korea, the primary voltage of the distribution stage is standardized as 13.2 kV in rms. In order to handle such the high voltage, a total of 10 modules are cascaded. The input voltage of each individual module is 1.32 kV, so that 1.7 kV or 3.3 kV switching devices can be employed according to the topology of the circuit. The outputs of the modules are paralleled while generating 500 V in DC. The final purpose of the SST is to supply 220 V/60 Hz load. To do this, a load inverter is connected at the output of the module. Since there are a lot of research articles for such a low voltage standalone inverter, the discussion about the inverter is not addressed in this paper.

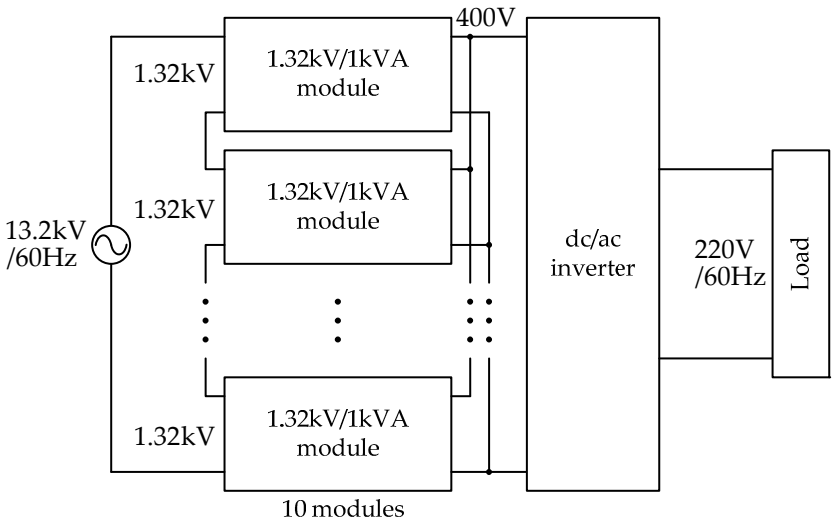

Figure 2. Power stage configuration of the 13.2 kV/10 kVA SST.

Figure 3 illustrates the circuit configuration of the 1.32 kV/1 kVA module. Here, the three-level PFC converter is implemented for PFC operation of the input current as well as establishing the DC-link voltage which is the sum of V_{dch} and V_{dcl}. It should be noticed that the three-level PFC converter is a unidirectional converter so that the reverse power flow from the load to the grid is not allowed. Nevertheless, the three-level PFC topology is beneficial in the application, where the unidirectional

SST is necessary, because of the efficiency and the simple control. Moreover, the DC-link voltage imbalance is less than other bidirectional three-level topologies such as neutral point clamped (NPC) and T-type NPC structures due to the less number of non-controllable switching states and balanced high frequency (HF) transformer construction [20,26]. At the output of the three-level PFC converter, the LLC converter is connected to produce 500 V DC output from 2.5 kV DC-link voltage as well as guaranteeing an electrical isolation. It should be noticed that the LLC converter is operated in the open-loop control manner to simplify entire control loop of the SST. It will be detailed in a later section.

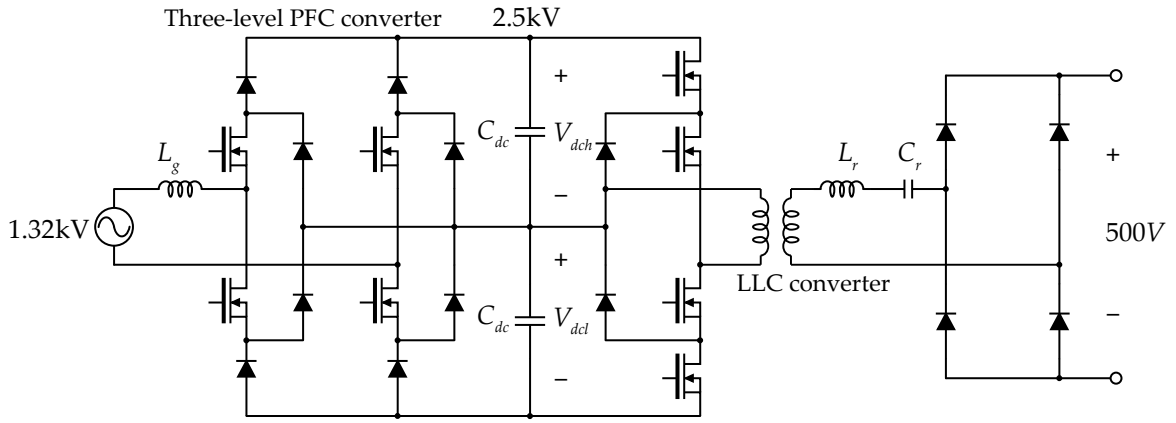

Figure 3. Circuit configuration of the 1.32 kV/1 kVA module. PFC: power factor correction.

2.2. Three-Level PFC Converter Operation

The operation modes of the three-level PFC converter are determined by the direction of the input current and the status of the switching devices. Figure 4 depicts the current conduction paths of the converter when the input current i_g is under positive cycles. Here, four different modes are addressed according to the switching functions which are expressed as the combinations of the switching signals as follows:

$$Q = (q_1, q_2, q_3, q_4) \tag{1}$$

where q_1, q_2, q_3, and q_4 are the elements of the switching function which correspond to the status of Q_1, Q_2, Q_3, and Q_4, respectively. Here, the value of an element becomes 1 if the matching switch turns on whereas it becomes 0 when the switch turns off.

Figure 4a shows the current conducting path when all switches are turned on. At this moment, i_g flows through L_g, Q_2, D_2, D_3, Q_3, and the voltage source, and the energy is stored in the inductor L_g. Even if Q_1 and Q_3 turn on, no power flows from the DC-link to the grid because of the blocking diodes D_{1p} and D_{3p}. The inductor current i_g and the pole voltage of the PFC converter v_{inv} are represented as:

$$\frac{di_g}{dt} = \frac{v_g}{L_g} \tag{2}$$

$$v_{inv} = 0\,\mathrm{V} \tag{3}$$

In Figure 4b, Q_3 turns off while the others are under turned on. In this case, i_g flows through L_g, Q_2, D_2, C_{dcl}, D_{4p}, Q_4, and the voltage source. The energy stored in L_g is transferred to the lower DC-link capacitor C_{dcl}. Here, the current flows from the source to the drain in Q_4. Since the gate signal of Q_4 is applied, the current conducting path in Q_4 does not pass the internal body diode, which has poor switching characteristics, but the channel whose conduction and switching losses are relatively lower than the body diode. By doing so, the losses induced in Q_4 can be significantly reduced. This is

based on exactly the same concept with a synchronous rectification mode of a DC-DC converter using MOSFETs [27–29]. The inductor current and the pole voltage are written as:

$$\frac{di_g}{dt} = \frac{v_g - V_{dcl}}{L_g} \tag{4}$$

$$v_{inv} = V_{dcl} \tag{5}$$

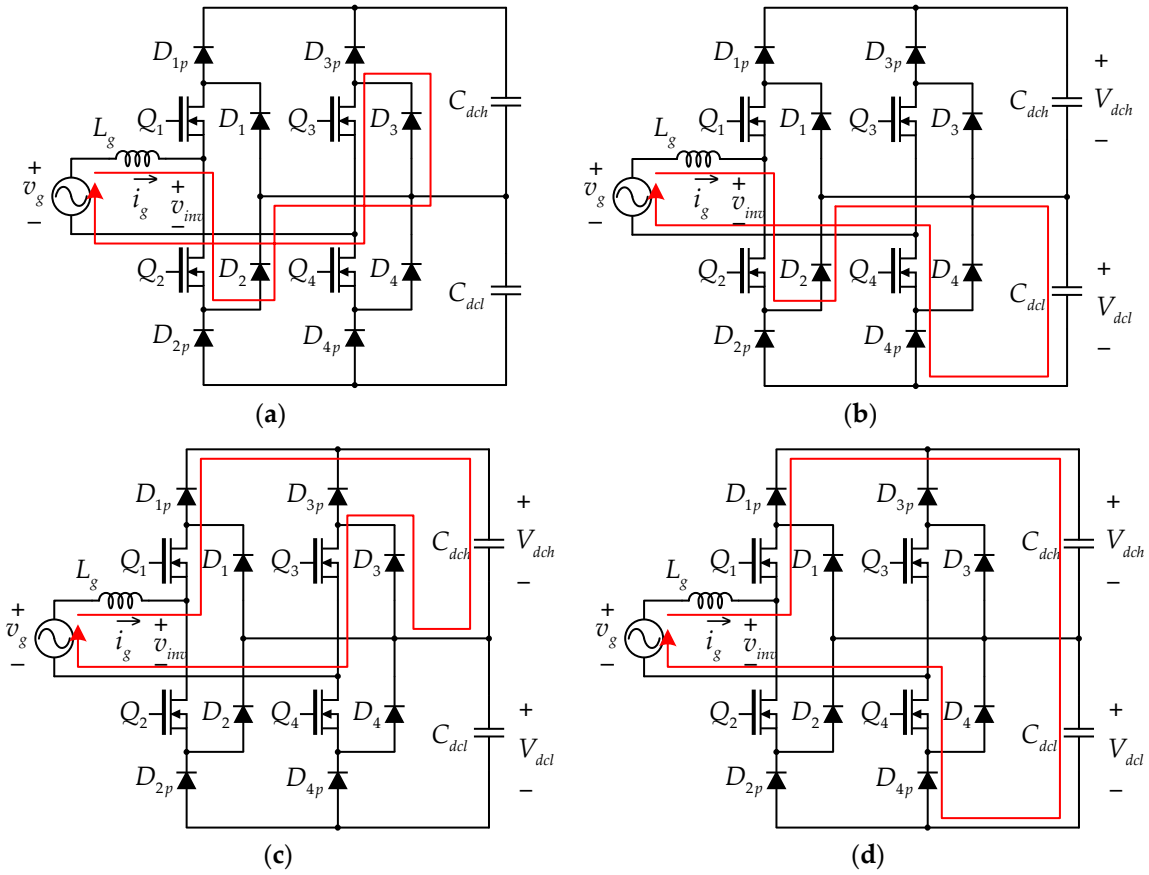

Figure 4. Operation modes of the three-level PFC converter under $i_g > 0$. (**a**) Q = (1,1,1,1); (**b**) Q = (1,1,0,1); (**c**) Q = (1,0,1,1); (**d**) Q = (1,0,0,1).

Figure 4c illustrates the current conduction path when Q is (1,0,1,1). Again, the stored energy in L_g is transferred to the DC-link, and the upper capacitor C_{dch} takes it. The current conduction path consists of L_g, Q_1, D_{1p}, C_{dch}, D_3, and the voltage source. Similar to the case of Figure 4b, Q_1 conducts the current from the source to the drain through the channel. While the pole voltage is the same with (5), the inductor current is obtained as below.

$$\frac{di_g}{dt} = \frac{v_g - V_{dch}}{L_g} \tag{6}$$

The last case where Q is (1,0,0,1) is shown in Figure 4d. At this instant, the inductor current passes through L_g, Q_1, D_{1p}, C_{dch}, C_{dcl}, D_{3p}, Q_4, and the voltage source as well as discharging the energy stored in L_g. Both Q_1 and Q_4 are conducted through the channels in reverse. The equations for i_g and v_{inv} are represented as follows:

$$\frac{di_g}{dt} = \frac{v_g - (V_{dch} + V_{dcl})}{L_g} \tag{7}$$

$$v_{inv} = V_{dch} + V_{dcl} \tag{8}$$

It is interesting that Q_1 and Q_4 keep turn-on continuously for positive cycles, and only Q_2 and Q_3 alter their switching status as can be seen in Figure 4. In fact, the modulation strategy using these switching combinations are suitable for reducing a conduction loss in a power stage employing MOSFETs, because the poor internal body diodes in MOSFETs do not turn on [30,31]. However, it may not be a good solution for a power stage using insulated gate bipolar transistors (IGBTs). In such cases, simple modulation methods [30–32] can be acceptable.

Similarly, the current conduction paths for $i_g < 0$ are shown in Figure 5. The operational principle is identical to the previous case where i_g is positive except the switching combinations and the pole voltage whose values can be 0 V, $-V_{dch}$, $-V_{dcl}$, and $-(V_{dch} + V_{dcl})$. As compared to the previous case, the status of Q_2 and Q_3 are not changed while the ones of Q_1 and Q_4 are continuously changed in every switching cycle.

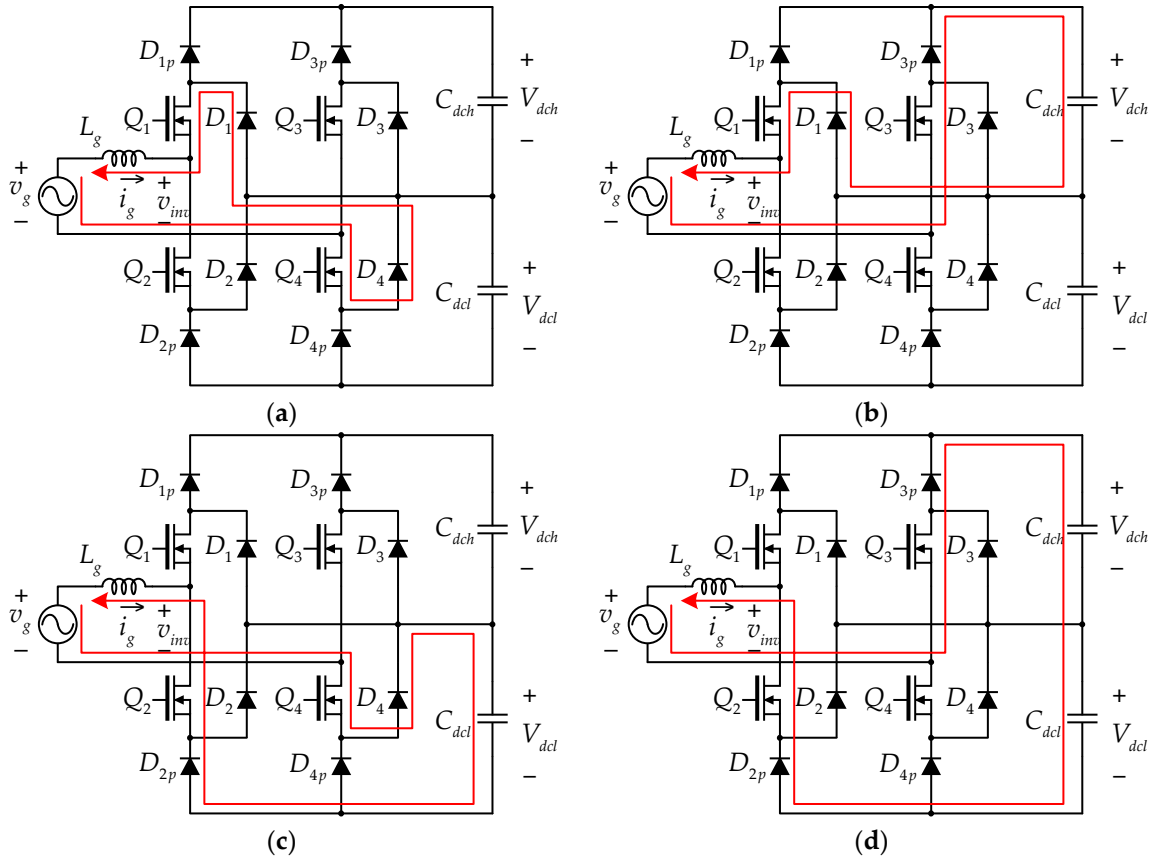

Figure 5. Operation modes of the three-level PFC converter under $i_g < 0$. (**a**) Q = (1,1,1,1); (**b**) Q = (1,1,1,0); (**c**) Q = (0,1,1,1); (**d**) Q = (0,1,1,0).

Table 2 summarizes the relationship between the switching functions and the pole voltages including all cases. If V_{dcl} and V_{dch} are well balanced, so that their magnitudes are the same as V_{dc}, the PFC converter has five levels in total: $-2V_{dc}$, $-V_{dc}$, 0 V, V_{dc}, and $2V_{dc}$. It is well-known that carrier-based modulation strategies are simple, and much research has been conducted for the carrier-based pulse-width-modulation strategies in NPC applications [33–35]. Hence, a simple carrier-based method is employed in this paper.

Table 2. The relationship between the switching function and the pole voltage.

Polarity of i_g	Switching Function Q	Pole Voltage v_{inv}
$i_g > 0$	(1,1,1,1)	0 V
	(1,1,0,1)	V_{dcl}
	(1,0,1,1)	V_{dch}
	(1,0,0,1)	$V_{dch} + V_{dcl}$
$i_g < 0$	(1,1,1,1)	0 V
	(1,1,1,0)	$-V_{dch}$
	(0,1,1,1)	$-V_{dcl}$
	(0,1,1,0)	$-(V_{dch} + V_{dcl})$

Figure 6a describes the modulator structure of the PFC converter to achieve the current conduction modes addressed in Figures 4 and 5. The limiter 1 only extracts the positive component from the original duty reference while the limiter 2 obtains the negative one. Let us assume that the grid current i_g is well regulated with unity power factor operation. When i_g is positive, Q_1 should be always turned on, and Q_2 is switching according to d_2. If i_g is negative, the roles of Q_1 and Q_2 are exchanged. For the switching leg consisting of Q_3 and Q_4, the inverse of the original duty reference is applied. By doing so, the effective switching frequency becomes double, and the switching ripple on the inductor current is significantly reduced.

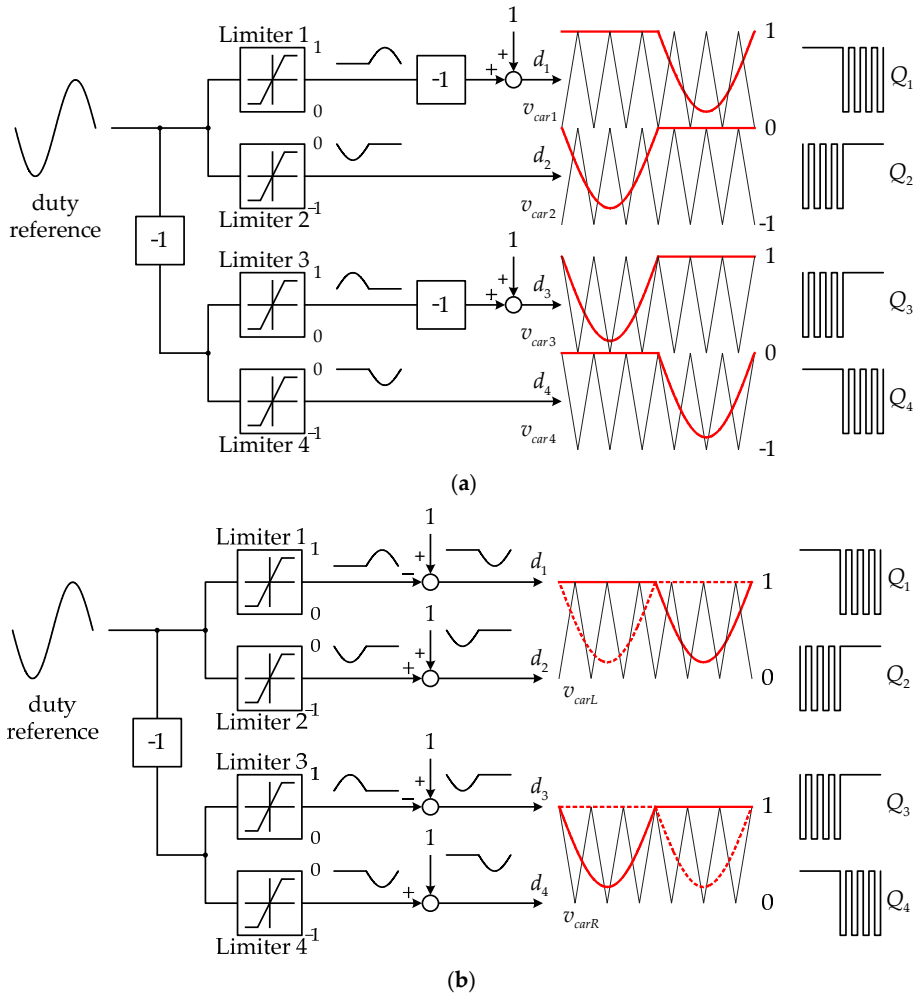

Figure 6. Modulation schemes for the PFC converter. (**a**) Original modulator; (**b**) Equivalent structure of the original modulator.

Although the structure shown in Figure 6a is completely suitable for the power stage in this paper, it requires four different carrier signals. This may be a significant burden for the digital controller, and the implementation will be complicated. To simplify the realization, the modified structure for the modulator is proposed in Figure 6b. In the modified structure, only two carrier signals (whose phase difference is 180 degrees) are necessary, and the method to extract individual duty references d_1, d_2, d_3, and d_4 is slightly different. By doing so, the process shown in Figure 6b is exactly equivalent to the structure illustrated in Figure 6a.

2.3. LLC Converter Operation

Figure 7 depicts the circuit configuration of the LLC converter. It is fed by the separate DC sources V_{dch} and V_{dcl} which are established by the output of the front-end PFC converter. The main switching circuit is implemented in the manner of NPC type inverter, but the switching scheme is different. In the LLC converter, the upper and the lower switch pairs are defined. The upper switch pair consists of Q_{c1} and Q_{c2} while the lower switch pair contains Q_{c3} and Q_{c4}. Unlike NPC inverters, each switch pair operates as a single switch, so that the switch elements in a switch pair alter their status simultaneously. As a result, the output voltage v_{pri} reveals a two-level voltage whose peak and valley values are V_{dch} and V_{dcl}. Meanwhile, the rating of individual switching devices can be cut by half due to the clamping action of D_{C1} and D_{C2}. At the output of the NPC inverter, the isolated HF transformer and the LC resonant tank are existent. Since the output of the resonant tank is AC voltage, the diode rectifier composed by D_{r1}, D_{r2}, D_{r3} and D_{r4} is necessary. In order to design the LLC converter, let us consider the equivalent resonant circuit as shown in Figure 8 where L_m, L_r and C_r are the magnetizing inductance of the HF transformer, the resonant inductor, and the resonant capacitor, respectively [36].

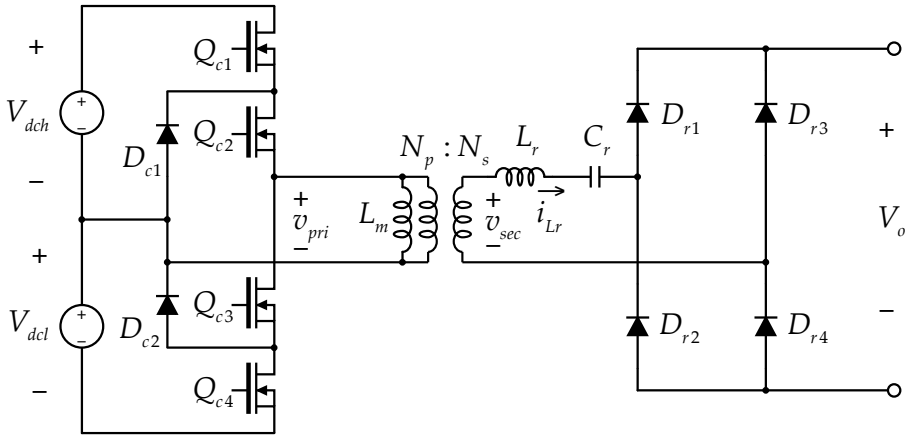

Figure 7. Circuit configuration of the LLC converter.

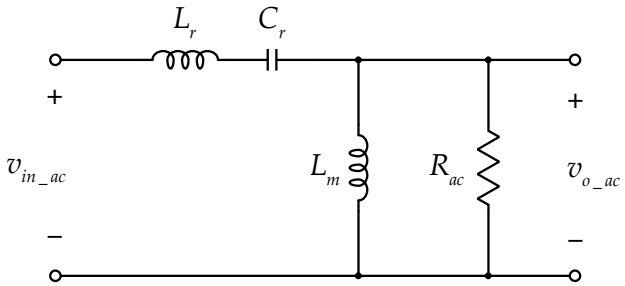

Figure 8. Equivalent resonant circuit [36].

The resonant tank gain is defined as follows:

$$K = \left| \frac{V_{o\_ac}(s)}{V_{in\_ac}(s)} \right| = \frac{F_x^2(m-1)}{\sqrt{(m \cdot F_x^2 - 1)^2 + Fx^2(F_x^2 - 1)^2(m-1)^2 Q^2}} \tag{9}$$

where $V_{o\_ac}(s)$, $V_{in\_ac}(s)$, Q, m, and F_x are the Laplace transformations of v_{in_ac} and v_{o_ac}, the quality factor, the ratio of the total primary inductance to resonant inductance, and the normalized switching frequency. They are represented as:

$$Q = \frac{\sqrt{\frac{L_r}{C_r}}}{R_{ac}} \tag{10}$$

$$m = \frac{L_r + L_m}{L_r} \tag{11}$$

$$F_x = \frac{f_s}{f_r} \tag{12}$$

Here, f_s is the switching frequency, and the resonant frequency f_r and the reflected load resistance R_{ac} are written as:

$$f_r = \frac{1}{2\pi\sqrt{L_r C_r}} \tag{13}$$

$$R_{ac} = \frac{8}{\pi^2}\frac{N_p^2}{N_s^2} R_o \tag{14}$$

where N_p, N_s, and R_o are the primary turns ratio, the secondary turns ratio, and the load resistance.

Figure 9 compares the voltage gains under different m and Q factors. In the figure, the voltage conversion ratio can be extended as decreasing m factor. However, a low m factor requires a low L_m, so that the magnetizing current increases. Thus, the conduction loss of the magnetic component is increased. In terms of Q factor, it is proportional to the load. According to the figure, the voltage gain cannot be higher with a heavy load. In fact, the voltage gain is changed by both m and Q factors.

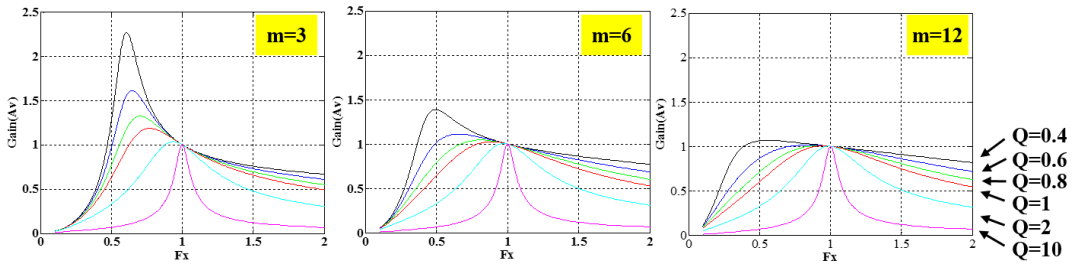

Figure 9. Comparison of the voltage gain under different m and Q factors.

One simple approach to select these parameters is setting the switching frequency to be the resonant frequency, so that F_x becomes 1 [36–38]. By doing so, (9) can be simplified as below.

$$K = \left| \frac{v_{o\_ac}}{v_{in\_ac}} \right| = \frac{(m-1)}{\sqrt{(m-1)^2}} = 1 \tag{15}$$

It means the voltage gain of the resonant tank is the unity. Hence, the output voltage is determined by the primary and the secondary turn ratio of the HF transformer. By this way, the LLC converter can be considered as a DC transformer.

2.4. Control Strategy of the Power Stages

In a single module, the switching frequency of the three-level PFC converter is effectively double the original one, because the interleaved operation is achieved by employing the two carriers with 180 degrees of phase difference. In the whole active front end stage, where a total of 10 modules are connected, the three-level PFC converters in the stage are cascaded to distribute such the high input AC voltage into the individual modules. In addition, the phase shift modulation is applied for the entire cascaded PFC converters.

Figure 10 depicts the carrier waveforms for individual modules. Let us assume that the number of the modules is represented as N. From the figure, the phase difference θ_n between nth module and the first module is represented as [39–41]:

$$\theta_n = \frac{180}{N}(n-1) \text{ degree} \tag{16}$$

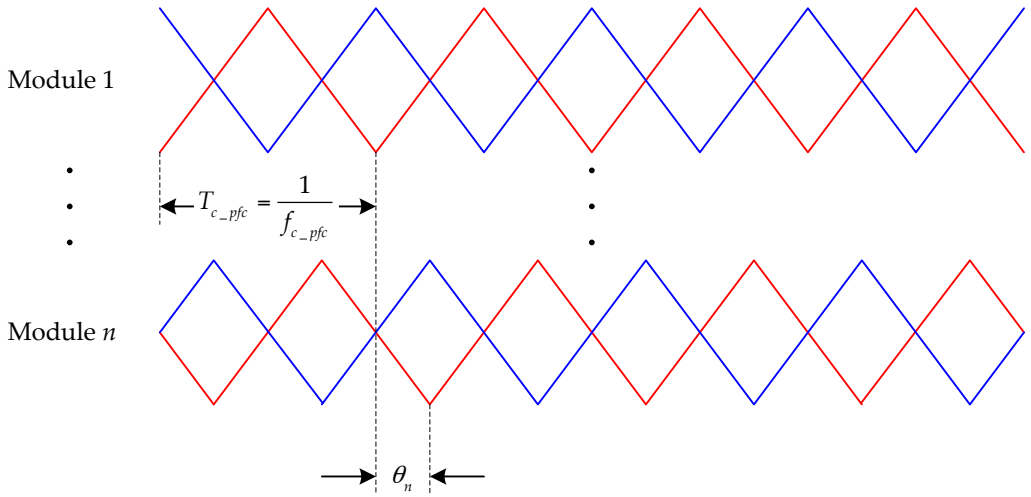

Figure 10. Carrier waveforms for individual modules.

The effective switching frequency f_{sw_pfc} considering the phase difference is written as:

$$f_{sw\_pfc} = 2N \times f_{c\_pfc} \tag{17}$$

where f_{c_pfc} is the carrier frequency of a switching leg. As can be seen in (17), the effective switching frequency can be increased as proportional to N. Figure 11 shows the entire control structure of the SST. For the isolated DC-DC stage, the switching signals are modulated with a fixed frequency with a fixed duty reference, so that technically no closed-loop control is applied to the stage. The isolated DC-DC stage only interfaces between the high voltage primary and the low voltage secondary sides. Once the turn ratio of the HF transformers in the isolated DC-DC stage is determined, the secondary output voltage V_o is directly proportional to the primary DC-link voltage. It means the regulation of V_o is achieved by adjusting the primary DC-link voltage. However, it is not that simple, because the primary DC-link voltage of the isolated DC-DC stage consists of cascaded multiple DC-links. It requires 10 DC-link voltage sensors. In addition, the signal conditioning circuitries to interface the individual DC-link voltage sensor require at least 20 kV of isolation capability. Apparently, these increase the implementation cost and complexity. In order to resolve this issue, the voltage controller $G_{vc}(s)$ directly regulates V_o by controlling the input current of the AFE stage. The controller consists of the voltage controller $G_{vc}(s)$ and the current controller $G_{cc}(s)$. For the voltage and the current controllers, a proportional-integral (PI) and a proportional-resonant (PR) structures are employed. The output

of $G_{vc}(s)$ is multiplied by the phase angle detected from the phase-locked-loop (PLL), and the input current reference i_{g_ref} is obtained. After that, i_g is regulated to track i_{g_ref} by the operation of $G_{cc}(s)$. The output of $G_{cc}(s)$ is d_{pfc} which is the duty reference of the AFE stage. The PFC modules in the AFE stage shares d_{pfc}, but the phases of individual PFC modules are different by reflecting (16).

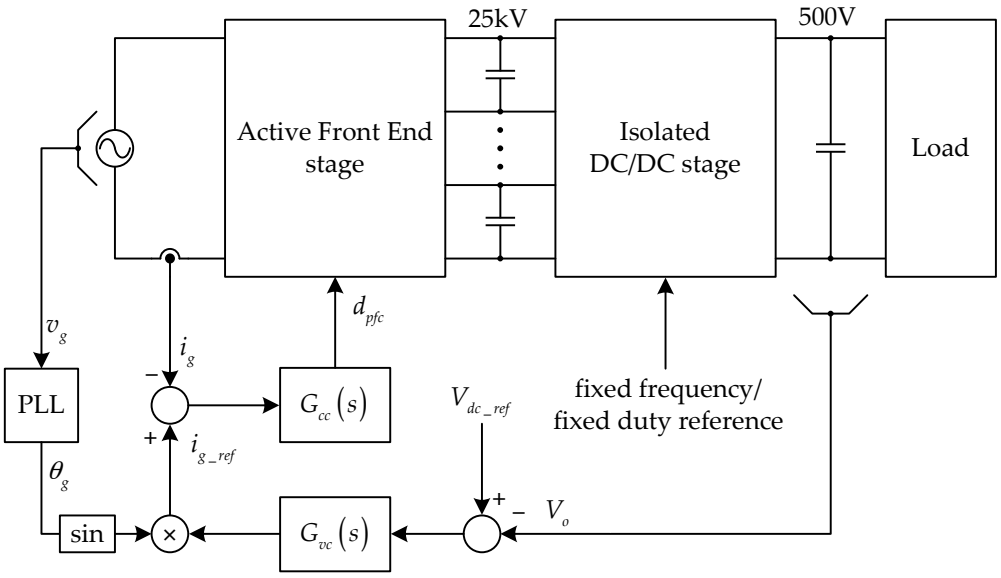

Figure 11. Control structure of the solid-state-transformer. PLL: phase-locked-loop.

3. Proposed Input Current Offset Compensation Method

For a grid-tied power electronic converter, the input AC current should not contain any DC offset component to prevent a DC excitation to the power grid and the distribution transformer, where the converter is connected. However, it is hard to avoid a measurement offset on the current sensor used in a converter. In order to mitigate the problem, an offset compensation algorithm is proposed. Figure 12a shows the proposed offset compensation method including the PR current controller. Assume that there is the DC offset I_{go} in the current measurement path. Then, the error, which is the input of the PR controller, is represented as:

$$i_{err} = i_{g\_ref} - i_g - I_{go} \tag{18}$$

Here, the estimated DC offset I_{go_est} is not contained. Then, the output of the PR controller only considering I_{go} is written as:

$$i_{err\_go} = -I_{go}\left(K_{pc} + \frac{K_{rc}s}{s^2 + \omega_r^2}\right) \tag{19}$$

where ω_r is the fundamental frequency of the grid. Since I_{go} can be considered as a unit step function with the gain I_{go}, the inverse Laplace transform of (19) is obtained as (20).

$$I_{err\_go} = K_{pc}I_{go} + \frac{K_{rc}I_{go}\sin(t\omega_r)}{\omega_r} \tag{20}$$

In fact (20) is a part of the duty reference d_{pfc}, and the first term of the right-hand-side (RHS) is apparently a DC component. From this, it is supposed that a DC offset induces a DC component in d_{pfc} which is the output of the PR controller.

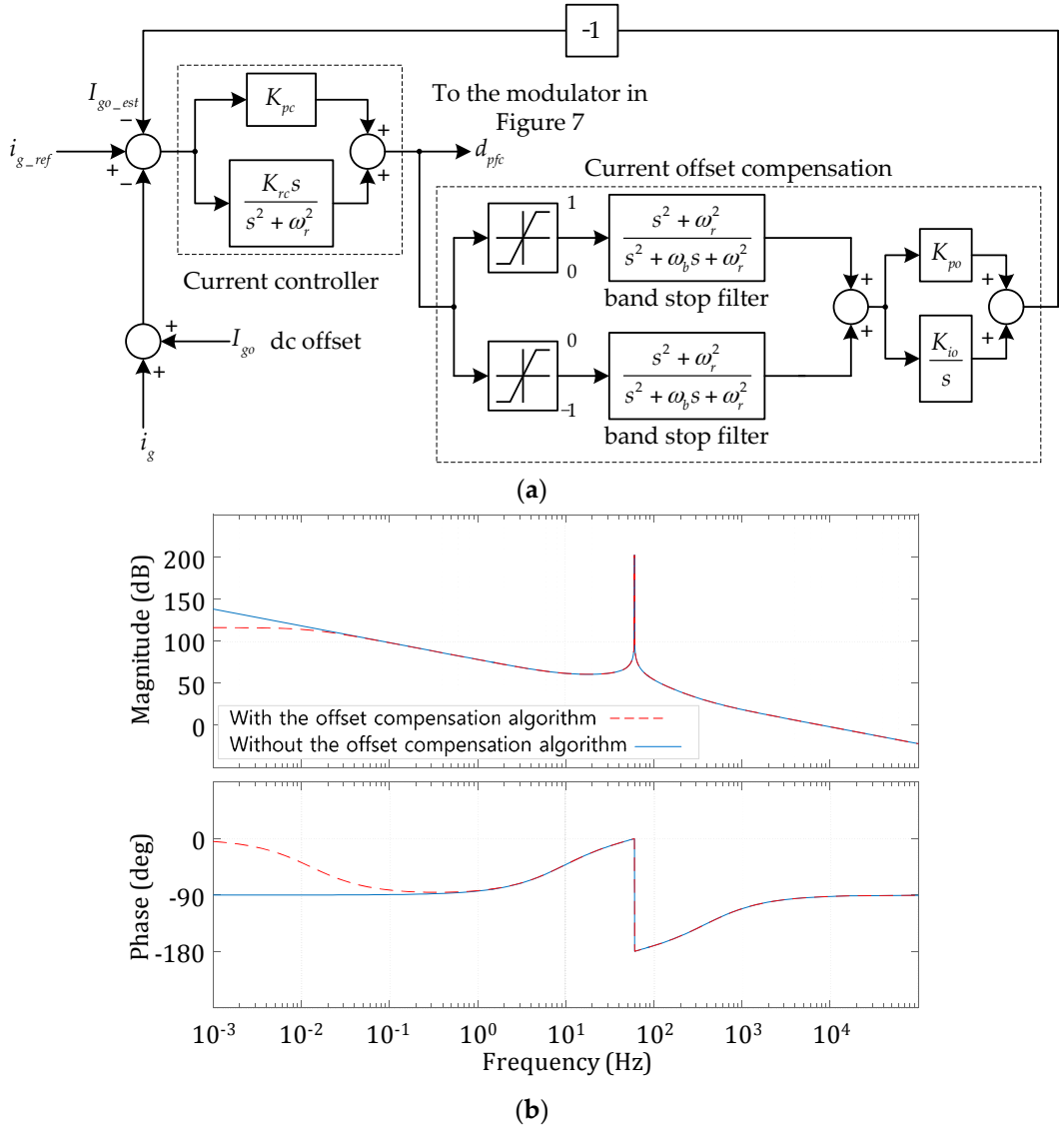

Figure 12. Proposed control structure and open-loop gain. (**a**) Current control structure with the offset compensation algorithm (**b**) open-loop gain of the control loop.

Here, d_{pfc} is taken as the input of the current offset compensation block, which consists of the limiters, the band stop filters (whose cut-off frequency is ω_r), and the proportional-integral (PI) estimator. In the compensation block, the positive and the negative parts of d_{pfc} are distinguished by the limiters. After that the band stop filters are applied the DC component $K_{pc} \cdot I_{go}$ in d_{pfc} is extracted. If I_{go} is a positive value, the upper branch in the current offset compensation block has a positive output while the lower block shows zero value. On the other hand, the lower block has a positive value with a negative I_{go}. The output of the PI estimator I_{go_est}, which is the estimated DC offset, is connected to the current feedback junction and is adjusted to obtain zero at the input of the estimator. As long as the input of the estimator is zero, it is supposed that there is no DC component in d_{pfc}. It means there is no DC offset in the current measurement path. Figure 12b analyzes the open-loop gain of the proposed control loop including the offset compensation algorithm. The duty reference to the inductor current model $G_{id}(s)$ is simply assumed as a first model shown in (21).

$$G_{id}(s) = \frac{V_{dch} + V_{dcl}}{L_g s} \tag{21}$$

Without the offset compensation algorithm, the loop-gain in Figure 12b shows a typical open-loop frequency response of an inductor current model adapting a *PR* controller whose proportional and resonant gains are 0.2 and 500, respectively. The magnitude at the fundamental frequency 60 Hz is evaluated as 200 dB. The phase margin is close to 90 degrees. For the offset compensation algorithm, the controller parameters are selected as ω_b = 62.83 rad/s, $K_{po} = 1 \times 10^{-5}$, and K_{io} = 0.2, respectively. As can be seen in the figure, the DC gain is slightly reduced with the offset compensation algorithm. However, it does not affect the entire control performance, because the operating frequency of the control system starts from 60 Hz.

4. Simulation Results

The simulation model of the module shown in Figure 3 is built in Power SIM 9.0 from Power SIM Corporation to examine the power conversion performance. Table 3 gives the parameters used for the simulation study. Figure 13a shows v_g, v_{inv}, and i_g. At the beginning, the module is operated at the no-load condition. After that, the full load is instantly applied, and the input current i_g increases. As analyzed in Table 1, v_{inv} has total 5 levels. Apparently, the unity PF operation is achieved. Figure 13b shows the plot of the secondary side voltage and the current of the HF transformer, v_{sec} and i_{Lr}. Due to the resonant tank consists of L_r and C_r, the shape of the secondary side current is sinusoidal.

Table 3. Parameters for the simulation.

Power Stage	Parameters	Values
active-front-end (AFE) converter	DC-link capacitance C_{dc}	250 μF
	Filter inductance L_g	10 mH
	Switching frequency f_{s_AFE}	20 kHz
LLC converter	Resonant inductance L_r	16 μH
	Resonant capacitance C_r	1 μF
	HF transformer turn ratio (N_p:N_s)	120:48
	Magnetizing inductance L_m	100 mH
	Switching frequency f_{s_LLC}	40 kHz
	DC-link capacitance C_o	470 μF

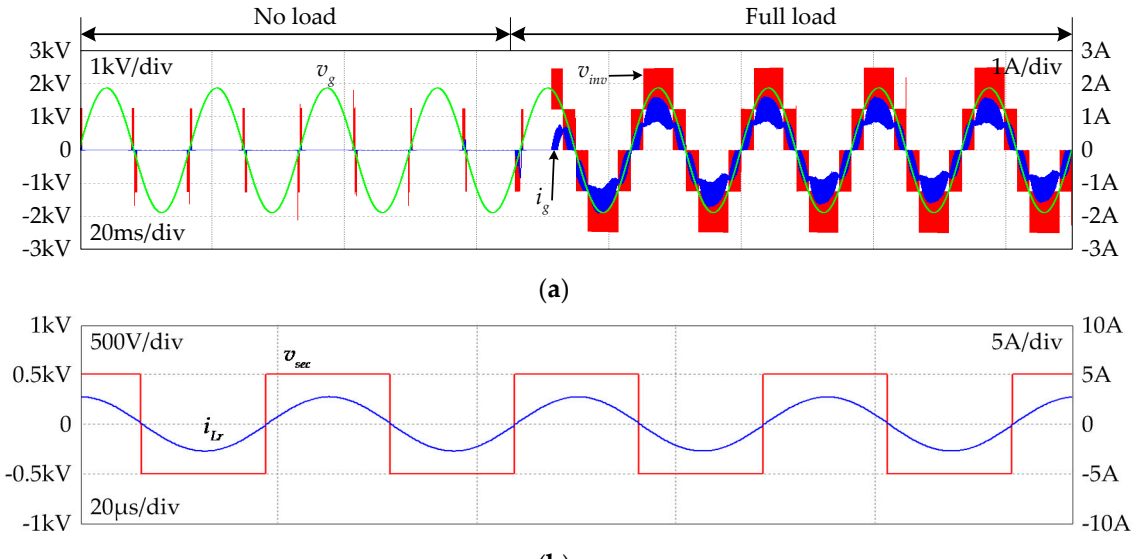

Figure 13. Simulation results. (**a**) v_g, v_{inv}, and i_g in transient state; (**b**) v_{sec} and i_{Lr} in steady-state.

Figure 14 shows the switching waveforms of the MOSFETs in the LLC converter. In the figure, v_{ds_Qc1}, v_{ds_Qc2}, v_{ds_Qc3}, and v_{ds_Qc4} represents the drain to source voltages of the switching devices Q_{c1}, Q_{c2}, Q_{c3}, and Q_{c4}, respectively. As can be illustrated in the figure, the device currents i_{Qc1}, i_{Qc2}, i_{Qc3}, and i_{Qc4} rise after the devices are fully turned on, so that the drain to source voltages are zero. It means zero-voltage-switching (ZVS) is achieved in the individual devices. A merit of LLC converters is high efficiency, which is expected due to the ZVS guaranteed in these devices.

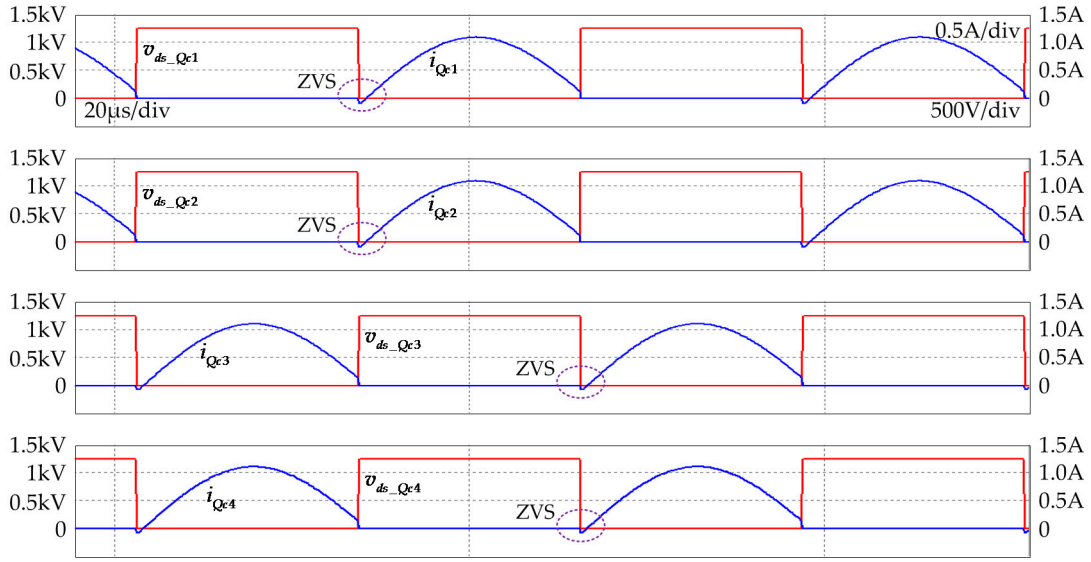

Figure 14. Switching waveforms of the drain to source voltages and the channel current in metal oxide semiconductor field effect transistors (MOSFETs) of the LLC converter.

Figure 15 represents the performance of the proposed offset compensation method. Initially, −0.5 A of current sensing offset is assumed with no compensation. After 3 cycles, the proposed method is applied, and the current offset is eliminated in 4 cycles.

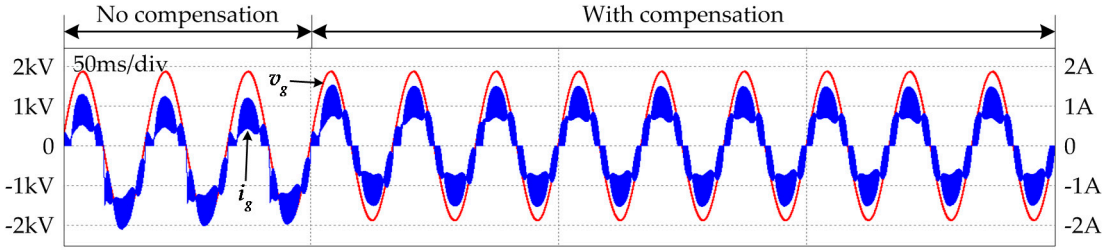

Figure 15. Simulated performance of the proposed offset compensation algorithm.

Since 10 modules are employed in the SST, the simulation with total modules working together has been performed. Figure 16 shows v_{inv} and i_g at the rated power condition 10 kVA. The input voltage is 13.2 kV in rms. With 10 modules, the input voltage has multiple steps due to the interleaved operation among individual modules, so that the input current ripple is significantly reduced. Theoretically, v_{inv} can have 39 steps with the maximum duty cycle. However, it has 31 steps in the simulation, because the duty cycle does not reach the maximum value.

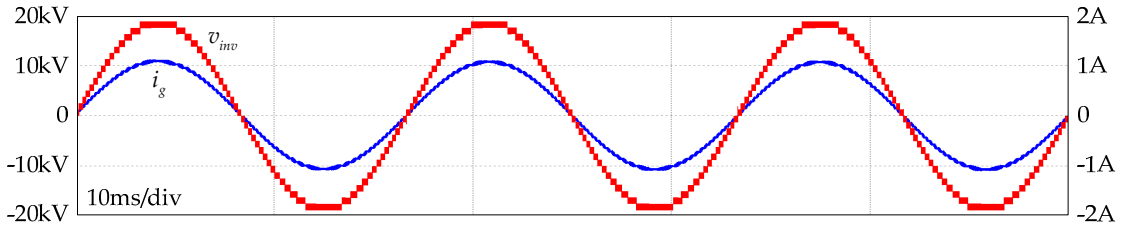

Figure 16. Simulated v_{inv} and i_g with 10 modules.

5. Experimental Results

Figure 17 shows a photograph of the experimental setup for the SST prototype. For the load, a resistor load bank is connected to the output of the power stage. The same parameters represented in Table 3 are utilized. To obtain 13.2 kV AC voltage in the laboratory, two transformers, the variac and the pole transformer, are employed. Since the pole transformer is connected to the output of the variac, variable high voltage can be easily obtained to test the SST prototype. In order to measure the high input voltage, a commercial potential transformer is used. For the AFE and the DC-DC converters, Cree's C2M1000170D MOSFETs and Global Power's GP2D005A170B devices have been utilized. They are both silicon carbide devices, and the switching frequency can be much higher than using traditional silicon devices. By doing so, the physical sizes of the magnetic components can be significantly reduced. Furthermore, a low switching loss is expected. The control structure of the SST contains a global and a local controller. The voltage and current control algorithms are implemented in the global controller using an in-house developed digital control board based on Texas Instruments' TMS320F28335. Since the number of the pulse-width-modulation channel in the digital controller is not enough to cover the SST system, which requires 80 channels, the local controllers using TMS320F28035 are equipped in the individual 1.32 kV/1 kVA modules. The local controllers receive the duty reference from the global controller, and they generate interleaved modulation signals. The communication between the global and the local controllers is realized through the optic connected serial peripheral interface buses. The SST was tested at the full load condition, 10 kVA.

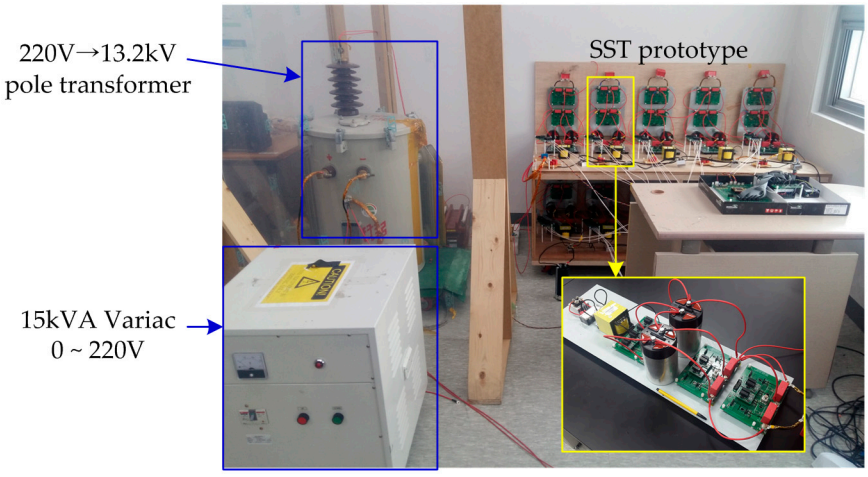

Figure 17. Experimental setup photograph.

Figure 18 demonstrates the switching voltage and the input current of the single AFE converter where the input voltage is 1.32 kV. As analyzed in the previous section, the switching voltage of the AFE converter has five steps. The input current has a significant current ripple, but the power factor is close to the unity. The switching voltage and the input current of the AFE stage with two cascaded

modules are shown in Figure 19. The input voltage is 2.6 kV at this condition. Due to the interleaved operation of the two modules, the input current ripple is considerably reduced. Through Figures 18 and 19, it can be recognized that the simulation results performed in the earlier section are well matched with the experimental results.

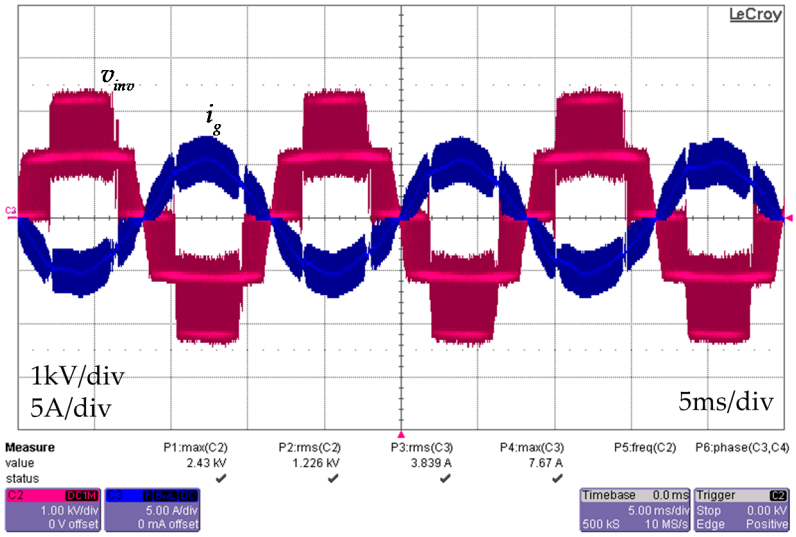

Figure 18. The switching voltage and the input current of the single AFE converter.

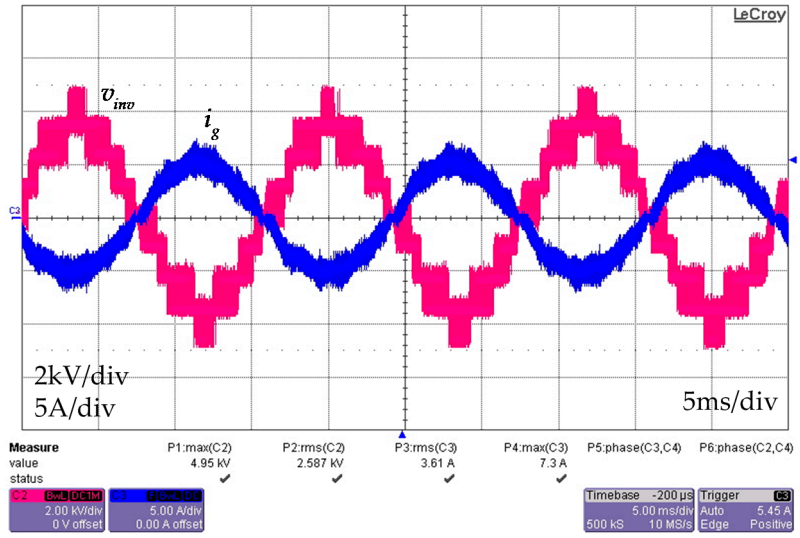

Figure 19. The switching voltage and the input current of the AFE converter cascaded in two modules.

Figure 20 shows v_{inv} and i_g when total 10 modules are operated under 13.2 kV input voltage. Since v_{inv} has multiple steps, which was confirmed in the simulation, its shape is close to sinusoidal. Compared to the previous results, the ripple in the input current is considerably mitigated. Note that the input current offset I_{go} is existent in the result due to the current measurement offset caused by the non-ideal characteristics of the signal conditioning circuit. In Figure 21, the proposed offset compensation algorithm is applied, so that the current offset I_{go} is eliminated.

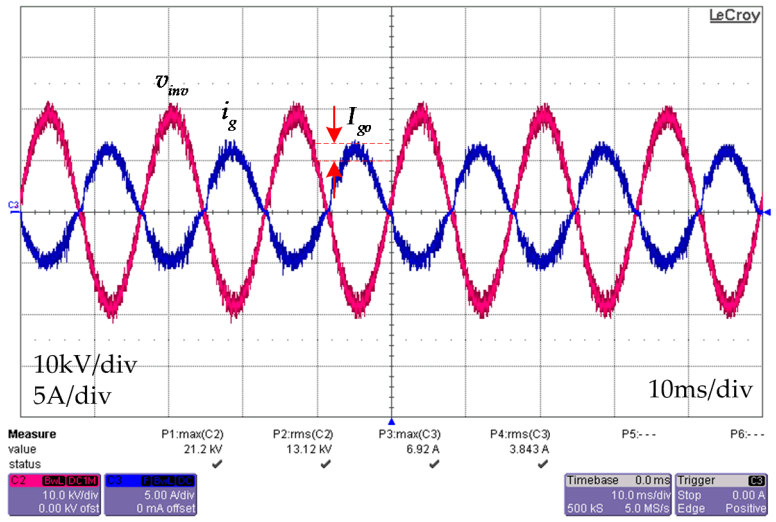

Figure 20. The switching voltage and the input current of the AFE converter cascaded in 10 modules with a current offset.

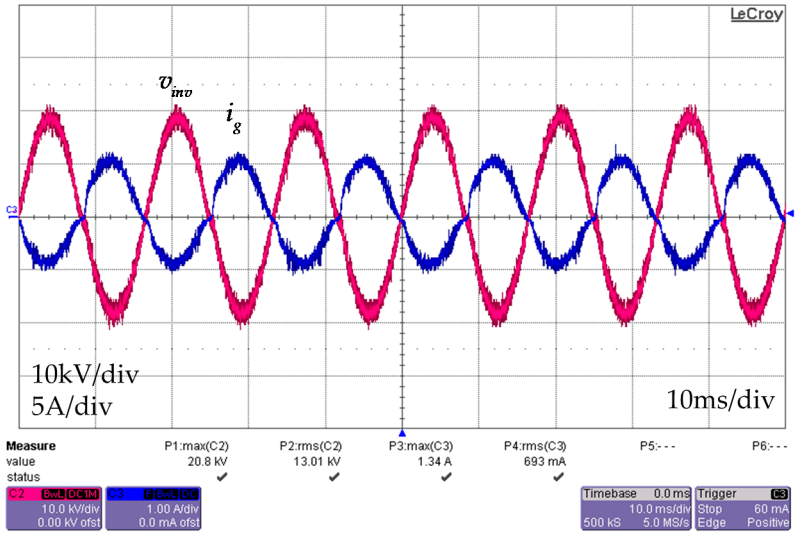

Figure 21. The switching voltage and the input current of the AFE converter cascaded in 10 modules with the proposed offset compensation algorithm.

Figure 22 shows the switching voltages and currents of the primary and the secondary sides of the HF transformer in the LLC resonant converter under 10 kVA operation. Since total 10 modules are employed, the output power of the LLC resonant converter is only 1 kW. From the figure, it is supposed that the soft-switching operation has occurred.

Figure 23 shows the thermal simulation of the power stage under 30 percent load with 2 h operating condition. In order to perform the thermal analysis, ANSYS R16.2 academic version is utilized. The ambient temperature is given as 20 degrees Celsius, and a natural cooling is assumed. The maximum temperature is measured as 36.8 degrees Celsius on the diodes. Although it is hard to sense the efficiency accurately, it is supposed that the power stage loss is not very high even under the high frequency hard switching condition.

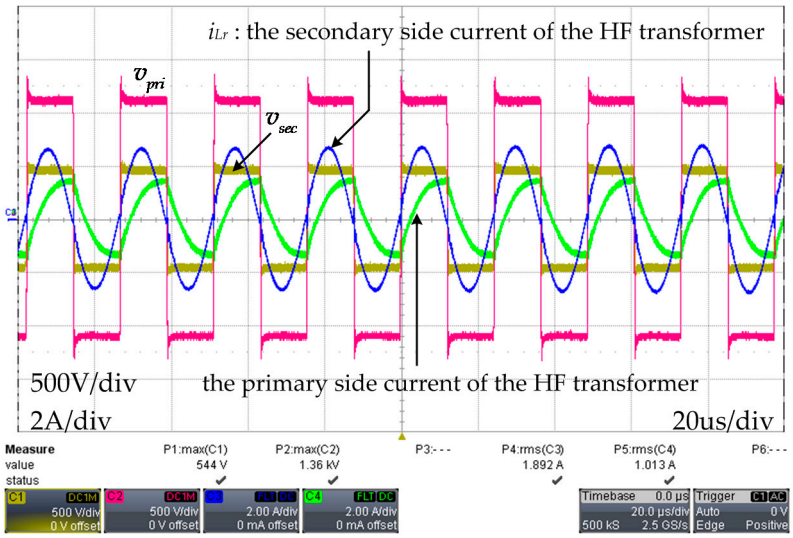

Figure 22. Experimental waveforms of an LLC resonant converter.

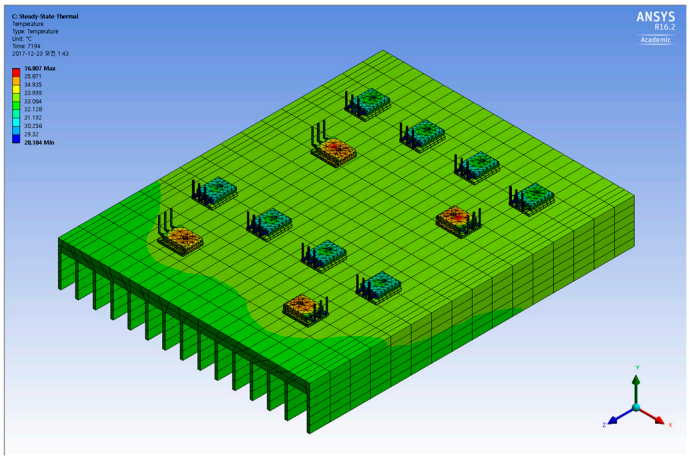

Figure 23. Thermal simulation of the power stage during the operation.

6. Conclusions

This paper describes the design and the control of the 10 kVA SST for 13.2 kV/220 V power distribution system. The proposed SST consists of the cascaded multi-level AFE converters, the isolated DC-DC converters, and the load inverter. The operations, the modulation strategies, and the control of the individual and the entire stages have been explained. In addition, the input current offset compensation method has been proposed to eliminate a potential current offset in the AFE stage. Since the SST can actively regulate the input current, the unity power factor with a low THD is achieved even under a nonlinear or a reactive load condition. On the other hand, the SST is able to supply a very well-regulated output voltage to the load under an input voltage sag or swell condition as long as the energy stored in the DC-links is enough to supply during transients. In order to verify the proposed structure, the 10 kVA SST has been built and tested. Through the experiments in the practical 13.2 kV AC grid, it is confirmed that the proposed SST can perform the power conversion between the 13.2 kV and the 220 V lines, so that it can be utilized as an alternative power distribution transformer in the grid.

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Author Contributions: Jeong-Woo Lim implemented the system, and performed the experiments. Younghoon Cho provided the idea, and managed the paper. Han-Sol Lee and Kwan-Yuhl Cho assisted the idea development and the paper writing.

Conflicts of Interest: The authors declare no conflict of interest.

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