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Standby-Loss Elimination in Server Power Supply †

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Abstract: In a server power system, a standby converter is required in order to provide the standby output, monitor the system's status, and communicate with the server power system. Since these functions are always required, losses from the standby converter are produced even though the system operates in normal mode. For these reasons, the losses deteriorate the total efficiency of the system. In this paper, a new structure is proposed to eliminate the losses from the standby converter of a server power supply. The key feature of the proposed structure is that the main direct current (DC)/DC converter substitutes all of the output power of the standby converter, and the standby converter is turned off in normal mode. With the proposed structure, the losses from the standby converter can be eliminated in normal mode, and this leads to a higher efficiency in overall load conditions. Although the structure has been proposed in the previous work, very important issues such as a steady state analysis, the transient responses, and how to control the standby converter are not discussed. This paper presents these issues further. The feasibility of the proposed structure has been verified with 400 V link voltage, 12 V/62.5 A main output, and a 12 V/2.1 A standby output server power system.

Keywords: phase-shifted full-bridge converter; standby flyback converter

1. Introduction

Nowadays, in order to reduce power consumption in internet data centers, it is prompted to increase the efficiency of a server computer power system. Because the brand-new certification requires extremely high efficiency at a 50% load condition, very sophisticated techniques are required. Also, the efficiency under a light load condition is getting more important in the server power system, because the brand-new certification requires meeting 10% load efficiency, whereas the former certification does not [1–3].

As shown in Figure 1, a server power system consists of a boost power-factor-corrector (PFC), direct current (DC)/DC, and standby converter stage. The boost PFC stage provides the input voltage of the DC/DC stage (V_{link}). The DC/DC stage provides tightly regulated output voltage (V_{out_main}). In this stage, a phase-shifted full-bridge (PSFB) converter is widely used because of small root-mean-square (RMS) current and zero-voltage-switching (ZVS) [3–7].

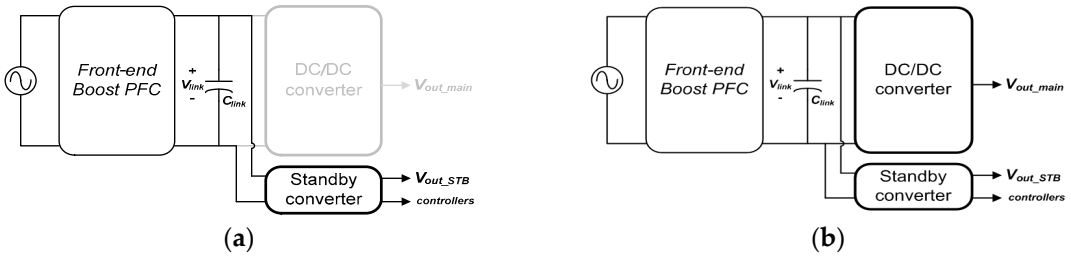


Figure 1. Operating modes of a server power system with conventional structure in (**a**) standby mode and (**b**) normal mode. PFC, power-factor-corrector; DC, direct current.

In order to improve the light load efficiency, various techniques have been proposed by researchers [8–11]. Among these techniques, [5,8] achieved higher efficiency simply by using a larger dead time to achieve ZVS in a light load condition, because a PSFB converter cannot provide sufficient ZVS energy in light load conditions [12–14]. These previous works have reduced the switching losses in light load conditions. However, removing switching losses shows improved efficiency only lower than a 10% load condition, as shown in [12–14]. This is because, with the optimized dead time, the lagging leg switches can be turned on when the drain-to-source voltage is at minimum. From the research, it can be noted that the switching losses rarely affect the system's efficiency in higher than 10% load conditions, although the ZVS energy is not sufficient for the full ZVS.

Figure 2 illustrates a simplified schematic of the standby converter and controllers. The standby converter provides standby output (V_{out_STB}) and supply voltage for the controllers. The purpose of the V_{out_STB} is to provide the output power to the server power system in the "standby state". The output power of V_{out_STB} is much smaller than the main output power. Usually, the standby output power is less than 30 W. This is because the standby output is used to maintain communication between the server power system and the power supply. Also, the secondary controller consumes a very small amount of power, such near 1 W. A microcontroller for communication and sequence control is powered by V_{out_STB}. The server system should monitor its state always, even when the main power is turned off. In this case, only a small output power is required to monitor the system status, so only the standby flyback converter with a small output power rating provides the standby output power. For the standby output, the flyback converter is widely used because of its small size and wide input-range capability [15–18]. Since V_{out_STB} should be regulated tightly, it is used for the feedback of the duty cycle of the standby converter. V_{out_STB} is used for the standby output and the input power of the controllers on the secondary side. Also, the standby converter provides the input power of the controllers on the primary side. As shown in Figure 2, the auxiliary turns are used for the primary side controllers. Due to cross-regulation issues, the supply voltage for the primary side controllers (V_{CCP}) cannot be regulated tightly, and V_{CCP} increases from 13 V to 20 V in a light load condition. For these reasons, a linear regulator is used to provide an accurate 12 V (V_{12P}) to the primary controllers. The loss of a linear regulator increases as V_{CCP} increases, because it is proportional to the difference between V_{CCP} and 12 V. Please note that the pulse-width-modulation (PWM) controller on the primary side cannot use V_{out_STB} as its power source, because V_{out_STB} is located on the secondary side. The primary side and the secondary side of the server power system should be isolated. As shown in Figure 2, V_{out_STB} and V_{12P} have different ground notation from each other [18].

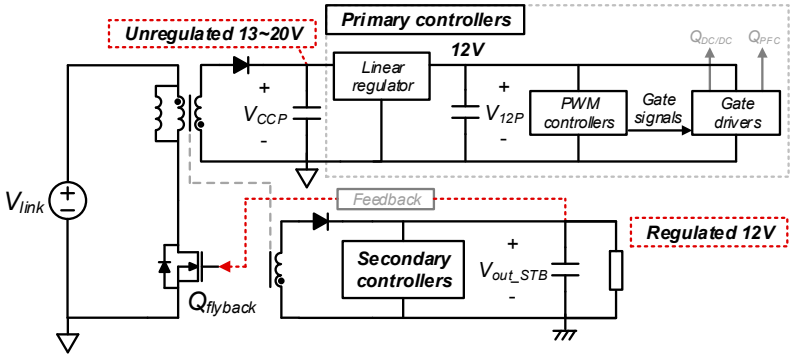


Figure 2. Simplified schematic of the standby flyback converter and controllers.

Figure 1a,b illustrates the standby mode and the normal mode of a server power supply. In the standby mode as shown in Figure 1a, only the standby converter is turned on, and the DC/DC converter is turned off. Therefore, V_{out_STB} and V_{CCP} are provided by the standby converter and V_{out_main} is zero. In the normal mode as shown in Figure 1b, the DC/DC converter is turned on and all outputs are provided. It should be noted that the losses of the standby flyback converter always exist regardless of operating mode. Therefore, the standby converter degrades the total system's efficiency in entire load conditions [15–20]. Therefore, it is required to reduce the losses from the standby flyback converter. Furthermore, V_{CCP} increases in a light load condition due to the cross-regulation problem, and the losses from the linear regulator are also increased in a lighter load condition.

For these reasons, standby-flyback-integrating structures have been studied in recent years [15–20]. By integrating the flyback converter into the main power conversion stage, these works reduced switching losses, resulting in the improved efficiency of the system. However, approaches in [15–17] require additional components and complex control signals. Also, the core loss of the flyback converter is always produced. Therefore, among the previous approaches, using an ORing diode [19,20] can be the simplest way to reduce the standby converter losses in applications where the V_{out_main} and V_{out_STB} are the same. However, just using an ORing diode [20] cannot eliminate the losses from the flyback converter. This is because the standby flyback converter should provide V_{CCP}.

In order to completely eliminate the losses from the standby converter in the normal mode, [19] proposed to turn off the standby converter. By using an ORing diode and an auxiliary winding, all outputs from the standby converter are provided by the DC/DC converter. Therefore, the standby converter can be turned off so that the standby losses can be eliminated. However, very important issues such as a steady state analysis, the transient responses, and how to control the standby converter are not discussed in [19]. In this paper, further analysis on the technique is presented.

2. The Proposed Structure and Its Control Scheme

The proposed structure is shown in Figure 3a. The PFC boost converter is omitted for simplicity, and it is assumed that the DC/DC converter has a constant input voltage (V_{link}). In order to provide V_{out_STB} and supply voltage for the primary side controllers (V_{CCP}), the DC/DC converter uses a merging diode (D_m), a small additional diode (D_a), and an auxiliary winding in the main transformer (N_{aux}) is used. The main purpose of the proposed structure is to turn off the standby flyback converter. In this case, V_{out_STB} cannot be provided without D_m. D_m is used to connect V_{out_main} to V_{out_STB}, so that V_{out_STB} can be provided even in the case where the standby flyback converter is turned off.

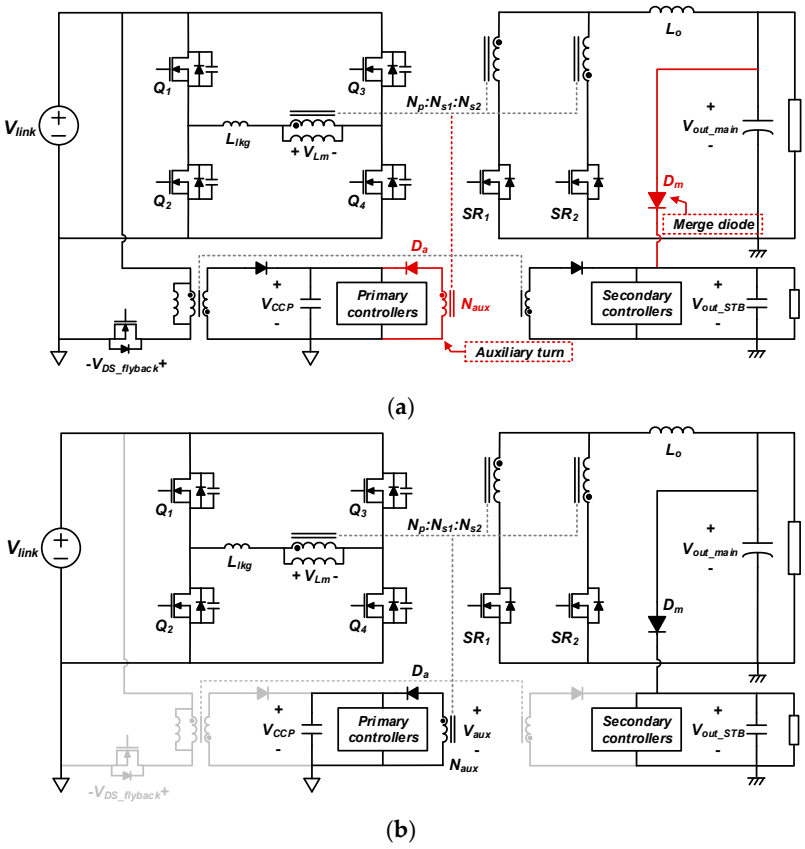


Figure 3. Schematics of (**a**) the proposed structure and (**b**) operation in normal mode.

The secondary side controllers can also be powered by another additional winding. However, please note that the secondary side controllers do not need to be powered by the auxiliary winding, because the main output voltage is the same as the standby output voltage. Also, since V_{out_STB} should be regulated tightly, it is better to share the main output voltage. When another auxiliary winding is used, another additional regulator should be used in order to regulate V_{out_STB}, since the auxiliary winding cannot provide an exact voltage level.

In standby mode, the proposed structure operates the same as the conventional structure. The flyback converter provides V_{out_STB} and V_{CCP}. The PSFB converter is turned off, since V_{out_main} has to be zero.

However, in the normal mode as shown in Figure 2b, the flyback converter can be completely turned off after the PSFB converter is turned on. It can be noted that all of the outputs of the standby converter can be provided by the PSFB converter with the proposed structure. V_{out_main} provides V_{out_STB} using D_m. Because the output current specification of the PSFB is much larger than that of the standby flyback converter, it is not a burden for the PSFB converter. Also, N_{aux} provides V_{CCP} using D_a.

2.1. Steady State Operation of the Proposed Structure in Normal Mode

Figure 4a shows a simplified equivalent circuit for V_{CCP}. As shown in Figure 4a, a parasitic resistance of auxiliary turn (R_{par}) and the reflected leakage inductance ($(N_{aux}/N_p)^2 L_{lkg}$) are connected in series with D_a, and the primary controllers can be regarded as a constant load current (I_{con}).

Figure 4b shows the key waveforms of the proposed structure. As shown in Figure 4b, voltage across the magnetizing inductance of the main transformer (V_{Lm}) alternates between V_{link} and $-V_{link}$. Then, the voltage across the auxiliary winding (V_{aux}) alternates between $V_{link}N_{aux}/N_p$ and $-V_{link}N_{aux}/N_p$. Because D_a rectifies only a positive half cycle of V_{aux}, V_{CCP} increases during t_0–t_1.

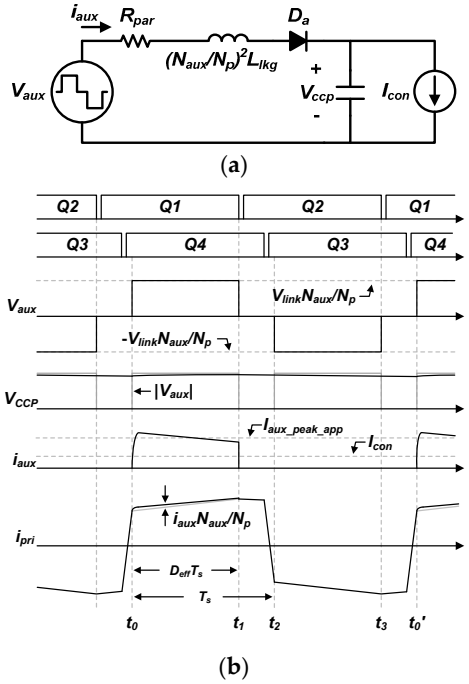


Figure 4. (**a**) Simplified equivalent circuit for V_{ccp}; (**b**) key waveforms of the proposed structure in normal mode.

The auxiliary circuit operates as a resistor-inductor-capacitor (RLC) resonant circuit. However, the inductance can be neglected because N_p is much larger than N_{aux} in the PSFB converter. In this case, the circuit in Figure 4a can be regarded as a switched capacitor circuit. The peak value of i_{aux} ($I_{aux\_peak\_app}$) is determined by R_{par}. Assuming that the resistor-capacitor (RC) time constant of the circuit is much larger than the switching period of the PSFB, i_{aux} can be considered as a square waveform wave and its average value becomes I_{con}. For these reasons, V_{CCP} and $I_{aux\_peak\_app}$ can be obtained by following Equations:

$$V_{CCP} \cong \frac{N_{aux}}{N_p} V_{link} \tag{1}$$

$$I_{aux\_peak\_app} = \frac{I_{con}}{D_{eff}} \tag{2}$$

where D_{eff} is an effective duty-cycle in the PSFB converter.

N_{aux} should be chosen to make V_{CCP} larger than required voltage for the primary side controllers. A linear regulator can be used to provide a precise voltage for the controllers, following V_{CCP}. In order to minimize the losses in the linear regulator, N_{aux} should be minimized, satisfying the condition that V_{CCP} should be larger than the required voltage for the controllers.

From (1), it should be noted that V_{CCP} becomes constant regardless of the output condition with the proposed structure, whereas V_{CCP} increases in a light load condition with the conventional structure, as mentioned in the introduction. Therefore, the losses from the linear regulator are also reduced in the proposed structure.

In the proposed structure, the primary current of the PSFB converter (i_{pri}) is equal to the sum of $i_{aux}N_{aux}/N_p$ and the primary current in the conventional PSFB converter. However, i_{pri} is almost same as the conventional PSFB converter; I_{con} is usually very small (much smaller than 1 A), and stepped down by the turns ratio N_{aux}/N_p. For these reasons, the proposed structure rarely affects the operation of the PSFB converter, so that the steady state characteristics of PSFB converter, such as the ZVS condition or effective duty cycle, are not affected.

2.2. N_{aux} and D_m Selection

V_{CCP} should be larger than V_{12P}. This is because the linear regulator has a step down conversion ratio, so N_{aux} should be large enough. On the other hand, in order to minimize the losses in the linear regulator, V_{CCP} should be as small as possible. Therefore, N_{aux} should be the minimum value satisfying $V_{CCP} > V_{12P}$. According to (1), it can be noted that N_{aux} should be an integer value which is larger than $N_p V_{12P}/V_{link}$.

In order to select D_m, consideration on the forward voltage drop of the merge diode is essential. The voltage regulation range of the server power supply is ±5% of the output voltage in this case. Therefore, the forward voltage drop should be smaller than its regulation range. The forward voltage drop of D_m should be smaller than its regulation range in the full load condition.

2.3. How to Disable the Standby Flyback Converter

The standby flyback converter can be disabled with a simple addition to the feedback circuits. Figure 5 shows the feedback circuit of the standby converter for the proposed structure. In the figure, the left side of the feedback circuit is for the conventional structure and the right side of the feedback circuit is proposed for the proposed structure. The added feedback circuit consists of an additional resistor R_a, diode D, and transistor Q_a, which is controlled by the STB_{VAR} signal. In standby mode, Q_a is turned on so that D is turned off. The additional circuits do not affect the feedback circuit, since the additional circuits are separated from the conventional feedback circuit. However, in normal mode, Q_a is turned off and D is conducted. Since R_a is connected to R_1 in parallel and the reference voltage of the control loop becomes smaller, the feedback circuit operates as if V_{out_STB} is larger than its appropriate value. In other words, the standby flyback converter is turned off.

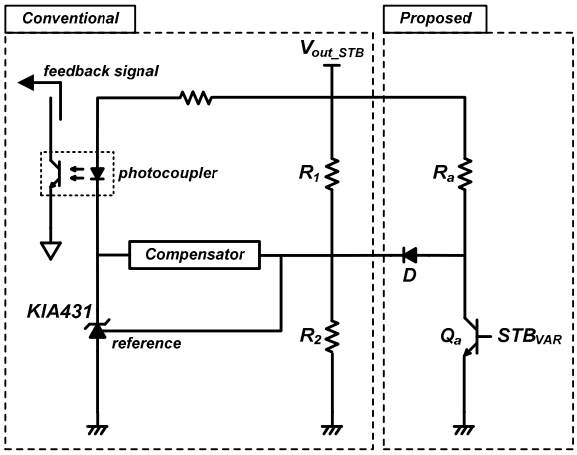


Figure 5. Feedback circuit of the standby converter for the proposed structure.

2.4. Transient Response When Disabling the Standby Converter

In the proposed structure, considerations on transient response are essential, since the flyback converter is turned on and off during its operation. Figure 6 shows the disabling sequence for the standby flyback converter in normal mode. After the DC/DC converter is turned on, V_{out_main} increases. The standby flyback converter should be turned off after V_{out_main} is regulated. Otherwise, V_{out_STB} will drop to V_{out_main}. Therefore, the STB_{VAR} signal should be low after V_{out_main} is regulated. In the proposed structure, the reference voltage is $2.5(1 + R_1/R_2)$ when the STB_{VAR} signal is high. However, when the STB_{VAR} signal becomes low, Q_a is turned off and the reference voltage of the controller loop becomes $2.5[1 + (R_1//R_a)/R_2]$. Therefore, the reference voltage decreases, and the expected value of V_{out_STB} without a merge diode is $2.5[1 + (R_1//R_a)/R_2]$.

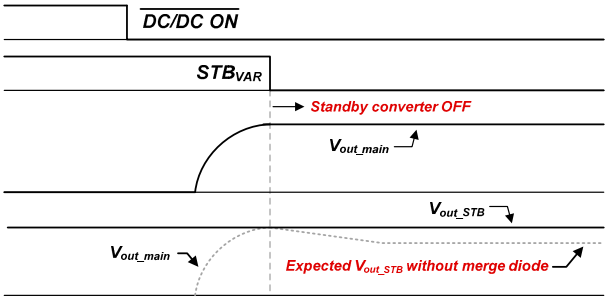


Figure 6. Disabling sequence for the standby flyback converter in normal mode.

2.5. Transient Response When Enabling the Standby Converter

There are two cases of shutdown in a server power supply. The first one is the DC/DC OFF case. In this case, the power system transits from the normal to the standby mode. Figure 7a illustrates the DC/DC OFF case. Note that the DC/DC ON signal is active and low. The server computer requests DC/DC OFF and the DC/DC converter is turned off. After DC/DC OFF is requested by the server, the STB_{VAR} signal is enabled and the standby converter wakes up before the DC/DC converter is turned off.

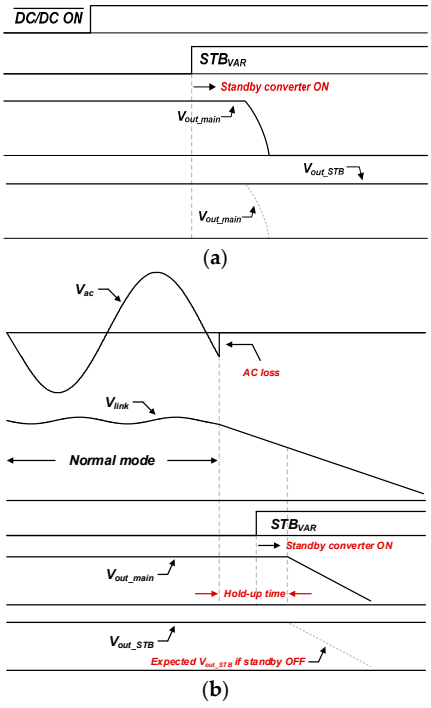


Figure 7. Enabling sequence for the standby flyback converter in shutdown cases (**a**) DC/DC OFF; (**b**) hold-up time. AC, alternating current.

The second one is the hold-up time. In general, a server power system should be able to regulate V_{out_main} after the alternating current (AC) loss for tens of milliseconds, and it is called the hold-up time condition. During the hold-up time, the standby flyback converter should be enabled before V_{out_main} decreases. Figure 7b illustrates the key waveforms during the hold-up time. After AC loss occurs, V_{link} decreases and the PSFB converter regulates V_{out_main}. After the hold-up time, V_{out_main} decreases. The standby converter should be turned on within the hold-up time after the AC loss, so that V_{out_STB} can be regulated by the standby converter even though V_{out_main} decreases. If the standby converter is not turned on during the hold-up time, V_{out_STB} should be decreased in the same way as V_{out_main}.

2.6. Control of the STB_{VAR} Signal

Figure 8 shows a flowchart for the STB_{VAR} signal. When the standby flyback is turned on, the system checks V_{out_main}. If V_{out_main} maintains at 12 V during a waiting time (T_w), the STB_{VAR} signal is disabled to turn off the flyback converter. When the flyback is turned off, the system checks whether DC/DC OFF or any shutdown signals are produced. If the conditions are produced, the STB_{VAR} signal is enabled so that the flyback is turned on immediately. The pre-existing microcontroller is fast enough to provide the STB_{VAR} signal in time.

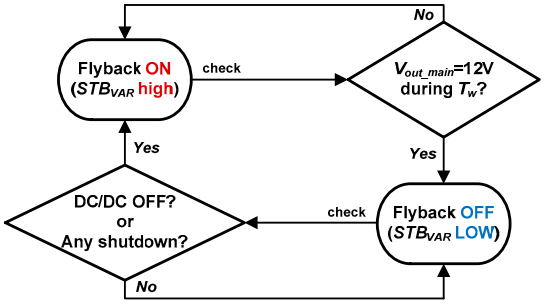
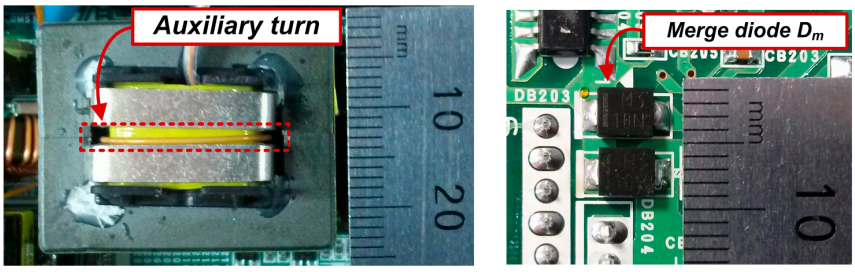


Figure 8. Flowchart for STB_{VAR}.

3. Experimental Results and Discussion

The feasibility of the proposed structure has been verified by a server power system with 12 V/62.5 A main output and 12 V/2.1 A standby output. The system is designed with N_p = 26, N_{s1} = N_{s2} = 1, N_{aux} = 1, and L_{lkg} = 15 µH. ES1D (200 V, 1 A, DO-214AC) is selected for D_a, M2FM3 (30 V, 6 A, M2F) is selected for the merge diode D_m, and ICE3AR0680JZ is selected for the standby flyback converter. The voltage regulation range of the server power supply is ±5% of the output voltage in this case. Therefore, V_{out_main} and V_{out_STB} should be regulated within 11.4–12.6V. Since the forward voltage drop of D_m is less than 0.4 V as the maximum value, it can be said that the forward voltage drop of the merge diode does not affect the regulation of V_{out_STB}. Figure 9 shows the implementation of the proposed structure. It can be noted that the auxiliary turn occupies a very small window area, so that it does not affect the design of the transformer. In addition, the merging diode D_m is very small so that the power density of the total system is not degraded.



(**a**) (**b**)

Figure 9. Implementation of the proposed structure (**a**) the auxiliary turn in main transformer; (**b**) ORing diode.

Figure 10 shows the experimental waveforms of the proposed structure at full load condition in normal mode. Figure 10a shows the disabling sequence of the standby flyback converter. $V_{DS\_flyback}$ represents the drain-to-source voltage of the main switch of the standby flyback converter. When the standby flyback converter is turned on, $V_{DS\_flyback}$ alterantes between zero and its peak value. In order to present the sequence clearly, the time division of the waveforms is set to 500 ms/div. Because the

switching period of the standby converter is much shorter than the division, $V_{DS\_flyback}$ occupies the black area in the figure when the standby converter is turned on. Negative *DC/DC ON* represents the control signal for V_{out_main} provided by the server system. Note that the signal is active and low, so that the LOW signal means that the server system commands the DC/DC converter to be turned on, and the HIGH signal means the system commands the DC/DC converter to be turned to OFF. Generally, one or two seconds are enough for the building/collapsing time after the DC/DC controlling signal is applied, although the time depends on the power supply vendor. As shown in Figure 10a, after *DC/DC OFF* becomes low, the DC/DC converter is turned on and V_{out_main} increases. After V_{out_main} is regulated, the STB_{VAR} signal becomes low to turn off the standby converter. Figure 10b,c shows the waveforms for V_{aux}, V_{CCP}, i_{pri}, and i_{aux} in a full load condition after the standby converter is turned off. V_{CCP} is provided by N_{aux} as shown in Figure 10b. N_{aux} provides 14 V of V_{ccp} so that the primary controllers can operate with 12 V input voltage, following a linear regulator. In the proposed structure, as shown in Figure 10c, i_{pri} of the PSFB converter is almost the same as that of the conventional one as mentioned before. Therefore, it can be noted that the proposed structure does not affect the efficiency of the PSFB converter.

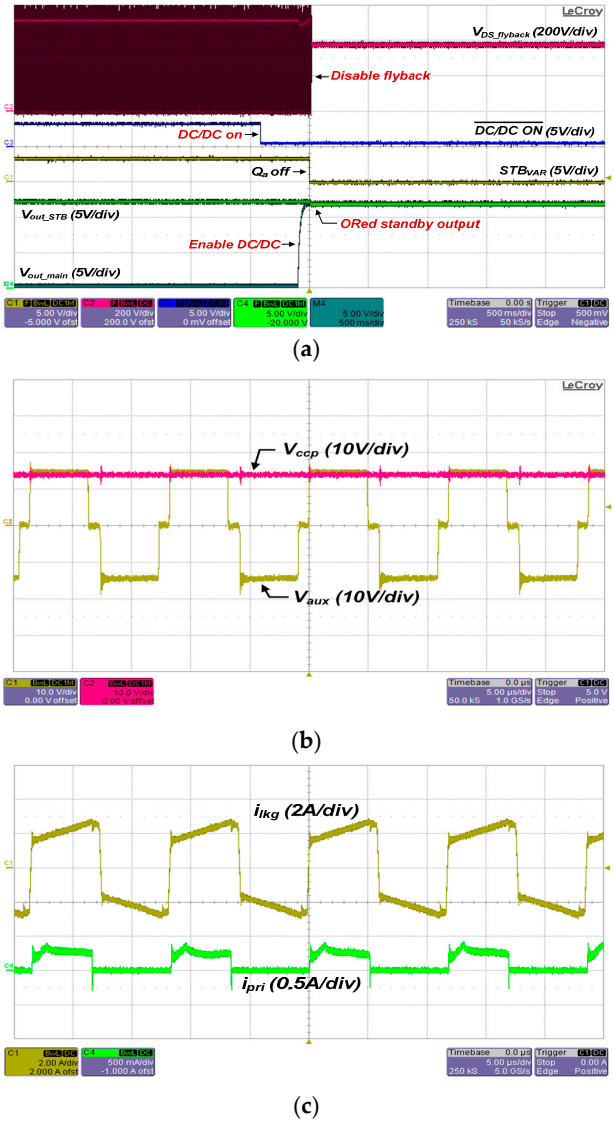


Figure 10. Experimental waveforms of the proposed structure at full load condition (**a**) disabling the standby flyback converter; (**b**) V_{aux} and V_{ccp}; (**c**) i_{lkg} and i_{aux} in normal mode.

Figure 11a illlustrates the experimental waveforms in the DC/DC OFF case. When the *DC/DC OFF* signal is applied, the STB_{VAR} signal is enabled and the standby converter wakes up to provide V_{out_STB}, and then the PSFB converter is turned off and V_{out_main} is zero while V_{out_STB} is adequately provided.

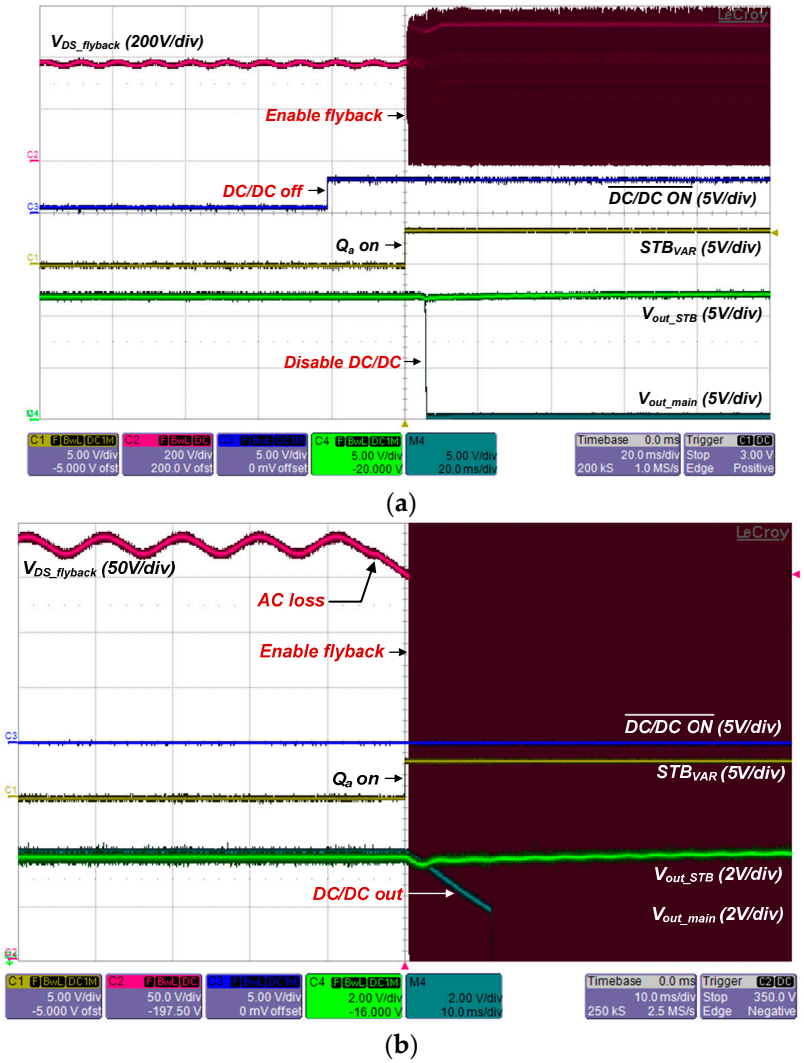


Figure 11. Experimental waveforms during shutdown transition at full load condition (**a**) DC/DC off; (**b**) hold-up time transition.

Figure 11b shows the waveforms during the hold-up time. After AC loss occurs, V_{link} decreases and the STB_{VAR} signal becomes high to turn on the standby converter. The standby converter is turned on before V_{out_main} decreases, so that V_{out_STB} can be stable during the full load transition.

Figure 12a,b shows the measured loss from the standby converter with the conventional structure (only the ORing diode has been implemented) and the efficiency of the proposed structure, respectively. From Figure 12a, it can be noted that the standby converter produces about 1.5 W of losses in entire load conditions. Furthermore, due to the cross regulation problem of the flyback converter, the losses from the standby stage are larger than 1.5 W. The standby converter is designed to have the boundary between the continuous conduction mode (CCM) and the discontinuous conduction mode (DCM) near 60% load condition. In a higher than 70% load condition, the flyback converter operates in continuous conduction mode (CCM). The flyback converter in DCM operation operates with valley switching. On the other hand, the flyback converter in CCM operates with full hard switching. Since the standby converter has higher switching loss in CCM operation, the standby converter has larger

losses in a higher than 70% load condition. In the proposed structure, since the PSFB converter provides all outputs of the standby flyback converter with much higher efficiency, the system efficiency increases in the entire load condition, as shown in Figure 12b. It should be noted that the efficiency is improved in entire load conditions, and the efficiency improvement is larger than the losses from the standby converter, since the proposed structure also reduced the losses from the linear regulator on the primary side.

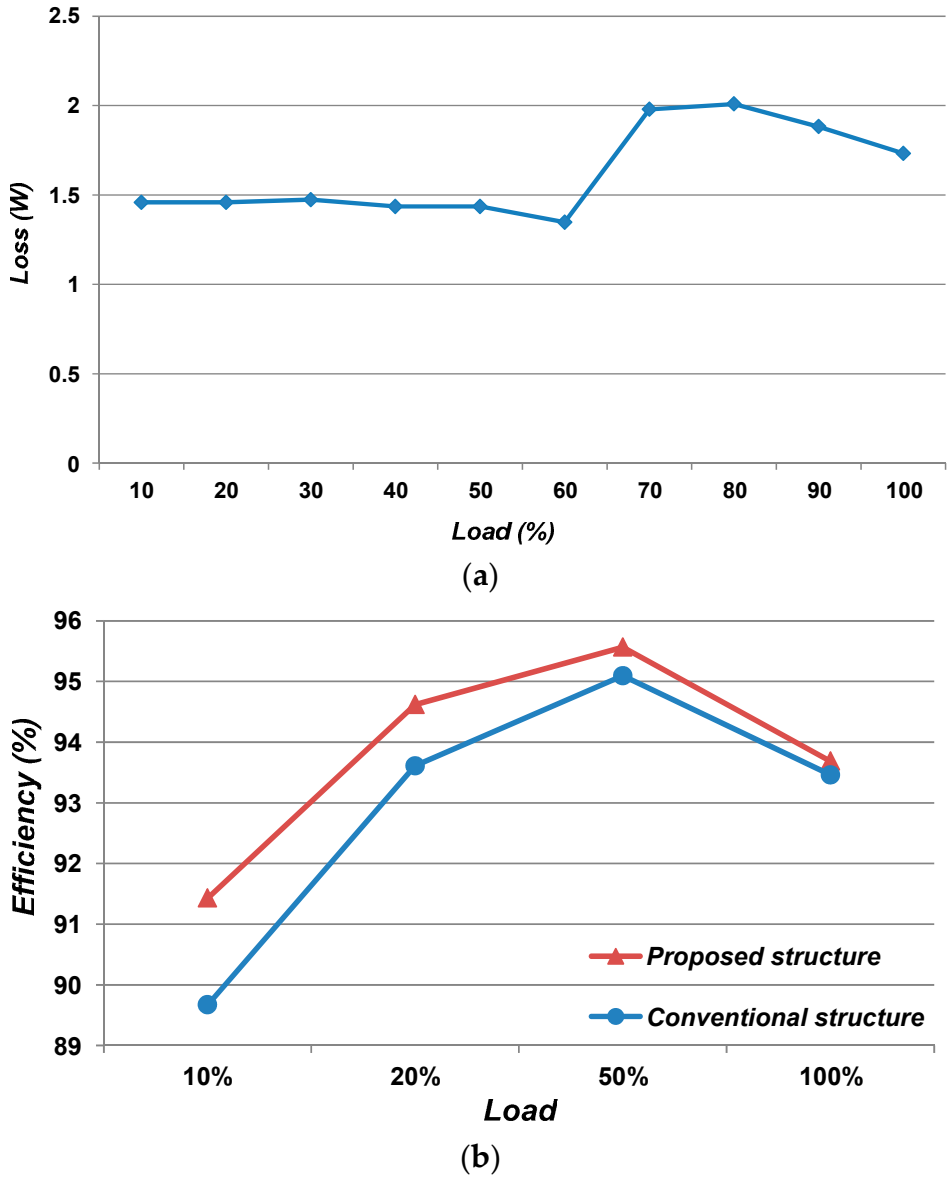


Figure 12. (**a**) Measured loss from the standby converter with conventional structure (ORing diode [20]) and (**b**) efficiency of the proposed structure (V_{link} = 400 V).

Table 1 represents the comparison of loss components between the proposed work and the previous works in normal mode operation. As shown in the table, it can be noted that the previous works [15–17] have a switch, transformer, and rectifier diode as the loss components related to V_{out_STB} in normal mode operation. On the other hand, the proposed structure has only two merge diodes (D_a, D_m) as the loss components in normal mode operation, because the standby converter is in the off-state by STBvar. That is, the losses in the previous works have not occurred in the proposed standby

structure. Therefore, it can be said that the proposed structure can achieve a higher efficiency compared to the previous works.

Table 1. Comparison of loss components in normal mode operation.

Items	[15]	[16]	[17]	Proposed Work
Loss components related to V_{out_STB} in a normal mode	A main switch A transformer Rectifier diodes	A main switch A transformer Rectifier diodes	An additional switch A transformer Rectifier diodes	Two merge diodes (D_a, D_m)

4. Conclusions

In this paper, a new structure to eliminate the losses from the standby converter is proposed for a server power supply. By using a simple multi-output structure, the losses of the standby flyback converter are completely eliminated by disabling it in normal mode. The proposed structure is powerful in that it uses a small number of additional components and can be implemented with a simple control scheme, without changing the normal operation of the PSFB converter, such as the zero-voltage-switching (ZVS) mechanism and the primary side currents. Therefore, the proposed structure is simple and effective for improving the efficiency of a server power system.

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Nomenclature

Vac	AC voltage
Vlink	DC-link voltage or input voltage of DC/DC converter in a server power system
Vout_main	Output voltage of DC/DC converter in a server power system
Vout_STB	Standby output in standby flyback converter
VCCP	Unregulated supply voltage for primary side controllers
V12P	Regulated supply voltage for primary side controllers
V_{aux}	Voltage across additional auxiliary winding (N_{aux}) of the transformer in DC/DC(PSFB) converter
$V_{DS\_flyback}$	Drain-to-source voltage of the main switch($Q_{flyback}$) in the standby(flyback) converter
$Q_{DC/DC}$	Switches in DC/DC converter or Q_1-Q_4 in Figure 3
Q_{PFC}	Switch in boost power-factor-corrector(PFC) in a server power system
$Q_{flyback}$	Main switch in standby(flyback) converter
Q_a	Additional transistor in the feedback circuit for the proposed standby structure
SR_1, SR_2	Switches for synchronous rectifier in DC/DC(PSFB) converter
D_a	ORing diode for the connection between V_{CCP} and V_{aux}
D_m	Diode for the connection between *Vout_STB* and *Vout_main*
D	Additional diode in the feedback circuit for the proposed standby structure
N_p	Primary windings of the transformer in DC/DC(PSFB) converter
N_{s1}, N_{s2}	Secondary windings of the transformer in DC/DC(PSFB) converter
N_{aux}	Additional auxiliary winding of the transformer in DC/DC(PSFB) converter
R_{par}	Parasitic resistance of N_{aux}
R	Additional resistor in the feedback circuit for the proposed standby structure
R_1, R_2	Resistors in the feedback circuit for the standby converter
L_{lkg}	Leakage inductance of the transformer in DC/DC(PSFB) converter

i_{aux}	Current flowing through N_{aux}
I_{con}	Current required in the primary side controllers
$I_{aux\_peak\_app}$	Peak current in i_{aux}
i_{pri}, i_{lkg}	Current flowing through N_p in DC/DC(PSFB) converter.
D_{eff}	Effective duty-cycle in DC/DC(PSFB) converter
DC/DC ON	Signal for on or off control in DC/DC converter, active low signal
STB_{VAR}	Signal for on or off control in standby converter, active high signal

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