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A High-Power DC-DC Converter Topology for Battery Charging Applications

Il-Oun Lee * and Jun-Young Lee

Department of Electric Engineering, Myongji Unversity, Yongin-Si 449-728, Korea; pdpljy@mju.ac.kr
* Correspondence: leeiloun@mju.ac.kr; Tel.: +82-31-330-6833

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Abstract: A DC-DC converter that can be applied for battery chargers with the power-capacity of over 7-kW for electric vehicles (EVs) is presented in this paper. Due to a new architecture, the proposed converter achieves a reduction of conduction losses at the primary side by as much as 50% and has many benefits such as much smaller circulating current, less duty-cycle loss, and lower secondary-voltage stress. In addition, its power handing capacity can be upsized easily with the use of two full-bridge inverters and two transformers. Besides, all the switches in the converter achieve zero-voltage switching (ZVS) during whole battery charging process, and the size of output filter can be significantly reduced. The circuit configuration, operation, and relevant analysis are presented, followed by the experiment on a prototype realized with a 7-kW charger. The experimental results validate the theoretical analysis and show the effectiveness of the proposed converter as battery charger.

Keywords: full-bridge converter; electric vehicle; hybrid electric vehicle; battery charger; zero-voltage-switching

1. Introduction

Due to global warming and decreasing availability of fossil fuels, electric vehicle (EV) penetration in the vehicle market is growing quickly. EVs need some form of rechargeable energy storage such as batteries. Recently, the capacity of the battery in EVs has kept increasing in order to extend the driving range after charging the battery once, and with this battery capacity increase, the power handing capacity of battery chargers is also continuously increasing to shorten the charging time [1]. For example, the Nissan Leaf used a 24-kWh lithium-ion battery in 2010, but uses a 30-kWh battery in 2017. For 2018, the availability of a 60-kWh battery is planned. According to this, on-board chargers are increasing increase from 3.3-kW to 10-kW to shorten or afford similar charging time performance in spite of the increased EV battery capacity [2]. This is because conventional 3.3-kW chargers need many more hours to fully charge increased capacity EV batteries due to their small power-capacity, which represents a large bottleneck in the popularization of EVs [3,4]. Simply increasing the power-capacity with conventional chargers causes serious problems such as poor efficiency, large circulating current, large switching power loss, and very high voltage stress. Against this background, research on new battery charger topologies that can handle higher power is required and in response, this paper presents a new circuit technology for higher-power battery chargers.

In general, battery chargers are composed of a power-factor corrector (PFC) and a DC-DC converter [5–9]. In the development of battery chargers, it is necessary to decrease the size and mass to facilitate ease of installation and cost-effectiveness. The conversion efficiency will also be higher during the overall battery charging time. In order to accomplish these goals, the use of higher switching frequency is recommended with soft-switching technologies [10–12]. However, the soft-switching

operation can fail according to load conditions and then switching power losses will increase greatly. In addition, because rectifier diodes in the DC-DC converter experience very high voltage stresses, very large conduction losses are generated, which is a serious problem for increasing the power-capacity of battery chargers [13]. To achieve higher efficiency, it is necessary to consider the interleaved or parallel operation of converters for battery chargers [14–18].

In this paper, a DC-DC converter that can be applied for battery chargers with a power-capacity of over 7-kW for EVs is presented. The proposed converter consists of two full-bridge inverters (TFBIs) in parallel at the primary side. They are worked in phase-shift manner to control the output. Two full-bridge diode rectifiers are adopted for the rectifier, sharing a diode-leg with lower voltage rating. Due to this architecture, the proposed converter achieves a reduction of conduction losses at the primary side by as much as 50% and has many benefits such as much smaller circulating current, less duty-cycle losses, and lower secondary-voltage stress. In addition, its power handing capacity can be upsized easily with the use of two full-bridge inverters and two transformers. Besides, all the active switches in the proposed converter achieve zero-voltage switching (ZVS) during the whole battery charging process, and the size of the output filter can be reduced significantly.

2. Circuit Operations

The circuit configuration of the proposed converter is shown in Figure 1, and Figure 2 shows its key operating waveforms. Two full-bridge inverters are worked in phase-shift and the active switches in each full-bridge inverter are triggered with a constant duty-ratio of about 50%. The gate signals for the switches in the leading full-bridge inverter are faster than those for the switches in the lagging full-bridge inverter as shown in Figure 2. In this paper, switches in the leading or lagging full-bridge inverters are referred to as leading or lagging switches, respectively.

Each switching period is divided into two half cycles, t_0–t_8 and t_8–t_{16}. Because the operational principles of two half cycles are symmetric, only the first half cycle is described. This half cycle can be subdivided into eight modes, whose operating circuits are shown in Figure 3.

For the simplicity of analysis, some assumptions are made as follows:

(1) Two transformers of T_1 & T_2 have the turns-ratio of $n = N_{S1}/N_{P1} = N_{S2}/N_{P2}$ and include the leakage inductors of L_{lk1} and L_{lk2}, respectively.
(2) The magnetizing inductor (L_{m2}) of T_2 has a sufficient large value to ignore the effect of the magnetizing current.
(3) All the active switches have the same output capacitance of C_{OSS}.
(4) The output inductor has a sufficient large value so that it can be seen as a current source.

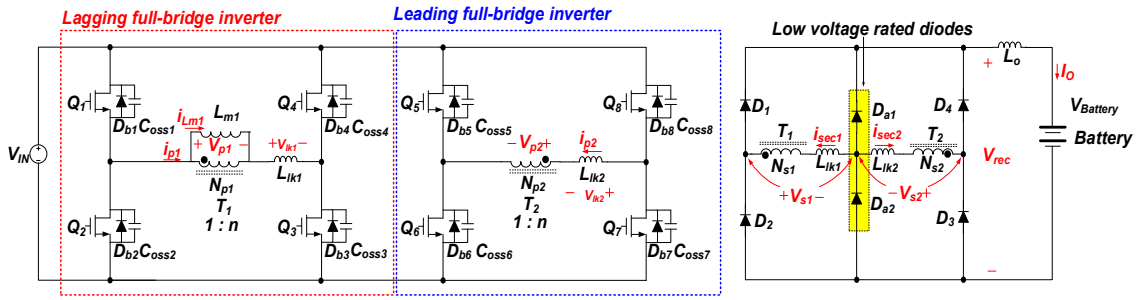


Figure 1. Proposed DC-DC converter for high-power electric vehicle battery charger.

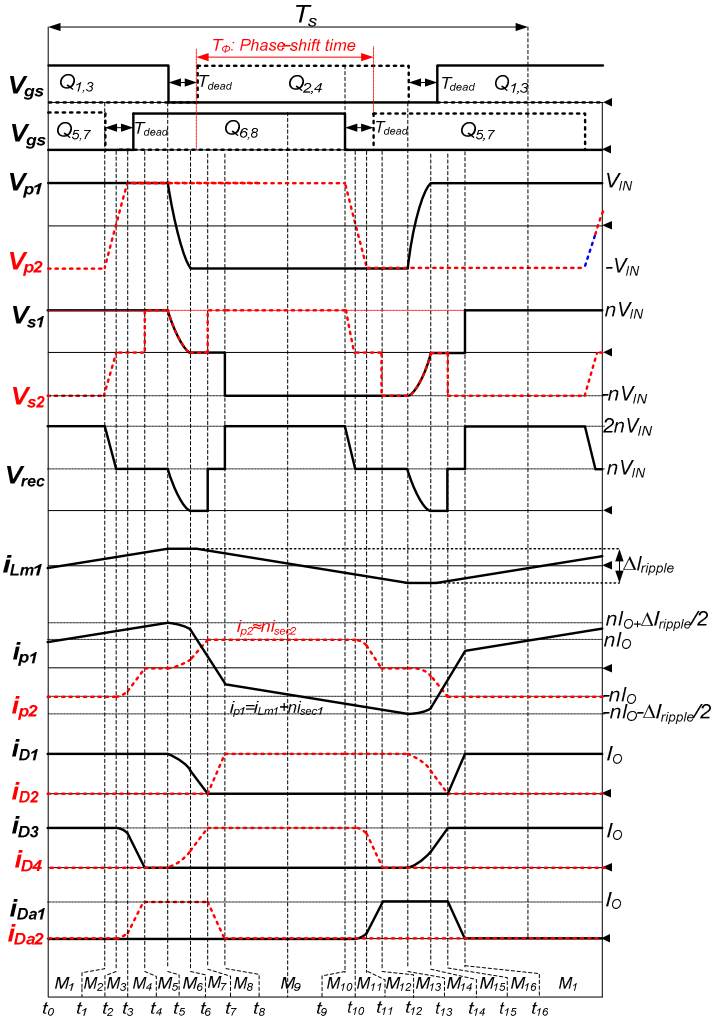


Figure 2. Key operating waveforms of the proposed converter in steady state.

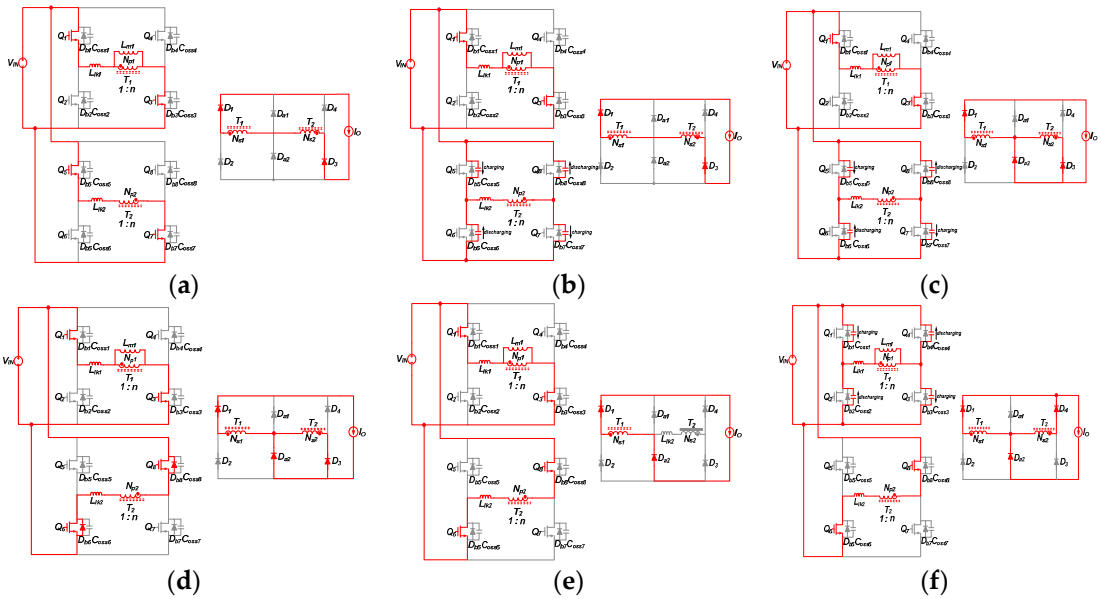


Figure 3. *Cont.*

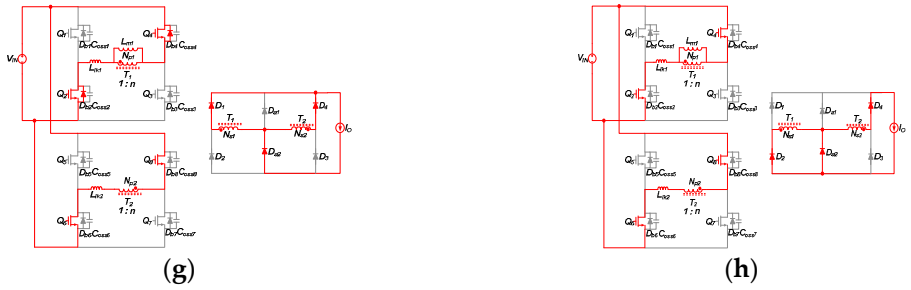


Figure 3. Operating circuits during the first half cycle: (**a**) Mode 1; (**b**) Mode 2; (**c**) Mode 3; (**d**) Mode 4; (**e**) Mode 5; (**f**) Mode 6; (**g**) Mode 7; and (**h**) Mode 8.

Mode 1 (t_0~t_1): Mode 1 begins when the $Q_{5,7}$ in leading switches and the $Q_{1,3}$ in lagging switches are in ON-state and the diodes of D_1 and D_3 are conducting. In this mode, the voltages at the primary side of $V_{p1}(t)$ and $V_{p2}(t)$ become positive and negative values of V_{IN}, respectively. The magnetizing current of T_1, $i_{Lm1}(t)$ starts linearly increasing, but the $i_{Lm2}(t)$ is nearly zero due to the very large magnetizing inductance of T_2. The voltages at the secondary side of $V_{s1}(t)$ and $V_{s2}(t)$ also become positive and negative values of the input voltage with the turns-ratio of n, respectively. The output voltage of rectifier, $V_{rec}(t)$ becomes $2nV_{IN}$ due to the sum of $V_{s1}(t)$ and -$V_{s2}(t)$. In this mode, the power is transferred from the input port to the output port via T_1, T_2, D_1, and D_3 and the primary currents of inverter stage can be expressed as follows:

$$\begin{aligned} i_{p1}(t) &= i_{Lm1}(t) + ni_{\sec 1}(t) = i_{Lm1}(t) + ni_{D1}(t) = i_{Lm1}(t) + nI_O, \\ i_{p2}(t) &= i_{Lm2}(t) + ni_{\sec 2}(t) \approx ni_{\sec 2}(t) = -ni_{D3}(t) = -nI_O \end{aligned} \tag{1}$$

Mode 2 (t_1~t_2): Mode 2 begins when the $Q_{5,7}$ are turned off at t_1. Then, with the energy stored in the output inductor L_O, the voltages across C_{OSS5} and C_{OSS7} are charged linearly and the voltages across C_{OSS6} and C_{OSS8} are discharged. $V_{p2}(t)$ increases from $-V_{IN}$ and $V_{p1}(t)$ is maintained at V_{IN}. The $V_{rec}(t)$ falls from $2nV_{IN}$ to nV_{IN}. The expression of primary currents in this mode is the same as in mode 1.

Mode 3 (t_2~t_3): When the $V_{p2}(t)$ becomes zero, mode 3 starts. Then the $V_{s2}(t)$ is zero and the diode of D_{a2} begins to be ON. Because D_{a2} is ON, $V_{s2}(t)$ is maintained at zero in this mode and a resonance behavior between the output capacitances of all the leading switches and L_{lk2} occurs in the leading full-bridge inverter. With the resonance, the voltages across $C_{OSS5\&7}$ are continuously charged and the voltages across $C_{OSS6\&8}$ are discharged. The $V_{p2}(t)$ increases from zero to V_{IN}, and $V_{p1}(t)$ is maintained at V_{IN}.

Mode 4 (t_3~t_4): The $V_{p2}(t)$ becomes V_{IN} in mode 3 and then mode 4 starts. The body diodes of $Q_{6,8}$, D_{b6} and D_{b8}, start to conduct and $Q_{6,8}$ are turned on with ZVS. In mode 4, $V_{s2}(t)$ is continuously zero, thus the input voltage of V_{IN} applies to the leakage inductor of L_{lk2}. Due to the positive voltage applied to L_{lk2}, D_{a2} begins to commutate with D_3. $V_{p1}(t)$ and $V_{rec}(t)$ are maintained at V_{IN} and nV_{IN}, respectively. In this mode, the input power is transferred to the output load through T_1, T_2, D_1, D_{a2}, and D_3, and the currents can be analyzed as follows.

$$\begin{aligned} &i_{p1}(t) = i_{p1}(t_3) + \tfrac{V_{IN}}{L_{m1}}(t-t_3),\ i_{p2}(t) = -nI_O + \tfrac{V_{IN}}{L_{lk2}}(t-t_3),\ i_{Da2}(t) = \tfrac{V_{IN}}{nL_{lk2}}(t-t_3), \\ &i_{D1}(t) = I_O,\ and\ i_{D3}(t) = I_O - i_{Da2}(t). \end{aligned} \tag{2}$$

Mode 5 (t_4~t_5): Mode 5 begins when the commutation between D_3 and D_{a2} is completed at t_4 and only D_1 and D_{a2} are conducting. In this mode, the $i_{p2}(t)$ is zero, and the input power is transferred to the output load through T_1, D_1, and D_{a2}.

Mode 6 (t_5~t_6): Mode 6 starts when $Q_{1,3}$ are turned off at t_5. At the same time, diode D_4 starts to conduct and another resonance, which consists of the output capacitances of all the lagging switches and the two leakage inductors of L_{lk1} and L_{lk2}, occurs in the lagging full-bridge inverter. By the

resonance, the voltages across $C_{OSS1\&3}$ are discharged, and the voltages across of $C_{OSS2\&4}$ are charged. The $V_{p1}(t)$ decreases from V_{IN} to $-V_{IN}$ and $V_{rec}(t)$ decreases to zero. The commutation between D_1 and D_4 is also progressed.

Mode 7 (t_6~t_7): When the $V_{p1}(t)$ becomes $-V_{IN}$ in Mode 6, Mode 7 begins. Then the body diodes of $Q_{2,4}$, D_{b2} and D_{b4}, start to be ON and $Q_{2,4}$ is turned on with ZVS. In Mode 7, the $V_{s1}(t)$ and $V_{s2}(t)$ are zero, and thus $V_{rec}(t)$ is also zero. Due to this, the output load is powered from the energy stored in the output inductor L_O at t_6. Because $V_{p1}(t) = -V_{IN}$, $V_{p2}(t) = V_{IN}$, and $V_{s1}(t) = V_{s2}(t) = 0$, the voltages across two leakage inductors, L_{lk1} and L_{lk2}, equal to $-V_{IN}$ and V_{IN}, respectively. Then the $i_{p1}(t)$ and $i_{D1}(t)$ decrease linearly and the $i_{p2}(t)$ and $i_{D4}(t)$ increase linearly as follows.

$$\begin{array}{l} i_{p1}(t) = i_{p1}(t_6) - \frac{V_{IN}}{L_{lk1}}(t - t_6), i_{p2}(t) = i_{p2}(t_6) + \frac{V_{IN}}{L_{lk2}}(t - t_6), \\ i_{D4}(t) = I_O - i_{D1}(t) = i_{p2}(t)/n, \; and i_{Da2}(t) = I_O. \end{array} \tag{3}$$

Mode 8 (t_7~t_8): Mode 8 begins when the current through D_4 reaches to the output current I_O and D_1 is turned off. Then the $V_{s1}(t)$ is zero and $V_{s2}(t)$ becomes nV_{IN}. Thus, the V_{IN} appears on L_{lk1} and the commutation between D_2 and D_{a2} starts. The $V_{rec}(t)$ equals to nV_{IN}. The currents in this mode can be represented as follows.

$$\begin{array}{l} i_{p1}(t) = i_{p1}(t_7) - \frac{V_{IN}}{L_{lk1}}(t - t_7), \; i_{D2}(t) = I_O - i_{Da2}(t) = \frac{V_{IN}}{nL_{lk1}}(t - t_7), \\ i_{p2}(t) = nI_O, \; and \; i_{D4}(t) = I_O. \end{array} \tag{4}$$

At the end of Mode 8, $i_{D2}(t)$ reaches to I_O and the diode of D_{a2} is turned off naturally. Then, the input power is transferred to the output load through the path of T_1, T_2, D_2, and D_4.

3. Circuit Analysis

3.1. DC Analysis

Since the intervals of modes 2, 6, and 8 in Figure 2 are practically very narrow, the output voltage of the rectifier in the proposed converter, $V_{rec}(t)$ can be simply given as in Figure 4a. Figure 4b shows the counter part in the conventional converter, which is a traditional phase-shift full-bridge (PSFB) converter or a topology consisting of two PSFB converters operated in parallel for larger power processing.

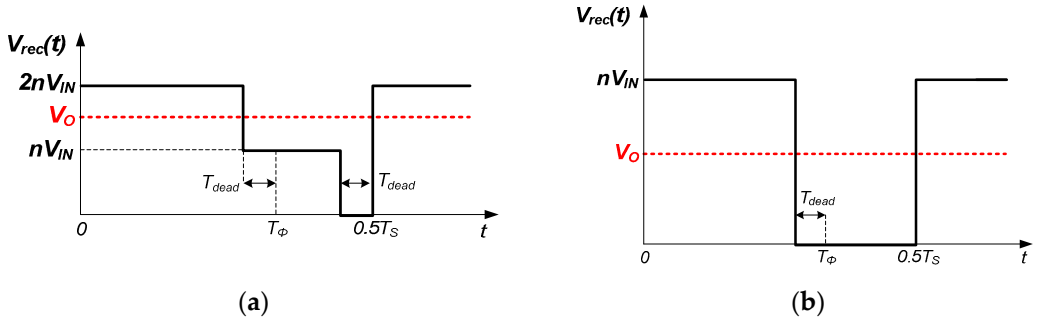


Figure 4. Simplified rectifier output waveform (**a**) in the proposed converter and (**b**) in the conventional converter consisting of two parallel-operated PSFB converters.

In the comparison of the two figures, we can see that the proposed converter do not have freewheeling intervals, where the $V_{rec}(t)$ is maintained at zero level. Due to this, the proposed converter is able to transfer the input power to the output load continuously, and hence a small inductor can be required for the output filter. And any circulating current is not generated ideally at the primary side. By averaging the $V_{rec}(t)$ in Figure 4a, the voltage gain of the proposed converter can be acquired as follows.

$$M(D) = \frac{V_O}{V_{IN}} = 2n(D + 0.5) \text{ and } D = (T_\phi - 2T_{dead})/T_S \quad (5)$$

where T_S is a switching period.

From Figure 4b, the voltage gain for the conventional converters is obtained as

$$M(D) = \frac{V_O}{V_{IN}} = 2nD \text{ and } D = (T_\phi - T_{dead})/T_S. \quad (6)$$

The normalized $M(D)$ (supposing n = 1) of the proposed converter is shown in Figure 5 along with the conventional converters. Figure 5 indicates that the proposed converter has much higher voltage gain than the conventional converters. Due to this, the proposed converter can be designed with much smaller turns-ratio (n) than the conventional converter. This contributes to the improvement of the conduction loss in the primary side and the voltage stress on diodes in the secondary side.

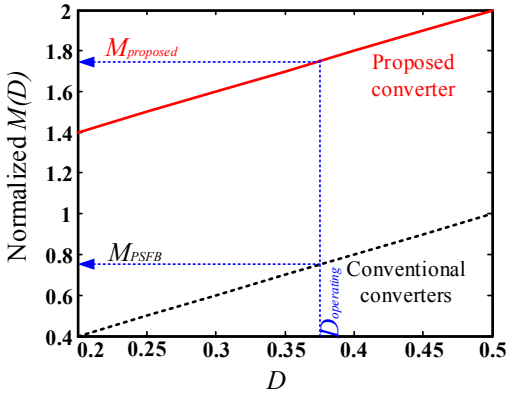


Figure 5. Normalized DC gain versus duty-cycle.

3.2. Output Inductor

From the voltage and current of the output inductor L_O, the L_O is can be calculated as

$$L_O = V\frac{\Delta T}{I_{ripple}} \quad (7)$$

where V is the voltage across L_O during the time of ΔT, and I_{ripple} is the current ripple through L_O.

Then, for the conventional and proposed converters, the output filter inductor can be obtained as in Equations (8) and (9) using Equations (5)–(7) with $V_{rec}(t)$s in Figure 4a,b.

$$L_{O\_PSFB} = \frac{V_O}{2I_{PP}}(D - 0.5)T_S. \quad (8)$$

$$L_{O\_proposed} = \frac{V_O}{I_{PP}}(1 - \frac{0.5}{D + 0.5})(0.5 - D)T_S. \quad (9)$$

Figure 6 shows the output inductance calculated based on Equations (8) and (9) in function of duty-cycle at the case that V_O = 250 V, I_{ripple} = 1A, and f_S = 100 kHz. As a result, we can know that the output inductor for the proposed converter is much smaller than it for the conventional converter.

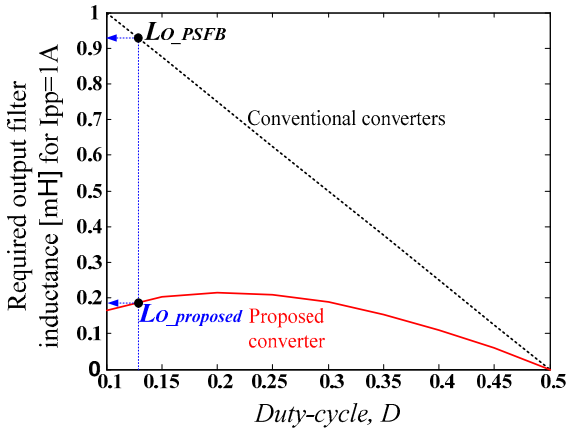


Figure 6. Required output inductance versus operating duty-cycles.

3.3. Soft Switching Characteristic

As described in the operating modes, the ZVS for the leading switches is formed through two resonant phases. Firstly, by the large energy stored in the output inductor, the drain-to-source voltage of the leading switches is discharged from V_{IN} to $0.5V_{IN}$ linearly. After that, the voltage is fully discharged by the resonance formed by the energy stored in the leakage inductor L_{lk2}. The ZVS condition for the leading switches can be expressed as follows.

$$nI_O z_{O1} \sin \omega_{O1}(T_{dead} - \frac{V_{IN}C_{OSS}}{nI_O}) \geq 0.5V_{IN}. \tag{10}$$

In the view of energy, the Equation (10) can be represented as

$$\frac{1}{2}L_{lk2}(nI_O)^2 \geq \frac{8}{3}C_{OSS}(0.5V_{IN})^2 = (\frac{8}{3}C_{OSS}V_{IN}^2) \times \frac{1}{4}. \tag{11}$$

As seen in Equation (11), the voltage remaining at the leading switches, which should be removed by the energy stored in L_{lk2}, is only 25% of the original energy. Due to this, the ZVS operation for the leading switches can be acquired easily with the small inductance of L_{lk2} under wide load variation. If the current through L_{m2} is considered to ensure the ZVS, the ZVS equation in Equation (11) can be modified as in Equation (12).

$$z_{O1}(0.5\Delta I'_{ripple} + nI_O) \sin \omega_{O1}(T_{dead} - \frac{V_{IN}C_{OSS}}{0.5\Delta I'_{ripple} + nI_O}) \geq 0.5V_{IN}.$$

or

$$\frac{1}{2}L_{lk2}(nI_O + 0.5\Delta I'_{ripple})^2 \geq \frac{8}{3}C_{OSS}(0.5V_{IN})^2 = (\frac{8}{3}C_{OSS}V_{IN}^2) \times \frac{1}{4} \tag{12}$$

where $\Delta I'_{ripple}$ is the current ripple of L_{m2}. Because the energy that is discharged by $\Delta I'_{ripple}$ is also 25% of the original energy as shown in Equation (12), $\Delta I'_{ripple}$ can be designed with a small value.

The ZVS condition of the lagging switches is obtained as follows.

$$z_{O2}(0.5\Delta I_{ripple} + nI_O) \sin \omega_{O2}T_{dead} \geq V_{IN} \tag{13}$$

or

$$\frac{1}{2}(L_{lk1} + L_{lk2})(0.5\Delta I_{ripple} + nI_O)^2 \geq \frac{8}{3}C_{OSS}V_{IN}^2. \tag{14}$$

From Equation (13) or (14), it is known that the ZVS of the lagging switches can be easily achieved under wide load variation due to the term of L_{lk1} + L_{lk2} and the ripple of $i_{Lm1}(t)$, ΔI_{ripple}. Typically,

a large leakage inductor increases duty-cycle loss and hence a trade-off between leakage inductor's values and magnitude of ΔI_{ripple} should be conducted in Equation (14) for optimally designing the proposed converter. In order to extend the ZVS range to no load condition with reasonable leakage inductors' values, the proposed converter uses the magnetizing inductor of T_1, L_{m1} (or ΔI_{ripple}) in this paper. Then, someone could think that the conduction loss generated in the lagging full-bridge inverter will increase as in the conventional phase-shift full-bridge converter with a small magnetizing inductance. However, the RMS current in the lagging full-bridge inverter is not increased in spite of the small magnetizing inductance of T_1. The average value of the magnetizing current in T_1 becomes zero within a half-switching period and thus its contribution to the RMS current is negligible at heavy load conditions. This principle is well explained analytically in [18].

3.4. Operation of the Proposed Converter During Battery Charging

Figure 7 shows the battery charging profile for general battery chargers [19]. At the beginning, the DC-DC converter gradually ramps up charging current with a staircase wave to avoid damaging the battery until each battery cell voltage reaches to the threshold voltage or the battery voltage reaches to point A. This charging sequence is defined as pre-charging mode. After the pre-charging mode, the DC-DC converter is switched to constant-current mode and the battery voltage is linearly charged up to the maximum battery voltage, i.e., 450 V or the point C. If the battery voltage reaches to point C, the DC-DC converter lies finally under constant-voltage mode and the charging current gradually decreases. This mode is stopped when the charging current reaches to the pre-defined termination current as indicated in Figure 7.

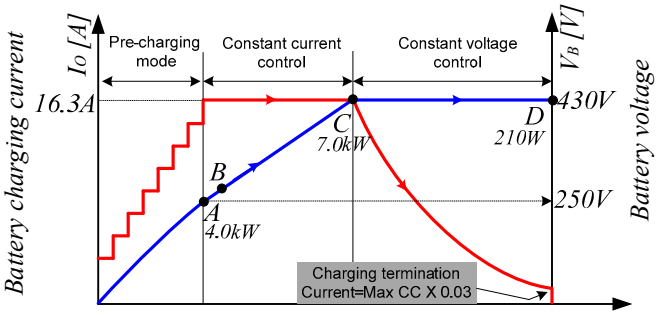


Figure 7. General battery charging profile [19].

Figure 8 shows the operations, relevant operating waveforms, and equivalent circuits of the proposed converter with the battery charging profile shown in Figure 7. For the pre-charging mode where the processed power is small, the leading full-bridge inverter in the proposed converter is disenabled and only the lagging full-bridge inverter charges up the battery by adjusting the phase-shift time of T_α in between the two legs in the lagging full-bridge inverter indicated in Figure 8a. That is, in this mode, the lagging full-bridge inverter operates like the traditional PSFB converter, and the phase-shift time of T_α decreases as the output voltage or battery voltage increases during the pre-charging mode. When the battery voltage reaches to point A, the T_α becomes zero degree and the gate signal of Q_1 (or Q_2) is identical with of Q_3 (or Q_4). At the same time, the leading full-bridge inverter is enabled and the proposed converter starts to work by adjusting the phase-shift time of T_Φ between the two inverters as in Figure 2. At point B, most of the power is transferred to the battery through the lagging full-bridge inverter as seen in Figure 8b because the battery voltage is still low or the phase-shift time of T_Φ is small. As the charging point moves from A to C, the battery voltage or the charging power increases and T_Φ also increases. Then, the power processed by the leading full-bridge inverter gradually increases, and each inverter naturally handles half the total power at the maximum power point, C. These operations make it possible for the proposed converter to achieve higher efficiency during the whole battery charging process.

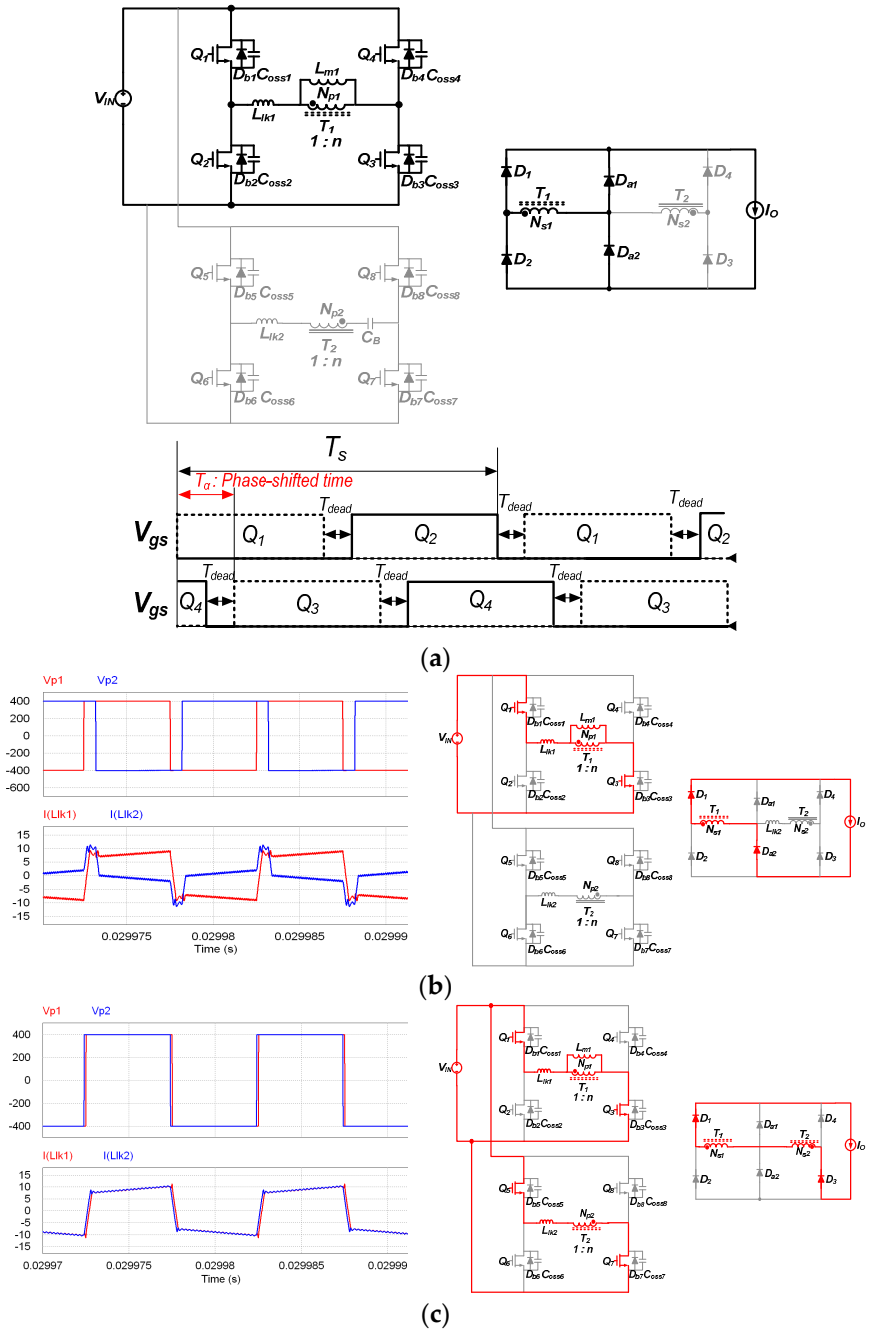


Figure 8. Operations of the proposed converter with the battery charging profile in Figure 7. (**a**) In the pre-charging mode; (**b**) At the point B; and (**c**) At the point C.

3.5. Voltage Stress

Figure 9 shows the equivalent circuits of the rectifier in the proposed converter during two powering modes. From the figure, the diodes' voltage stress can be derived as in Table 1. The voltage stress of the two conventional converters is also described in the table, where n is the turns-ratio of the proposed converter and n_{c1} and n_{c2} mean the turns-ratios of two conventional converters, respectively. For a quantitative analysis, it is assumed that the input voltage is 400 V, and all the converters operate with the charging profile in Figure 7. Then, each turns-ratio for transformers can be calculated using Equations (10) and (11). However, due to practical factors such as dead-times between driving signals and the duty-cycle loss caused by leakage inductors, the calculated turns-ratios

should be lightly increased in practice. Considering this, the turns-ratios are determined as n = 0.61, n_{c1} = 1.4, and n_{c2} = 1.22, respectively. Accordingly, it is noted that the proposed converter needs four high-voltage-rated diodes and two low-voltage-rated diodes. On the other hand, both the conventional converters need only high-voltage-rated diodes. Considering that lower-voltage-rated diodes feature many benefits such as much lower voltage drop and better reverse-recovery, the use of two low-voltage-rated diodes for the center-leg in the proposed converter contribute to the reduction of the power loss compared to the two conventional converters, thus enhancing the conversion efficiency.

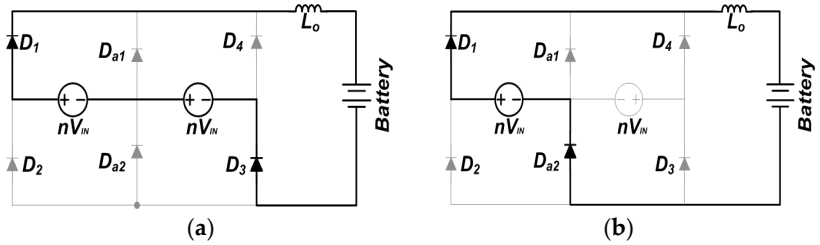


Figure 9. Equivalent circuits of rectifier stage in the proposed converter during powering modes. (**a**) Powering operation during Mode 1; (**b**) Powering operation during Mode 5.

Table 1. Voltage stress of diodes in the rectifier.

Diodes	Proposed Converter	Single PSFB Converter	Parallel-Connected PSFB Converter
$D_{1\text{-}4}$	$2nV_{IN}$ (488V)	$n_{c1}V_{IN}$ (560V)	$n_{c1}V_{IN}$ (560V)
$D_{5\text{-}8}$	*Not used*	*Not used*	$n_{c1}V_{IN}$ (560V)
$D_{a1\&a2}$	nV_{IN} (244V)	*Not used*	*Not used*

3.6. Loss Comparison and Component Counts

A loss comparison between the proposed converter and conventional converters is carried out at point B, C, and D indicated in Figure 7. Firstly, as indicated in Figure 10, the primary-conduction loss of the proposed converter is much lower than that of the conventional converters. This is because in the proposed converter, the lagging full-bridge inverter processes most of the power at point B and the power at maximum power point C is processed in parallel by both inverters. The smaller turn-ratio also contributes to the reduction of the primary-conduction loss. The primary-switching loss of the proposed converter becomes advantageous as the output power decreases. This is due to the wide ZVS load range. Compared with the conventional converters, the secondary-conduction loss of the proposed converter is also improved due to the deployment of two low-voltage-rated diodes for D_{a1} and D_{a2}. Figure 10d shows the sum of primary-conduction loss, primary-switching loss, and secondary-conduction loss. Because of the improvements of power loss as shown in Figure 10d, it is possible that the proposed converter achieves higher conversion efficiency compared to the conventional converters during whole battery charging process.

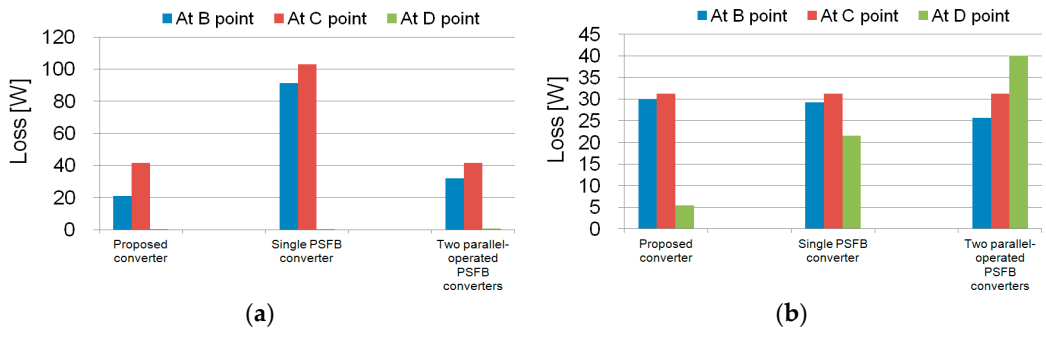


Figure 10. *Cont.*

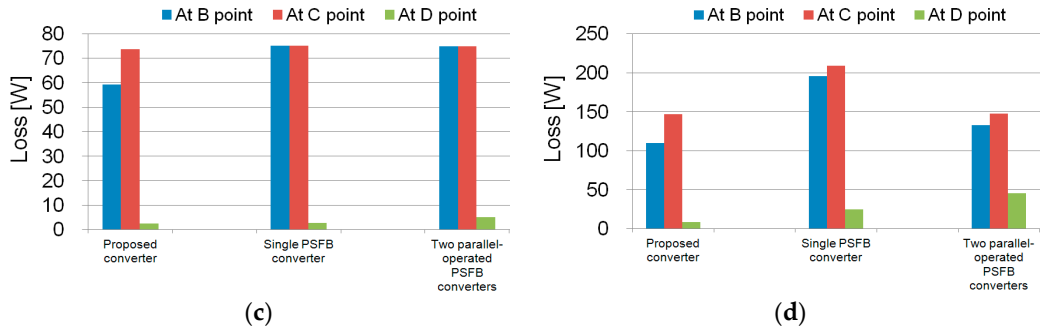


Figure 10. Loss comparison calculated at 6.6-kW design. (**a**) Primary conduction loss; (**b**) Primary switching loss; (**c**) Secondary conduction loss; (**d**) Total loss.

Table 2 shows component count. Although the proposed converter handles the high power of over 7-kW, the number of the component in the proposed converter is less than it of the two parallel-operated PSFB converters.

Table 2. Component count.

Items	Proposed Converter	Single PSFB Converter	Parallel-Connected PSFB Converter
Switch	8	4	8
Diode	6	4	8
Transformer	2	1	2
Resonant inductor	0	1	2
Output inductor	1	1	2
Total	17	11	22

In summary, considering the power loss in Figure 10 and the number of components, it can be said that the proposed converter is more suitable than the conventional converters for battery charger applications with the power-capacity of over 7-kW.

4. Experimental Results

In order to confirm the feasibility of the proposed converter, a prototype with the power capacity of 7-kW was built with the following specifications:

- V_{IN} = 400 V, V_O = 250–430 V, $I_{O(max)}$ = 16.3 A
- Switching frequency: f_S = 100 kHz

Table 3 shows the components used in the prototype converter and the prototype converter is shown in Figure 11.

Table 3. Component lists.

Part	Items
Main switches (Q_1–Q_8)	IPW65R080CFDA
Rectifier diodes (D_1–D_4)	C4D20120D (1200 V, 33 A, Vf = 2.2 V)
Auxiliary diodes (D_{a1}, D_{a2})	FFH50US60S (600 V, 50 A, Vf = 1.54 V)
Transformers (T_1, T_2)	EE6565, n = 0.61 For T_1, L_m = 855.8 µH, L_{lk} = 8.26 µH For T_2, L_m = 845.2 µH, L_{lk} = 8.32 µH
Output inductor (L_o)	200 µH, CH467060#2
Output capacitor (C_o)	47 µF
Controller	TMS320F28335

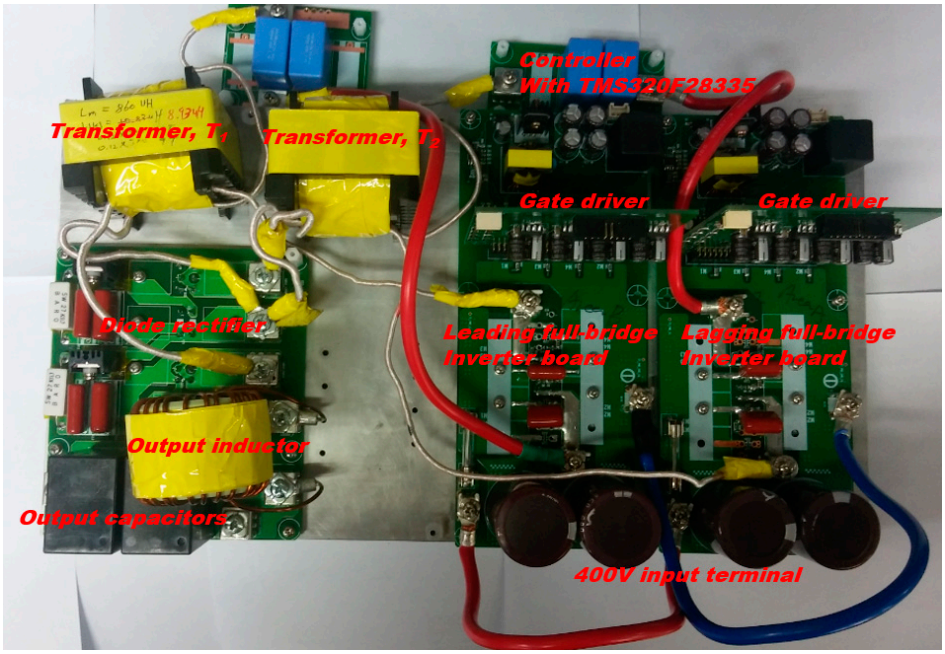
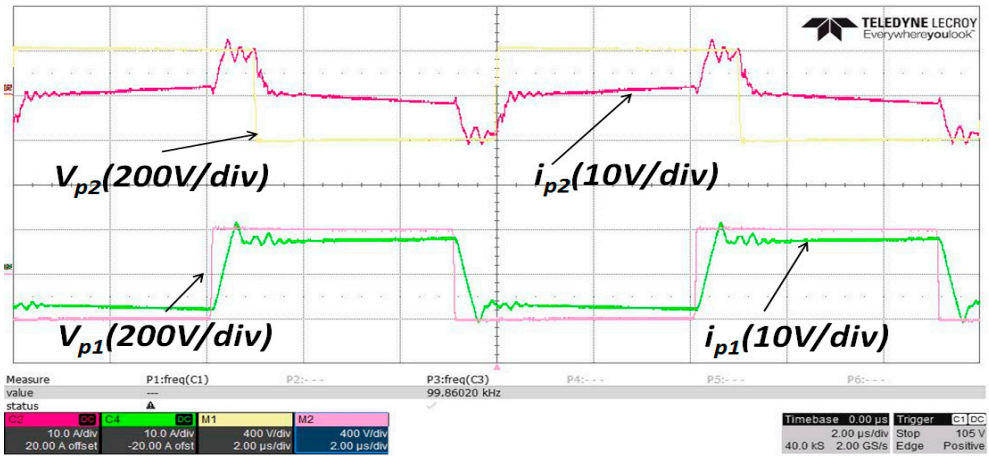


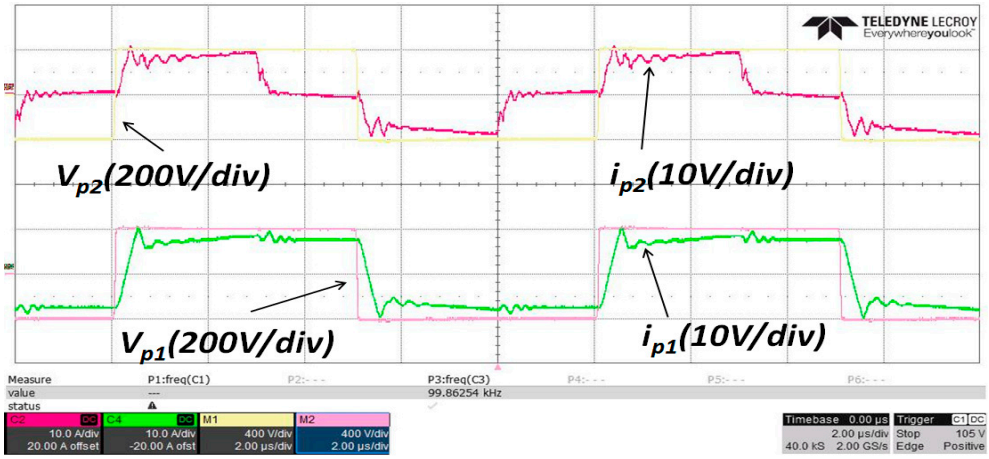
Figure 11. Prototype of the proposed converter developed at 7-kW.

Figures 12 and 13 show the key operating waveforms when the operating point of the proposed converter is moving from point B to C, which is indicated in Figure 7. As shown in the figures, all the measured waveforms are well following the theoretical waveforms described in Figures 2 and 8. Moreover, it is confirmed from the experimental waveforms that the proposed converter has no circulating current on the primary side during battery charging. We can also see that from the rectifier diodes' voltage waveforms in Figure 14, the diodes in the center leg of the proposed converter have much lower voltage stress compared to the outer leg diodes. Consequently, the proposed converter can use much better diodes with low voltage rating in the center leg, and the power is transferred using the two low-voltage rated diodes with smaller on-state voltage when the proposed converter moves from point B to C. Due to this operation, the conduction loss in the rectifier stage can be lower than it in the conventional converters.

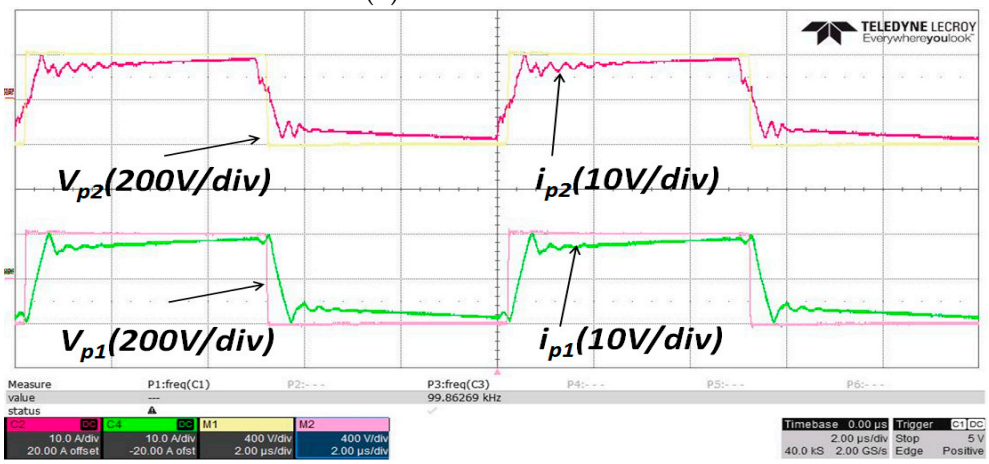


(**a**) *Vo* = 250 V@4 kW

Figure 12. *Cont.*

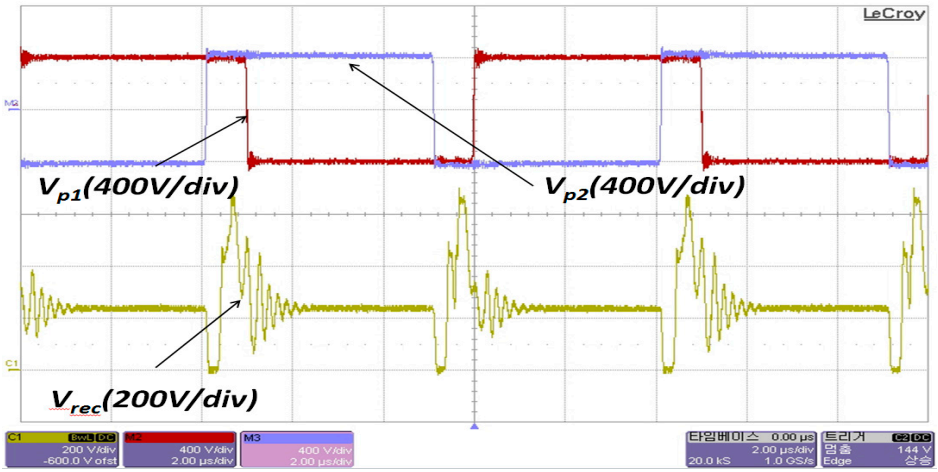


(**b**) *Vo* = 350 V@5.7 kW



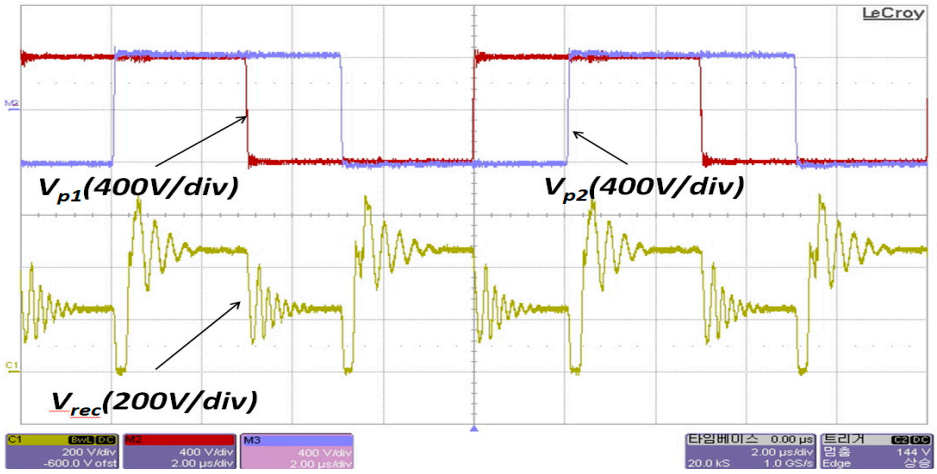
(**c**) *Vo* = 430 V@7 kW

Figure 12. V_{p1}, i_{p1}, V_{p2}, and i_{p2} when the proposed converter is moving from point B to C.

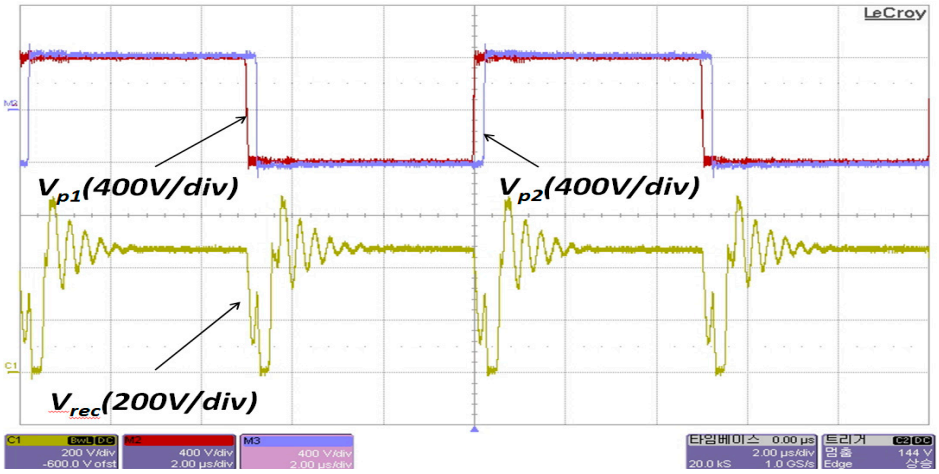


(**a**) *Vo* = 250 V@4 kW

Figure 13. *Cont.*



(**b**) *Vo* = 350 V@5.7 kW



(**c**) *Vo* = 430 V@7 kW

Figure 13. V_{rec} when the proposed converter is moving from point B to C.

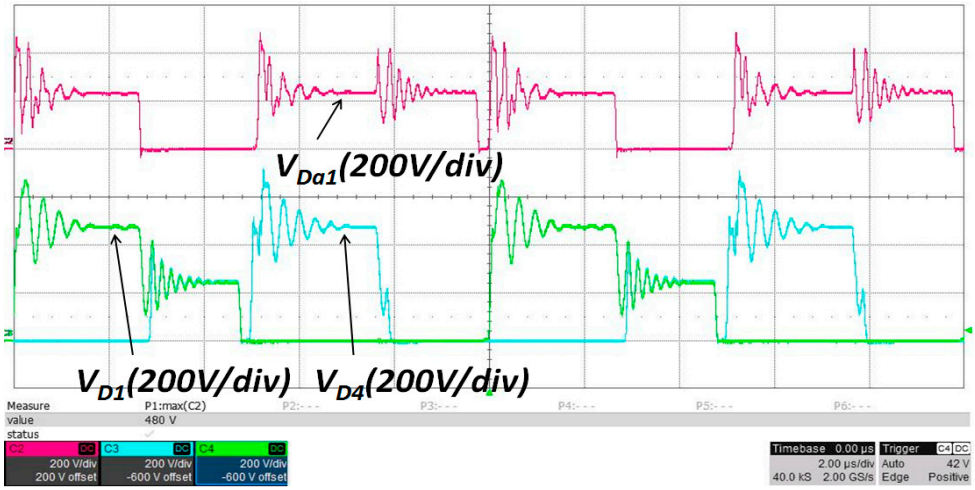
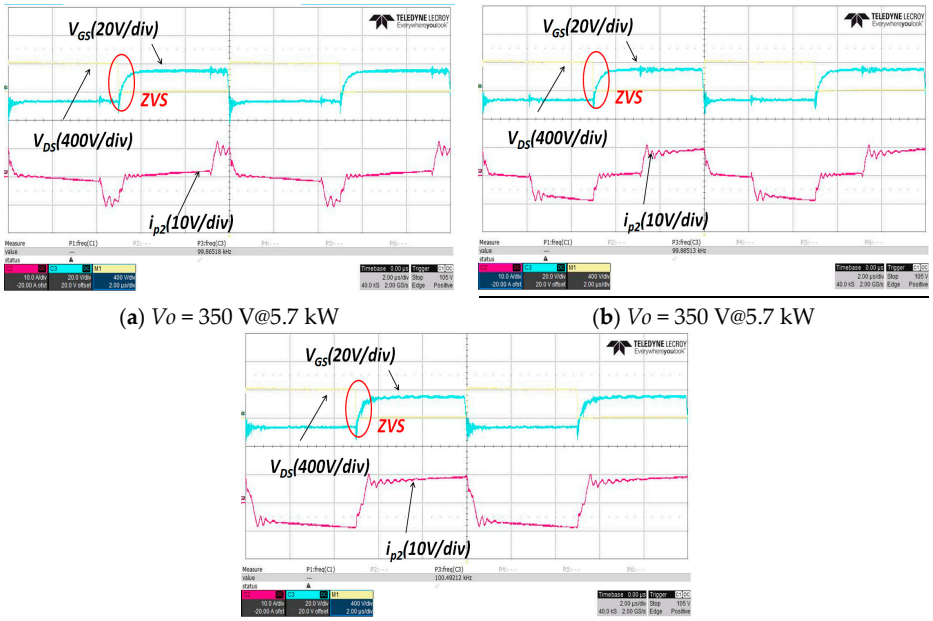


Figure 14. Diode voltage stress when *Vo* = 350 V@5.7 kW in the CC charging.

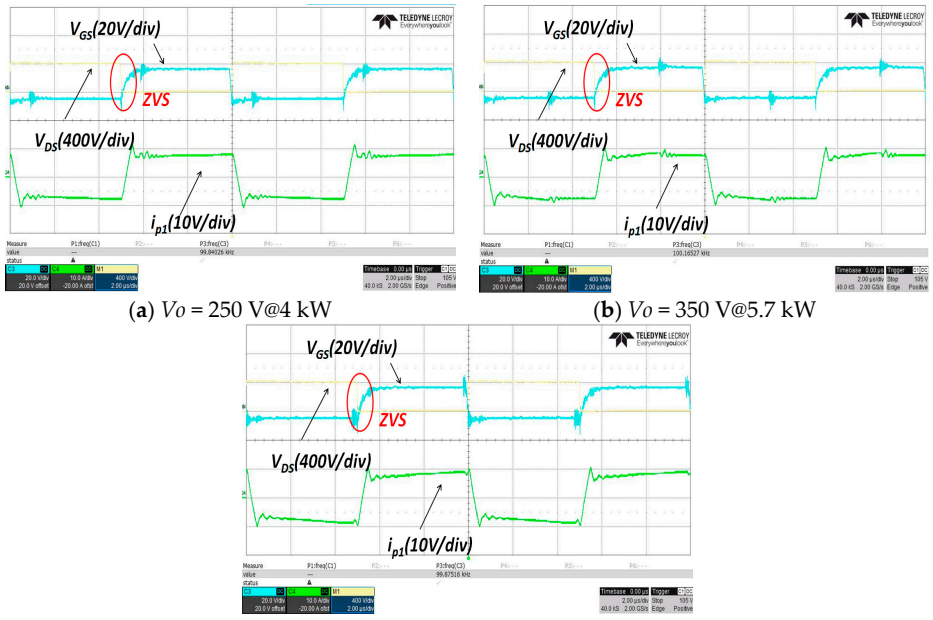
Figures 15 and 16 show the ZVS waveforms during the constant-current (CC) charging mode. During the overall charging mode in Figure 7, all the switches in the proposed converter are turned on after the drain-to-source voltage decays zero as in the waveforms.



(**a**) *Vo* = 350 V@5.7 kW (**b**) *Vo* = 350 V@5.7 kW

(**c**) *Vo* = 430 V@7 kW

Figure 15. ZVS waveforms in the lagging full-bridge inverter side during the CC charging.



(**a**) *Vo* = 250 V@4 kW (**b**) *Vo* = 350 V@5.7 kW

(**c**) *Vo* = 430V@7 kW

Figure 16. ZVS waveforms in the leading full-bridge inverter side during the CC charging.

Figure 17 shows the measured efficiencies. As seen in Figure 17, the proposed converter has the maximum of 96.7% at the full load or the point C in Figure 7, and the high efficiency is maintained during the battery charging. This is due to ZVS operation under all operating conditions, the design without the effect of duty-loss, much reduced circulating current, and the two lower-voltage-rated diodes in the rectifier.

In the Figure 18, the output inductors in the conventional PSFB and proposed converters, which are designed at 7-kW, are compared. As analyzed in the Section 3, the proposed converter uses a much smaller inductor.

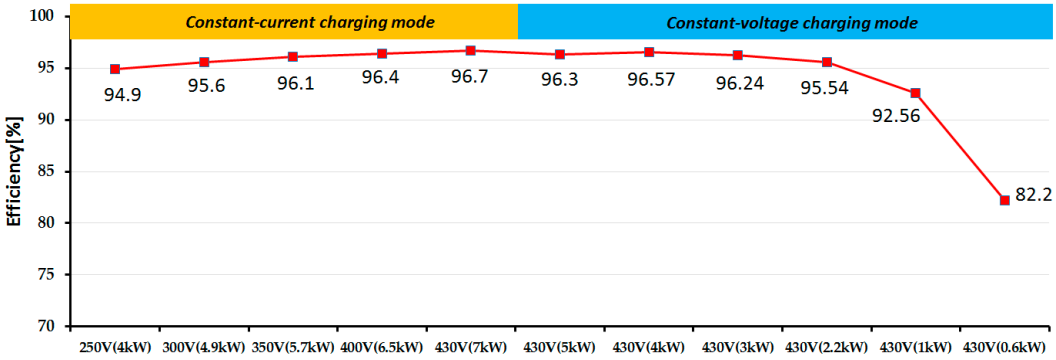


Figure 17. Measured efficiency during battery charging

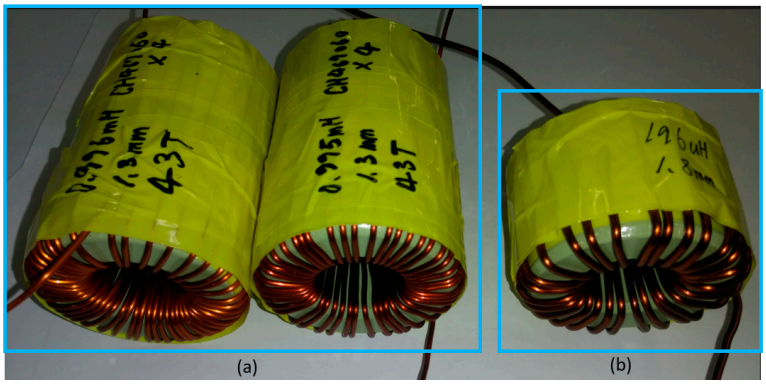


Figure 18. Output inductors for the charging current ripple of 1A at *fs* = 100 kHz and *Vo* = 250 V: (**a**) the output inductors for the conventional PSFB converters and (**b**) the output inductor for the proposed converter.

5. Conclusions

This paper proposes a DC-DC converter that can be applied for battery chargers with the power-capacity over 7-kW for EVs. Its advantages are summarized as follows:

(1) Considerable reduction of both primary- and secondary-conduction losses due to the parallel connection in the primary side and the use of two lower-voltage-rated diodes in the secondary side
(2) Additional reduction of primary-conduction loss by no circulating current
(3) Much better turn-ratio by less duty-loss compared to the conventional PSFB converter
(4) Wider ZVS range in all the switches
(5) Much smaller output inductor size
(6) Easy-to-increase power handing capability

The theoretical analysis of the proposed converter was presented in detail, and its feasibility was verified through the experiment with a 7-kW prototype converter. The experimental results show that the proposed converter can be applied for EV battery charger applications with higher power-capacity.

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Author Contributions: Il-Oun Lee defined the overall outline of the study and performed the numerical analysis, analyzed the data and drafted the paper. Il-Oun Lee designed and performed the experiments; Jun-Young Lee performed the analysis and experiments and finalized the paper.

Conflicts of Interest: The authors declare no conflict of interest.

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