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Concept Paper

Offset Voltage Control Scheme for Modular Multilevel Converter Operated in Nearest Level Control

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Abstract: This paper proposes an offset voltage control scheme for the modular multilevel converter (MMC) operated in nearest level control (NLC) to improve the total harmonic distortion (THD) of AC phase voltages. The offset (neutral-to-zero-point) voltage is adjusted so that the magnitude of each AC pole voltage maintains constant value with $N + 1$ level in the range of whole modulation index (MI). The validity of the proposed scheme was confirmed by computer simulations for the MMC with 22.9 kV/25 MVA and experimental works for the scaled MMC with 380 V/10 kVA. It was confirmed that the proposed control scheme can generate linearly variable AC phase voltages with improved THD in the over-modulation region as well as the normal-modulation region.

Keywords: high voltage direct current (HVDC) system; modular multilevel converter (MMC); sub-module (SM); nearest level control (NLC); Offset voltage; modulation index (MI); total harmonic distortion (THD)

1. Introduction

Recently, a high voltage direct current (HVDC) system with voltage source converter has been widely operated to transmit electricity generated in the offshore wind farm to the land [1–3]. A voltage source converter with insulated gate bipolar transistor (IGBT) can freely control the magnitude and phase angle of the output voltages, so that decoupled regulation of the active and reactive power is possible.

A three-level converter composed of multiple switching components and operated with pulse width modulation (PWM) has been initially proposed by ABB (Asea Brown Boveri). However, the system efficiency is relatively low, due to high switching loss and the harmonic level is also burdened [4,5].

In order to solve these problems, a modular multi-level converter (MMC) composed of series-connected sub-modules (SMs) with half- or full-bridge IGBTs and capacitors has been proposed [6–9]. MMC has the flexibility to match the system operation voltage by increasing or decreasing the number of series connected SMs. Each of the series connected SMs can be switched with low frequency to form the output voltage. So switching loss is relatively small. Also, the harmonic level of the output voltage is relatively low if the number of SMs is large enough. Therefore, MMC is known as the most suitable and efficient converter for the HVDC system connecting the offshore wind farm and the medium voltage direct current (MVDC) system [10–13].

Since the HVDC system is operated with the DC voltage of 200–320 kV, the number of SMs in MMC is about 150–300 for each arm. The modulation scheme to form the output voltage normally uses the nearest level control (NLC) that generates stepped sinusoidal waveform. On the other hand, the MVDC system is normally operated with a DC voltage of 2.4–20 kV [14]. The number of SMs in MMC is about 10–50 for each arm. The modulation scheme to form the output voltage normally uses a

phase shift carrier with pulse width modulation (PWM) or NLC considering the switching loss and harmonic levels [15–17].

NLC is simple to implement and has relatively low switching loss due to the low switching frequency. However, the operation level of the output voltage should be set by modulation index (MI). Total harmonic distortion (THD) is rather high when the operation level is low. In particular, the MMC in MVDC can be more influenced due to the small number of SMs [18,19].

This paper proposes a new offset voltage control scheme for the MMC operated in NLC to improve the THD of the output voltages and to generate linear phase voltages in the over-modulation region as well as the normal-modulation region. The operational characteristics of the proposed scheme are first analyzed through a theoretical approach, and then verified by computer simulations with PSCAD/EMTDC software and experiments with a scaled hardware.

2. MMC Operational Characteristics

2.1. Output Voltage Forming

Figure 1 shows a single phase configuration of MMC for ($j = a, b, c$). Each phase is composed of upper and lower arms and two arm reactors, in which N number of SMs is connected in series. In accordance with on/off operation of IGBT switches in the SM, a stepped voltage waveform appears at each arm and the output voltage of each phase can finally be generated by the voltages on the upper and lower arms [20,21].

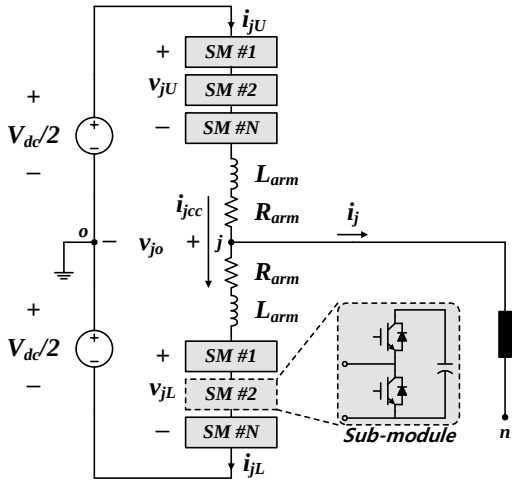


Figure 1. Single-phase circuit diagram for a modular multilevel converter (MMC).

The structure of SM for MMC could be a half-bridge, full-bridge, clamped double bridge, three-level neutral-point-clamped bridge, five-level cross-connected bridge, etc. [22,23]. The SM with the half-bridge is most commonly used in the commercial HVDC system, although other structures of SM have easy handling capabilities for the DC fault current. So, this paper has only considered the SM with a half-bridge structure.

The upper arm voltage v_{jU} by the switching operation of SMs can be expressed with the product of the turn-on number of SMs N_U and the SM voltage v_{cU} as shown in Equation (1). The lower arm voltage v_{jL} can be expressed with the product of the turn-on number of SMs N_L and the SM voltage v_{cL} as shown in Equation (2).

$$v_{jU} = N_U v_{cU} \tag{1}$$

$$v_{jL} = N_L v_{cL} \tag{2}$$

The currents through the upper- and lower-arms are defined by i_{jU} and i_{jL}, and the line current i_j on each phase can be deduced with Equation (3).

$$i_j = i_{jU} - i_{jL} \tag{3}$$

The common circulating current of upper- and lower-arms i_{jcc} can be deduced with Equation (4).

$$i_{jcc} = \frac{i_{jU} + i_{jL}}{2} \tag{4}$$

The currents on the upper- and lower-arms are respectively expressed with Equations (5) and (6), using the relationship of Equations (3) and (4).

$$i_{jU} = \frac{1}{2} i_j + i_{jcc} \tag{5}$$

$$i_{jL} = -\frac{1}{2} i_j + i_{jcc} \tag{6}$$

By applying Kirchhoff's voltage law to the circuit in Figure 1, the terminal voltage v_{jo} can be represented by Equations (7) and (8).

$$v_{jo} = \frac{V_{dc}}{2} - V_{jU} - R_{arm} i_{jU} - L_{arm} \frac{di_{jU}}{dt} \tag{7}$$

$$v_{jo} = -\frac{V_{dc}}{2} + V_{jL} + R_{arm} i_{jL} + L_{arm} \frac{di_{jL}}{dt} \tag{8}$$

Equation (9) can be induced by relating Equations (3), (7), and (8).

$$v_{jo} = \frac{v_{jL} - v_{jU}}{2} - \frac{1}{2} \left(R_{arm} + L_{arm} \frac{d}{dt} \right) i_j \tag{9}$$

According to Equation (9), the voltage drop is caused by the arm reactor. Its phase angle is equivalent to the lower arm voltage v_{jL} and shifted by 180° from the upper arm voltage v_{jU}.

2.2. Modulation and Harmonic Analysis

MMC normally generates the output voltage with PWM and stepped modulation. In PWM the reference signal is compared with triangular carriers to decide the switching position. In stepped modulation the reference signal is divided into segments with a certain time span and the cross point with the reference signal sets the switching position. Stepped modulation has less switching frequency and the generated output voltage changes less suddenly. Equal area method (EAM), selective harmonic reduction method (SHRM), and NLC are typical stepped modulation schemes. The first two schemes generate relatively low levels of harmonics, but require more computations. So, NLC is most widely used in MMC for high power application [24–26].

Figure 2 describes how to generate the output voltage in NLC modulation. NLC applies the rounding-off function to decide the point of level change. NLC generates an output voltage with simple computation close to the sine wave.

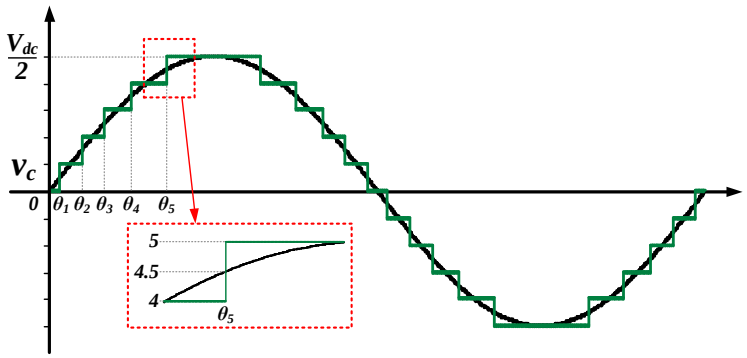


Figure 2. Operational principle of the nearest level control (NLC) modulation.

When MMC operates in NLC, the operation level can be decided by the magnitude of *MI* which is determined by the ratio of AC voltage to DC voltage.

$$MI = \frac{V_{ac \cdot peak}}{V_{dc}/2} \tag{10}$$

The terminal voltage command on the upper- and lower-arms can be defined by the cosine function and *MI*, thereby being expressed as Equations (11) and (12).

$$v^*_{jU\_pole} = \frac{V_{dc}}{2}(1 - MI\cos\omega t) \tag{11}$$

$$v^*_{jL\_pole} = \frac{V_{dc}}{2}(1 + MI\cos\omega t) \tag{12}$$

Figure 3 shows a block diagram for the NLC, and the number of SMs is decided by inputting the voltage command of upper- and lower-arm and rounding off. This method does not support equal charging and discharging for each SM during one power cycle. So, the voltage balancing algorithm for the SM capacitors is required [17–20].

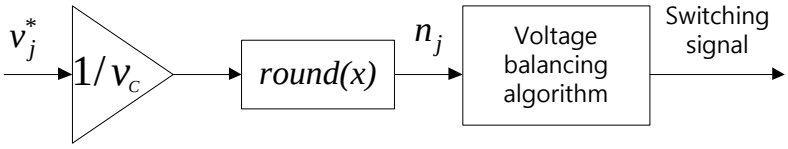


Figure 3. Block diagram for NLC modulation.

The voltage level is an important factor in NLC because it influences the average switching time and the THD of output voltage.

Fourier series for the waveform shown in Figure 2 can be expressed as the following equation.

$$v_{an}(\omega t) = \sum_{n=1}^{\infty} \frac{4V_c}{n\pi}(\cos(n\theta_1) + \cos(n\theta_2) + \cdots + \cos(n\theta_k))\sin(n\omega t) \tag{13}$$

Since the harmonic components only include the odd number of order. The root mean square (RMS) values for the fundamental component and the harmonic components can be expressed as the following equations.

$$\begin{cases} V_1 = \frac{2\sqrt{2}V_c}{\pi}(\cos(\theta_1) + \cos(\theta_2) + \cdots + \cos(\theta_k)) \\ V_3 = \frac{2\sqrt{2}V_c}{3\pi}(\cos(3\theta_1) + \cos(3\theta_2) + \cdots + \cos(3\theta_k)) \\ \vdots \\ V_{31} = \frac{2\sqrt{2}V_c}{31\pi}(\cos(31\theta_1) + \cos(31\theta_2) + \cdots + \cos(31\theta_k)) \end{cases} \tag{14}$$

THD of the output voltage is defined by the following equation.

$$THD_v = \frac{\sqrt{\sum_{n\neq 1} V_n^2}}{V_1} \tag{15}$$

Figure 4 shows calculated THDs for the output voltage with respect to the number of voltage levels when the voltage level is located at $9 \leq N \leq 200$. The THD of the output voltage stays as low as less than 1% if the voltage level is over 40. However, the THD of output voltage is largely changed if the voltage level is lower than 40.

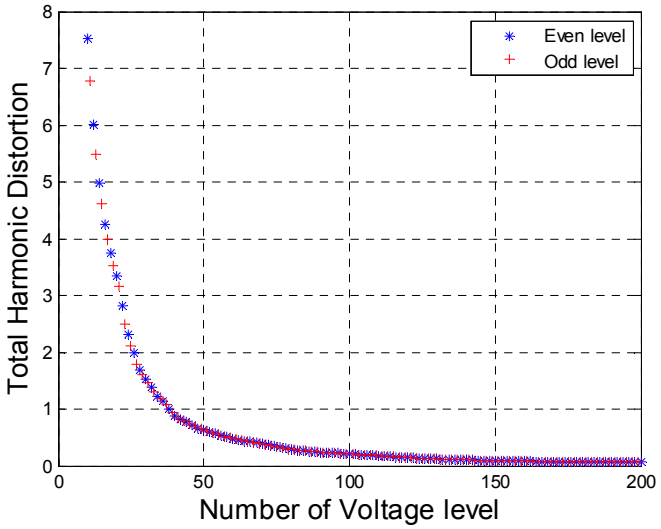


Figure 4. Total harmonic distortion (THD) according to output voltage level.

Figure 5 shows THD calculation results when the range of *MI* is set at $0.6 \leq MI \leq 1$, and in the case that the maximum voltage level is assigned to 10~25, THD can be reduced as the voltage level increases and the *MI* also increases. However, it decreases nonlinearly in a specific range, which is caused by the voltage level suddenly changing due to the *MI*. The timing of this change can be expressed by Equation (16) according to the variable range of *MI*.

$$\begin{cases} N+1 \text{ level} : \text{at} \left(\frac{N-1}{N} \leq MI\right) \\ N-1 \text{ level} : \text{at} \left(\frac{N-3}{N} \leq MI < \frac{N-1}{N}\right) \\ N-3 \text{ level} : \text{at} \left(\frac{N-5}{N} \leq MI < \frac{N-3}{N}\right) \end{cases} \tag{16}$$

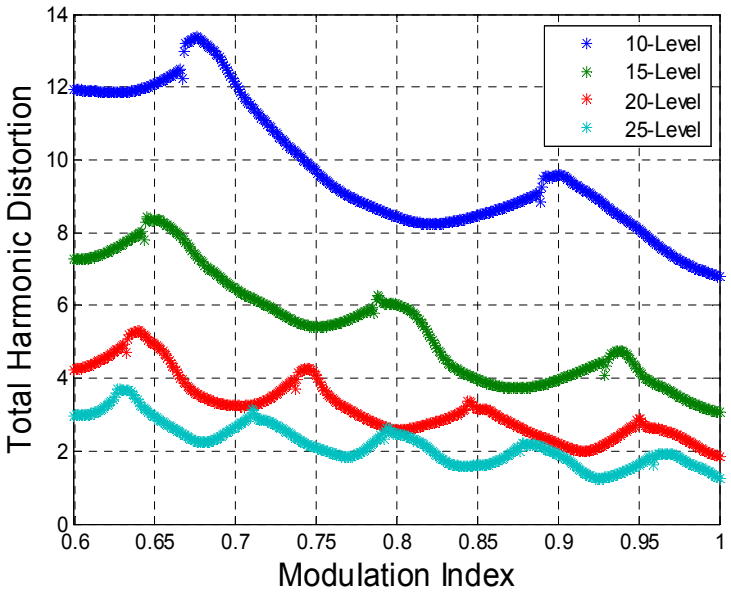


Figure 5. THD with respect to *modulation index* (*MI*) according to number of SMs.

3. Existing Modulation Scheme

Figure 6 shows an equivalent circuit for the MMC operated in NLC. The most traditional scheme is to generate the pole voltage same as the phase voltage command, which is called the sinusoidal modulation. In this case, the maximum phase voltage is limited to the half of the DC voltage. It can be linearly controlled until *MI* becomes 1, but it shows non-linear output when *MI* is over 1. The space vector modulation was a typical scheme to improve the sinusoidal modulation with offset voltage control [27–30].

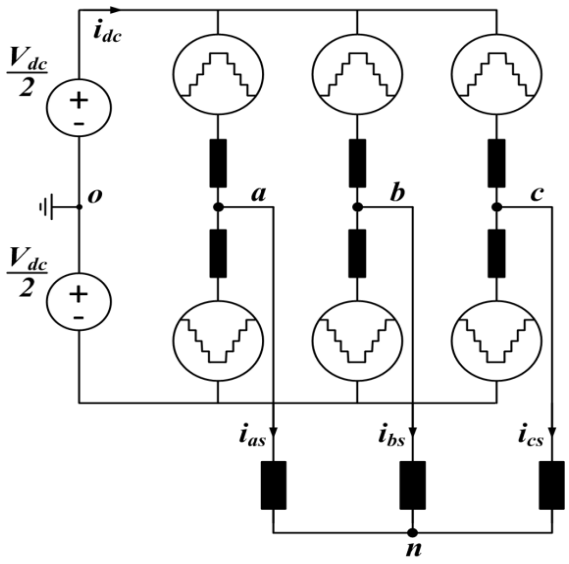


Figure 6. Equivalent Circuit for MMC operated in NLC.

The pole voltage v_{abco} which is the sum of the phase voltage v_{abcn} and the offset voltage v_{no} can be decided by the switching status of SM on each phase of MMC.

$$v_{abco} = v_{abcn} + v_{no} \tag{17}$$

To implement the space vector modulation, the absolute values of maximum and minimum pole voltage should be identically set as Equation (18). In this way, the offset voltage is defined as Equation (19).

$$v^*_{max} + v_{no} = -(v^*_{min} + v_{no}) \tag{18}$$

$$v_{no} = -\frac{v^*_{max} + v^*_{min}}{2} \tag{19}$$

In the space vector modulation, the offset voltage is linearly controlled until the *MI* is equal to $2/\sqrt{3}$. So, the magnitude of output voltage can be enlarged by 15.47% in comparison with the sinusoidal modulation. The reason is that the pole voltage decreases by the offset voltage which is one-sixth of the fundamental component. However, the decrease of MMC output voltage level causes an increase of the average switching frequency, capacitor voltage ripple, and output voltage THD.

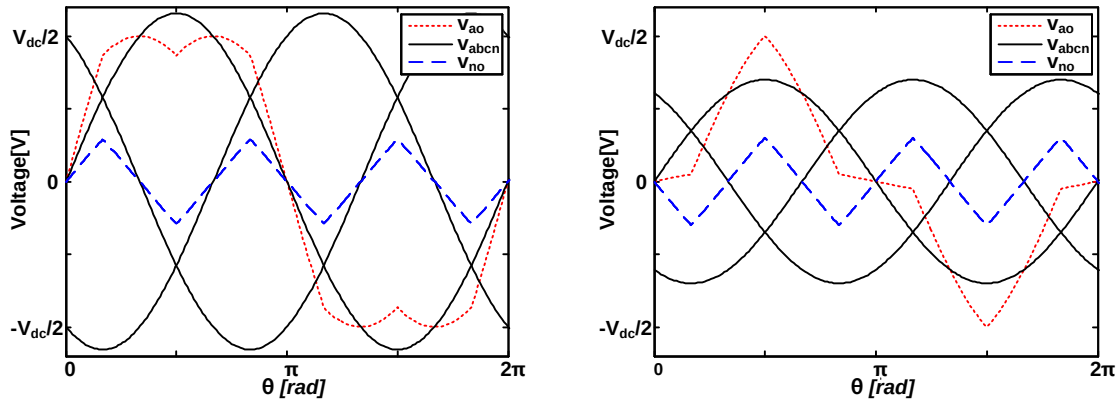
4. Proposed Modulation Scheme

This paper proposes a new scheme to compensate the decrease of the output voltage level so as to generate a constant pole voltage irrespective of the magnitude of *MI*. The proposed method uses a variable offset voltage which is represented by Equation (20).

$$v_{no} = -\alpha\frac{v^*_{max} + v^*_{min}}{2} \tag{20}$$

α is a variable to make the pole voltage constant. It can be induced by using the maximum value equation of the pole voltage and can be divided into two regions by the value of *MI*.

At first, the value of α has been analyzed in the region of $1 \leq MI \leq 2/\sqrt{3}$, where the pole voltage becomes smaller than the phase voltage due to the offset voltage. Figure 7a shows the pole voltage, phase voltage, and offset voltage in this region.



(**a**) $1 \leq MI \leq 2/\sqrt{3}$ (**b**) $0 < MI < 1$

Figure 7. Pole, Phase, and Offset voltages according to *MI*.

Equations (21)–(23) express the phase voltage with *MI* and DC voltage.

$$v_{an} = MI \times \frac{V_{dc}}{2}\sin\omega t \tag{21}$$

$$v_{bn} = MI \times \frac{V_{dc}}{2}\sin\left(\omega t - \frac{2}{3}\pi\right) \tag{22}$$

$$v_{cn} = MI \times \frac{V_{dc}}{2}\sin\left(\omega t + \frac{2}{3}\pi\right) \tag{23}$$

The pole voltage has four cases according to its phase angle. Equations (24)–(27) represent the pole voltages at each section.

$$v_{ao1} = v_{an} + \frac{\alpha}{2} v_{an} \ : at \left(0 \le \omega t_1 < \frac{\pi}{6}\right) \tag{24}$$

$$v_{ao2} = v_{an} + \frac{\alpha}{2} v_{cn} \ : at \left(\frac{\pi}{6} \le \omega t_2 < \frac{\pi}{2}\right) \tag{25}$$

$$v_{ao3} = v_{an} + \frac{\alpha}{2} v_{bn} \ : at \left(\frac{\pi}{2} \le \omega t_3 < \frac{5\pi}{6}\right) \tag{26}$$

$$v_{ao4} = v_{an} + \frac{\alpha}{2} v_{an} \ : at \left(\frac{5\pi}{6} \le \omega t_4 < \pi\right) \tag{27}$$

In order to obtain the maximum value of pole voltage, derivatives for the above equations have to be derived, which are expressed by Equations (28)–(31).

$$\frac{dv_{ao1}}{d(\omega t_1)} = MI \frac{V_{dc}(2+\alpha)}{4} \cos(\omega t_1) \tag{28}$$

$$\frac{dv_{ao2}}{d(\omega t_2)} = MI \frac{V_{dc}\sqrt{(\alpha-1)^2+3}}{4} \cos(\omega t_2 + \delta) \tag{29}$$

$$\frac{dv_{ao3}}{d(\omega t_3)} = MI \frac{V_{dc}\sqrt{(\alpha-1)^2+3}}{4} \cos(\omega t_3 - \delta) \tag{30}$$

$$\frac{dv_{ao4}}{d(\omega t_4)} = MI \frac{V_{dc}(2+\alpha)}{4} \cos(\omega t_4) \tag{31}$$

$$\text{where, } \delta = \tan^{-1} \frac{\sqrt{3}\alpha}{4-\alpha} \tag{32}$$

From the above equations, the phase angle of the pole voltage ωt is calculated as Equations (33)–(36).

$$\omega t_1 = \frac{\pi}{2} \ : at \left(0 \le \omega t_1 < \frac{\pi}{6}\right) \tag{33}$$

$$\omega t_2 = \frac{\pi}{2} - \tan^{-1} \frac{\sqrt{3}\alpha}{4-\alpha} \ : at \left(\frac{\pi}{6} \le \omega t_2 < \frac{\pi}{2}\right) \tag{34}$$

$$\omega t_3 = \frac{\pi}{2} + \tan^{-1} \frac{\sqrt{3}\alpha}{4-\alpha} \ : at \left(\frac{\pi}{2} \le \omega t_3 < \frac{5\pi}{6}\right) \tag{35}$$

$$\omega t_4 = \frac{\pi}{2} \ : at \left(\frac{5\pi}{6} \le \omega t_4 < \pi\right) \tag{36}$$

The maximum value of pole voltage at ωt_2 and ωt_3 can be obtained from Equations (34) and (35). The maximum value of pole voltage at this range is represented by Equation (37), and α can be derived by Equation (38).

$$v_{ao \cdot peak} = MI \frac{V_{dc}}{2} \frac{\sqrt{(\alpha-1)^2+3}}{4} = \frac{V_{dc}}{2} \tag{37}$$

$$\alpha = -\sqrt{\frac{4}{MI^2} - 3} + 1 \ : at \left(1 \le MI \le \frac{2}{\sqrt{3}}\right) \tag{38}$$

In the second, the value of α has been analyzed in the region of $0 < MI < 1$, where the pole voltage becomes larger than the phase voltage because of offset voltage. Figure 7b shows the pole voltage, phase voltage, and offset voltage in this region. The pole voltage always stays at the maximum value in the phase angle of $\omega t = \pi/2$.

In this section, the pole voltage can be defined as Equation (39).

$$v_{ao} = v_{an} + \frac{\alpha}{2} + v_{bn} = v_{an} + \frac{\alpha}{2} v_{cn} = MI \frac{V_{dc}\sqrt{(\alpha-1)^2+3}}{4} \sin(\omega t \pm \delta) \tag{39}$$

where, $\sin(\omega t \pm \delta)$ is equal to $\cos\delta$ at $\omega t = \pi/2$.

From Equation (32) $\cos\delta$ is derived as the following equation.

$$\cos\delta = \frac{4-\alpha}{2\sqrt{(\alpha-1)^2+3}} = \sin\left(\frac{\pi}{2} \pm \delta\right) \tag{40}$$

So, the maximum value of pole voltage is represented by (41). From this equation the value of α can be calculated as shown in Equation (42).

$$v_{ao \cdot peak} = MI \frac{V_{dc}}{2} \times \frac{4-\alpha}{4} = \frac{V_{dc}}{2} \tag{41}$$

$$\alpha = 4 - \frac{4}{MI} \ : at \ (0 < MI \leq 1) \tag{42}$$

Figure 8 shows a graph that is describing the value of α with respect to the range of *MI*. The graph shows that α has negative value when *MI* is smaller than 1.0, while it has positive value when *MI* is larger than 1.0.

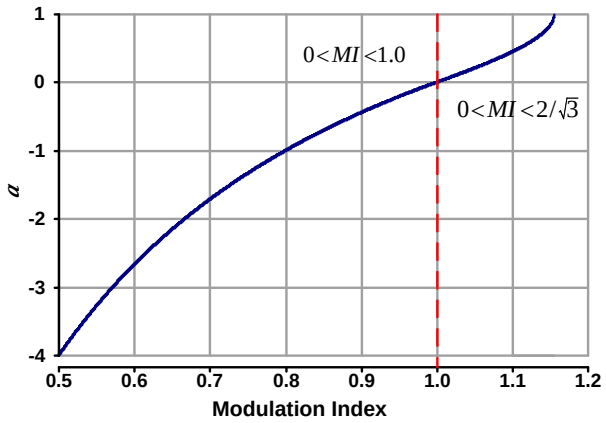


Figure 8. Variable α with respect to *MI*.

Figure 9 shows the algorithm of the proposed offset voltage control including the NLC modulation. The reference of phase voltage is set through sensing the voltage and current and conducting the current control. α is decided according to the value of *MI*. The references of offset voltage and pole voltage are decided by Equations (20) and (17) respectively. The reference of the pole voltage is passed through the NLC algorithm to obtain the switching pulses. The algorithm of the proposed offset voltage control can be easily implemented on the digital signal processor (DSP) board for real-time operation because it does not require a long running time.

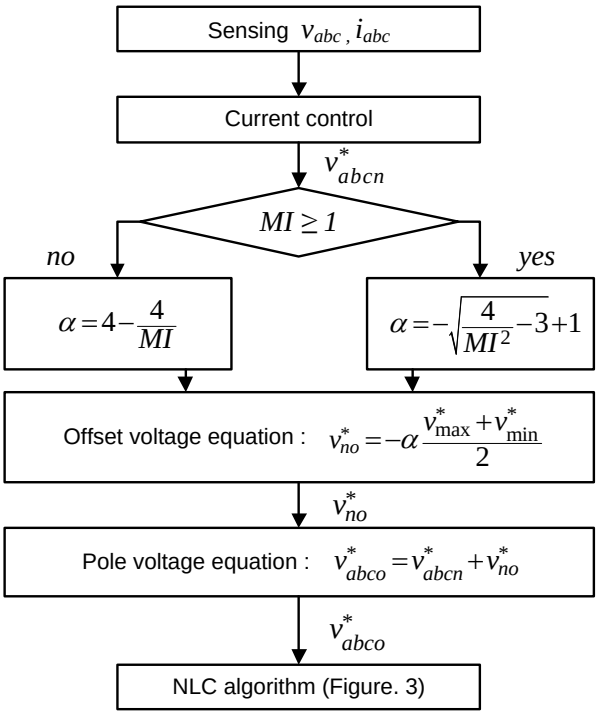


Figure 9. Flowchart of proposed method.

5. Computer Simulation

In order to verify the proposed scheme, simulation model has been implemented with PSCAD/EMTDC software. The circuit parameters for the simulation model are described in Table 1. The proposed offset voltage control has been implemented using the C-code interface module.

Table 1. Circuit Parameters for Simulation Model.

Parameter	Value
Line Voltage (RMS)	22.9 kV
DC Link Voltage	20 kV
Rated Power	25 MVA
Transformer	Y22.9 kV–Δ11.0 kV
Arm Reactor	2.5 mH
SM Capacitor	9600 uF
Number of SMs	12 per Arm

Figure 10 shows the simulation results for the sinusoidal modulation. The pole voltage, phase voltage, offset voltage, and line-to-line voltage are shown according to the change of *MI*. When the *MI* decreases from $2/\sqrt{3}$ to 0.8 with a constant slope, the output voltage level for NLC is decided by Equations (43) and (44). Therefore, the pole voltage decreases to 11-level, where the *MI* is less than 0.9167 because the MMC is designed to be 13-level.

$$N+1 \text{ level } : \text{at } \left(\frac{N-1}{N} \leq MI \right) \tag{43}$$

$$N-1 \text{ level } : \text{at } \left(\frac{N-3}{N} \leq MI < \frac{N-1}{N} \right) \tag{44}$$

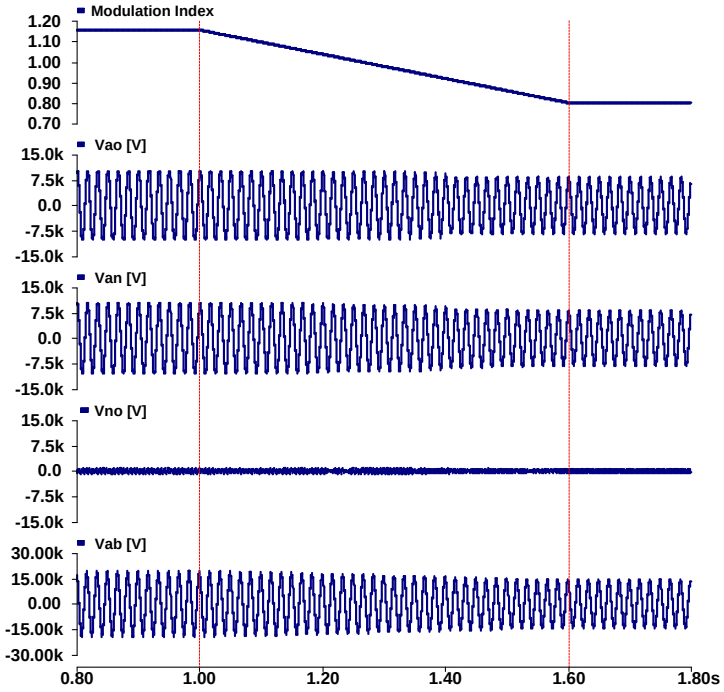


Figure 10. Simulation waveform with sinusoidal method.

Figure 11 shows simulation results for the space vector modulation. In this modulation, the output voltage level is decided by Equations (45)–(47) according to the range of *MI*. Therefore, the pole voltage decreases to 11-level, where the *MI* is less than 1.058. It becomes 9-level, where the *MI* is less than 0.866.

$$N+1 \text{ level } : \text{at } \left(\frac{2}{\sqrt{3}} \frac{N-1}{N} \leq MI \right) \tag{45}$$

$$N-1 \text{ level } : \text{at } \left(\frac{2}{\sqrt{3}} \frac{N-3}{N} \leq MI < \frac{2}{\sqrt{3}} \frac{N-1}{N} \right) \tag{46}$$

$$N-3 \text{ level } : \text{at } \left(\frac{2}{\sqrt{3}} \frac{N-5}{N} \leq MI < \frac{2}{\sqrt{3}} \frac{N-3}{N} \right) \tag{47}$$

Figure 12 shows the simulation results for the proposed NLC modulation. In this modulation, the output voltage level is maintained at 13-level in all range of *MI*. The phase voltage becomes the difference between the pole voltage and the offset voltage. The phase voltage and the line-to-line voltage are linearly generated, which is different from the previous two modulations.

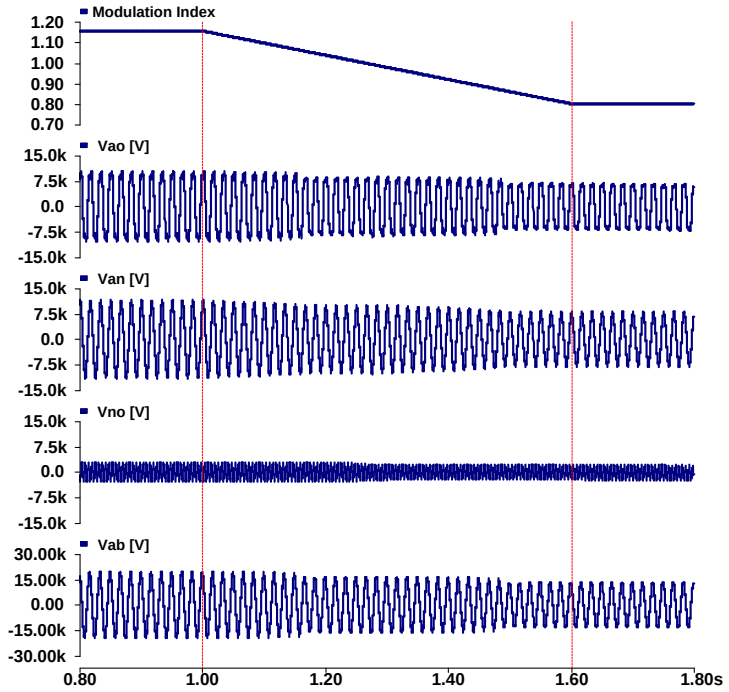


Figure 11. Simulation waveform with space vector method.

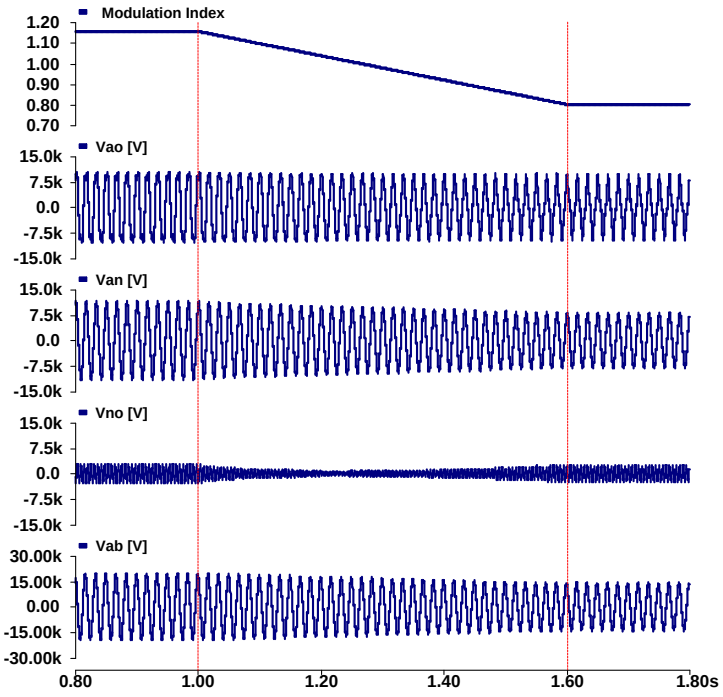
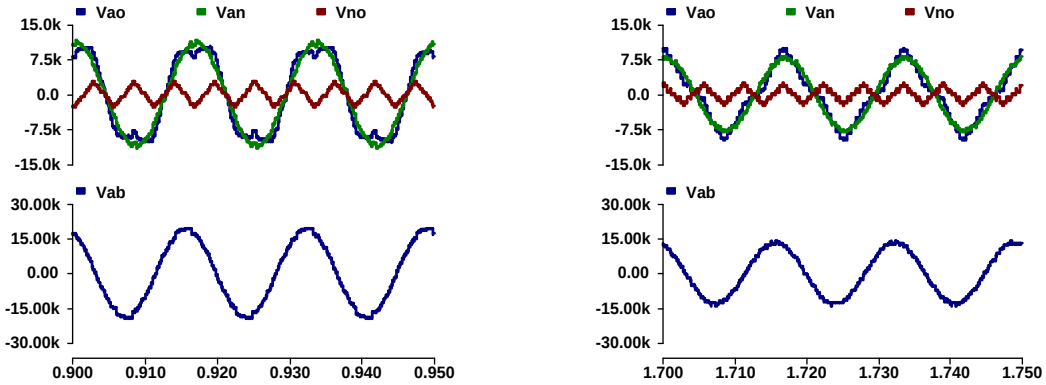


Figure 12. Simulation waveform with proposed method.

Figure 13 describes the expanded waveform for the pole voltage, phase voltage, and offset voltage for two values of *MI*. Figure 13a shows that the phase voltage can be linearly generated at the $MI > 1$ by controlling the offset voltage. Also, Figure 13b shows that the pole voltage is generated at the maximum value that is half of the DC voltage. So, the output voltage is generated with 13-level at the $MI = 0.8$ by controlling the offset voltage.



(**a**) $MI = 2/\sqrt{3}$ (**b**) $MI = 0.8$

Figure 13. Expanded waveforms with proposed scheme.

Table 2 shows the comparison results for three modulation schemes. The proposed scheme maintains the pole voltage level constant irrespective of the change of *MI*. This offers ripple reduction of the SM capacitor voltage and THD reduction of the phase voltage.

Table 2. Comparison of modulation schemes.

Item	Modulation Schemes		
	Sinusoidal	**Space Vector**	**Proposed**
Offset Voltage	-	$v_{no} = -\frac{v^*_{max}+v^*_{min}}{2}$	$v_{no} = -\alpha\frac{v^*_{max}+v^*_{min}}{2}$
Maximum Phase Voltage	$MI \times \frac{V_{dc}}{2}$	$MI \times \frac{V_{dc}}{\sqrt{3}}$	$MI \times \frac{V_{dc}}{\sqrt{3}}$
Maximum Pole Voltage	$MI \times \frac{V_{dc}}{2}$	$MI \times \frac{V_{dc}}{\sqrt{3}}$	$\frac{V_{dc}}{2}$
Output Voltage Level	Dependent on phase voltage magnitude		Independent on phase voltage magnitude

6. Experimental Verification

To verify the proposed scheme though experimental results, a scaled hardware was built in the lab, with circuit parameters that are described in Table 3. In the scaled hardware, each phase has 24 SMs, which is 12 SMs for each upper- and lower-arm. In total 72 SMs are mounted in the rack for implementing 3-phase MMC. The controller consists of one master controller and six arm controllers which were developed by DSP boards based on TMS320F28335. All command signals are delivered down to arm controllers from the master controller.

Table 3. Circuit Parameters for scaled Hardware.

Parameter	Value
Line Voltage (RMS)	380 V
DC Link Voltage	1000 V
Rated Power	10 kVA
Transformer	Y380 V–Δ551 V
Arm Reactor	5 mH
SM Capacitor	3300 uF
Number of SMs	12 per Arm

Figure 14 shows the experimental results for the sinusoidal modulation, which show the pole voltage, phase voltage, and offset voltage according to the change of *MI*. When the *MI* decreases from $2/\sqrt{3}$ to 0.8 with constant slope, the pole voltage decreases to 11-level where the *MI* is less than 0.9167.

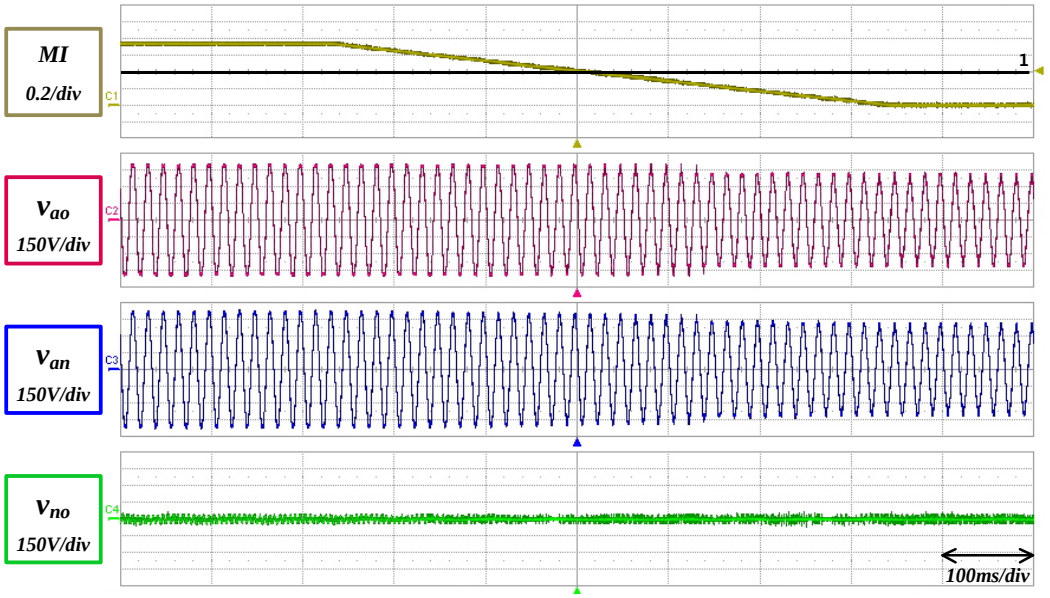


Figure 14. Hardware waveform with sinusoidal method.

Figure 15 shows the experimental results for the space vector modulation when the *MI* is changed with same way. The output voltage was checked to become 11-level where the *MI* is less than 1.058. Also, it was checked to become 9-level where the *MI* is less than 0.866.

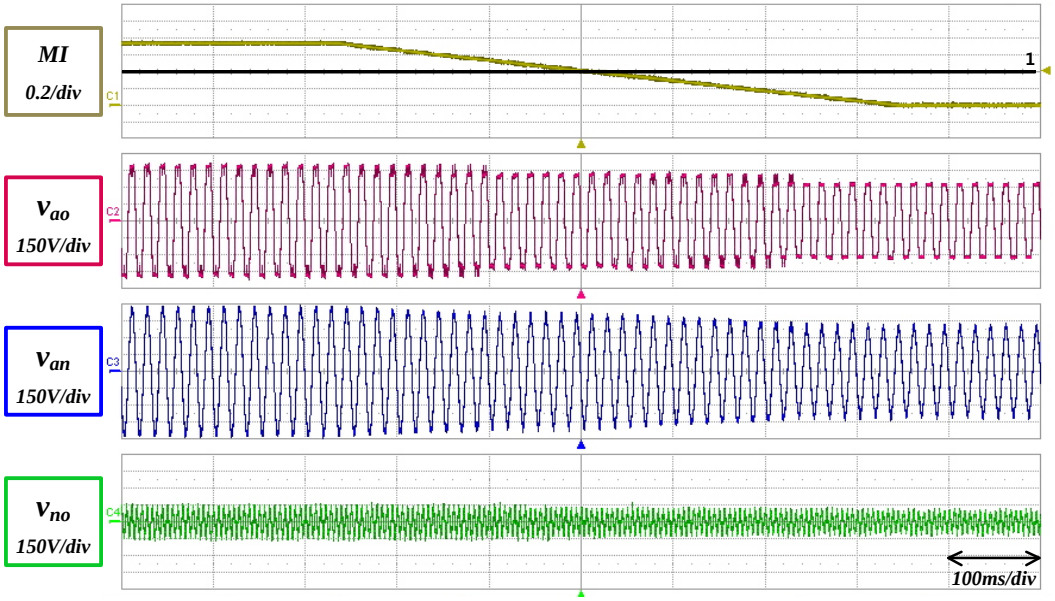


Figure 15. Hardware waveform with space vector method.

Figure 16 shows the experimental results for the proposed modulation, when the *MI* is changed in the same way. The pole voltage shows a constant maximum level in all ranges and the phase voltage is generated by the difference between the terminal voltage and the offset voltage. The generated phase voltage is relatively linear in comparison with other two modulations.

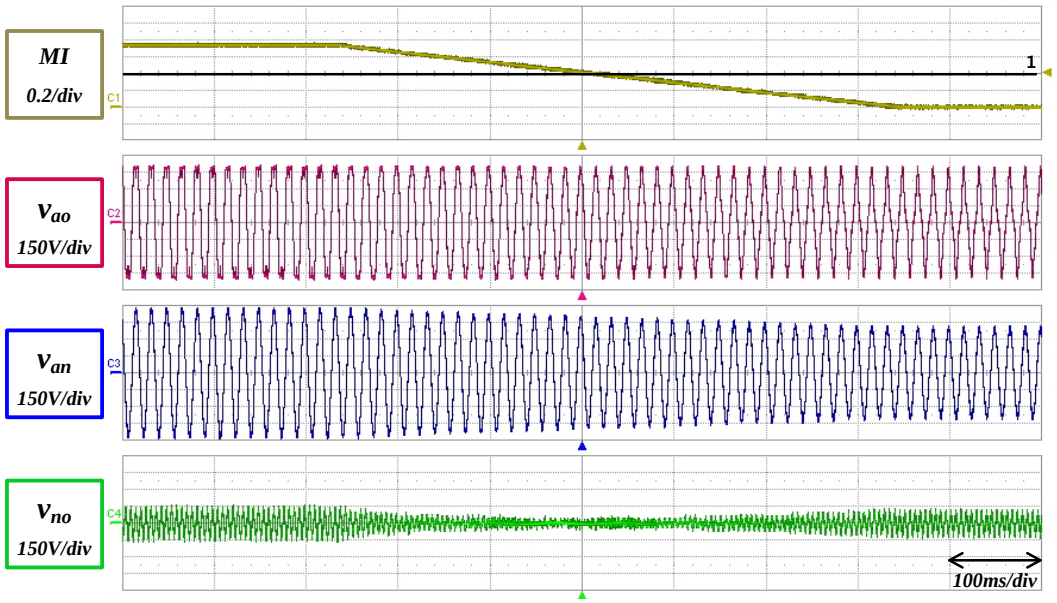
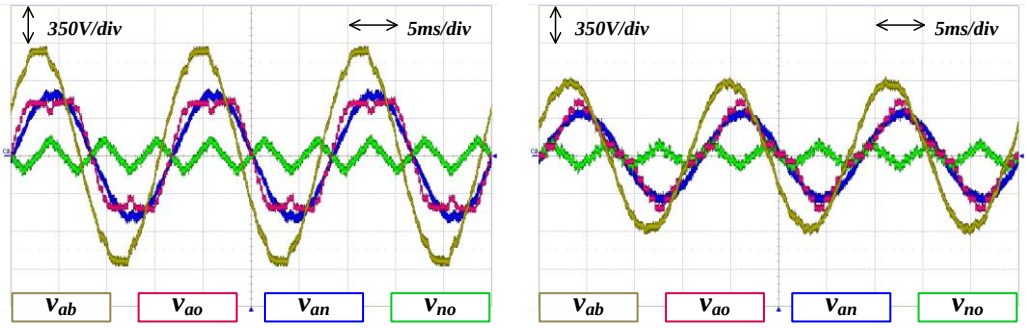


Figure 16. Hardware waveform with proposed method.

Figure 17a shows expanded waveforms for the pole voltage, phase voltage, line-to-line voltage, and offset voltage when the MMC is operated in 13-level at $MI = 2/\sqrt{3}$. The THDs of the pole voltage and the line-to-line voltage are 21.02% and 2.07% respectively. In order to decrease the magnitude of the pole voltage less than the phase voltage, the offset voltage is added. Figure 17b shows the same voltages for when the MMC is operated in 13-level at $MI = 0.8$. The THDs of the pole voltage and the line-to-line voltage are 22.24% and 2.17% respectively. In order to increase the magnitude of the pole voltage larger than the phase voltage, the offset voltage is added. Both waveforms confirm that the pole has a constant maximum level in all the ranges of MI.



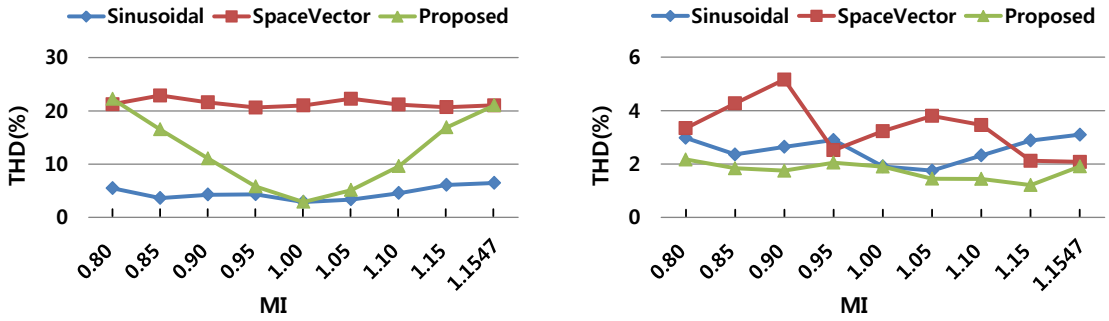
(**a**) Waveforms at $MI = 2/\sqrt{3}$ (**b**) Waveforms at $MI = 0.8$

Figure 17. Expanded waveforms with proposed modulation.

Figure 18 shows the comparison results of THD for three modulation schemes with respect to the MI change. The space vector modulation has the offset voltage that is one-third of fundamental voltage. So, THD of pole voltage has a constant value in the MI range from 0.8 to 1.1547. On the other hand, the THD is changeable in the proposed modulation. The THD of line-to-line voltage shows greater improvement than the other two modulations.

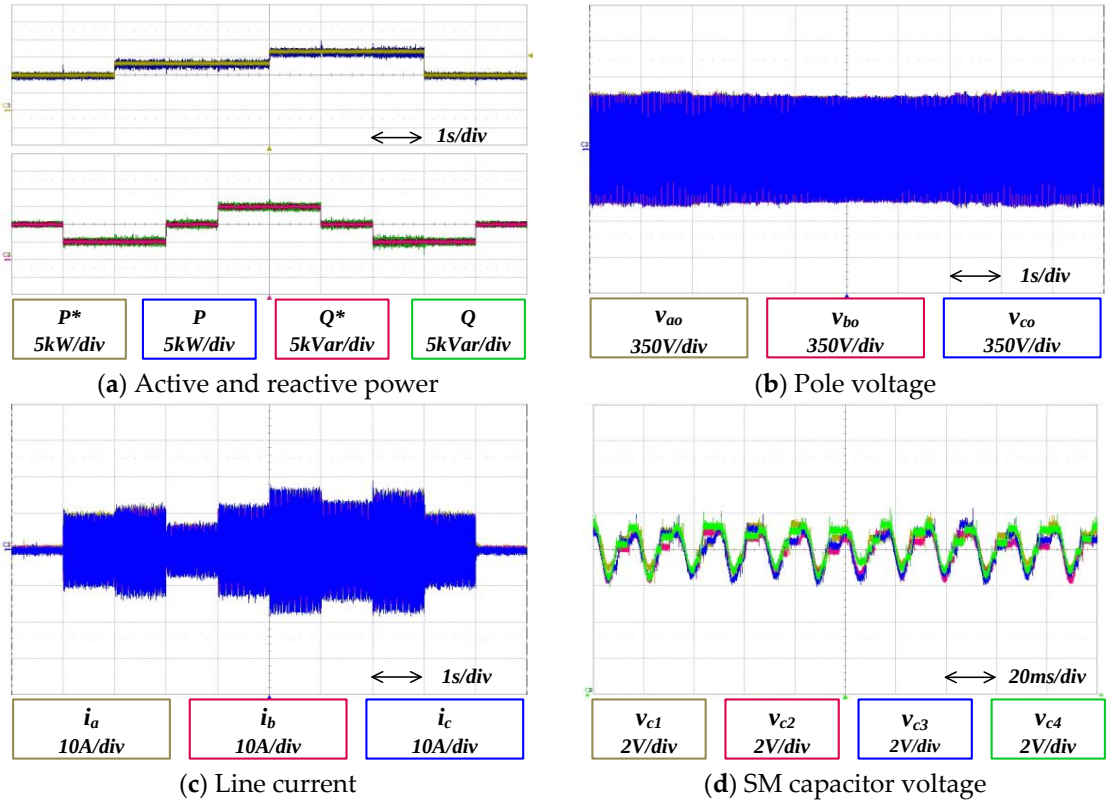
Figure 19a shows the active power and reactive power variations with step manner, in which the active power P changes 0, 5, 10, 0 kW and the reactive power changes 0, −10, 0, 10, 0, −10, 0 kVar. The measured active- and reactive-power follow the command values accurately. Figure 19b shows

the generated pole voltage which is accurately controlled in magnitude and phase. Figure 19c shows the line current which changes with step manner according to the active- and reactive power change. Figure 19d shows variations of the SM capacitor voltage when the active power is 8 kW and the reactive power −6 kVar. The SM capacitor voltage shows balanced although irregular ripples exist due to the sudden voltage change.



(**a**) Pole voltage (**b**) Line-to-line voltage

Figure 18. THD analysis results for three modulation schemes.



(**a**) Active and reactive power (**b**) Pole voltage

(**c**) Line current (**d**) SM capacitor voltage

Figure 19. Major waveforms with proposed method.

7. Conclusions

This paper proposes a new offset voltage control scheme for the MMC operated in NLC to improve the THD of the output voltages and to generate linearly variable phase voltages in the over-modulation region as well as the normal-modulation region.

The feasibility of the proposed scheme was analyzed with computer simulations for the 25 MVA 20 kV MMC with 12 SMs per each arm. Based on the simulation results, a scaled hardware with

10 kVA 1000 V rating was built in the lab and tested to confirm the feasibility of actual implementation. Experimental results also confirm that the proposed offset voltage control is very effective to reduce the THDs of the phase voltage in the whole range of *MI*. The NLC modulation with proposed offset voltage control is expected to be widely applicable for the MMC of the medium voltage DC system which is composed of relatively smaller numbers of SMs.

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Nomenclature

EAM	Equal area method	N_U	Turn-on number of upper arm SMs
HVDC	High voltage direct current	N_L	Turn-on number of lower arm SMs
IGBT	Insulated gate bipolar transistor	V_{ac}	Output AC voltage
MI	Modulation index	V_{dc}	DC link voltage
MVDC	Medium voltage direct current	v_{abco}	Pole voltage
N	Number of sub-modules	v_{abcn}	Phase voltage
NLC	Nearest level control	v_{jo}	Pole voltage
PSC	Phase shift carrier	v_{jn}	Phase voltage
PWM	Pulse width modulation	v_{jL}	Lower arm voltage
SHRM	Selective harmonic reduction method	v_{jU}	Upper arm voltage
SM	Sub-module	$v_{jo\cdot peak}$	Maximum value of pole voltage
THD	Total harmonic distortion	v_j^*	Voltage command
i_j	Phase current	$v_{jU\_pole}^*$	Upper arm pole voltage reference
i_{jcc}	Circulating current	$v_{jL\_pole}^*$	Lower arm pole voltage reference
i_{jL}	Lower arm current	v_{no}	Offset voltage
i_{jU}	Upper arm current	v_{max}^*	Maximum pole voltage
j	*a*-, *b*-, *c*-phase	v_{min}^*	Minimum pole voltage

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