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Modified Synchronous Reference Frame Based Shunt Active Power Filter with Fuzzy Logic Control Pulse Width Modulation Inverter

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Abstract: Harmonic distortion in power networks has greatly reduced power quality and this affects system stability. In order to mitigate this power quality issue, the shunt active power filter (SAPF) has been widely applied and it is proven to be the best solution to current harmonics. This paper evaluates the performance of the modified synchronous reference frame extraction (MSRF) algorithm with fuzzy logic controller (FLC) based current control pulse width modulation (PWM) inverter of three-phase three-wire SAPF to mitigate current harmonics. The proposed FLC is designed with a reduced amount of membership functions (MFs) and rules, and thus significantly reduces the computational time and memory size. Modeling and simulations of SAPF are carried out using MATLAB/Simulink R2012a with the power system toolbox under steady-state condition, and this is followed with hardware implementation using a TMS320F28335 digital signal processor (DSP), Specrum Digital Inc., Stafford, TX, USA. The results obtained demonstrate a good and satisfactory response to mitigate the harmonics in the system. The total harmonic distortion (THD) for the system has been reduced from 25.60% to 0.92% and 1.41% in the simulation study with and without FLC, respectively. Similarly for the experimental study, the SAPF can compensate for the three-phase load current by reducing THD to 5.07% and 7.4% with and without FLC, respectively.

Keywords: active power filter (APF); modified synchronous reference frame (MSRF) d-q theory; fuzzy logic controller (FLC); low pass filter (LPF); high pass filter (HPF); band pass filter (BPF)

1. Introduction

Nowadays the growth of power quality problems due to power electronic equipment such as adjustable speed drive, programmable logic controller, electronic lightning, together with other nonlinear loads, is an issue for power engineers. This problem generates harmonics and thereby causes changes in the electrical nature of the current and voltage of the power supply. The problem leads to significant economic losses due to fact that some electrical equipment are sensitive to this power quality problem [1]. The active power filters (APFs) are widely preferred over passive filters as a solution to various power quality (PQ) problems arising from the load or source [2]. This is because passive filters have many drawbacks such as resonance with the system impedance, heavy weight and bulky sizes, sensitivity to the system parameter variation, and possible system overload by ambient harmonic load [3–5].

Among various types of active power filters, shunt active power filter (SAPF) is the most widely applied tool in mitigating current harmonics generated by non-linear loads [6,7]. The performance of SAPF strictly depends on three important parts which are significant in its design; these include the control strategy employed in reference current generation, DC bus voltage control, and the current control used for switching pulses' generation for the inverter [8–12]. Employing a proportional-integral (PI) controller in the current control scheme of the pulse width modulation voltage source inverter (PWM-VSI) of SAPF is troubling. It requires precise linear mathematical models which are hard to obtain in practice. Furthermore, due to its severe dynamic interactions among the flow of active and reactive power, it may not provide satisfactory results under parameter variations and load disturbances [13]. These drawbacks are resolved with the introduction of fuzzy logic controller (FLC), as it does not require any tedious mathematical model and works with imprecise inputs. In addition, it is also capable of handling non-linearity and is more robust than the conventional PI regulators. The only challenge in operating FLC for SAPF applications lies in hardware limitations, such as memory, speed, and cost, which make it difficult to execute all sets of rules adequately in a complex system that requires multiple inputs' and multiple outputs' controllers.

In the context of the FLC-based current control scheme, a hierarchical neuro-fuzzy approach has been applied to improve the performance of the current control scheme [10]. However, the hierarchical neuro-fuzzy approach requires the implementation of two-stage FLCs which greatly increases the complexity of the designed current control scheme. Besides, it requires a large design of fuzzy membership functions (MFs) and control rules: (3×3) membership functions with nine rules for the first stage FLC and (5×5) membership functions with 25 rules for the second stage FLC.

Therefore, this study presents a single stage FLC current control scheme with a reduced amount of fuzzy membership functions and control rules to avoid complexities and to consequently reduce the computational time and memory size significantly. The controller's speed will be increased due to a substantial decrease in the size of the rule base and the number of FLC circuits. More importantly, the proposed FLC-based current control scheme greatly reduces system requirements for practical implementation. The design concept and effectiveness of the proposed algorithm are verified using MATLAB-Simulink. Moreover, a laboratory prototype is developed with the proposed algorithm downloaded in the TMS320F28335 digital signal processor (DSP) for further validation.

The paper is organized as follows. In Section 2, the proposed SAPF is described. Section 3 presents the details of the harmonics extraction algorithm used in the SAPF. Then Section 4 presents the FLC-based current control scheme. The simulation and experimental results are presented and discussed in Sections 5 and 6, respectively. Finally, Section 7 concludes and highlights the significant contributions of this work.

2. Proposed SAPF

The proposed three-phase SAPF is connected at the point of common coupling (PCC) between the three-phase supply and the nonlinear load, as shown in Figure 1. The nonlinear load consists of a three-phase full bridge rectifier which is further connected to an inductive (RL) load. The SAPF operates by injecting compensation current into the utility via PCC to cancel out the current harmonics and at the same time drawing a small amount of current from the utility to regulate its switching losses. It can be used to eliminate current harmonics and compensate reactive power at the source side. The instantaneous current and the source voltage are expressed as follows:

$$i_S(t) = i_L(t) + i_C(t) \tag{1}$$

$$v_S = V_{Sm} sin\, \omega t \tag{2}$$

where $i_S(t)$ is the source current, $i_L(t)$ is the load current, and $i_C(t)$ is the compensation current. v_S is the source voltage while V_{Sm} is the maximum peak value of the source voltage.

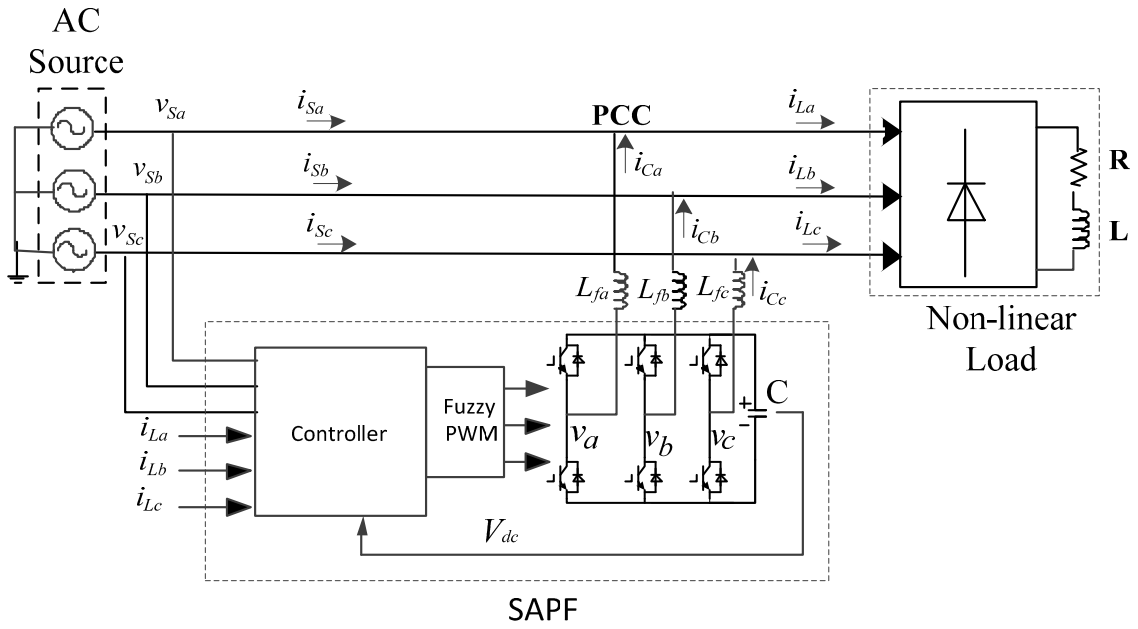


Figure 1. Block diagram of the three phase shunt active power filter (SAPF).

3. Control Strategies

Control strategies for generating compensation currents can be achieved through frequency domain or time domain correction techniques. In the frequency domain, the control strategy for the extraction of compensation commands is based on Fourier analysis of the distorted voltage or current signals [3,14]. Among its setbacks are that this technique involves mathematical computation, which requires time to be executed. Furthermore, for better performance, a good and fast processor must be employed. However, the control strategy in the time domain technique is easy to implement and does not require many mathematical manipulations. It is applied based on the instantaneous derivation of compensation commands in the form of either current or voltage of the distorted signal. In the time domain control technique, the numerical filter is a key issue in the separation of fundamental components from the harmonics. This is an important operation that requires filters such as a low pass filter (LPF), high pass filter (HPF), or band pass filter (BPF). Various control strategies have been used in the generation of the harmonic reference signal from the load current in the time domain, such as the synchronous reference theory (SRF) or d-q theory [15–17], synchronous detection (SD) method [18], and instantaneous power theory or p-q theory [19]. The SRF method is extensively used in three-phase systems and is recognized as the most simple and easily implemented technique in harmonic extraction. When compared with the p-q theory and SD method, the SRF method provides the best compensation performance as it is insensitive to voltage perturbations.

3.1. Modified Synchronous Reference Frame (MSRF)

In this work, the MSRF technique is employed for the extraction of the harmonics so as to generate the reference signals. This method is based on the SRF technique, and it consists of simplified unit vector generation instead of the phase-locked loop (PLL) circuit for synchronization purposes [20,21], DC bus capacitor for voltage regulation, and stationary/rotating frames for the extraction of harmonic currents [14]. Although the MSRF technique shares a few similar features with the conventional SRF method, the main difference is in the calculation of rotating angles for the reference d-q frame [22–25]. Despite using the α-β voltages for calculating the transformation angle, low pass filters (LPF) are used in reducing the voltage harmonics of the input signals, and are consequently used in control process. This filter is essential because the method becomes less affected by harmonics from the source

voltage [15,26]. The extracted signal is compared with the compensation or inverter's current so as to produce the required pulses for the inverter. Figure 2 shows the diagram of the modified SRF method.

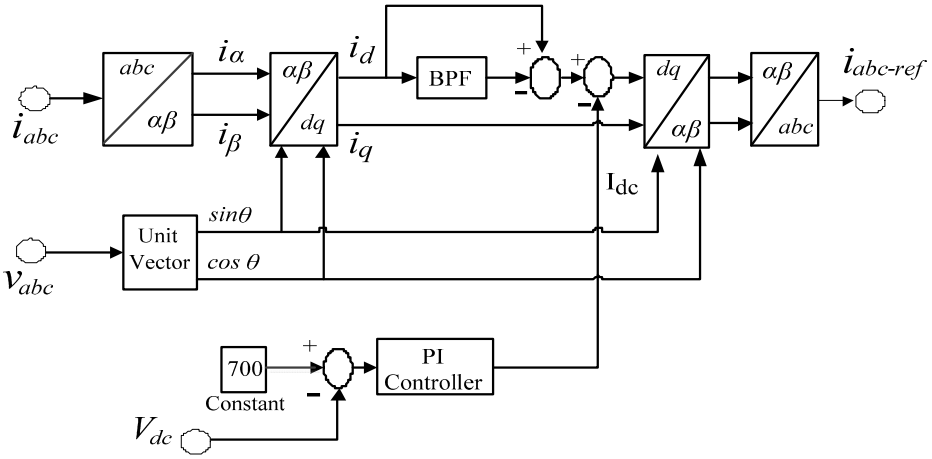


Figure 2. Block diagram of modified synchronous reference frame (MSRF) method.

In implementing the MSRF method, the three-phase supply currents i_a, i_b, and i_c are transformed into the two-phase (α-β) current in the stationary frame, with i_α and i_β as described by Equation (3).

$$\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = \begin{bmatrix} 1 & -\frac{1}{2} & \frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \tag{3}$$

Next, in order to transform from the α-β plane to the d-q rotating frame, the unit vector circuit is applied to produce sine and cosine signals, so as to ensure proper synchronization of the current with the utility voltage. In the d-q frame, the current expression is given by

$$\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \begin{bmatrix} sin(\theta) & -cos(\theta) \\ cos(\theta) & sin(\theta) \end{bmatrix} \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} \tag{4}$$

where θ represents the phase angle of the voltage.

At properly selected frequencies, the entire harmonics with the DC quantities are transformed to non-DC quantities using a band pass filter:

$$\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \begin{bmatrix} \bar{i}_d + \tilde{i}_d \\ \bar{i}_q + \tilde{i}_q \end{bmatrix} \tag{5}$$

where $\bar{i}_d$ (fundamental) and $\tilde{i}_d$ (distorted) represent the fundamental and harmonic components of the d-frame load current. A similar relation holds for the $\bar{i}_q$ (fundamental) and $\tilde{i}_q$ (distorted) components.

Once the required harmonics components are eliminated from the distorted load current, the algorithm is further developed to compute the desired reference current signals; hence, the d-q rotating frame is transformed back to the stationary frame. Thus i_α and i_β are obtained as given below:

$$\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = \begin{bmatrix} sin(\theta) & -cos(\theta) \\ cos(\theta) & sin(\theta) \end{bmatrix}^{-1} \begin{bmatrix} \tilde{i}_d \\ \tilde{i}_q \end{bmatrix} \tag{6}$$

The reference currents $i_{\alpha-ref}$ and $i_{\beta-ref}$ are given by

$$\begin{bmatrix} i_{\alpha-ref} \\ i_{\beta-ref} \end{bmatrix} = \begin{bmatrix} sin(\theta) & cos(\theta) \\ -cos(\theta) & sin(\theta) \end{bmatrix} \begin{bmatrix} \widetilde{i}_d \\ \widetilde{i}_q \end{bmatrix} \tag{7}$$

Lastly, in the *abc* frame the currents are given thus:

$$\begin{bmatrix} i_{a-ref} \\ i_{b-ref} \\ i_{c-ref} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & 0 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} \\ \frac{1}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} i_{\alpha-ref} \\ i_{\beta-ref} \end{bmatrix} \tag{8}$$

These extracted reference currents are utilized for the generation of switching pulses for the inverter.

3.2. Unit Vector

For generating the synchronization vector, a simple and efficient approach is adopted in calculating the output of the unit vector model in the MSRF method. Figure 3 shows the diagram of a unit vector generation.

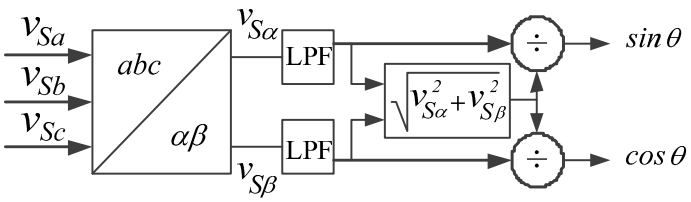


Figure 3. Block diagram of the unit vector generation.

It has an important characteristic of contributing to the balance of the AC voltage network [7]. Ideally the main voltage and current are assumed to be sinusoidal without any phase shift between each other regardless of the load current composition. Thus, the desired source voltage can be given as

$$\begin{aligned} v_{Sa} &= V_{Sm}\, sin(\omega t) \\ v_{Sb} &= V_{Sm}\, sin(\omega t - 120^o) \\ v_{Sc} &= V_{Sm}\, sin(\omega t + 120^o) \end{aligned} \tag{9}$$

where V_{Sm} denotes the peak value of the source voltage and ω is the angular fundamental frequency. The unit voltage model is determined by the equation below.

$$\begin{aligned} \tfrac{v_{Sa}}{V_{Sm}} &= sin(\omega t) \\ \tfrac{v_{Sb}}{V_{Sm}} &= sin(\omega t - 120^o) \\ \tfrac{v_{Sc}}{V_{Sm}} &= sin(\omega t + 120^o) \end{aligned} \tag{10}$$

The unit sine vector model has an amplitude equal to unity in the steady-state, while it varies in accordance to the load variation in the transient condition.

$$\begin{bmatrix} v_{S\alpha} \\ v_{S\beta} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & \frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} v_{Sa} \\ v_{Sb} \\ v_{Sc} \end{bmatrix} \tag{11}$$

Next, for generating the synchronizing vector, instantaneous source voltages are sensed and then computed. The process involves transforming three-phase supply voltage to α-β voltage by the Clarke

transformation as in Equation (11). The output of the Clarke transformation is the voltage in α-β coordinates, which can be simplified as in the equations below.

$$\begin{aligned} v_{S\alpha} &= \frac{\sqrt{3}}{2} V_{Sm}\, sin(\omega t) \\ v_{S\beta} &= \frac{\sqrt{3}}{2} V_{Sm}\, cos(\omega t) \end{aligned} \tag{12}$$

The generated estimated space vector magnitude is given by Equation (13);

$$\overline{V_S} = \overline{V_{S\alpha\beta}} = v_{S\alpha} + j v_{S\beta} = \sqrt{{v_{S\alpha}}^2 + {v_{S\beta}}^2} \tag{13}$$

By dividing the α-β components of the source voltage with the magnitude of space vector, the unit vector generation is thus defined as

$$cos\,\theta = \frac{v_{S\alpha}}{\sqrt{{V_{S\alpha}}^2 + {V_{S\beta}}^2}} = \frac{\left(\sqrt{3}/2\right) V_{Sm}\, sin(\omega t)}{\left(\sqrt{3}/2\right) V_{Sm}} = sin(\omega t) \tag{14}$$

$$sin\,\theta = \frac{v_{S\alpha}}{\sqrt{{V_{S\alpha}}^2 + {V_{S\beta}}^2}} = \frac{-\left(\sqrt{3}/2\right) V_{Sm}\, sin(\omega t)}{\left(\sqrt{3}/2\right) V_{Sm}} = -cos(\omega t) \tag{15}$$

One advantage of this scheme is the fact that angle θ is evaluated straight from the source voltage and thus enablies it to be frequency independent. The low pass filters (LPFs) shown in Figure 3 are used to decrease the voltage harmonics at the input source.

4. Fuzzy Logic Current Control

The quality of the applied current control strategy influences the performance of the PWM voltage source inverter. In order to implement the direct current control technique, both load and compensation currents are sensed [27–31]. The three output reference signals are obtained using the reference current extraction control technique. The PWM switching pulses are generated by sensing the three-phase compensation currents from the SAPF and by comparing with their reference extracted signals. The hysteresis technique and sinusoidal PWM technique are widely used by many researchers, due to their simplicity and fast dynamic responses. However, the major setback of the hysteresis current controller in the operation of SAPF is uneven switching frequency which leads to acoustic noise and difficulty in designing input filters during load variation [32]. The challenge due to the switching frequency can be minimized by reducing the band width of the hysteresis band. However, this increases the current error and thus, produces more distortion in the output current. In order to reduce this problem to a certain extent, a fuzzy PWM controller is used to improve the performance of the VSI. Pulse width modulation (PWM) is a powerful technique for controlling analog circuits in digital form with a microprocessor's digital outputs. The key advantage of the PWM technique is that the on-off behavior changes the average power of the signal with the output signal alternates between on and off within a specified period. This helps to control the delivered power, so that power loss in the switching devices is very low. The PWM switching frequency must be higher than the working frequency of the load (the connected equipment), which means that the resultant waveform observed by the load must be as smooth as possible.

Recently, FLC has been an interesting and fruitful area for research. The concept was first developed by Zadeh in 1965 [33,34]. It is used instead of classical conventional controllers like the proportional integral and derivative (PID) and proportional and integral (PI) to improve the performance of a system. It is a simple idea comprised of four different parts: fuzzifier, knowledge base, inference, and defuzzifier. Fuzzy logic incorporates human skills and the experience of the operator in the design of a controller for adjusting a process whose input-output relationship is defined by a group of fuzzy control rules. Initially, a crisp set of input data is collected and transformed to

a fuzzy set using fuzzy linguistic variables, fuzzy linguistic terms, and membership functions [35]. This is known as fuzzification. Knowledge base comprises data and the rule base so as to coordinate with the other unit. Meanwhile, inference is developed based on this set of rules. Finally, the result is converted back into a specific control output value at the defuzzification stage. One advantage of fuzzy logic control is that it does not require any accurate mathematical model of a system [36].

In this work, the FLC is designed with two inputs known as error and change in error (e and ce) and an output called actuatinsig. Figure 4 shows the diagram of the input variables while Figure 5 shows the output variable. By referring to phase a, the error signal e is the variance between the extracted current reference i_{a-ref} and compensation or inverter current i_{a-inv} from VSI.

$$\text{Error} = i_{a-inv} - i_{a-ref} \tag{16}$$

The Mamdani "min" inference engine was employed due to its simplicity and easy implementation. The design controller consists of the following specifications:

- For the two input variables, three fuzzy sets are configured involving two Bell functions and one Gaussian membership function, that are N (negative), Z (zero), and P (positive), as shown in Figure 4.
- In the case of output variables, five fuzzy sets comprised of the triangular membership function are configured as shown in Figure 5, N (negative), LN (less negative), Z (zero), LP (less positive), and P (positive).
- Defuzzification using centroid means.

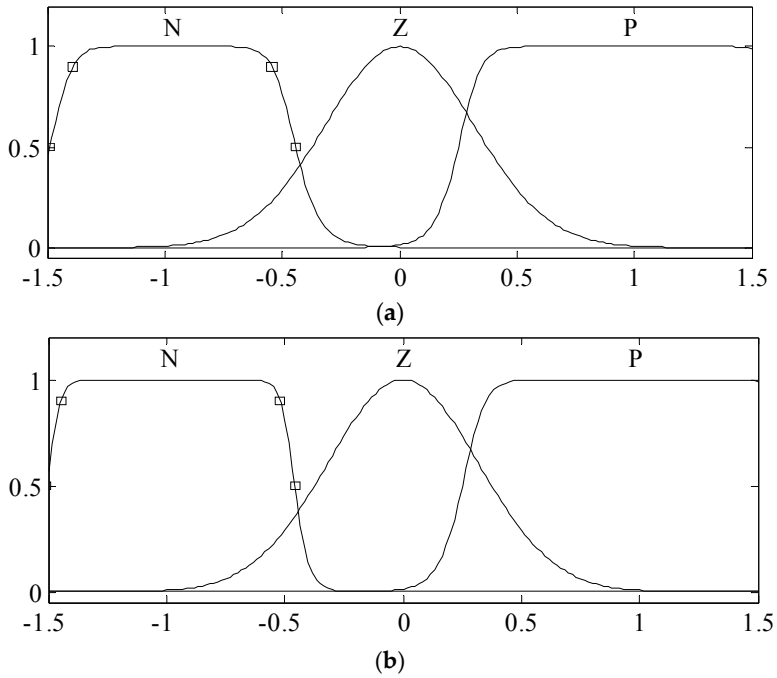


Figure 4. Inputs variables of fuzzy logic controller (FLC): (**a**) "e" and (**b**) "ce".

Below are the nine rules used in this FLC. Table 1 shows the fuzzy rule table.

1. If (error is N) and (c error is N) then (output is N).
2. If (error is N) and (c error is Z) then (output is LN).
3. If (error is N) and (c error is P) then (output is Z).
4. If (error is Z) and (c error is N) then (output is LN).

5. If (error is Z) and (c error is Z) then (output is Z).
6. If (error is Z) and (c error is P) then (output is LP).
7. If (error is P) and (c error is N) then (output is Z).
8. If (error is P) and (c error is Z) then (output is LP).
9. If (error is P) and (c error is P) then (output is P).

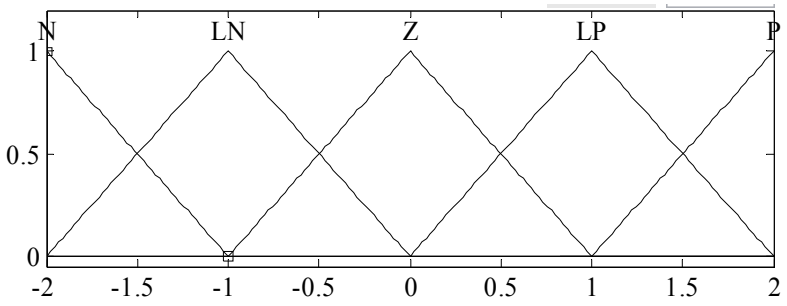


Figure 5. Output variable "actuatinsig" of FLC.

Table 1. Fuzzy-rule table.

Change in Error (ce)	Error (e)		
	N	**Z**	**P**
N	N	LN	Z
Z	LN	Z	LP
P	Z	LP	P

The design is made with few membership functions so as to reduce the complexity and increase the speed. Increasing the fuzzy rules will lead to more implementation costs, less efficiency, and tough tuning routines.

The change in the error signal is derived from the error signal and is determined by incorporating a unit delay block on the control path. The error and change in the error signals are transformed to smaller values and moved into a saturation block by means of scaling components. The saturation block enforces the upper and lower bounds on the signal (taking values between −0.522 to 0.522). If the input signal bounds fall inside specified lower and upper limits, the input signal passes without any alteration. Meanwhile, if the input signal falls not within a specified range, the signal is cropped at the upper or lower bounds. The result from the saturation blocks functions as an input tfor the fuzzy logic regulators. The output of the fuzzy logic regulators is used in generating switching signals for VSI. The carrier signal has values between −0.44 to 0.44 with a switching frequency of 12.5 kHz. The switching diagram (with the PWM-fuzzy logic technique) used for the generation of pulses for each phase, is shown in Figure 6.

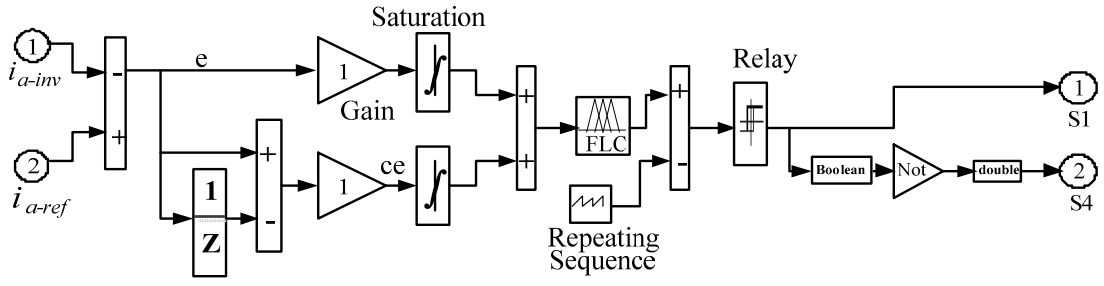


Figure 6. Fuzzy logic based current control scheme for generating switching pulses.

5. Simulation Results

The simulation model of the SAPF and its control algorithms are developed and tested in MATLAB/Simulink. Table 2 summarizes all the design parameters applied in this work. In order to evaluate the effectiveness of the proposed FLC-based current control scheme (with a FLC controller), a comparative analysis is performed by comparing its performance with another similar current control scheme without using the FLC controller. Initially, the functionality of the unit vector synchronizer is tested to ensure effective synchronization of SAPF with the operating power system. Next, the mitigation performance of SAPF is evaluated under steady-state and transient-state conditions.

Table 2. Design parameters used for the simulation work.

System Parameters	Values
Supply frequency	50 Hz
Supply voltage/Phase (peak value)	220 V
Source impedance (R_S, L_S)	0.15 Ω, 0.03 mH
Line impedance (Rr, Lr)	1 Ω, 1 mH
Load impedance (R_L, L_L)	40 Ω, 2 mH
Filter inductance	3 mH
DC voltage	700 V
Capacitance (C_{dc})	3000 μF

Figure 7 shows the output waveform of the unit vector synchronizer: the sine and cosine function needed for synchronization purposes and for the generation of reference current signals. It is clear that the sine and cosine functions are effectively generated, thus ensuring proper generation of the required reference current signals. Meanwhile, Figure 8 shows the source voltage and current waveforms before compensation. The result reveals that before connecting SAPF, the source current is clearly distorted as a result of the harmonics generated by the non-linear load. The distorted current shows that the load current component now comprises both the fundamental and harmonics signals. According to the fast Fourier transform (FFT) analysis shown in Figure 9, the THD value obtained as a result of the harmonic distortion in the current signal is 25.60%. In order to reduce the harmonics in the power system, SAPF is applied by injecting compensation current at the PCC.

On the other hand, Figure 10 shows the FFT analysis of the source current after connecting the SAPF. It is clear that SAPF using the proposed current control scheme (with the FLC controller) has effectively reduced the high THD value of the source current from 25.60% to 0.92%. Meanwhile, SAPF without the FLC controller performs poorly with a THD value of 1.41%. In other words, by using the proposed FLC-based current control scheme, the THD value of the source current can be further reduced by 0.49%.

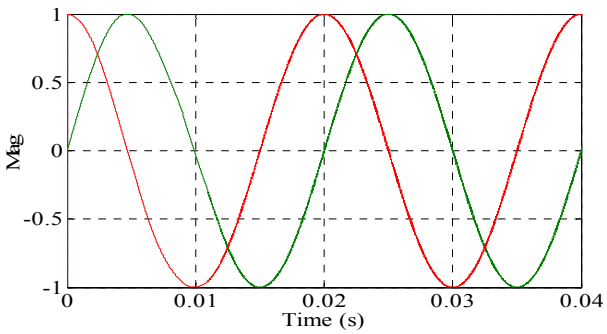


Figure 7. Sine and cosine function from the unit vector circuit.

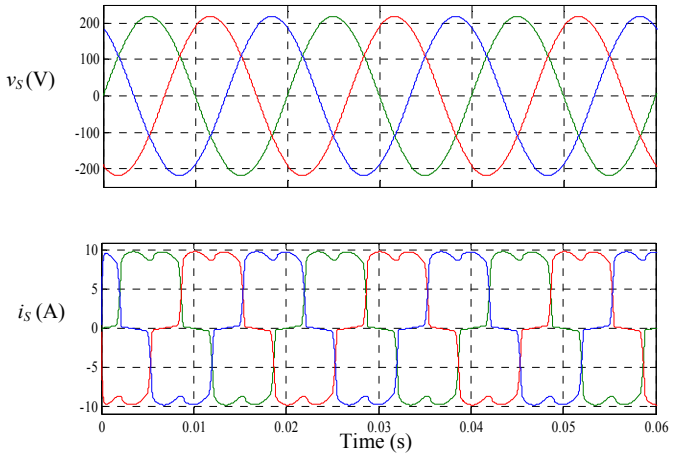


Figure 8. Source voltage v_S and source current i_S before compensation.

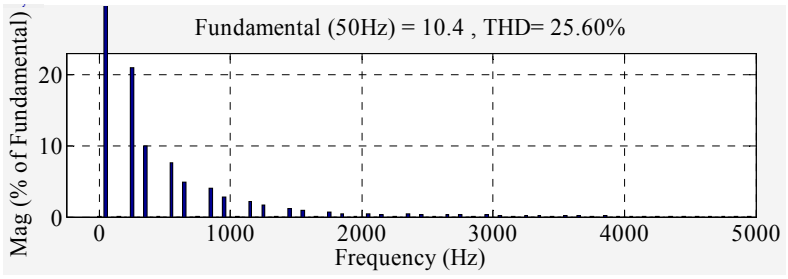


Figure 9. Fast Fourier transformation (FFT) analysis of the source current before compensation.

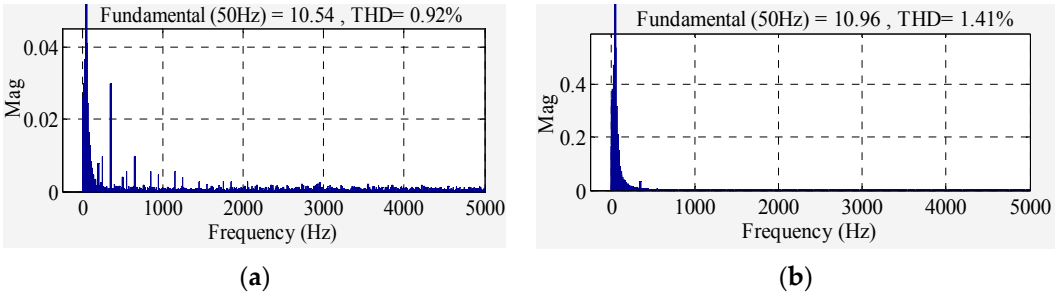


Figure 10. FFT analysis of the source current after compensation obtained from SAPF (**a**) with FLC and (**b**) without FLC.

Next, Figure 11 shows the simulation waveform of SAPF which includes the source voltage after compensation v_S, source current after compensation i_S, compensation current, and DC bus capacitor voltage resulting from the SAPF utilizing the current control scheme with and without the FLC controller. From the results, it is clearly shown that the source current is now sinusoidal and in phase with the source voltage for both cases. The results confirmed the effectiveness of the FLC design in compensating for the current harmonics of the non-linear load in the system.

Furthermore, the proposed FLC-based current control scheme is also evaluated under the transient-state condition. For this evaluation, two transient-state conditions are created by varying the resistor of the inductive load from 40 Ω to 20 Ω (low to high current) and also from 20 Ω to 40 Ω (high to low current). Figures 12 and 13 provide simulation results for the transient behavior of the SAPF in current harmonics mitigation under transient-state conditions. Specifically, it shows waveforms of the source voltage after compensation, source current after compensation, load current, compensation current, and the DC side voltage resulting from the SAPF utilizing the current control scheme with

and without the FLC controller. The findings reveal that the SAPF utilizing the proposed FLC-based current control scheme shows an effective transient performance with a response time of 0.02 s. The findings confirmed the effectiveness of the SAPF in compensating for the current harmonics generated by the non-linear load under transient-state conditions.

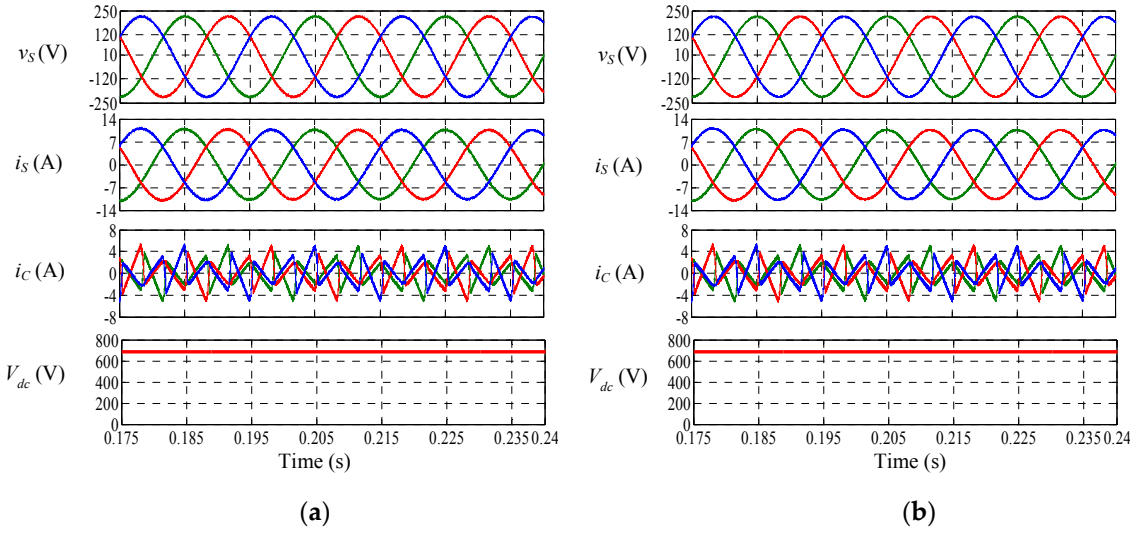


Figure 11. Simulation result of SAPF which includes the three-phase source voltage v_S, source current i_S, compensation current i_C, and DC bus voltage V_{dc}, obtained from SAPF (**a**) with FLC and (**b**) without FLC.

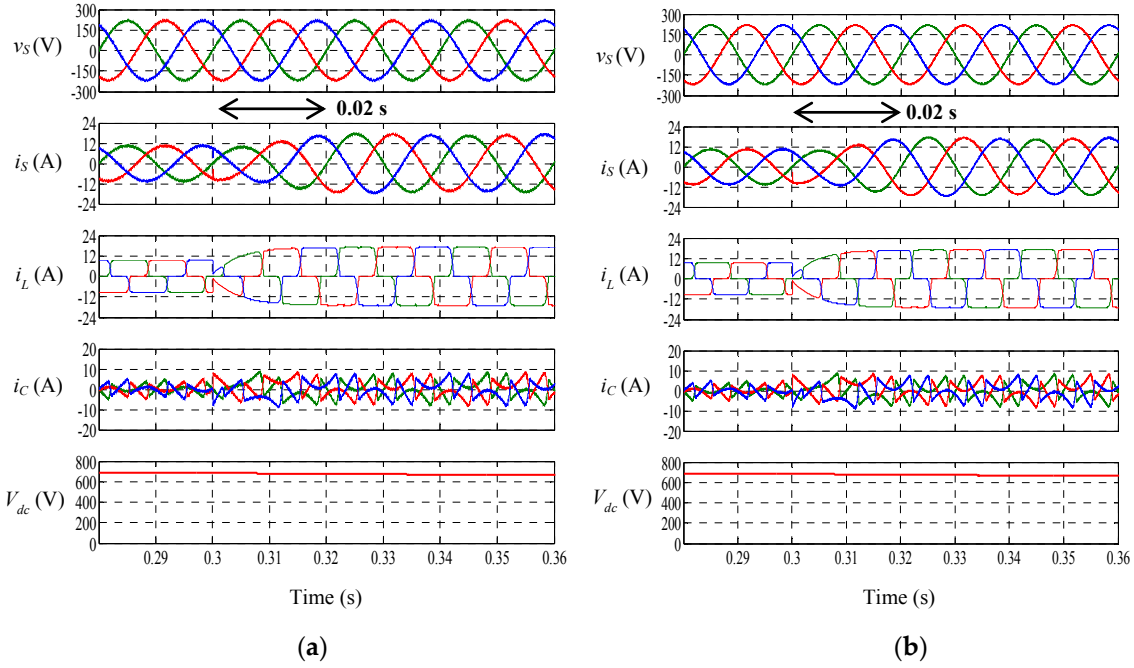


Figure 12. Simulation result of SAPF under transient-state condition of low to high current which includes the three-phase source voltage v_S, source current i_S, compensation current i_C, and DC bus voltage V_{dc}, obtained from SAPF (**a**) with FLC and (**b**) without FLC.

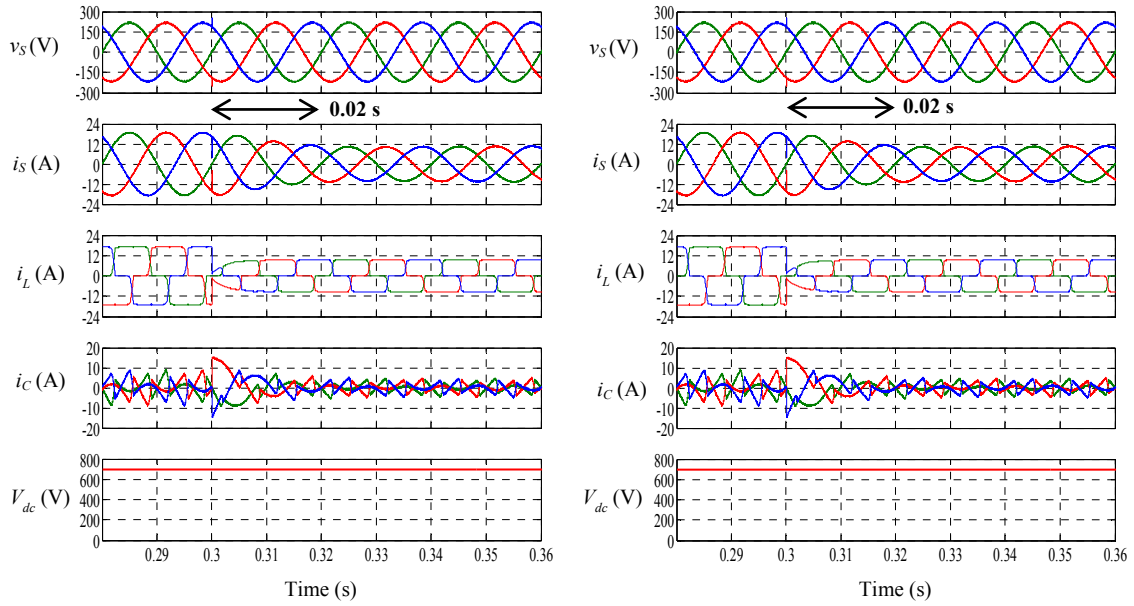


Figure 13. Simulation result of SAPF under transient-state condition of high to low current which includes the three-phase source voltage v_S, source current i_S, compensation current i_C, and DC bus voltage V_{dc}, obtained from SAPF (**a**) with FLC and (**b**) without FLC.

6. Experimental Verification

The hardware set up consists of three main parts: the measurement circuit implemented with the Hall Effect current and voltage sensors, driver circuit, and the DSP-based control unit, as displayed in Figure 14. The measurement circuit converts the three-phase current/voltage into 0–3 V level signals which serve as inputs to the A/D (analog-to-digital) module of the control circuit. Basically, the main role of DSP is to estimate the reference compensating current based on the modified d-q theory and also to generate the PWM modulation control tracking of the current using a fuzzy logic controller. The output signal generated from the DSP control circuit is driven into a driver circuit. Six isolated DC supply voltages of ±15 V are used in the driver circuit to convert the driving signal level from 0 V and 3 V, to −15 V and +15 V, respectively.

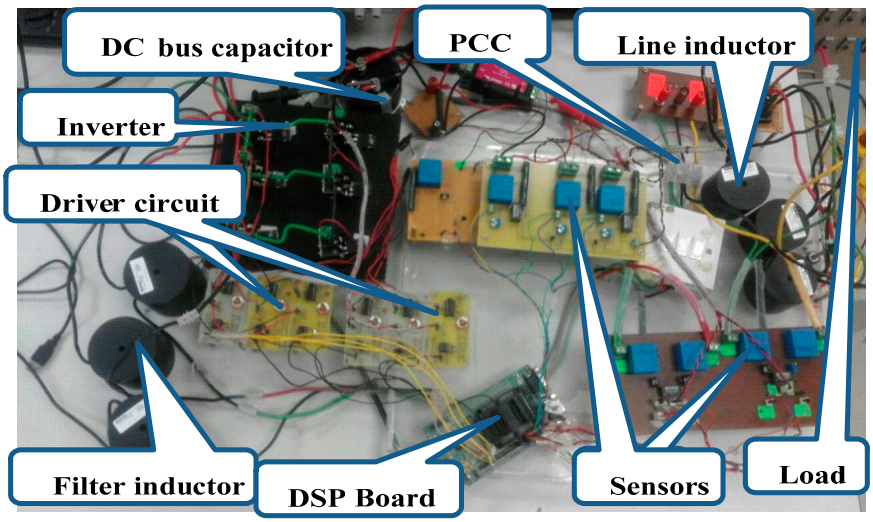


Figure 14. Picture of the hardware set up.

The result shown in Figure 15 are waveforms of the voltage and current (v_{Sa} and i_{La}) of phase A under balanced system conditions from the non-linear circuit before compensation. From Figure 15, it is obvious that the current waveform is distorted due to the presence of non-linear load in the network.

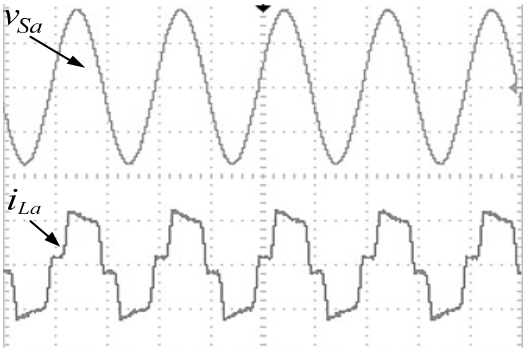


Figure 15. Experimental result displaying the phase a source voltage v_{Sa} (40 V/div) and source current i_{Sa} (5 A/div) waveforms before compensation.

In order to mitigate the harmonic currents, SAPF is applied to the system to cancel them out by injecting the compensation current at PCC. Figure 16 shows experimental results which includes the phase a source voltage v_{Sa}, source current i_{Sa}, load current i_{La}, and compensation current i_{Ca} waveforms resulting from the SAPF utilizing the current control scheme with and without FLC. From the results, it shows that in both cases the source current is now sinusoidal and in phase with the source voltage. However, the SAPF using the proposed current control scheme (with the FLC controller) is revealed to have effectively mitigated the harmonics with a THD value of 5.07%. Meanwhile, the SAPF without the FLC controller performs poorly with a high THD value of 7.40%. In other words, by using the proposed FLC-based current control scheme, the THD value of the source current can be further reduced by 2.33%. Figures 17 and 18 provide similar observations on the sinusoidal and in phase behavior of the source current. Next, Figure 19 presents the steady-state DC side voltage of the SAPF utilizing the current control scheme with and without FLC. In both cases the V_{dc} is approximately 230 V.

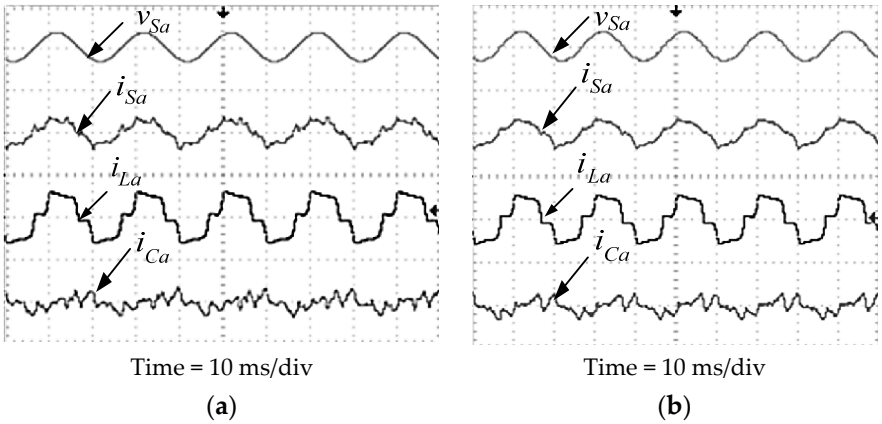
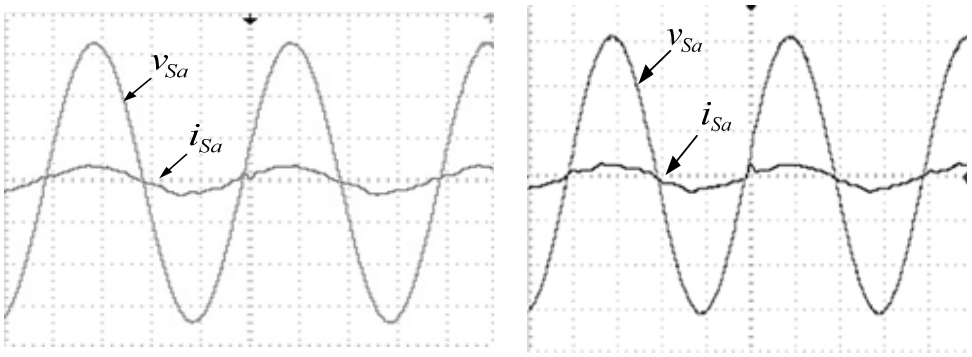
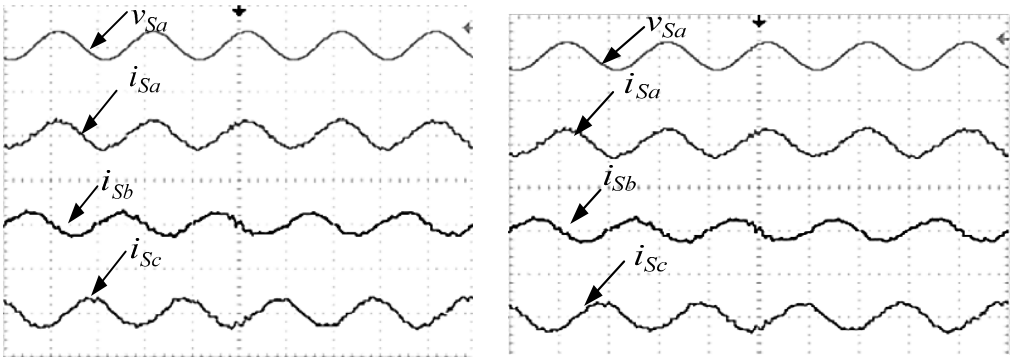


Figure 16. Steady-state experimental result showing the phase a source voltage v_{Sa} (200 V/div), source current i_{Sa} (20 A/div), load current i_{La} (10 A/div), and compensation current i_{Ca} (10 A/div), resulting from SAPF (**a**) with FLC and (**b**) without FLC.



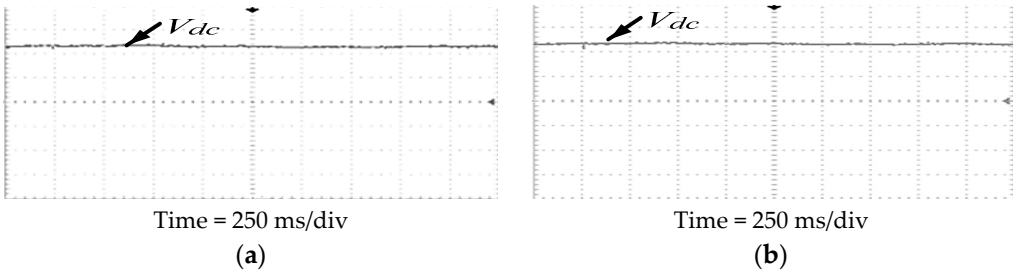
(**a**) (**b**)

Figure 17. Phase a source voltage v_{Sa} (20 V/div) and source current i_{Sa} (20 A/div), resulting from SAPF (**a**) with FLC and (**b**) without FLC.



(**a**) (**b**)

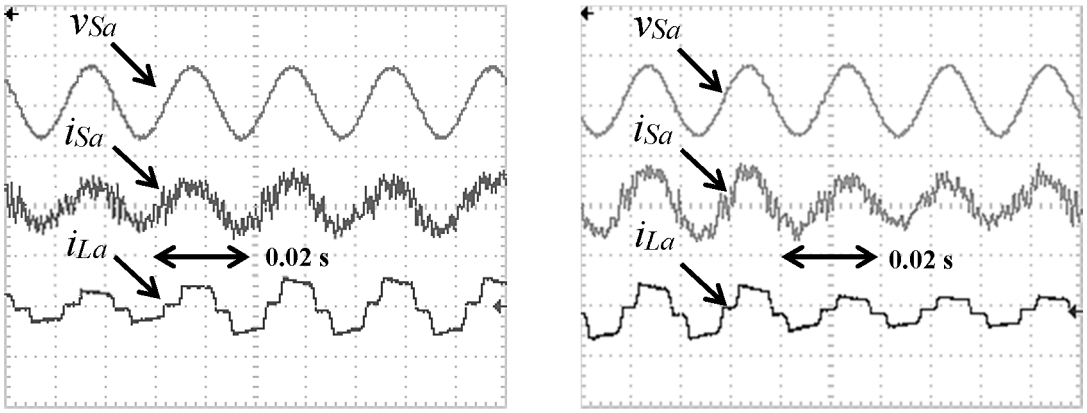
Figure 18. Steady-state experimental results which include the phase a source voltage v_{Sa} (200 V/div) and three-phase source current i_{Sa}, i_{Sb}, and i_{Sc} (20 A/div), resulting from SAPF (**a**) with FLC and (**b**) without FLC.



(**a**) (**b**)

Figure 19. DC bus voltage V_{dc} (200 V/div) resulting from SAPF (**a**) with FLC (**b**) without FLC.

Furthermore, the proposed FLC-based current control scheme is also evaluated under two similar transient-state conditions (low to high current and high to low current changes) which are applied previously in the simulation study. Figure 20 shows the performance of the SAPF under the two transient-state conditions. The findings reveal that the SAPF utilizing the proposed FLC-based current control scheme has an effective transient performance with a response time of 0.02 s. Hence, it confirms the effectiveness of the SAPF in compensating for the current harmonics generated by the non-linear loads under transient-state conditions.



Time = 10 ms/div (**a**) Time = 10 ms/div (**b**)

Figure 20. Experimental results of SAPF utilizing the proposed FLC-based current control scheme which includes the phase a source voltage v_{Sa} (100 V/div), source current i_{Sa} (10 A/div), and load current i_{La} (10 A/div), obtained under transient-state conditions of (**a**) low to high and (**b**) high to low currents.

7. Conclusions

This paper presents MSRF based SAPF with a current control scheme employing FLC to compensate for the current harmonics in the three-phase three-wire system using the MATLAB/Simulink platform and it is experimentally validated with DSP TMS320F28335. The control scheme is capable of suppressing the harmonics in the system in balanced sinusoidal conditions. The operating principle of the MSRF technique is similar to the conventional SRF method, and the main difference is that it consists of simplified unit vector generation instead of the conventional PLL circuit to produce the sine and cosine angles for synchronization purposes. The technique is efficient with good performance capabilities. FLC is used to improve the performance of the PWM current controller. The designed FLC consists of a reduced amount of MFs which aims to reduce complexities and ease implementation. This decreases the tough tuning routines and implementation costs, making the system more efficient. The simulation results show the effectiveness of the control algorithms in mitigating the harmonics in the system by reducing the THD from 25.60% to 0.92% and 1.41% with and without FLC, respectively. The experimental results also show that the three-phase SAPF utilizing these control strategies can compensate for the three-phase load current by reducing the THD to 5.07% and 7.4% with and without FLC, respectively. Furthermore, both the simulation and experimental findings have shown the effectiveness of the proposed current control scheme under transient-state conditions by achieving a response time of 0.02 s.

Author Contributions: The main part of the research work was designed and conducted by Suleiman Musa, and includes modelling and simulation, followed by experimental setup, and analyses of the results obtained. Furthermore, Suleiman Musa was also mainly responsible for the manuscript preparation. Mohd Amran Mohd Radzi contributed immensely in simulation, experimental, and manuscript preparation. Hashim Hizam, Noor Izzri Abdul Wahab, Yap Hoon, and Muhammad Ammirrul Atiqi Mohd Zainuri also have actively contributed in verifying the work and finalizing the manuscript.

Conflicts of Interest: The authors declare no conflict of interest.

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