

## Article

# A Switching Frequency Optimized Space Vector Pulse Width Modulation (SVPWM) Scheme for Cascaded Multilevel Inverters

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**Abstract:** This paper presents a novel switching frequency optimized space vector pulse width modulation (SVPWM) scheme for cascaded multilevel inverters. The proposed SVPWM is developed in a  $\alpha\beta'$  coordinate system, in which the voltage vectors have only integer entries and the absolute increment of coordinate values between adjacent vectors is equal to dc-bus voltage of power cells (1 pu). The new SVPWM scheme is built with three categories of switching paths. During each switching path, the change of one phase voltage is limited in 1 pu. This contributes to decrease the number of commutations of switches. The proposed SVPWM scheme is validated on a 7-level cascaded inverter and the results show that it significantly outperforms traditional SVPWM schemes in terms of decreasing the number of switch commutations.

**Keywords:** space vector pulse width modulation (SVPWM); switching frequency optimized; cascaded multilevel inverter; switching path planning

## 1. Introduction

Multilevel inverters have been selected as a preferred power converter topology for high voltage and high power applications [1,2]. They are widely used in medium voltage motor driver [3], high-voltage direct current (HVDC) transmission systems [4], static var generator (SVG) [5], active power filter (APF) [6] and other applications [7,8]. Several topologies for multilevel inverters have been proposed in the past decades, including diode-clamped [9], flying capacitor [1], cascaded H-bridge [10] and modular multilevel [11]. For a given multilevel converter topology, modulation scheme is a key factor [12–17]. Among various modulation schemes, space vector pulse width modulation (SVPWM) scheme is an attractive candidate due to its flexibility to optimize switching waveforms and its convenience to be implemented in digital signal processors [1,12–14]. Generally, most SVPWM schemes can be implemented with the following three steps:

- (1) Locate the reference voltage vector and select three nearest space vectors.
- (2) Calculate the duty cycles for the three space vectors.
- (3) Generate the switching sequences with specific constraint.

Because the space vector diagram of multilevel inverters is comprised of equilateral triangles in traditional  $\alpha\beta$  coordinate system, the location of reference voltage vector and the duty cycles of the three nearest vectors are obtained with extensive computation. Consequently, the implementation of SVPWM schemes in  $\alpha\beta$  coordinate system usually becomes more complex as the number of levels increases. To speed up Step 1 and Step 2, various coordinate systems have been developed [18–21].

The determination of redundancies with specific constraint in Step 3 remains a big challenge for SVPWM schemes. In order to decrease the number of commutations of switches, some switching techniques have been developed in [22,23]. By carefully selecting redundant switching positions in upper type triangle, lower type triangle and the section number, a minimum loss SVPWM scheme was proposed in [22]. However, as the number of level increases, the selecting complexity of the redundancies increases and no generalized technique for redundancies and switching state transitions is developed. Based on two mappings, a SVPWM scheme is proposed in [23]. Because the different “modes” need to be determined and the region number of the modulation triangle should be calculated in the SVPWM scheme, the rule of determining the switching sequences is still challenging so far.

In this paper, a novel switching frequency optimized SVPWM scheme is proposed and the main contributions are summarized below: (1) the proposed SVPWM scheme is developed in a  $\alpha'\beta'$  coordinate system; (2) The change of one phase voltage is limited in 1 pu during each switching path; (3) The experimental results show that the proposed method significantly outperforms the traditional SVPWM schemes in terms of decreasing the number of commutations of switches.

The paper is organized as follows: Section 2 describes the concepts of basic switching mode and switching path. Section 3 presents the principle of the SVPWM scheme. The experimental results and comparative analysis are presented to validate the theoretical analysis in Section 4. Finally, the conclusions are presented in Section 5.

## 2. Basic Switching Modes and Switching Paths

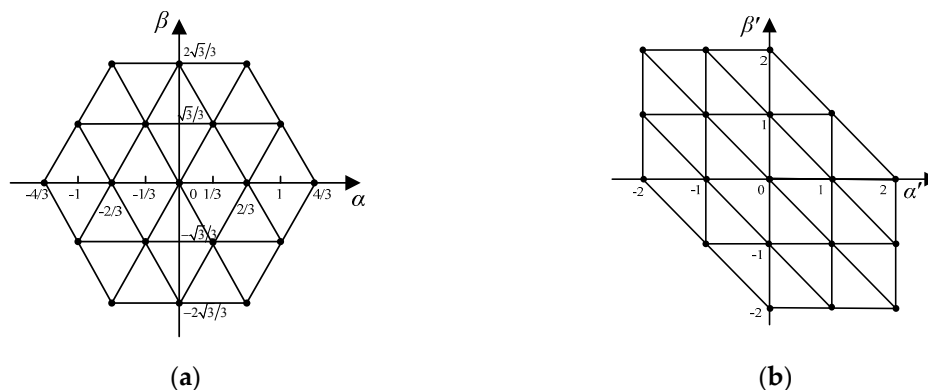
### 2.1. $\alpha'\beta'$ Coordinate System

A  $\alpha'\beta'$  coordinate system is our developed coordinate system in [24]. In the  $\alpha'\beta'$  coordinate system, voltage vectors have integer entries and the absolute coordinate increment between adjacent vectors is equal to 1. The transformation matrix among the  $\alpha'\beta'$  coordinate system, the traditional  $\alpha\beta$  coordinate system [1] and  $abc$  coordinate system are written in Equation (1):

$$\begin{bmatrix} \alpha' \\ \beta' \end{bmatrix} = \begin{bmatrix} \frac{\sqrt{3}}{2} & \frac{\sqrt{2}}{2} \\ -\frac{\sqrt{3}}{2} & \frac{\sqrt{2}}{2} \end{bmatrix} \begin{bmatrix} \alpha \\ \beta \end{bmatrix} = \begin{bmatrix} 1 & 0 & -1 \\ -1 & 1 & 0 \end{bmatrix} \begin{bmatrix} a \\ b \\ c \end{bmatrix} = \begin{bmatrix} a - c \\ -a + b \end{bmatrix}, \quad (1)$$

where,  $a$ ,  $b$  and  $c$  are the normalized three phase voltages of multilevel inverters.  $[\alpha \ \beta]^T$  and  $[\alpha' \ \beta']^T$  are the coordinate values of  $[a \ b \ c]^T$  in the traditional  $\alpha\beta$  coordinate system and the  $\alpha'\beta'$  coordinate system, respectively.

The projections of vectors for 3-level inverter in the  $\alpha\beta$  and  $\alpha'\beta'$  coordinate system are shown in Figure 1, where, each vector is represented by one dot.



**Figure 1.** Space vector diagram for 3-level inverter in different coordinate systems, (a) in the traditional  $\alpha\beta$  coordinate system (b) in the  $\alpha'\beta'$  coordinate system.

## 2.2. Three Basic Switching Modes

The basic switching mode and switching path are defined as follows:

(1) Basic switching mode: the value of  $a$ ,  $b$  or  $c$  is changed with 1 pu between two adjacent switching states. There are three kinds of basic switching modes in space vector diagram, and the three kinds of basic switching modes is named as diagonal switching mode, vertical switching mode, and horizontal switching mode in the paper, respectively. The three kinds of basic switching modes are illustrated in Figure 2.

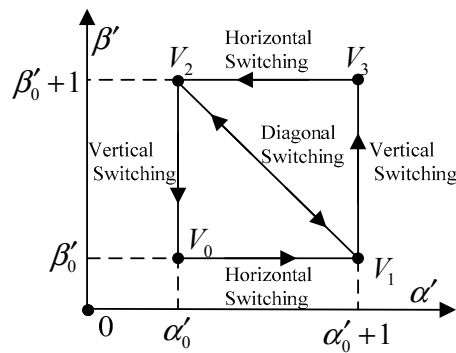


Figure 2. Locus of three basic switching modes.

(2) Switching path: a trajectory is formed by a finite number of basic switching modes in turn.

The increment expression of Equation (1) is described in Equation (2).

$$\begin{cases} \Delta\alpha' = \Delta a - \Delta c \\ \Delta\beta' = -\Delta a + \Delta b' \end{cases} \quad (2)$$

where,  $\Delta a$ ,  $\Delta b$  and  $\Delta c$  are the increment of  $a$ ,  $b$  and  $c$  in the  $abc$  coordinate system.  $\Delta\alpha'$  and  $\Delta\beta'$  are the increment of  $\alpha'$  and  $\beta'$ .

If phase A voltage is changed with 1 pu in one basic switching mode, subject to:

$$\Delta a = \pm 1; \Delta b = \Delta c = 0, \quad (3)$$

Substituting Equation (3) in Equation (2), the expression of the diagonal switching mode is written in Equation (4):

$$\begin{cases} \Delta\alpha' = \Delta a = \pm 1 \\ \Delta\beta' = -\Delta a = \mp 1' \end{cases} \quad (4)$$

If phase B voltage is changed with 1 pu in one basic switching mode, subject to:

$$\Delta b = \pm 1; \Delta a = \Delta c = 0, \quad (5)$$

Substituting Equation (5) in Equation (2), the expression of the vertical switching mode is written in Equation (6):

$$\begin{cases} \Delta\alpha' = 0 \\ \Delta\beta' = \Delta b = \pm 1' \end{cases} \quad (6)$$

If phase C voltage is changed with 1 pu in one basic switching mode, subject to:

$$\Delta c = \pm 1; \Delta a = \Delta b = 0, \quad (7)$$

Substituting Equation (7) in Equation (2), the expression of the horizontal switching mode is written in Equation (8):

$$\begin{cases} \Delta\alpha' = -c = \mp 1 \\ \Delta\beta' = 0 \end{cases}, \quad (8)$$

As shown in Figure 2, the locus of diagonal switching mode is from  $V_2$  to  $V_1$ , the locus of vertical switching mode is from  $V_2$  to  $V_0$  or  $V_1$  to  $V_3$ , and the locus of vertical switching mode is from  $V_3$  to  $V_2$  or  $V_0$  to  $V_1$ . The increment relationships between  $a$ ,  $b$ ,  $c$  and  $\alpha'$ ,  $\beta'$  are listed in Table 1.

**Table 1.** Three basic switching modes.

Switching Mode	$\Delta a$	$\Delta b$	$\Delta c$	$\Delta\alpha'$	$\Delta\beta'$
diagonal	$\pm 1$	0	0	$\pm 1$	$\mp 1$
vertical	0	$\pm 1$	0	0	$\pm 1$
horizontal	0	0	$\pm 1$	$\mp 1$	0

### 2.3. Characteristics of Switching Paths

It is shown in Figures 1b and 2 that any triangle is formed by the above-mentioned three basic switching modes. If a switching path is composed of three sides of a triangle by end to end, the constraint relationships of the realization of the starting vector before and after the switching path can be written-in Equation (9):

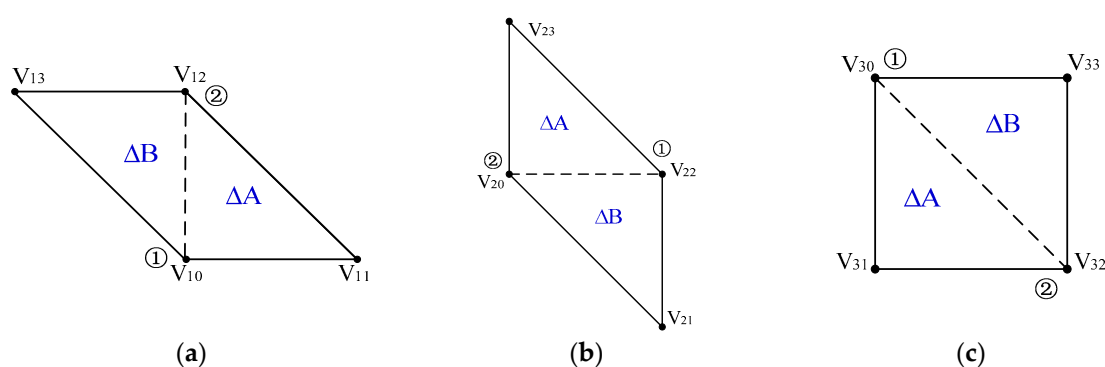
$$(\hat{a}_0, \hat{b}_0, \hat{c}_0) = (a_0, b_0, c_0) \pm (1, 1, 1), \quad (9)$$

where,  $(a_0, b_0, c_0)$  and  $(\hat{a}_0, \hat{b}_0, \hat{c}_0)$  are the realization of the starting vector before and after switching path, respectively. The sign of  $(1, 1, 1)$  is determined by the direction of switching path. If the direction of switching path is clockwise, the sign is positive, otherwise the sign is negative.

However, if the switching path is composed of four sides of a quadrangle by end to end, the constraint relationships of the realization of the starting vectors before and after switching path can be written as:

$$(\hat{a}_0, \hat{b}_0, \hat{c}_0) = (a_0, b_0, c_0), \quad (10)$$

There are three kinds of quadrangles formed by right triangle  $\Delta A$  and  $\Delta B$ , and the three kinds of quadrangles are shown in Figure 3.



**Figure 3.** Three kinds of quadrangles, (a) the first kind; (b) the second kind; (c) the third kind.

As described above, if switching paths consist of the four sides of the quadrangles, the proposed SVPWM scheme will be achieved.

### 3. The Proposed SVPWM Scheme

#### 3.1. Trajectory and Traversing Graphs of Reference Voltage Vector

Generally, the three normalized phase voltages  $a_r$ ,  $b_r$  and  $c_r$  for reference voltage vector  $V_r$  can be defined in Equation (11):

$$\begin{cases} a_r = V_m \cos(\omega t) / E \\ b_r = V_m \cos(\omega t - 2\pi/3) / E, \\ c_r = V_m \cos(\omega t - 4\pi/3) / E \end{cases} \quad (11)$$

where,  $V_m$  and  $\omega$  are the peak voltage and angular frequency.  $E$  is dc-bus voltage of power cells.

Substituting Equation (11) in Equation (1):

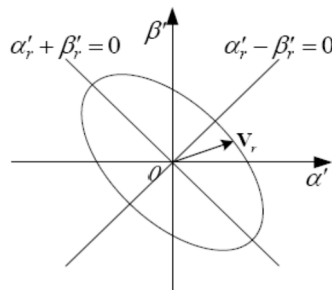
$$\begin{bmatrix} \alpha'_r \\ \beta'_r \end{bmatrix} = \frac{\sqrt{3}V_r}{E} \begin{bmatrix} \sin(\omega t + \frac{\pi}{3}) \\ \sin(\omega t - \frac{\pi}{3}) \end{bmatrix}, \quad (12)$$

where,  $[\alpha'_r, \beta'_r]^T$  is the coordinate values of  $V_r$ .

Equation (12) can be rewritten as:

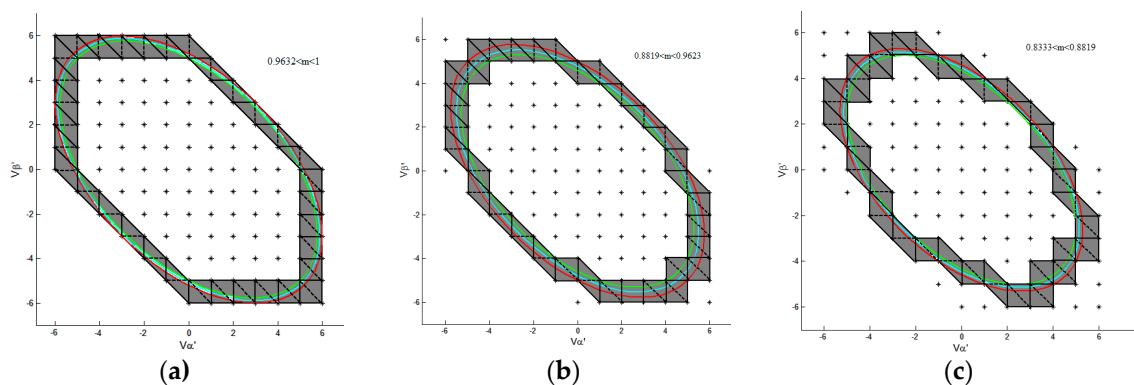
$$\begin{cases} \alpha'_r + \beta'_r = \sqrt{3}V_r \sin(\omega t) / E \\ \alpha'_r - \beta'_r = 3V_r \cos(\omega t) / E \end{cases} \quad (13)$$

The trajectory of  $V_r$  is shown in Figure 4. It can be seen that the trajectory of  $V_r$  is an ellipse.



**Figure 4.** Trajectory of  $V_r$ .

Figure 5 demonstrates the different traversing graphs of reference voltage vector for 7-level inverter with different modulation indexes.



**Figure 5.** Traversing graphs of reference voltage vector with different modulation indexes for 7-level inverter, (a)  $0.9632 < m < 1$ ; (b)  $0.8819 < m < 0.9632$ ; (c)  $0.8333 < m < 0.8819$ .

where,  $m$  is modulation index, and the red and green ellipses are the trajectories of reference voltage vector with maximum modulation index and minimum modulation index in the corresponding case. If  $m$  is between maximum and minimum modulation index, the trajectories of reference voltage vector is plotted with cyan ellipse. As shown in Figure 5, any traversing graph is composed of three kinds of quadrilaterals.

### 3.2. Switching Path Planning

As shown in Figure 3, there are two common vertexes, named as interface vector ① and interface vector ②. If the interface vector is chosen as a starting vector, the three vectors in the same triangle can be applied with two basic switching modes. Otherwise, at least three basic switching modes are needed.

For example, if interface vector ① ( $V_{10}$ ) is chosen as the starting vector in  $\Delta A$  in Figure 3a, the three vectors can be applied with the switching path  $V_{10} \rightarrow V_{11} \rightarrow V_{12}$ . If interface vector ② ( $V_{12}$ ) is chosen as starting vector, the three vectors can be applied with the switching path  $V_{12} \rightarrow V_{11} \rightarrow V_{10}$ . However, if vector  $V_{11}$  is chosen as a starting vector, the three vectors is applied with the switching path  $V_{11} \rightarrow V_{12} \rightarrow V_{10}$  or  $V_{11} \rightarrow V_{10} \rightarrow V_{12}$ . Hence, the non-common vertexes should be not chosen as a starting vector in the proposed SVPWM scheme.

The switching paths of the proposed SVPWM scheme are divided into three categories: switching paths in a triangle, switching paths not in a triangle but in a quadrilateral and switching paths between quadrilaterals.

#### 3.2.1. Switching Paths in a Triangle

The switching paths in the same triangle for the three kinds of quadrangles are illustrated in Figures 6–8, respectively, where,  $V'_{xout}(x = 1, 2, 3)$  are the first, the second and the third vector in the previous switching path, and  $V_{xout}(x = 1, 2, 3)$  are the first, the second and the third vector in the current switching path. The vertex with red circles is the third vector in the previous switching path. The direction of the switching path is marked with blue arrows.

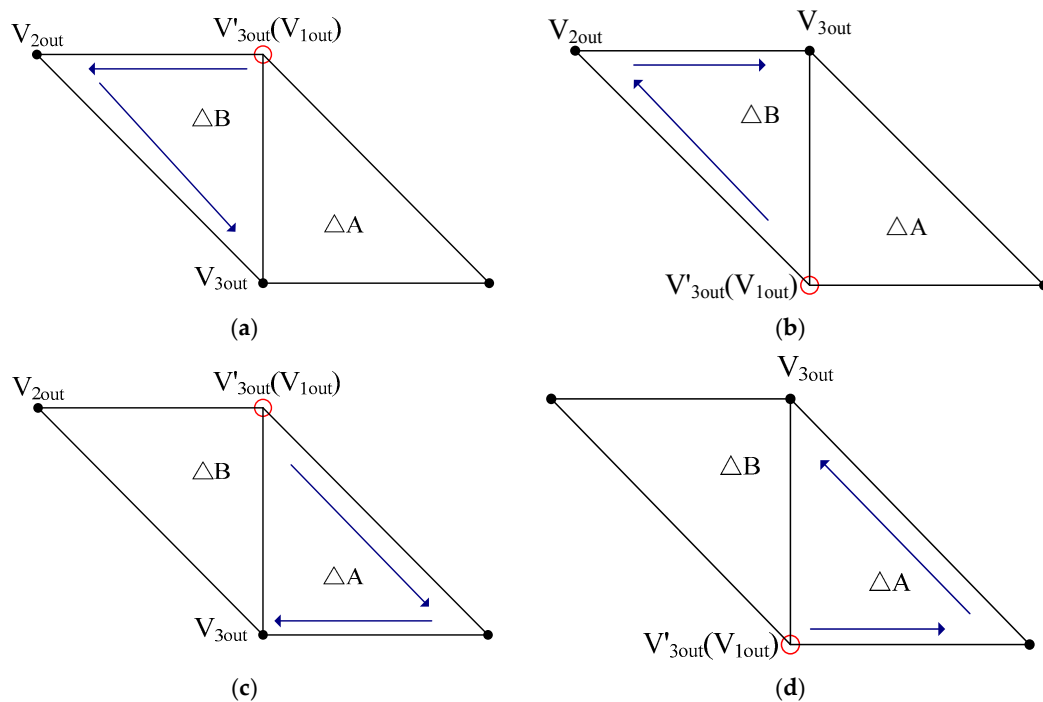
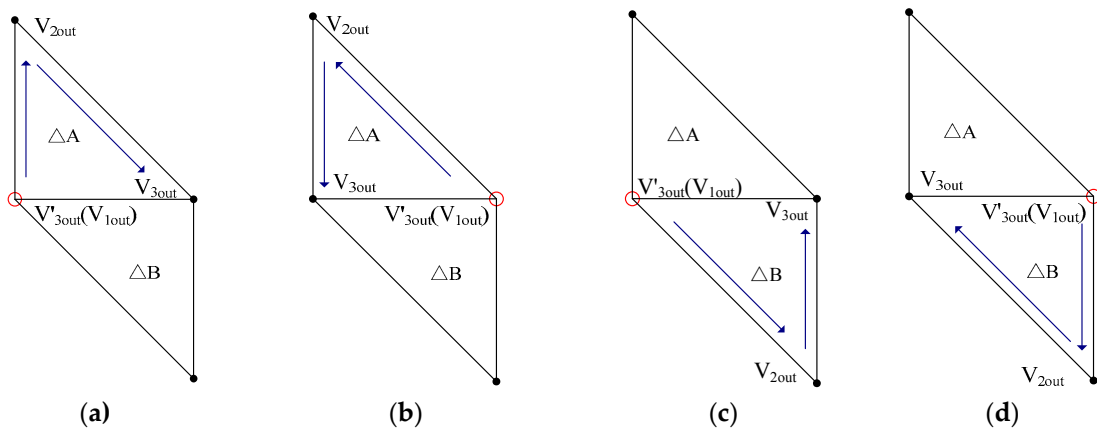
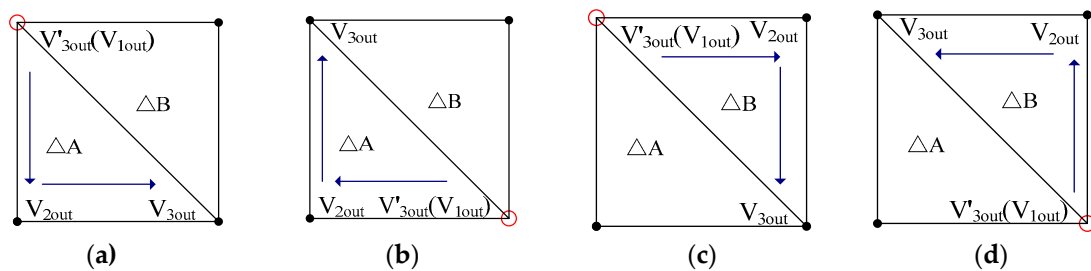


Figure 6. Switching paths in the first kind of quadrangle, (a) state 1; (b) state 2; (c) state 3; (d) state 4.



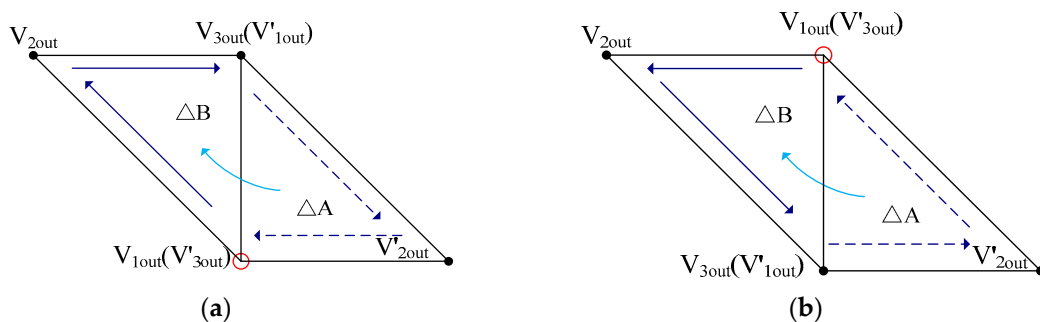
**Figure 7.** Switching paths in the second kind of quadrangle, (a) state 1; (b) state 2; (c) state 3; (d) state 4.



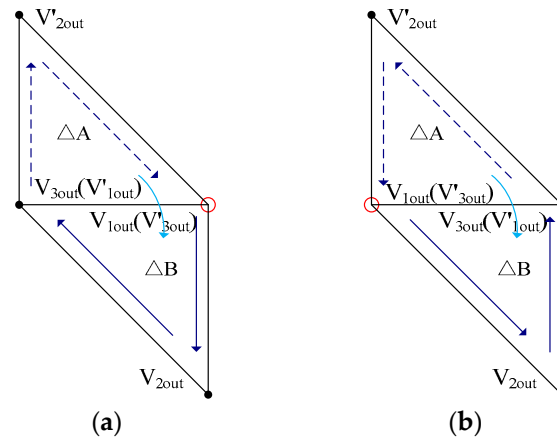
**Figure 8.** Switching paths in the third kind of quadrangle, (a) state 1; (b) state 2; (c) state 3; (d) state 4.

### 3.2.2. Switching Paths not In a Triangle but in a Quadrilateral

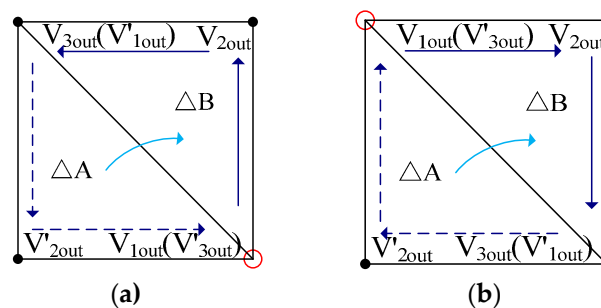
The feature in this situation is that the switching path is from  $\Delta A$  into  $\Delta B$ . The switching paths for the three kinds of quadrangles are shown in Figures 9–11, respectively. Where, the solid and dashed arrows represent the direction of the current switching path and the previous switching path, respectively. The cyan arrows are the locus of reference vector.



**Figure 9.** Switching paths in the first kind of quadrangle, (a) state 1; (b) state 2.



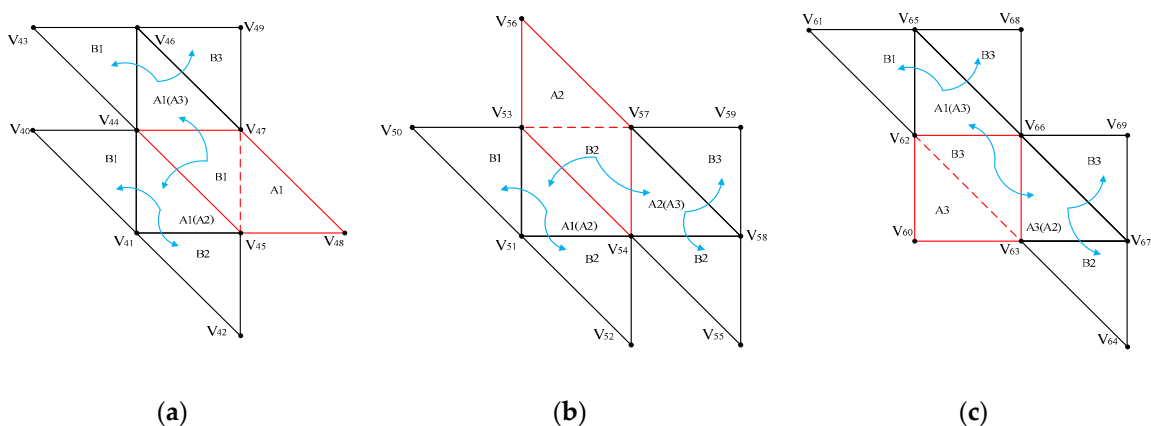
**Figure 10.** Switching paths in the second kind of quadrangle, (a) state 1; (b) state 2.



**Figure 11.** Switching paths in the third kind of quadrangle, (a) state 1; (b) state 2.

### 3.2.3. Switching Paths between Quadrilaterals

The feature in this situation is that the switching path is from  $\Delta B$  into  $\Delta A$ . The transition graph between the first kind of quadrilateral and other kinds of quadrilaterals, the transition graph between the second kind of quadrilateral and other kinds of quadrilaterals, and the transition graph between the third kind of quadrilateral and other kinds of quadrilaterals are shown in Figure 12a–c, respectively. In Figure 12,  $AX$  ( $X = 1, 2, 3$ ) and  $BX$  ( $X = 1, 2, 3$ ) represent  $\Delta A$  and  $\Delta B$  triangle in the  $X_{th}$  kind of quadrilateral, and  $AX$  ( $AY$ ) ( $X \neq Y$ ) represents the common  $\Delta A$  triangle in  $X_{th}$  and  $Y_{th}$  kind of quadrilateral.  $V_{4x}$  ( $x = 1, 2, \dots, 9, 10$ ),  $V_{5x}$  ( $x = 1, 2, \dots, 9, 10$ ) and  $V_{6x}$  ( $x = 1, 2, \dots, 9, 10$ ) are the vectors in the transition graph. The feasible switching paths between different kinds of quadrilaterals are listed in Tables 2–4.



**Figure 12.** Transition graphs between different kinds of quadrilaterals, (a) the first kind of quadrilateral; (b) the second kind of quadrilateral; (c) the third kind of quadrilateral.



**Table 2.** Feasible switching paths between the first kind and other kinds of quadrilaterals.

Adjacent Quadrilateral	Starting Vector	Switching Path	Note
the first kind of quadrilateral	$V_{47}$	$V_{47} \rightarrow V_{44} \rightarrow V_{47} \rightarrow V_{46}$	B1 into A1(A3)
	$V_{45}$	$V_{45} \rightarrow V_{44} \rightarrow V_{47} \rightarrow V_{46}$	B1 into A1(A3)
the first kind of quadrilateral	$V_{47}$	$V_{47} \rightarrow V_{44} \rightarrow V_{45} \rightarrow V_{41}$	B1 into A1(A2)
	$V_{45}$	$V_{45} \rightarrow V_{41} \rightarrow V_{45} \rightarrow V_{44}$	B1 into A1(A2)
the second kind of quadrilateral	$V_{47}$	$V_{47} \rightarrow V_{44} \rightarrow V_{45} \rightarrow V_{44} \rightarrow V_{41}$	B1 into A1(A2)
	$V_{45}$	$V_{45} \rightarrow V_{44} \rightarrow V_{41}$	B1 into A1(A2)
the third kind of quadrilateral	$V_{47}$	$V_{47} \rightarrow V_{44} \rightarrow V_{46}$	B1 into A1(A3)
	$V_{45}$	$V_{45} \rightarrow V_{44} \rightarrow V_{47} \rightarrow V_{44} \rightarrow V_{46}$	B1 into A1(A3)

**Table 3.** Feasible switching paths between the second kind and other kinds of quadrilateral.

Adjacent Quadrilateral	Starting Vector	Switching Path	Note
the first kind of quadrilateral	$V_{57}$	$V_{57} \rightarrow V_{54} \rightarrow V_{53} \rightarrow V_{54} \rightarrow V_{52}$	B2 into A1(A2)
	$V_{53}$	$V_{53} \rightarrow V_{54} \rightarrow V_{51}$	B2 into A1(A3)
the second kind of quadrilateral	$V_{57}$	$V_{57} \rightarrow V_{54} \rightarrow V_{53} \rightarrow V_{51}$	B2 into A1(A2)
	$V_{53}$	$V_{53} \rightarrow V_{54} \rightarrow V_{53} \rightarrow V_{54}$	B2 into A1(A2)
the second kind of quadrilateral	$V_{57}$	$V_{57} \rightarrow V_{54} \rightarrow V_{57} \rightarrow V_{58}$	B2 into A2(A3)
	$V_{53}$	$V_{53} \rightarrow V_{54} \rightarrow V_{57} \rightarrow V_{58}$	B2 into A2(A3)
the third kind of quadrilateral	$V_{57}$	$V_{57} \rightarrow V_{54} \rightarrow V_{58}$	B2 into A1(A3)
	$V_{53}$	$V_{53} \rightarrow V_{54} \rightarrow V_{57} \rightarrow V_{54} \rightarrow V_{58}$	B2 into A1(A3)

**Table 4.** Feasible switching paths between the third kind and other kinds of quadrilateral.

Adjacent Quadrilateral	Starting Vector	Switching Path	Note
the first kind of quadrilateral	$V_{62}$	$V_{62} \rightarrow V_{66} \rightarrow V_{65}$	B3 into A1(A3)
	$V_{63}$	$V_{63} \rightarrow V_{66} \rightarrow V_{62} \rightarrow V_{66} \rightarrow V_{65}$	B3 into A1(A3)
the second kind of quadrilateral	$V_{62}$	$V_{62} \rightarrow V_{66} \rightarrow V_{63} \rightarrow V_{66} \rightarrow V_{67}$	B3 into A3(A2)
	$V_{63}$	$V_{63} \rightarrow V_{66} \rightarrow V_{67}$	B3 into A3(A2)
the third kind of quadrilateral	$V_{62}$	$V_{62} \rightarrow V_{66} \rightarrow V_{63} \rightarrow V_{67}$	B3 into A3(A2)
	$V_{63}$	$V_{63} \rightarrow V_{66} \rightarrow V_{63} \rightarrow V_{67}$	B3 into A3(A2)
the third kind of quadrilateral	$V_{62}$	$V_{62} \rightarrow V_{66} \rightarrow V_{62} \rightarrow V_{65}$	B3 into A1(A3)
	$V_{63}$	$V_{63} \rightarrow V_{66} \rightarrow V_{62} \rightarrow V_{65}$	B3 into A1(A3)

### 3.3. Realization of Vectors

Some vectors have redundant switching states when transformed back to *abc* coordinate system. The realizations of vectors in the SVPWM scheme are classified in two categories: the realization of the first vector and the realization of other vectors.

#### 3.3.1. Realization of the First Vector

Realization of the first vector is obtained with the following steps:

Step (1): Divide the space vector diagram into 3 zones, as shown in Figure 13.

Step (2): Identify the number of zone for the first vector.

Step (3): If the first vector was located in zone I, the realization of the first vector is obtained with the realization  $(-n, n, n)$  of vector  $(-2n, 2n)$ , and the switching path consists of the first kind of quadrilaterals.

Step (4): If the first vector was located in zone II, the realization of the first vector is obtained with the realization  $(-n, n, n)$  of vector  $(-2n, 2n)$ , and the switching path consists of the second kind of quadrilaterals.

Step (5): If the first vector was located in zone III, the realization of the first vector is obtained with the realization  $(n, n, -n)$  of vector  $(2n, 0)$ , and the switching path is comprised of the third kind of quadrilaterals.

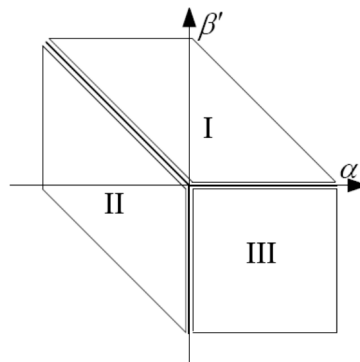


Figure 13. Space vector diagram with three zones

For simplicity, the realization of vector  $(2, -1)$  for 5-level inverter is illustrated in Figure 14. Here, vector  $(2, -1)$  is located in Zone III, and the realization of vector  $(4, 0)$  is  $(2, 2, -2)$ . The switching path  $(4, 0) \rightarrow (3, 0) \rightarrow (3, -1) \rightarrow (2, -1)$  is chosen in the  $\alpha'\beta'$  coordinate system, and the corresponding switching path  $(2, 2, -2) \rightarrow (2, 2, -1) \rightarrow (2, 1, -1) \rightarrow (2, 1, 0)$  is obtained in  $abc$  coordinate system. Hence, the realization of vector  $(4, 0)$  is  $(2, 1, 0)$ .

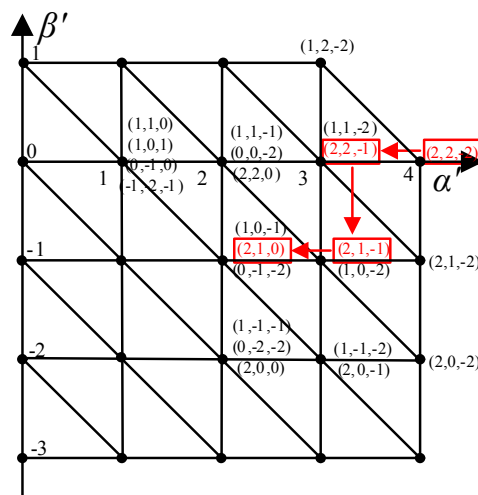
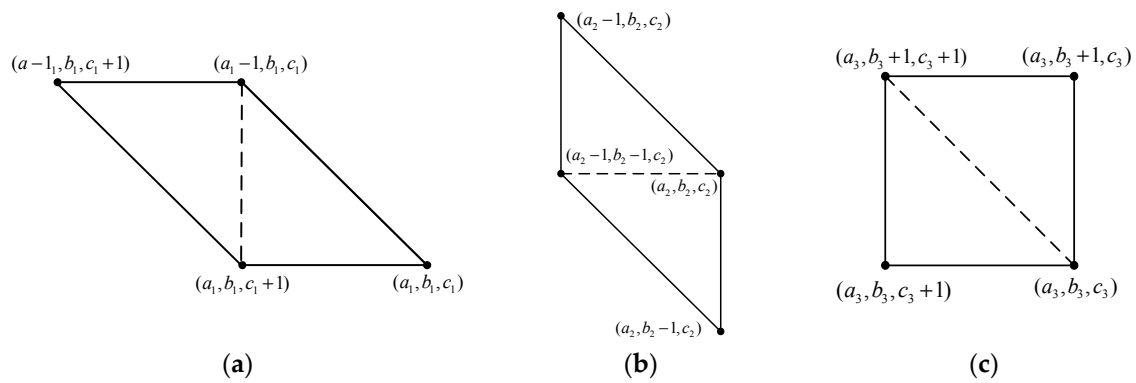


Figure 14. Realization of vector  $(2, -1)$ .

### 3.3.2. Realization of Other Vectors

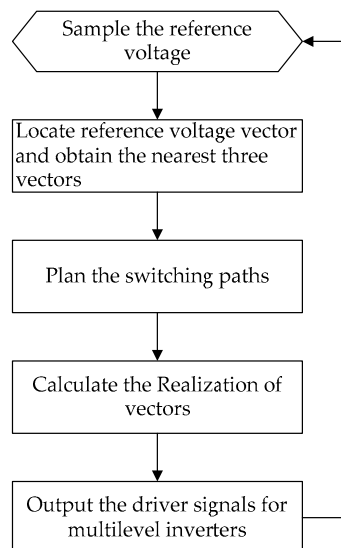
Upon the realization of the first vector, the realization of other vectors can be achieved with the increment relationships between  $(a, b, c)$  and  $(\alpha', \beta')$  in the three basic switching modes, as shown in Figure 15.



**Figure 15.** Realization of other vectors, (a) in the first kind of quadrilateral; (b) in the second kind of quadrilateral; (c) in the third kind of quadrilaterals

### 3.4. Flowchart of the Implementation of the SVPWM Scheme

The flowchart of the implementation of the SVPWM scheme is shown in Figure 16. The location of reference voltage vector and the selection strategy for the nearest three vectors can be obtained in [24]. The planning of the switching paths is demonstrated in Section 3.2, and the realization of vectors is described in Section 3.3.



**Figure 16.** Flowchart of the implementation of the SVPWM scheme.

## 4. Experimental Results

### 4.1 Experimental Setup

A 7-level cascaded multilevel inverter is built in the laboratory, as shown in Figure 17. Nine isolation DC power for the 7-level inverter are formed by nine 200 W isolation transformers and diode rectifier bridges. The dc-bus voltage of power cells is selected as 50 V. The model of switches in the inverter is IRFP460, and the driver circuits are composed of high-speed opt-coupler (model: 6N137) and IR2110. The inverter is controlled by a TMS320F28335 floating-point DSP from Texas Instruments (Dallas, TX, USA). The experimental setup is shown in Figure 18.

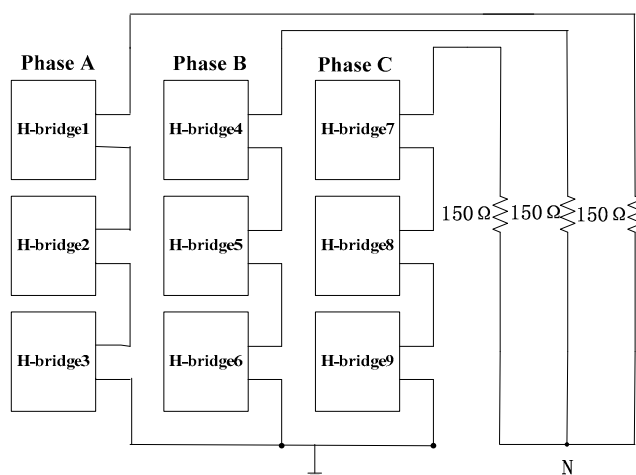


Figure 17. 7-level cascaded multilevel inverter.

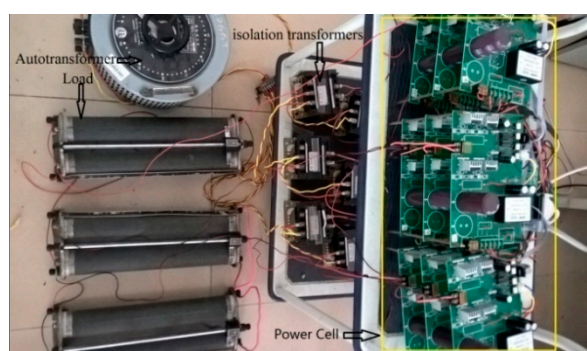
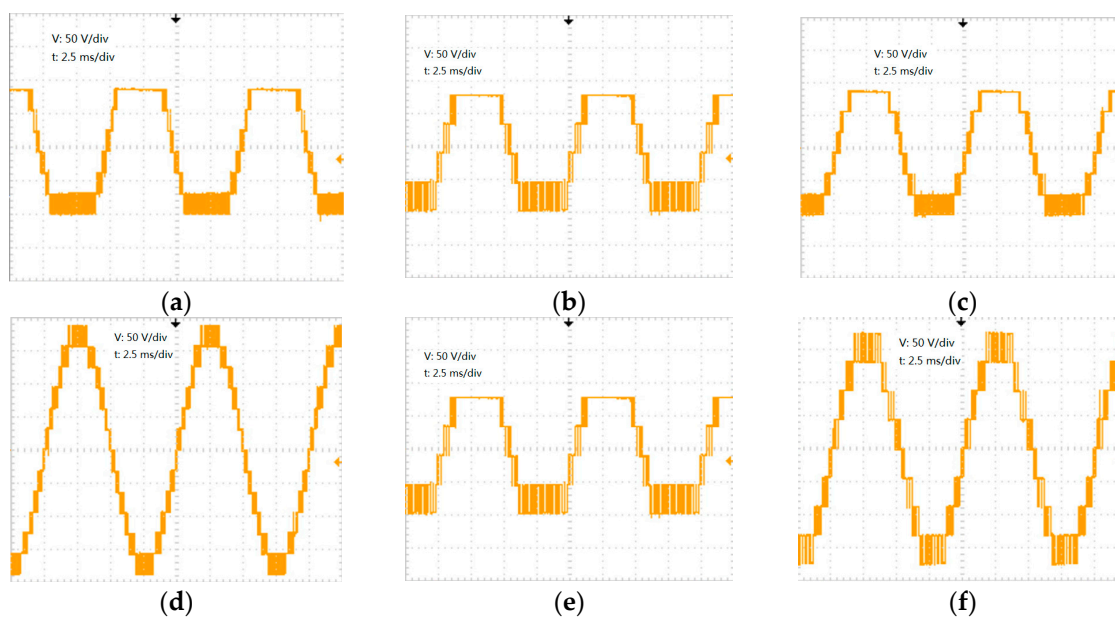
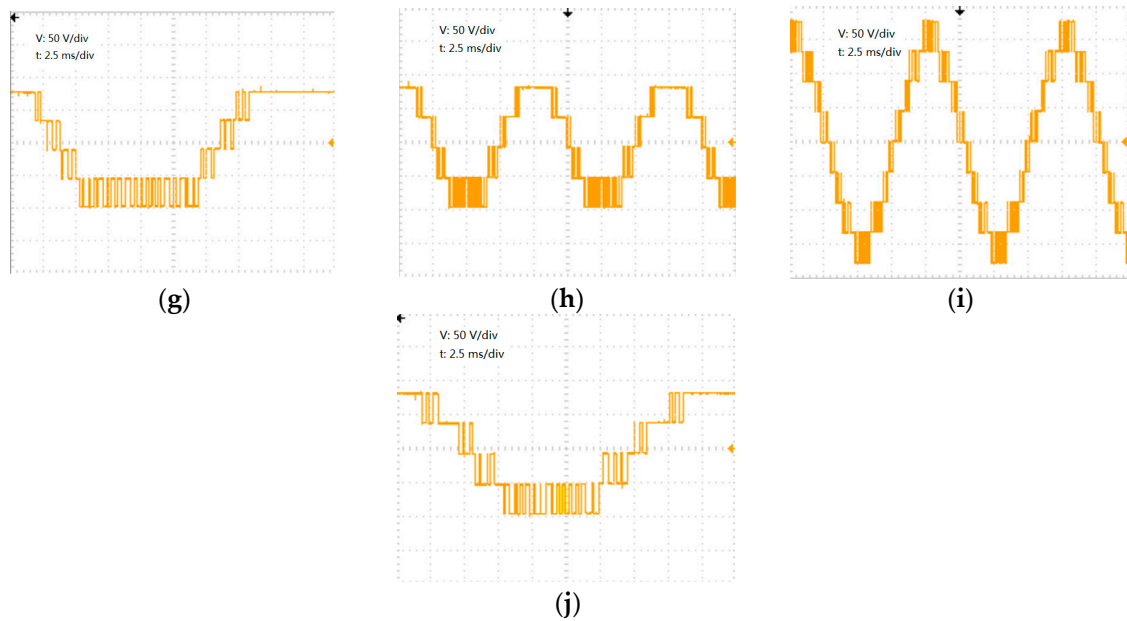


Figure 18. Experimental setup.

#### 4.2. Experimental Results

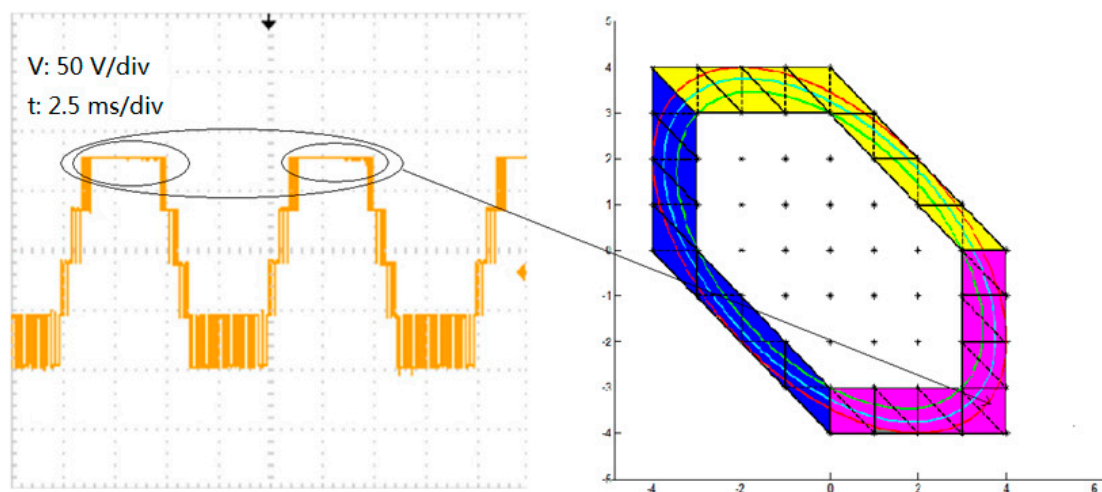
The waveforms of the 7-level inverter with different modulation indexes are shown in Figure 19. Where, the fundamental frequency of output voltage is set to be 100 Hz.





**Figure 19.** Waveforms of the 7-level inverter, (a) phase voltage A with  $m = 0.981$ ; (b) line-to-line voltage AB with  $m = 0.981$ ; (c) phase voltage A with  $m = 0.922$ ; (d) line-to-line voltage AB with  $m = 0.922$ ; (e) phase voltage A with  $m = 0.75$ ; (f) details of the waveform in (f); (g) phase voltage A with  $m = 0.665$ ; (h) phase voltage A with  $m = 0.665$ ; (i) line-to-line voltage AB with  $m = 0.665$ ; (j) details of the waveform in (j).

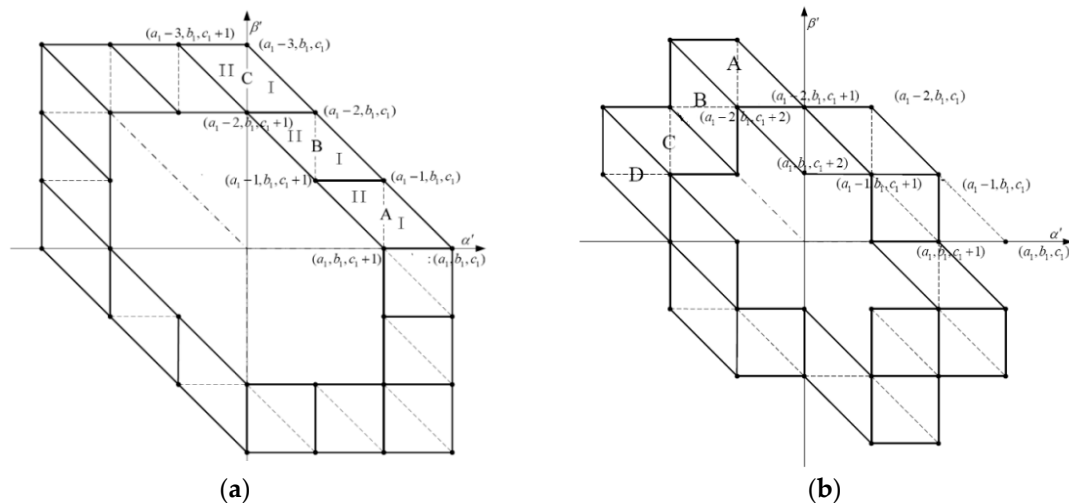
As seen from Figure 19e,j, the phase voltage is kept at the highest level for some time without changing. The corresponding graph on unchanged parts of the phase voltage A and the traversing graph is illustrated in Figure 20.



**Figure 20.** Corresponding graph on unchanged parts of the phase voltage A and traversing graph.

As shown in Figure 20, there is no diagonal switching mode in the magenta region. Hence, the phase voltage A remains unchanged. The similar conclusions can be obtained in the yellow region and the blue region. For simplicity, we choose 5-level inverter to analyze the number of commutations of switches for different switching paths.

There are two traversing graphs when the reference voltage are in the outermost layer, and the switching paths for the two traversing graphs are shown in Figure 21. Where, solid lines stand for the feasible basic switching modes, and dotted lines are the forbidden basic switching modes.



**Figure 21.** Switching paths for 5-level inverter in the outermost layer, (a) the first class switching path, (b) the second class switching path.

If interface vector ① is chosen as the starting vector, the number of commutations of switches is  $2M_j$  in a quadrilateral. Where,  $M_j = M_{j1} + M_{j2}$ .  $M_{j1}$  and  $M_{j2}$  are the number of sampling points in  $\Delta A$  and  $\Delta B$ , respectively. If the starting vector of current quadrilateral and the ending vector of previous quadrilateral are the same vector, an extra switching modes need to be added. Therefore, the maximum number of commutations of switches for the first class switching path is:

$$S_{\max\_1} = 2 \sum_{j=1}^J M_j + J + 3 = 2M + J + 3, \quad (15)$$

where,  $M_j = M_{j1} + M_{j2}$ , and  $J$  is the number of quadrilateral.

With the above statistical method, the maximum number of commutations of switches for the second class switching path can be calculated as:

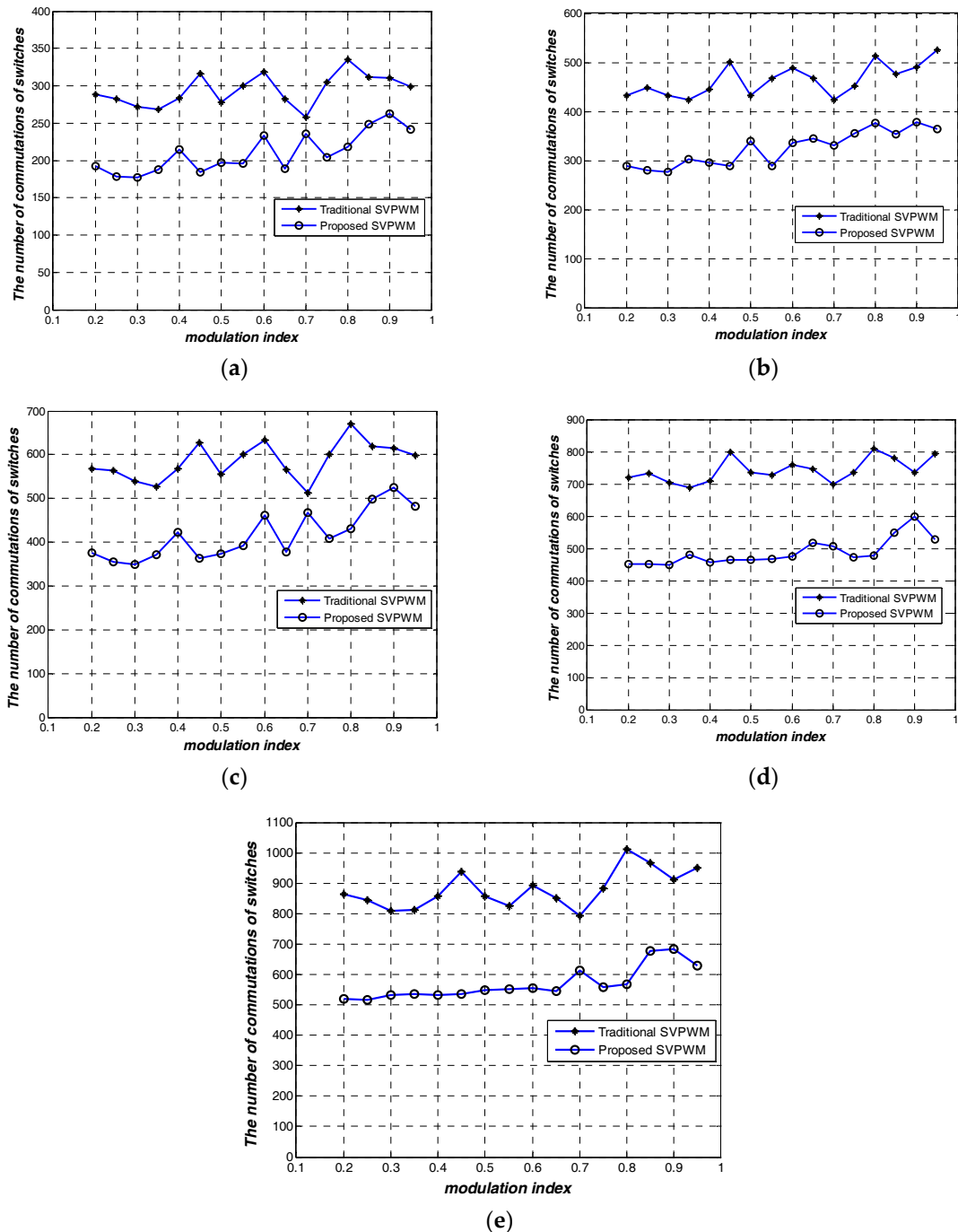
$$S_{\max\_2} = 2 \sum_{j=1}^J M_j + J + 9 = 2M + J + 9, \quad (16)$$

Table 5 lists the number of commutations of switches for 5-level inverter in the first class switching paths shown in Figure 20a.

**Table 5.** Number of commutations of switches for 5-level inverter.

Number of Sampling Points in one Period	Maximum Number from Theoretical Calculation (Times)	Experimental Results (Times)
42	108	103
63	150	149
84	192	190

As shown in Table 5, the actual number of commutations of switches is consistent with the theoretical calculation. The numbers of commutations of switches in one period with different number of sampling points by the proposed SVPWM scheme and the classical SVPWM scheme are shown in Figure 22. Where, the same realizations of all vectors are used by classical SVPWM scheme.



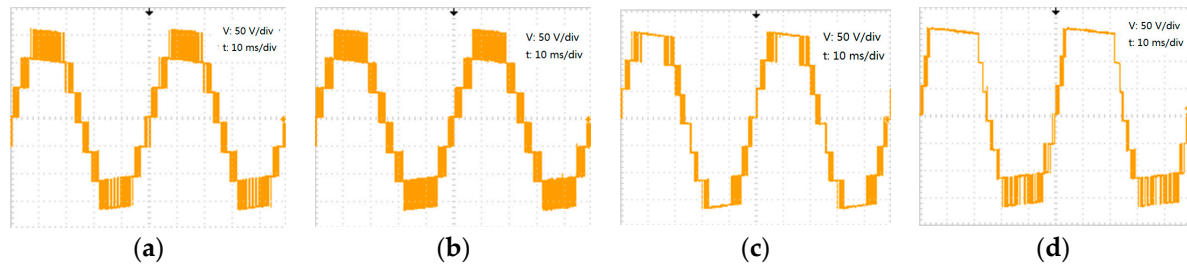
**Figure 22.** Numbers of commutations of switches with different number of sampling points in one period, (a) 42 sampling points; (b) 64 sampling points; (c) 84 sampling points; (d) 105 sampling points; (e) 126 sampling points.

As shown in Figure 22, the average difference in terms of the number of commutations of switches is about 45% between the traditional SVPWM scheme and the proposed SVPWM scheme, which confirms the effectiveness of the proposed method in decreasing the number of commutations of switches.

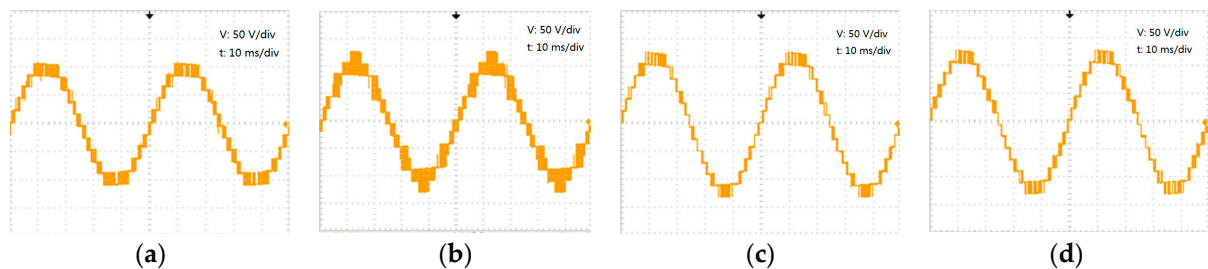
Because all switching paths are comprised of the three switching modes, only one phase voltage limited in 1 pu is achieved. Compared to other PWM schemes [25–27], the proposed SVPWM scheme is also an effective way to decrease the  $di/dt$  of the output current and  $dV/dt$  of the output voltage for multilevel inverters as well as reduce the switching losses of switches.

### 4.3. Compared with Other PWM Schemes

Phase voltage and line-to-line voltage waveforms with in-phase disposition PWM (IPDPWM) scheme, phase shifted PWM (PSPWM) scheme, classical SVPWM scheme and proposed SVPWM scheme are shown in Figures 23 and 24, respectively. Where, the fundamental frequency of output voltage is 20 Hz. The modulation index  $m = 0.94$ , and the carrier frequency or the sampling frequency for these PWM schemes is 4200 Hz.

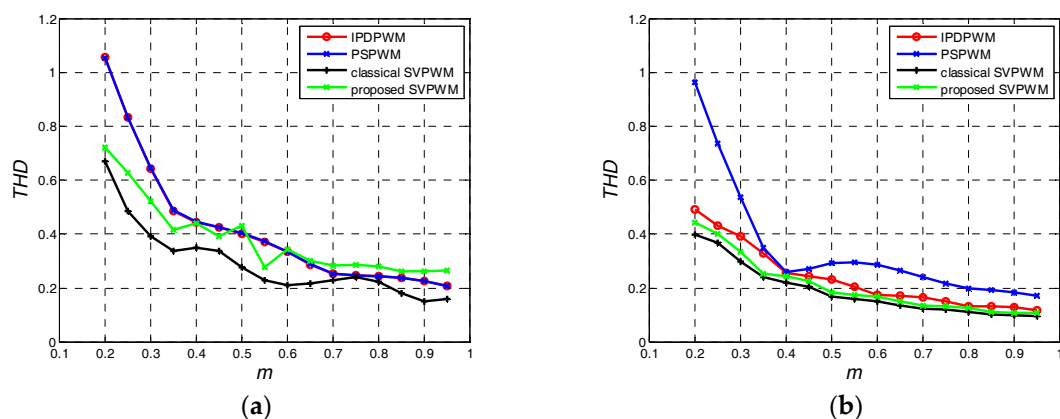


**Figure 23.** Phase voltage of 7-level inverter with different PWM schemes, (a) IPDPWM; (b) PSPWM; (c) classical SVPWM; (d) proposed SVPWM.



**Figure 24.** Line-to-line voltage of 7-level inverter with different PWM schemes, (a) IPDPWM; (b) PSPWM; (c) classical SVPWM; (d) proposed SVPWM

The THDs of phase voltage and line-to-line voltage of the multilevel inverter with different modulation indexes for the four PWM schemes are shown in Figure 25.



**Figure 25.** THDs of phase voltage and line-to-line voltage of 5-level inverter with different PWM schemes, (a) phase voltage; (b) line-to-line voltage

As IPDPWM scheme and PSPWM scheme belong to carrier modulation scheme, the THDs of phase voltage and line-to-line voltage with the two PWM schemes are higher than these of the other scheme. Because phase voltage is kept constant for some time to decrease the number of commutations of the switches in the proposed SVPWM scheme, the THDs of phase voltage with the proposed SVPWM scheme is higher than these of classical SVPWM scheme. However, the THDs of line-to-line voltage with the proposed SVPWM scheme is similar to these of classical SVPWM scheme.



This is because that the proposed SVPWM scheme is derived from classical SVPWM scheme. As shown in Figure 25, the THD difference between the proposed SVPWM scheme and the classical SVPWM scheme is about 1.2%. Hence, if the proposed SVPWM scheme is used in motor speed control system, the time response of the rotor speed is slightly lower than that of the classical SVPWM scheme.

## 5. Conclusions

This paper proposes a novel switching frequency optimized SVPWM. The proposed SVPWM is developed in a  $\alpha'\beta'$  coordinate system. By planning the switching paths, only one phase voltage limited in dc-bus voltage of power cells is achieved. The experimental results show that the proposed method significantly outperforms the traditional SVPWM in terms of decreasing the number of commutations of switches.

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**Conflicts of Interest:** The authors declare no conflict of interest.

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