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# A SVPWM to Eliminate Common-Mode Voltage for Multilevel Inverters

**Xiongmin Tang [1], Chengjing Lai [1], Zheng Liu [2] and Miao Zhang [1,*]**

[1] School of automation, Guangdong University of Technology, 510006 Guangzhou, China; tangxiongmin@126.com (X.T.); laichengjing@126.com (C.L.)

[2] School of Electrical and Information Engineering, Changsha University of Science and Technology, 410004 Changsha, China; leo_johncn@163.com

* Correspondence: bezhangm@gdut.edu.cn; Tel.: +86-020-3932-2552

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**Abstract:** This paper presents a new space vector pulse width modulation (SVPWM) to eliminate common-mode voltage (CMV) for multilevel inverters. The proposed SVPWM is performed in a new coordinate system, in which the converter voltage vectors have only integer entries and the absolute coordinate increment between adjacent vectors is equal to 1. The location of the reference vector, detection of the nearest three CMV vectors, and duty cycles of the nearest three CMV vectors are all obtained by simple calculations, no lookup table is needed and the SVPWM is computationally fast. Compared with earlier pulse width modulations (PWMs), the realization of the CMV vectors is very simple, and the CMV of multilevel inverters are limited to zero with any modulation index. Because the SVPWM is independent of the level number of the inverter, the proposed SVPWM is suitable for any level of inverter. This paper also thoroughly compares the proposed SVPWM with prior PWMs. Experimental results are also given in the paper.

**Keywords:** SVPWM; common-mode voltages; multilevel inverters

## 1. Introduction

Great progress has been made in the development of multilevel inverters in recent years [1–3]. It is well known that common-mode voltages (CMVs) are linked with excessive bearing currents, which may cause premature motor bearing failure. The causes of the bearing currents and their effect on the bearing currents have been well explained by References [4–6].

For decades, passive filters and active filters [7–9] have been proposed to reduce the impact of CMVs. However, these methods cause the volume and the control of the equipment to increase significantly. Therefore, in order to reduce the impact of CMV, it is necessary to adjust the control strategies.

For multilevel inverters, some vectors have redundant switching states, and these redundant switching states can be used to decrease or eliminate the CMV. Based on this idea, different modulation methods are proposed to reduce or eliminate the CMV.

Due to the simple principle and the low harmonic distortion characteristics of sinusoidal pulse width modulation (SPWM), SPWM is widely used in multilevel inverters. Hoverer, the amplitude and the rate of change of CMV remain large, especially with high modulation indexes. This has a great influence on motor-type load. To solve this problem, a carrier modulation pulse width modulation (PWM) for a 3-level neutral point clamped (NPC) inverter is presented in Reference [10]. Because the non-nearest vectors for two triangles were selected in the PWM, this causes the total harmonic distortion (THD) of the line-to-line voltage to be higher than the conventional method. Similar PWMs have been presented in References [11–14]. However, these PWMs are difficult to extend to higher

levels. The SVPWM proposed in Reference [15] can be easily extended to higher level inverters. However, the maximum change of CMV is still limited to 1/3 of DC bus voltages of power cells.

To eliminate the CMV of multilevel inverters, zero CMVs are selected to synthesize the reference vector in the PWMs. However, most of these PWMs [16–19] are limited to 3-level or 5-level inverters, and have many unresolved issues, such as the fast location of the reference vector, the simple realization of the vectors, etc.

To address the issue, a new SVPWM to eliminate CMV for an n-level inverter is proposed in this paper. The SVPWM is carried out in a new coordinate system named the $\alpha'\beta'$ coordinate system. This new SVPWM has the following salient features:

(1) Location of the reference vector, detection of the nearest three CMV vectors, and duty cycles are all obtained by simple calculations. No lookup table is required, less memory is needed, and the SVPWM is computationally fast.
(2) Compared with earlier PWMs, the realization of the CMV vectors is very simple.
(3) CMVs of multilevel inverters are limited to zero with any modulation index.
(4) The PWM is suitable for any level of inverter.

The rest of the paper is organized as follows: Section 2 presents principle of the SVPWM. Section 3 gives experimental results and comparative analysis with other PWMs. Section 4 gives our concluding remarks.

## 2. Principle of the SVPWM

### 2.1. $\alpha'\beta'$ Coordinate System

A $\alpha'\beta'$ coordinate system is our developed coordinate system [20], and this coordinate system has been successfully applied in a capacitor voltage balancing control for diode-clamped multilevel inverters [21] and a zero-order voltage constraint for cascaded multilevel inverters [20]. In the $\alpha'\beta'$ coordinate system, the multilevel inverter voltage vectors have only integer entries, and the absolute coordinate increment between adjacent vectors is equal to 1. The transformation matrix between the $\alpha'\beta'$ coordinate system, the traditional $\alpha\beta$ coordinate system, and the *abc* coordinate system are written as:

$$\begin{bmatrix} \alpha' \\ \beta' \end{bmatrix} = \begin{bmatrix} \frac{\sqrt{3}}{2} & \frac{\sqrt{2}}{2} \\ -\frac{\sqrt{3}}{2} & \frac{\sqrt{2}}{2} \end{bmatrix} \begin{bmatrix} \alpha \\ \beta \end{bmatrix} = \begin{bmatrix} 1 & 0 & -1 \\ -1 & 1 & 0 \end{bmatrix} \begin{bmatrix} a \\ b \\ c \end{bmatrix} = \begin{bmatrix} a-c \\ -a+b \end{bmatrix} \quad (1)$$

where, $a$, $b$ and $c$ are the normalized three phase voltages of multilevel inverters. $[\alpha\ \beta]^T$ and $[\alpha'\ \beta']^T$ are the coordinate values of $[a\ b\ c]^T$ in the traditional $\alpha\beta$ coordinate system and the $\alpha'\beta'$ coordinate system, respectively. The projections of vectors for 3-level inverter in the $\alpha\beta$ and $\alpha'\beta'$ coordinate system are shown in Figure 1, where each vector is represented by one dot. $V_{ref}$ and $V'_{ref}$ are the reference vectors in the $\alpha\beta$ and $\alpha'\beta'$ coordinate systems, respectively.

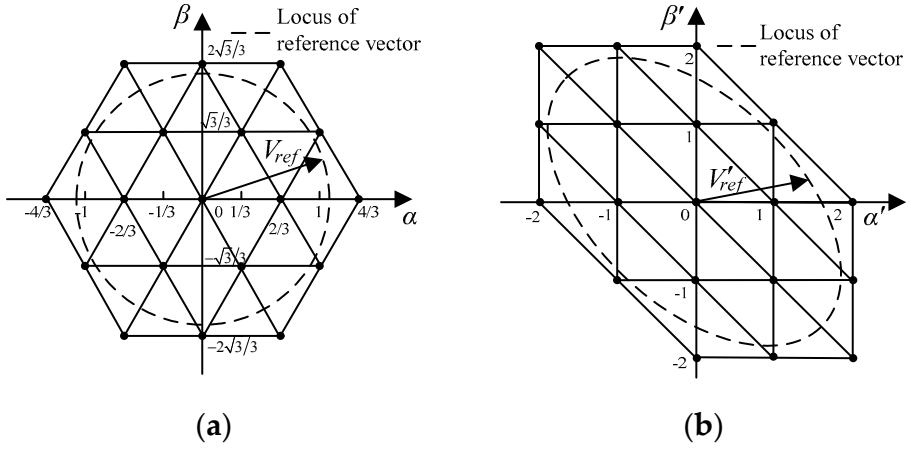



**Figure 1.** Space vector diagram for a 3-level inverter, (**a**) in the traditional αβ coordinate system, and (**b**) in the $\alpha'\beta'$ coordinate system.

### 2.2. Profile of Zero CMV

For convenience, the normalized CMV of multilevel inverters is define as:

$$N = a + b + c \tag{2}$$

With the definition, the Equation (1) can be rewritten as follows:

$$\begin{bmatrix} a \\ b \\ c \end{bmatrix} = \begin{bmatrix} 1 & 0 & -1 \\ -1 & 1 & 0 \\ 1 & 1 & 0 \end{bmatrix}^{-1} \begin{bmatrix} \alpha' \\ \beta' \\ N \end{bmatrix} = \frac{1}{3} \begin{bmatrix} \alpha' - \beta' + N \\ \alpha' + 2\beta' + N \\ -2\alpha' - \beta' + N \end{bmatrix} \tag{3}$$

The normalized CMV can be eliminated by designing for $N = 0$, and the constraint is given by the following:

$$\begin{cases} \beta' - \alpha' = -3a \\ 2\beta' + \alpha' = 3b \\ \beta' + 2\alpha' = -3c \end{cases} \tag{4}$$

Since the three sub-equations in Equation (4) are linearly dependent, Equation (4) can be simplified as:

$$\begin{cases} \beta' - \alpha' = -3a \\ \beta' + 2\alpha' = -3c \end{cases} \tag{5}$$

As shown in Equation (5), the zero CMV of the multilevel inverter must be at the intersection of the two abovementioned equations.

For $n$-level multilevel inverters, the following additional constraints should be satisfied:

$$\begin{cases} -n \le a \le n \\ -n \le b \le n \\ -n \le c \le n \end{cases} \tag{6}$$

hence,

$$\begin{cases} |\alpha'| \le 2n \\ |\beta'| \le 2n \\ |\alpha' + \beta'| \le 2n \end{cases} \tag{7}$$

After some substations and manipulations, the boundary condition for zero CMV can be obtained as:

$$\begin{cases} -3n \le \beta' - \alpha' \le 3n \\ -3n \le 2\beta' + \alpha' \le 3n \\ -3n \le \beta' + 2\alpha' \le 3n \end{cases} \tag{8}$$

From Equations (5) and (8), the space vector diagram of zero CMV for 7-level multilevel inverters is plotted in Figure 2, where each star stands for a zero CMV vector.

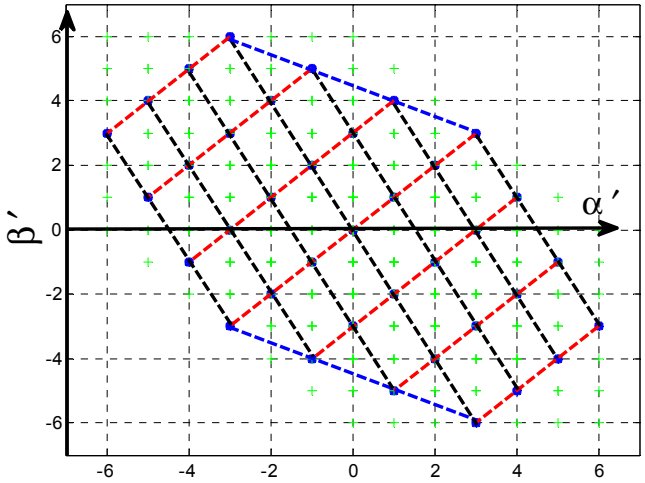



**Figure 2.** Space vector diagram of a zero common-mode voltage (CMV) vectors for a 7-level multilevel inverter.

### *2.3. Detection of the Nearest Three CMV Vectors*

As shown Figure 2, the space vector diagram composed of CMV vectors are very different from the classical space vector diagram. Hence, the location of the reference vector and the detection of the nearest three CMV vectors cannot be achieved with traditional reference vector location methods and classical vectors detection technologies [22]. In order to use the existing location methods and vectors detection technologies, the space vector diagram is divided into three zones, which are formed by the following three inequalities, respectively:

$$\begin{cases} \beta' > \alpha' \\ \beta' < -2\alpha' \end{cases} \tag{9}$$

$$\begin{cases} \beta' > -2\alpha' \\ \beta' > -0.5\alpha' \end{cases} \tag{10}$$

$$\begin{cases} \beta' < \alpha' \\ \beta' < -0.5\alpha' \end{cases} \tag{11}$$

The three zones in space vector diagram for a 7-level inverter are shown in Figure 3.

Based on the zone division in the space vector diagram, the location of the reference vector and the detection of the nearest three CMV vectors can be made with existing location methods and vectors detection technologies.

If the reference vector is in zone 1, the four adjacent vectors $V_0$–$V_3$ around the reference vector can be calculated as:

$$\begin{cases} V_0 = [floor(\alpha'_r) floor(\beta'_r)] = [\alpha'_0 \beta'_0] \\ V_1 = [floor(\alpha'_r) + 2floor(\beta'_r) - 1] = [\alpha'_0 + 2\beta'_0 - 1] \\ V_2 = [floor(\alpha'_r) + 1floor(\beta'_r) - 2] = [\alpha'_0 + 1\beta'_0 - 2] \\ V_3 = [floor(\alpha'_r) + 1floor(\beta'_r) + 1] = [\alpha'_0 + 1\beta'_0 + 1] \end{cases} \tag{12}$$

where $\alpha'_r$ and $\beta'_r$ are the normalized three phase voltages of the reference vector. The floor function rounds towards negative infinity.

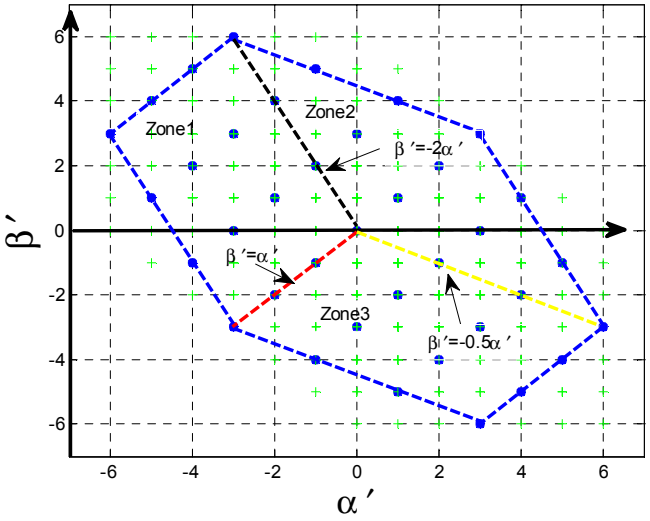



**Figure 3.** Three zones in a space vector diagram for an 11-level inverter.

Because $V_0$ and $V_1$ are always two of the nearest three vectors, the third vector $V_{sel}$ can be obtained by:

$$\begin{array}{ll} \text{if } \beta'_r + 0.5 \cdot \alpha'_r \leq 1.5(N_1 + N_2) & \text{then } V_{sel} = V_2 \\ & \text{else } V_{sel} = V_3 \end{array} \tag{13}$$

where $N_1 = \text{ceil}((\beta'_r - \alpha'_r)/3)$, $N_2 = \text{floor}((\beta'_r + 2\alpha'_r)/3)$. The ceil function rounds towards positive infinity.

If the third vector was $V_2$, the duty cycles of the three vectors are calculated as:

$$\begin{cases} d_{V0} = (\alpha'_r - \beta'_r + 3N_1)/3 \\ d_{V1} = (\alpha'_r + 2\beta'_r - 3N_2 - 3N_1)/3 \\ d_{V2} = (1 - d_{V0} - d_{V1}) \end{cases} \tag{14}$$

And, if the third vector was $V_3$, the duty cycles of the three vectors are obtained from:

$$\begin{cases} d_{V0} = (2\alpha'_r + \beta'_r + 3N_2)/3 \\ d_{V1} = (-\alpha'_r - 2\beta'_r + 3N_2 + 3N_1)/3 \\ d_{V3} = (1 - d_{V0} - d_{V1}) \end{cases} \tag{15}$$

By following the above mentioned steps, the location of the reference vector and the detection of the nearest three CMV vectors in zone 2 and in zone 3 can be obtained easily.

After the CMV vector is selected, the realization of the CMV vectors is obtained from:

$$\begin{cases} a = (\alpha' + \beta')/3 \\ b = a + \beta' \\ c = a - \alpha' \end{cases} \tag{16}$$

Without complicated calculations, the realization of the CMV vectors is calculated.

Clearly, the location of the reference vector, detection of the nearest three CMV vectors, duty cycles, and realization of the CMV vectors are all obtained by simple calculations, and no lookup table is needed. Hence, the proposed SVPWM is computationally fast.

## 3. Experimental Results

### *3.1. Experimental Setup*

A 7-level cascaded multilevel inverter was built in the laboratory, as shown in Figure 4. Nine isolation DC powers for the 7-level inverter were formed by nine 200 W isolation transformers and diode rectifier bridges. The dc-bus voltage of power cells was selected to be 50 V. The model of switches in the inverter was IRFP460, and the driver circuits for the switches were a compound of a high-speed opt-coupler (model: 6N137) and IR2110. The 7-level inverter was controlled by a TMS320F28335 floating-point digital signal processor (DSP) from Texas Instruments. The experimental setup is shown in Figure 5.

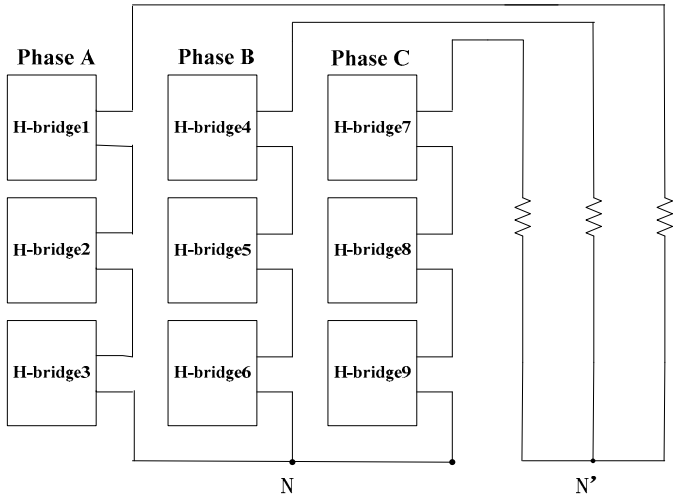



**Figure 4.** 7-level cascaded multilevel inverter.

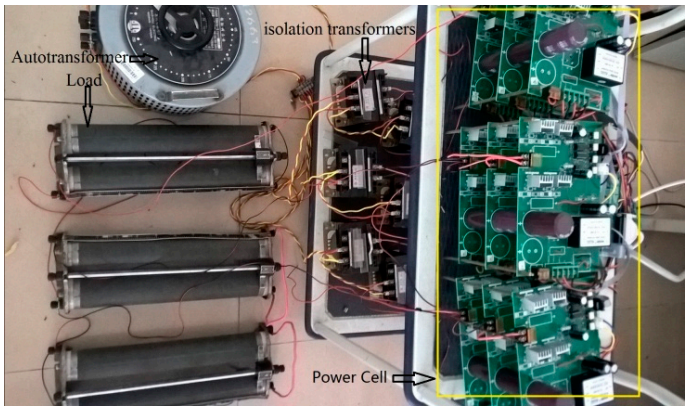



**Figure 5.** Experimental setup.

### *3.2. Experimental Results*

The waveforms, including phase voltage, line-to-line voltage and CMV, with different modulation indices are presented in Figures 6–8, respectively. In these figures, the fundamental frequency of the output voltage is 20 Hz, and there are 84 sampling points in a working period. The modulation index $m$ is equal to 0.868, 0.797 and 0.707, respectively.

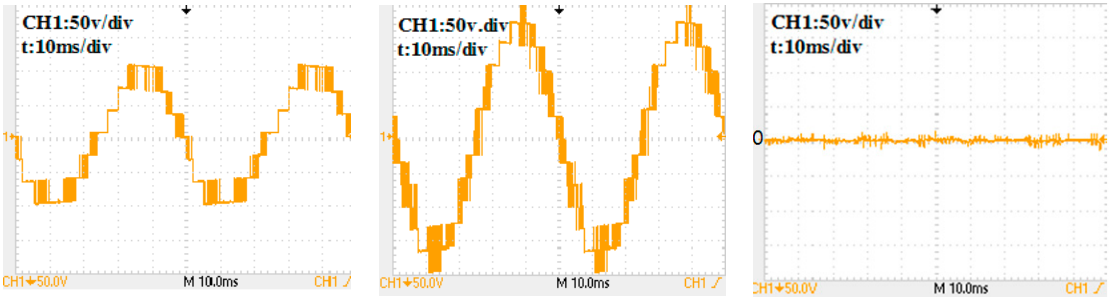



**Figure 6.** Experimental waves with $m$ = 0.868: (**a**) phase voltage; (**b**) line-to-line voltage; (**c**) CMV.

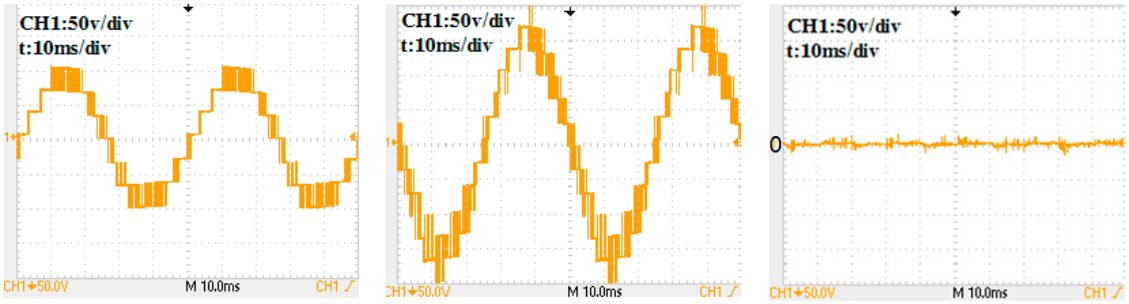



**Figure 7.** Experimental waves with $m$ = 0.791: (**a**) phase voltage; (**b**) line-to-line voltage; (**c**) CMV.

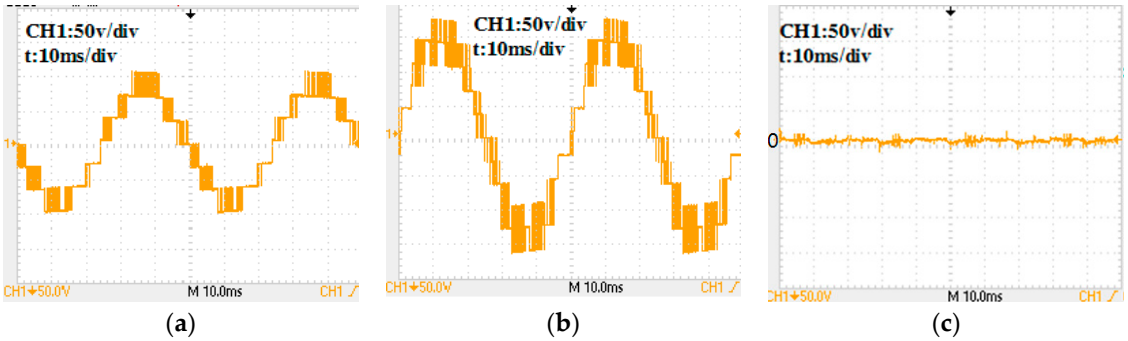


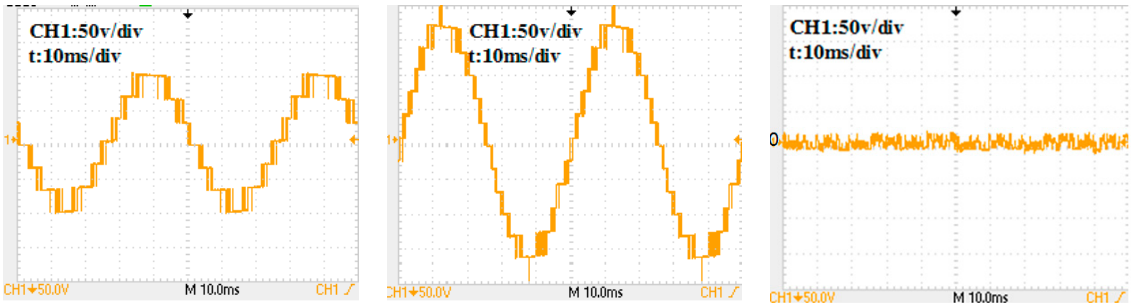

**Figure 8.** Experimental waves with $m$ = 0.707: (**a**) phase voltage; (**b**) line-to-line voltage; (**c**) CMV.

As can be seen from the waveforms, the CMV of the cascaded multilevel inverter is kept at zero with any modulation index when the proposed SVPWM is adopted.

### *3.3. Comparison with Prior PWMs*

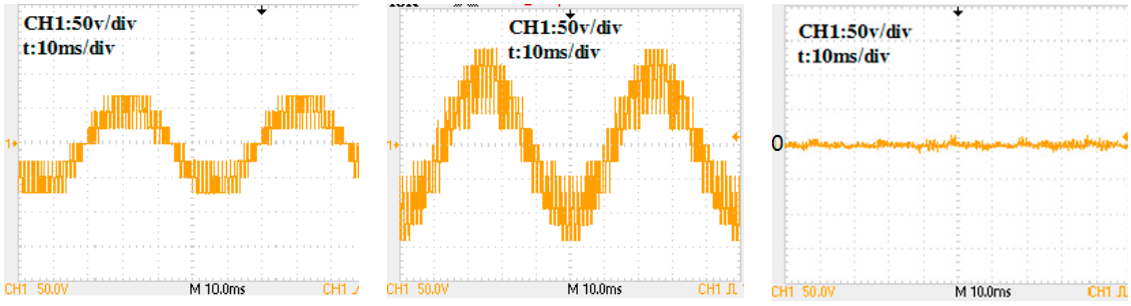
The waveforms of phase voltage, line-to-line voltage and CMV for a 7-level inverter by traditional CMV limiting SVPWM [15] and CMV eliminating PWM [20] are shown in Figures 9 and 10, respectively. In Figures 9 and 10, the fundamental frequency of the output voltage is 20 Hz, there are 84 sampling points in a working period, and the modulation index is 0.868.

The THD of phase voltage, line-to-line voltage and the number of commutations of the switches for a 7-level multilevel and an 11-level multilevel with different modulation indexes for the three PWMs are shown in Figures 11 and 12, respectively.



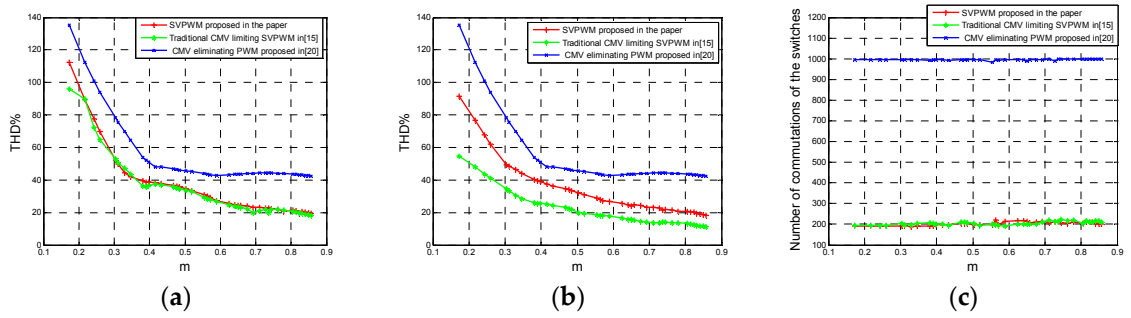

(**a**) (**b**) (**c**)

**Figure 9.** Experimental waves by traditional CMV-limiting SVPWM proposed in Reference [15] for a 7-level inverter: (**a**) phase voltage; (**b**) line-to-line voltage; (**c**) CMV.



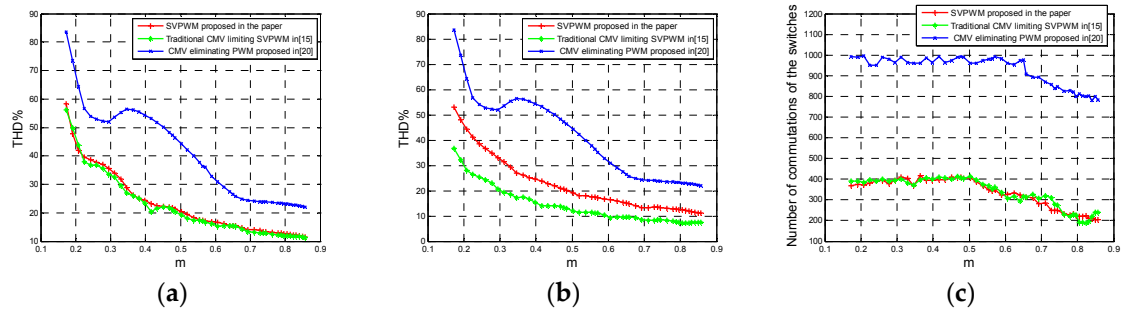

(**a**) (**b**) (**c**)

**Figure 10.** Experimental waves by a CMV-eliminating PWM proposed in Reference [20] for a 7-level inverter: (**a**) phase voltage; (**b**) line-to-line voltage; (**c**) CMV.




(**a**) (**b**) (**c**)

**Figure 11.** Comparison of the three PWMs in a 7-level inverter with different modulation indices: (**a**) THD of phase voltage; (**b**) THD of line-to-line voltage; (**c**) the number of commutations of switches.




(**a**) (**b**) (**c**)

**Figure 12.** Comparison of the three PWMs mentioned above in an 11-level inverter with different modulation indices: (**a**) THD of phase voltage; (**b**) THD of line-to-line voltage; (**c**) the number of commutations of switches.

As shown in Figures 9 and 10, while the CMV of multilevel inverters can be limited to 1/3 of the dc-bus voltage of power cells by traditional CMV-limiting SVPWM, the CMV of multilevel inverters can be eliminated by the proposed SVPWM.

It is shown in Figures 11 and 12 that the THD of the phase voltage by the SVPWM proposed in this paper is almost exactly the same as the THD of the phase voltage by the traditional CMV-limiting SVPWM, and similar findings have been obtained for the number of commutations of the switches by the two SVPWMs as well. This is because the reference vector is synthesized with the three nearest vectors in both of these SVPWMs.

However, the THD of line-to-line voltage by the proposed SVPWM is higher than that by the traditional CMV-limiting SVPWM. This is because the distance between the selected vectors in the proposed SVPWM is longer than that in the traditional SVPWM. Because the distances between the three selected vectors decrease with the increasing of the number of level, the difference of the THD of line-to-line voltage becomes smaller.

Although the CMV can be eliminated by the CMV-eliminating PWM proposed in Reference [20], the PWM is still a carrier modulation. This makes the THD of phase voltage, the THD of line-to-line voltage and the number of commutations of the switches higher than those achieved by the proposed SVPWM.

## 4. Conclusions

A new SVPWM to eliminate common-mode voltages for multilevel inverters is proposed in this paper. The proposed SVPWM is performed in the $\alpha'\beta'$ coordinate system. Based on the constraints of zero CMVs in the $\alpha'\beta'$ coordinate system, the nearest three vectors are selected and their duty cycles are calculated by simple calculations. Experimental results for a 7-level inverter verified the proposed SVPWM. The proposed SVPWM scheme has the following significant advantages compared with prior SVPWM schemes:

(1) Switching states and duty cycles are all obtained by simple calculations, and the SVPWM is computationally fast.
(2) Compared to earlier PWMs, the realization of the CMV vectors is very simple.
(3) CMVs of multilevel inverters are limited to zero, and the SVPWM works well with any modulation index.
(4) The proposed SVPWM is suitable for any level inverter. A more detailed comparison between the proposed SVPWM and prior PWMs is given. The advantages of this SVPWM make it a preferred SVPWM for the elimination of the common-mode voltages of multilevel inverters.

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**Author Contributions:** Xiongmin Tang wrote the paper and performed the experimental work; Chengjing Lai contributed to the writing and arranging of the analytical data; Zheng Liu contributed to perform the simulation work. Miao Zhang contributed to providing reagents/materials/analysis tools and supervised the paper.

**Conflicts of Interest:** The authors declare no conflict of interest.

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