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Design and Evaluation of an Efficient Three-Phase Four-Leg Voltage Source Inverter with Reduced IGBTs

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Abstract: This paper presents a new three-phase four-leg voltage source inverter (VSI), which achieves a high cost effectiveness for mega-watt level system applications. The proposed four-leg inverter adopts the integrated topology with thyristors and insulated-gate bipolar transistors (IGBTs), which aims to reduce the number of IGBTs. In order to handle the zero sequence current, a neutral leg via incorporating IGBTs is artfully integrated with the regular phase legs. Furthermore, the modelling principles are elaborated and analyzed, which emphasizes switching states and voltage vectors in six segments based on the states of thyristors. Finally, by using the carrier-based pulse width modulation (PWM) method, the closed-loop current control of the proposed inverter is verified by both simulation and experimentation.

Keywords: power inverter; voltage source inverter; four-leg inverter; cost-effectiveness; current control; pulse width modulation

1. Introduction

Three-phase voltage source inverters (VSI) are widely used in industrial applications such as uninterruptable power supply (UPS) [1,2], motor drives [3–5], wireless power transfer [6] and distributed power generation system [7,8]. Unfortunately, this conventional topology is hard to keep the neutral point potential in a constant level under unbalanced load conditions, which leads to asymmetric output voltage [9]. To solve this problem, a split capacitor three-phase inverter is investigated in [10], but such a topology poses a problem of low DC voltage utilization. Alternatively, the three-phase four-leg VSI that connects the neutral point to the fourth leg is investigated by [11–18]. In fact, three-phase four-leg VSI is widely used in various industrial applications, such as distributed power generation, three phase UPS systems and series active filters, where the balanced three-phase voltage output is required during unbalanced load conditions [19–21]. However, the topology and control algorithm of the four-leg VSI are inherently more complex than the traditional three-phase type.

There has been a substantial increasing trend in control strategy investigations on three-phase four-leg inverters, including the carrier-based pulse width modulation (PWM) [22,23], space vector modulation algorithm [24,25], and digital predictive control [26,27]. Firstly, a minimally switched control algorithm is studied, which can minimize switching operations and monitor the current polarity for three-phase four-leg inverter [28]. Then, a selective harmonic elimination (SHE) control strategy on

a three-phase four-leg inverter is reported in [29], where the lower order nontriplen harmonics are eliminated by using Fourier-based equations on line-to-line basis as conventional SHE technology to express the control signals of three legs. In addition, two methods that mitigate the load neutral point voltage (LNPV) for three-phase four-leg inverters are analyzed, which are based on the PWM strategy and the common mode filter, respectively [30]. Moreover, a decoupled sequence control strategy, employing positive sequence, negative sequence, and zero sequence controllers is studied in [31].

However, the available publications on three-phase four-leg inverters are limited to eight-insulated-gate bipolar transistors (IGBTs) topologies, as illustrated in Figure 1a. In mega-watt level applications, the IGBT with a rated current of thousands of ampere is not cost-effective and is not suitable for some cost-sensitive situations.

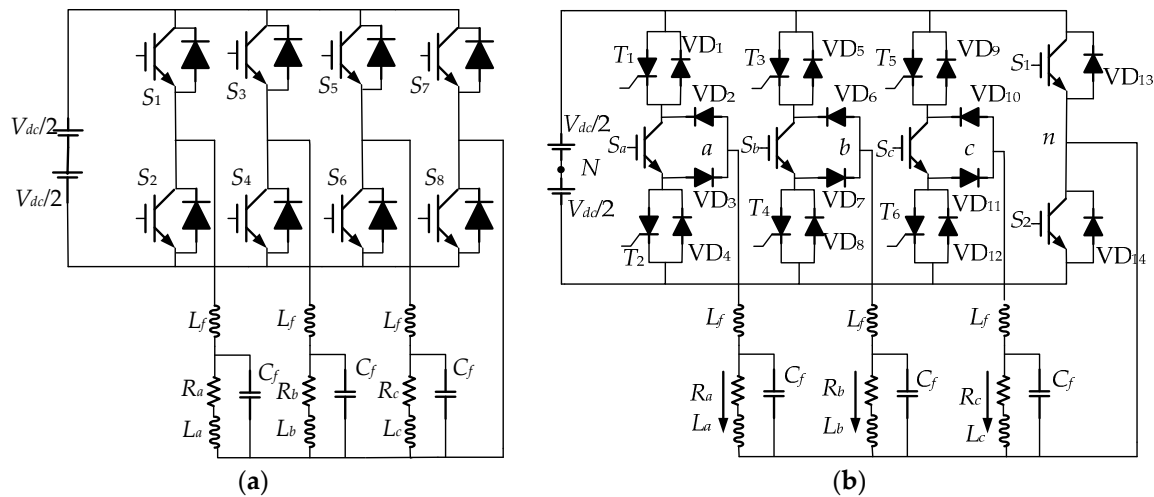


Figure 1. Configurations of a three-phase four-leg inverter, (a) Conventional topology with eight IGBTs; (b) Proposed topology with five IGBTs.

The purpose of this paper is to propose and evaluate an IGBT-reduced three-phase four-leg VSI that possesses the attractive feature of four-leg inverters. The proposed topology can reduce cost significantly, especially for mega-watt level applications such as electric ship propulsion systems, microgrid converters, motor drives, and so on. In Section 2, the configuration of the proposed inverter and the operation principle will be introduced. Section 3 will be devoted to deducing the representation of inverter output voltages as a three-dimensional space vector in a stator oriented $\alpha\beta\gamma$ rectangular coordinate. In Section 4, closed-loop current control strategy of the proposed inverter will be presented. Then, simulation and experiment results will be given to verify the validity of the proposed inverter in Section 5. Consequently, a quantitative comparison between the proposed inverter and the conventional three-phase four-leg inverter will be made in Section 6. Finally, conclusions will be drawn in Section 7.

2. Topology and Operation Principle of the Proposed Inverter

The proposed cost-effective three-phase four-leg VSI is shown in Figure 1b. In particular, the proposed inverter has the definite benefit of the reduction of three IGBTs. In addition, according to the current market price, with a rated current of one thousand ampere, the thyristor is much cheaper than the IGBT. Though the number of gating signals and control complexity increase inherently due to the existence of the fourth leg, it possesses the advantage of handling unbalanced loads over the three-leg inverter.

From Figure 1b, it also can be found that the thyristors are employed in phase legs, while the IGBTs and diodes are in the fourth leg. Upon the commutation of the phase current alone, the thyristors turn off naturally. Thus, the zero-crossing point of phase currents is the major factor which determines

the switching time of thyristors. Also, it is worth mentioning that the directions of injected currents for the analysis of the converter operation modes are shown in Figure 1b. Normally, the thyristors in the same leg are not allowed to be switched on or off simultaneously. In particular, the upper one is switched on during the positive cycle, while the lower one is on during the negative cycle. Consequently, there are six combinations for upper thyristor switching states and each combination corresponds to a specific time interval, as shown in Figure 2.

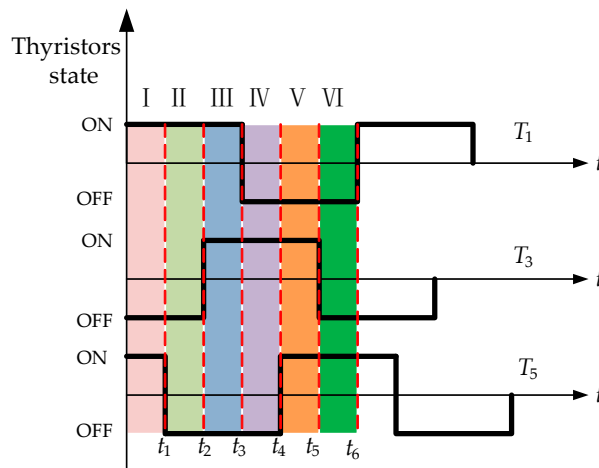


Figure 2. Six divided segments based on the thyristor states.

In Segment I, T_1 is switched on, T_3 is off and T_5 is on. For phase a , when S_a is turned on, current flows through T_1 , S_a , and VD_3 . When S_a is turned off, the freewheeling current flows through VD_4 , as shown in Figure 3a. It should be noted the current direction in phase b is negative in Segment I. Thus, the current flows through VD_6 , S_b , and T_4 when S_b is on, and the current passes through the freewheeling diode VD_5 when S_b is off. Meanwhile, phase c is in the same condition as phase a , while the fourth leg can be analyzed as a typical inverter leg. According to these situations, the thyristor-IGBT combined leg can be regarded as the same flowing path as a typical inverter leg. Therefore, based on the proposed topology, one IGBT can provide the flowing path for both positive and negative currents, whereas the current needs to pass through two different IGBTs in the conventional inverter leg.

The current flow paths for the other five segments can be analyzed in the same manner, while all individual paths are illustrated in Figure 3b–f.

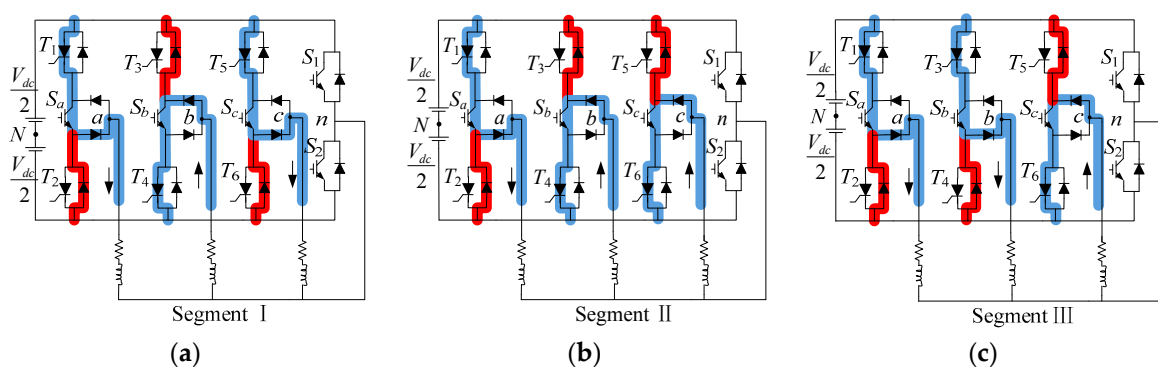


Figure 3. Cont.

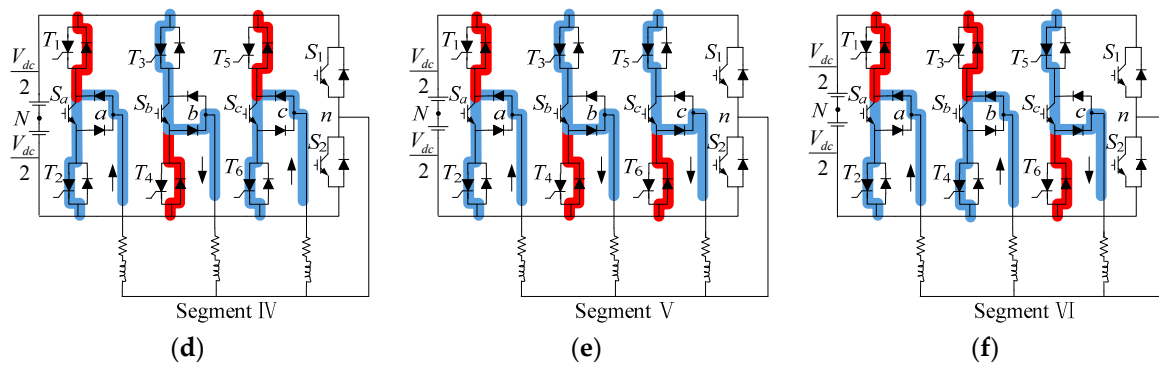


Figure 3. Current flow path in six segments: (a) Segment I; (b) Segment II; (c) Segment III; (d) Segment IV; (e) Segment V; (f) Segment VI.

3. Mathematical Modelling

It should be noted that when the thyristors are involved, the voltage equations would differ from those produced by the conventional three-phase four-leg inverter. Referring to the middle point of the direct current (DC) link, the voltages in each leg are defined separately for the positive and negative cycles of the alternating current (AC) which is based on consideration of the thyristor states. The relationship can be described as,

$$\begin{bmatrix} v_{aN} \\ v_{bN} \\ v_{cN} \\ v_{nN} \end{bmatrix} = \begin{bmatrix} 2S_a - 1 \\ 2S_b - 1 \\ 2S_c - 1 \\ 2S_1 - 1 \end{bmatrix} \times \frac{V_{dc}}{2} \quad (T_1, T_3, T_5 \text{ is on}) \quad (1)$$

$$\begin{bmatrix} v_{aN} \\ v_{bN} \\ v_{cN} \\ v_{nN} \end{bmatrix} = \begin{bmatrix} 1 - 2S_a \\ 1 - 2S_b \\ 1 - 2S_c \\ 2S_1 - 1 \end{bmatrix} \times \frac{V_{dc}}{2} \quad (T_1, T_3, T_5 \text{ is off}) \quad (2)$$

where v_{aN} , v_{bN} , v_{cN} , and v_{nN} are the voltage potentials between points a , b , c , n and N , respectively.

$$S_i = \begin{cases} 1, & \text{when } S_i \text{ is on} \\ 0, & \text{when } S_i \text{ is off} \end{cases} \quad (i = a, b, c, 1) \quad (3)$$

Referring to Figure 1b, the phase voltage that is represented in the matrix can be governed by

$$\begin{bmatrix} v_{an} \\ v_{bn} \\ v_{cn} \\ v_n \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 & -1 \\ 0 & 1 & 0 & -1 \\ 0 & 0 & 1 & -1 \\ 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} v_{aN} \\ v_{bN} \\ v_{cN} \\ v_{nN} \end{bmatrix} \quad (4)$$

where v_{an} , v_{bn} , and v_{cn} are the voltage potentials between points a , b , c , and n , respectively.

Normally, a four-leg inverter consists of $2^4 = 16$ possible switching states, while for the new topology, the states of thyristors have to be considered beside the states of IGBTs. The relationship between phase voltage and switching states of phase a are summarized in Table 1, where the UT stands for “Upper Thyristor”. Based on the same rationale, the phase voltages of phase b and phase c can be analyzed in the same manner.

Table 1. Switching States and Phase Voltage of Phase *a*.

Switching States		Phase <i>a</i>						
S_1	1			0				
UT	1	0		1		0		
S_a	1	0	1	0	1	0	1	0
v_{an}	0	$-V_{dc}$	$-V_{dc}$	0	V_{dc}	0	0	V_{dc}

It can be seen that there are, in total, eight switching-state combinations in accordance to three voltages for each phase. When the states of UT are opposite, the corresponding phase voltage is inverse. This feature can be utilized to simplify the control algorithm of the proposed inverter. The typical converter's modes of voltage vectors are analyzed in the aforementioned six segments, also known as intervals, individually.

Since the state of the thyristor does not change within one segment, the voltage vectors can only be defined according to the IGBT state in each segment. Therefore, the basic voltage vectors of 16-switching states are expressed in a binary system as 0000, 0001, ..., 1111, respectively, where the switching states are described in the order of S_a , S_b , S_c , and S_1 . The distributions of the voltage vectors in all six segments can be obtained via Equations (1)–(4). The corresponding results are summarized in Table 2.

Table 2. Switching Combinations and Voltage Vectors.

Vectors	States	v_{an}, v_{bn}, v_{cn}					
		I	II	III	IV	V	VI
V_0	0000	0, 1, 0	0, 1, 1	0, 0, 1	1, 0, 1	1, 0, 0	1, 1, 0
V_1	0001	−1, 0, −1	−1, 0, 0	−1, −1, 0	0, −1, 0	0, −1, −1	0, 0, −1
V_2	0010	0, 1, 1	0, 1, 0	0, 0, 0	1, 0, 0	1, 0, 1	1, 1, 1
V_3	0011	−1, 0, 0	−1, 0, −1	−1, −1, −1	0, −1, −1	0, −1, 0	0, 0, 0
V_4	0100	0, 0, 0	0, 0, 1	0, 1, 1	1, 1, 1	1, 1, 0	1, 0, 0
V_5	0101	−1, −1, −1	−1, −1, 0	−1, 0, 0	0, 0, 0	0, 0, −1	0, −1, −1
V_6	0110	0, 0, 1	0, 0, 0	0, 1, 0	1, 1, 0	1, 1, 1	1, 0, 1
V_7	0111	−1, −1, 0	−1, −1, −1	−1, 0, −1	0, 0, −1	0, 0, 0	0, −1, 0
V_8	1000	1, 1, 0	1, 1, 1	1, 0, 1	0, 0, 1	0, 0, 0	0, 1, 0
V_9	1001	0, 0, −1	0, 0, 0	0, −1, 0	−1, −1, 0	−1, −1, −1	−1, 0, −1
V_{10}	1010	1, 1, 1	1, 1, 0	1, 0, 0	0, 0, 0	0, 0, 1	0, 1, 1
V_{11}	1011	0, 0, 0	0, 0, −1	0, −1, −1	−1, −1, −1	−1, −1, 0	−1, 0, 0
V_{12}	1100	1, 0, 0	1, 0, 1	1, 1, 1	0, 1, 1	0, 1, 0	0, 0, 0
V_{13}	1101	0, −1, −1	0, −1, 0	0, 0, 0	−1, 0, 0	−1, 0, −1	−1, −1, −1
V_{14}	1110	1, 0, 1	1, 0, 0	1, 1, 0	0, 1, 0	0, 1, 1	0, 0, 1
V_{15}	1111	0, −1, 0	0, −1, −1	0, 0, −1	−1, 0, −1	−1, 0, 0	−1, −1, 0

Note: The unit of the output voltage is V_{dc} .

The phase voltages can also be expressed regarding the load and current as

$$\begin{bmatrix} v_{an} \\ v_{bn} \\ v_{cn} \end{bmatrix} = L_f \begin{bmatrix} \frac{di_a}{dt} \\ \frac{di_b}{dt} \\ \frac{di_c}{dt} \end{bmatrix} + L_f C_f \begin{bmatrix} \frac{d^2 u_{sa}}{dt^2} \\ \frac{d^2 u_{sb}}{dt^2} \\ \frac{d^2 u_{sc}}{dt^2} \end{bmatrix} + \begin{bmatrix} u_{sa} \\ u_{sb} \\ u_{sc} \end{bmatrix} \quad (5)$$

where

$$\begin{bmatrix} u_{sa} \\ u_{sb} \\ u_{sc} \end{bmatrix} = \begin{bmatrix} L_a \frac{di_a}{dt} \\ L_b \frac{di_b}{dt} \\ L_c \frac{di_c}{dt} \end{bmatrix} + \begin{bmatrix} R_a i_a \\ R_b i_b \\ R_c i_c \end{bmatrix} \quad (6)$$

Moreover, (5) in $\alpha\beta\gamma$ coordinate can be further formulated as

$$\begin{bmatrix} v_\alpha \\ v_\beta \\ v_\gamma \end{bmatrix} = L_f \begin{bmatrix} \frac{di_\alpha}{dt} \\ \frac{di_\beta}{dt} \\ \frac{di_\gamma}{dt} \end{bmatrix} + C_f \begin{bmatrix} \frac{d^2 u_{s\alpha}}{dt^2} \\ \frac{d^2 u_{s\beta}}{dt^2} \\ \frac{d^2 u_{s\gamma}}{dt^2} \end{bmatrix} + \begin{bmatrix} u_{s\alpha} \\ u_{s\beta} \\ u_{s\gamma} \end{bmatrix} \quad (7)$$

where

$$\begin{bmatrix} u_{s\alpha} \\ u_{s\beta} \\ u_{s\gamma} \end{bmatrix} = \begin{bmatrix} L_a \frac{di_a}{dt} \\ L_b \frac{di_b}{dt} \\ L_c \frac{di_c}{dt} \end{bmatrix} + \begin{bmatrix} R_a i_a \\ R_b i_b \\ R_c i_c \end{bmatrix} \quad (8)$$

In particular, the quantities v_{an} , v_{bn} , v_{cn} and i_a , i_b , i_c in Equation (5) can be transformed to $\alpha\beta\gamma$ coordinate.

Through (1)–(8), the voltage vectors v_α , v_β and v_γ in $\alpha\beta\gamma$ coordinate can be obtained from Segment I to Segment VI, respectively. v_α and v_β form a hexagon in the $\alpha\beta$ plane as shown in Figure 4, where each vector corresponds to a combination of different switching states in different segments. Moreover, it should be noted that v_γ is determined by the state of the fourth leg. The graphical representation of all voltage vectors in the six segments in $\alpha\beta\gamma$ coordinate is shown in Figure 5. It can be seen that there are fourteen nonzero voltage vectors and two zero vectors in each segment. However, the same voltage vector in different segments is formed by different corresponding switching state combinations. For instance, 0110 in Segment I forms the same voltage vector as 0100 in Segment II. Moreover, there are seven $\alpha\beta$ planes in each coordinate. The distance between each of them is $1/3$.

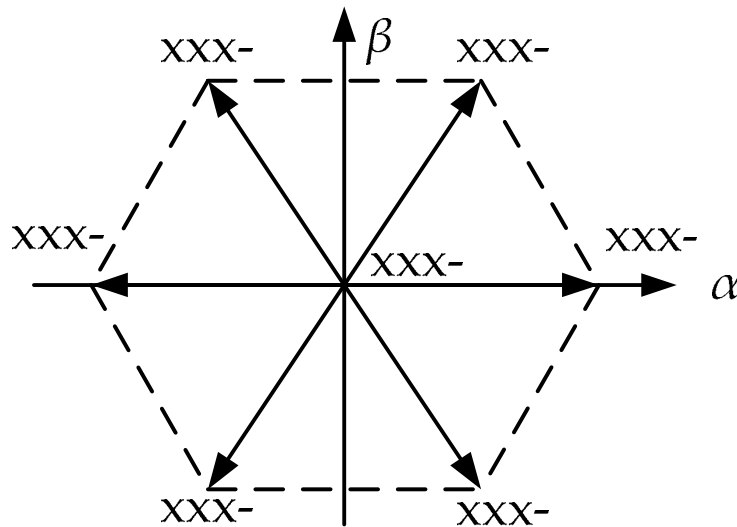


Figure 4. Switching projection of inverter vectors in $\alpha\beta$ plane.

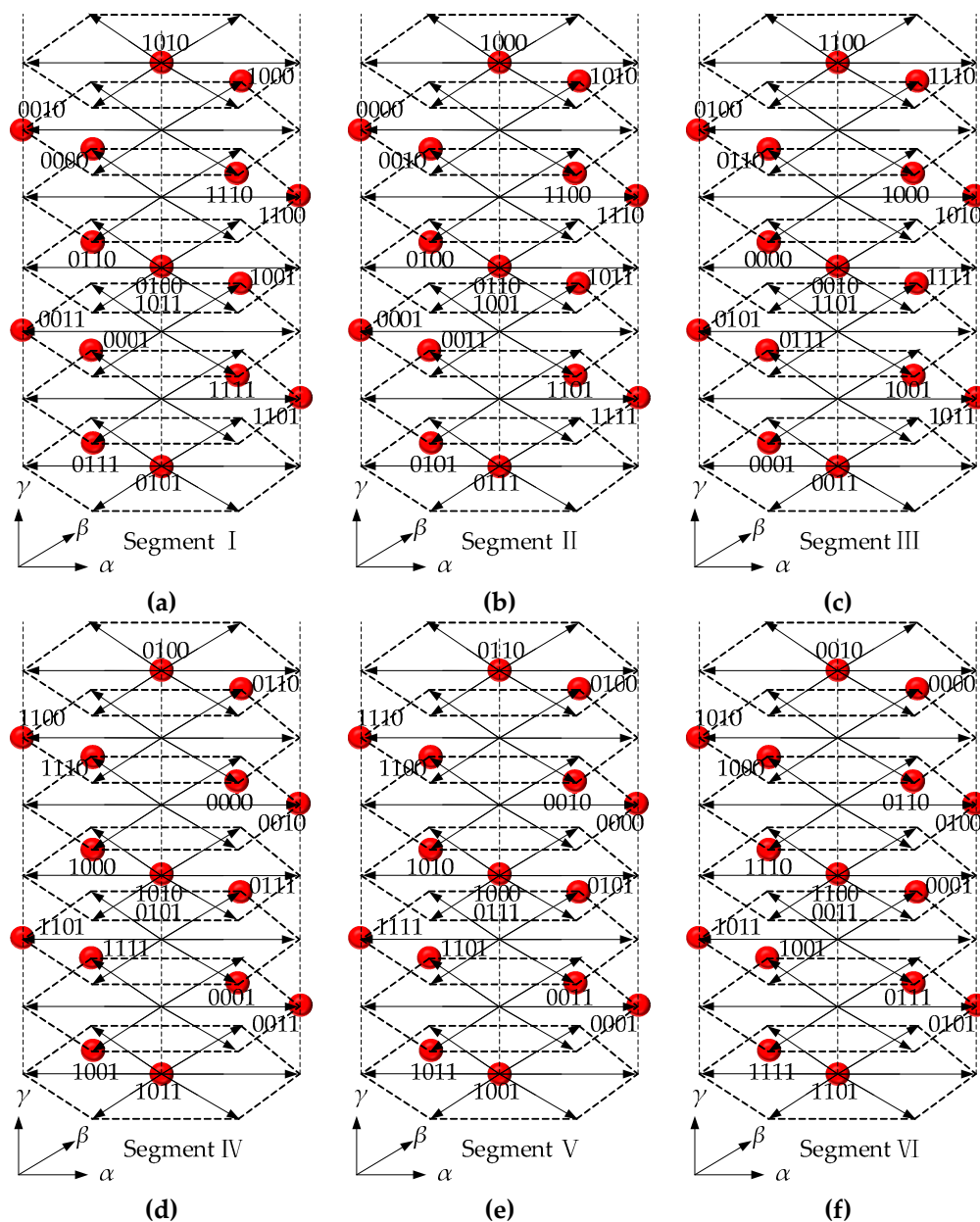


Figure 5. Switching projection of inverter vectors in $\alpha\beta\gamma$ plane: (a) Segment I; (b) Segment II; (c) Segment III; (d) Segment IV; (e) Segment V; (f) Segment VI.

4. Current Control Algorithm for Proposed Inverter

Carrier-based pulse width modulation (PWM) with proportional resonant (PR) controllers and a pulse computational module (PCM) are employed to regulate the output currents of the proposed inverter. The control algorithm is depicted in Figure 6.

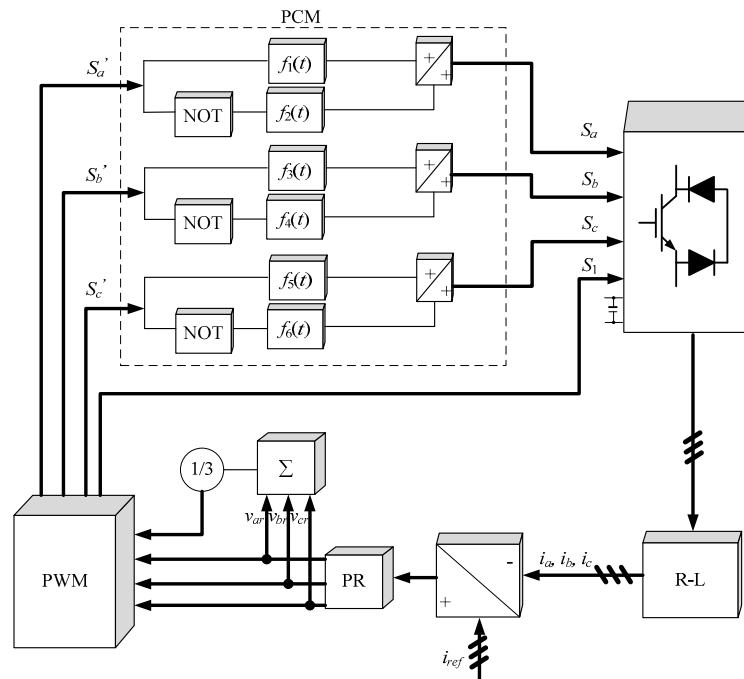


Figure 6. Current control diagram of the proposed inverter.

The PR regulator is used due to its capability of tracking the AC current with zero steady-state error. The practical PR controller is described by the transfer function [32]:

$$G(s) = k_p \left[1 + \frac{s}{T_i(s^2 + \omega_r s + \omega_0^2)} \right] \quad (9)$$

where k_p is the proportional gain, T_i is the integral gain, ω_r is the resonant cut off frequency, and ω_0 is equal to the inverter frequency.

The error between the measured current and the reference are sent to the PR controller to produce commands v_{ar} , v_{br} and v_{cr} . It is worth mentioning that the neutral leg is commanded by the average of the other three phase voltages,

$$v_M = \frac{1}{3}(v_{ar} + v_{br} + v_{cr}) \quad (10)$$

Each modulator generates a signal for one inverter leg when keeping with the principle of PWM. However, except for the neutral leg, the signals produced by PWM modulator have to be processed through a PCM before sending them to IGBTs. According to Table 1, it indicates that the opposite state thyristor corresponds to the inverse phase voltage. Therefore, the switching signal values generated from the PWM modulator for phase legs in the negative cycle should be flipped using a “NOT” function. This computation process can be expressed through the piecewise functions where, the pulse computation function for the positive cycle of phase a is shown as:

$$f_1(t) = \begin{cases} 1, & nT + \Delta t \leq t \leq nT + \frac{T}{2} + \Delta t, \quad n = 0, 1, 2, 3 \dots \\ 0, & nT + \frac{T}{2} + \Delta t \leq t \leq (n+1)T + \Delta t, \quad n = 0, 1, 2, 3 \dots \end{cases} \quad (11)$$

the pulse computation function for the negative cycle of phase a is shown as:

$$f_2(t) = \begin{cases} 0, & nT + \Delta t \leq t \leq nT + \frac{T}{2} + \Delta t, \quad n = 0, 1, 2, 3 \dots \\ 1, & nT + \frac{T}{2} + \Delta t \leq t \leq (n+1)T + \Delta t, \quad n = 0, 1, 2, 3 \dots \end{cases} \quad (12)$$

the pulse computation function for the positive cycle of phase b is shown as:

$$f_3(t) = \begin{cases} 1, & nT + \frac{T}{3} + \Delta t \leq t \leq nT + \frac{5T}{6} + \Delta t, \quad n = 0, 1, 2, 3 \dots \\ 0, & nT + \frac{5T}{6} + \Delta t \leq t \leq (n+1)T + \frac{T}{3} + \Delta t, \quad n = 0, 1, 2, 3 \dots \end{cases} \quad (13)$$

the pulse computation function for the negative cycle of phase b is shown as:

$$f_4(t) = \begin{cases} 0, & nT + \frac{T}{3} + \Delta t \leq t \leq nT + \frac{5T}{6} + \Delta t, \quad n = 0, 1, 2, 3 \dots \\ 1, & nT + \frac{5T}{6} + \Delta t \leq t \leq (n+1)T + \frac{T}{3} + \Delta t, \quad n = 0, 1, 2, 3 \dots \end{cases} \quad (14)$$

the pulse computation function for the positive cycle of phase c is shown as:

$$f_5(t) = \begin{cases} 1, & nT + \frac{2T}{3} + \Delta t \leq t \leq (n+1)T + \frac{T}{6} + \Delta t, \quad n = 0, 1, 2, 3 \dots \\ 0, & (n+1)T + \frac{T}{6} + \Delta t \leq t \leq (n+1)T + \frac{2T}{3} + \Delta t, \quad n = 0, 1, 2, 3 \dots \end{cases} \quad (15)$$

the pulse computation function for the negative cycle of phase c is shown as:

$$f_6(t) = \begin{cases} 0, & nT + \frac{2T}{3} + \Delta t \leq t \leq (n+1)T + \frac{T}{6} + \Delta t, \quad n = 0, 1, 2, 3 \dots \\ 1, & (n+1)T + \frac{T}{6} + \Delta t \leq t \leq (n+1)T + \frac{2T}{3} + \Delta t, \quad n = 0, 1, 2, 3 \dots \end{cases} \quad (16)$$

here, T is the period of the phase current.

Using the PCM, all IGBTs are controlled. Phase shift factor Δt is defined in piecewise functions. The optimum value of Δt is tuned to reduce the total harmonics distortion (THD) of the output current. To control the thyristors, a triggering pulse is sent to the upper thyristor at the start of each positive cycle and to the lower thyristor at the start of each negative cycle. When the current crosses zero, the thyristor is switched off accordingly.

5. Verification Results of Proposed Topology

In order to verify the proposed topology, simulations and experiments are conducted and analyzed. The system parameters for the simulation are listed in Table 3. The closed-loop current feedback control was implemented.

Table 3. Key Parameters of Simulation System.

Parameters	Values
DC link voltage	100 V
AC filter inductor for each phase	5 mH
Ac filter capacitor for each phase	1.5 μ F
Switching frequency	5 kHz
Load inductor	1.5 mH
Load resistor	3-phase variable resistors

5.1. Simulation Results

Using the current feedback PWM scheme, the proposed inverter is operated with a balanced load, as shown in Figure 7. With the support of the PR controller loop, the static performance of the current is satisfactory. Moreover, the output current and phase voltage are well-balanced. Subsequently, the unbalanced load condition is investigated with the load resistors of 2 Ω , 1 Ω and 0.5 Ω , respectively. As shown in Figure 8a, the output currents stay balanced regardless of the unbalanced loads. In the meantime, the line to line voltages in balanced and unbalanced load conditions are shown in Figures 7c and 8c, respectively. It can be observed that under the unbalanced loads, the current THD is slightly increased, from 1.45% to 1.55%. Furthermore, when the inverter is operated as the controlled current

source, the appropriate adjustments of the output voltages are shown in Figure 8b. In this way, the amplitudes of the output currents are kept constant under unbalanced loads.

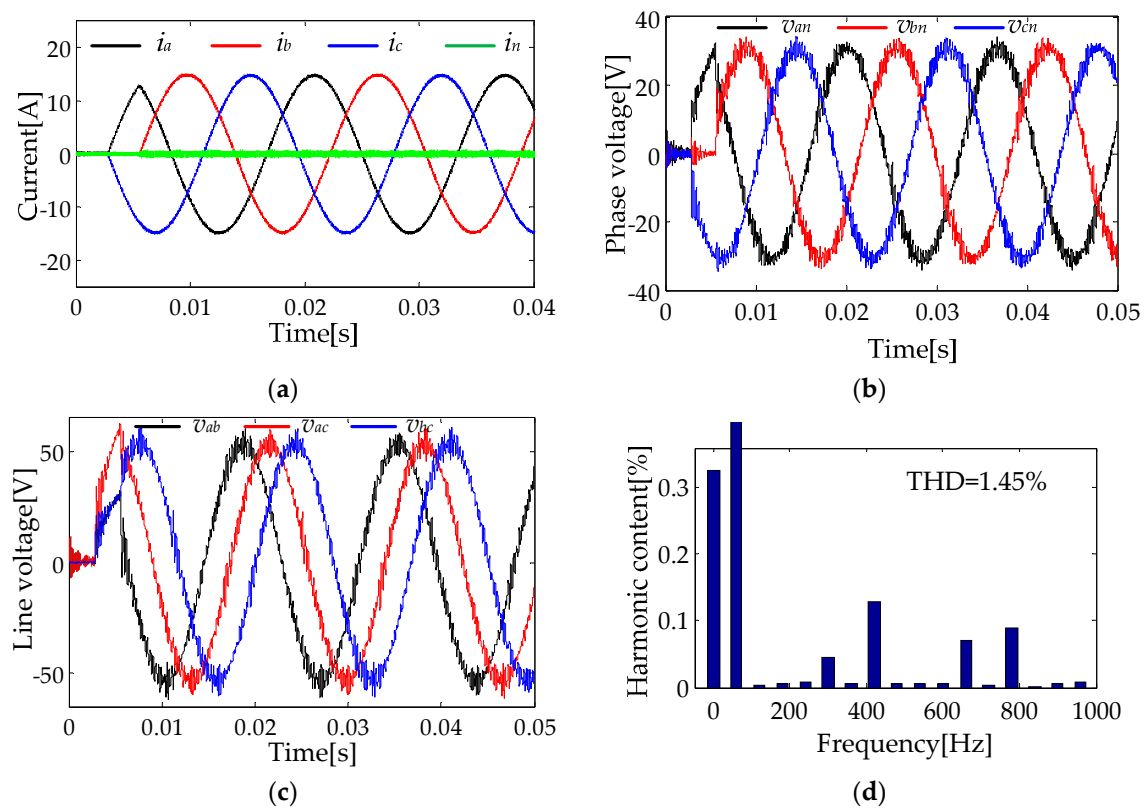


Figure 7. Simulated results of the closed-loop current control scheme in a balanced load condition: (a) Output currents; (b) Output phase voltages; (c) Output line to line voltages; (d) THD of phase a current.

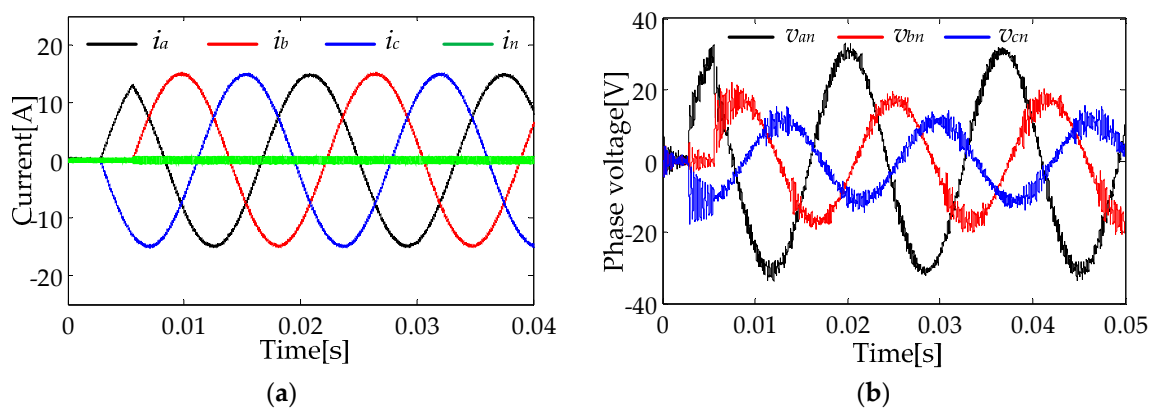


Figure 8. Cont.

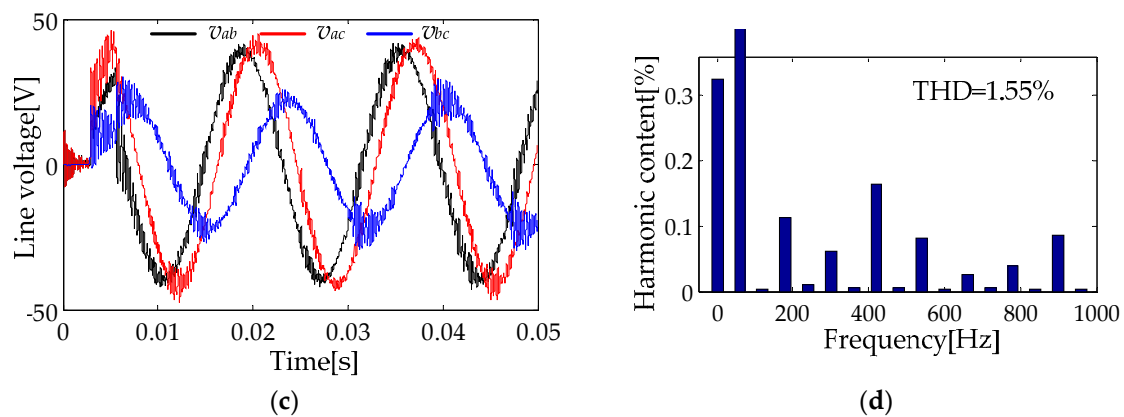


Figure 8. Simulated results of the closed-loop current control scheme in an unbalanced load condition: (a) Output currents; (b) Output phase voltages; (c) Output line to line voltages; (d) THD of phase a current.

5.2. Experimental Results

To further verify the performance of the proposed converter, a prototype of the new converter is built as shown in Figure 9. The experimental setup mainly includes the inverter prototype, drive circuit for IGBTs, drive circuit for thyristors, current sensors, R-L load, DC power supply and a dSPACE 1104 controller. The load parameters are: $R = 5 \, \Omega$, $4 \, \Omega$, $3 \, \Omega$ and $L = 5 \, \text{mH}$.

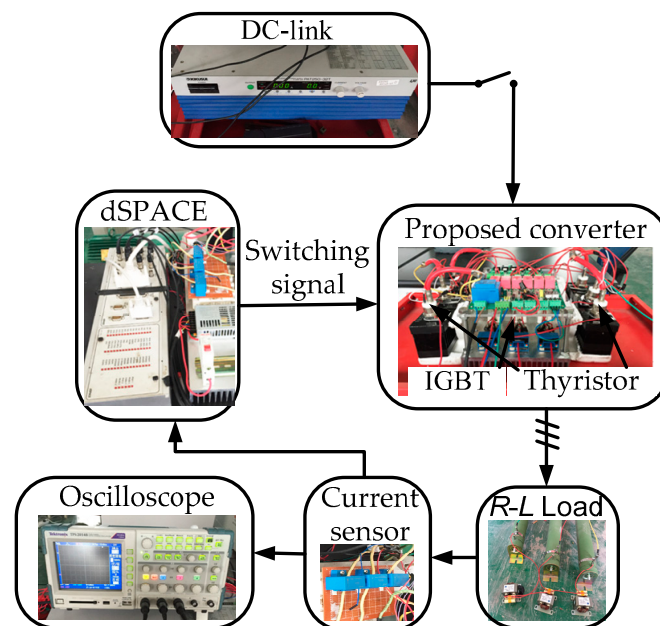


Figure 9. Experimental prototype.

The validity of the improved PWM-PR controller current control algorithm for the proposed three-phase four-leg converter is investigated. It can be observed from Figure 10a that the triggering pulse for the upper thyristor is generated when the current crosses zero from negative to positive, while the triggering pulse for the lower thyristor is generated when the current crosses zero from positive to negative. Figure 10b,c shows the phase current waveforms and THD of the proposed converter at a steady 2 A reference current with an unbalanced load. By importing the data from oscilloscope into Matlab, the THD of phase a current is obtained as 5.42%.

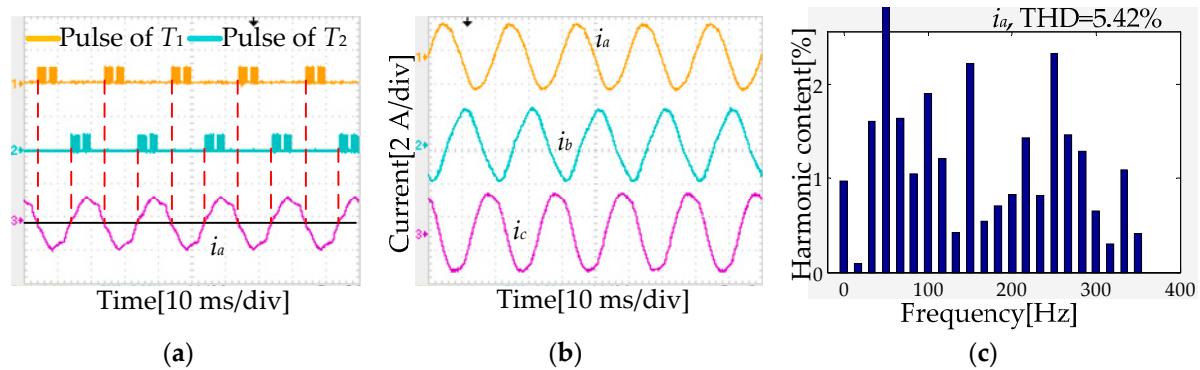


Figure 10. Experiment results of the proposed converter: (a) Triggering pulses for phase *a* thyristors; (b) Output three-phase currents; (c) THD analysis of phase *a* current.

Therefore, the characteristics of the proposed three-phase four-leg converter are verified by simulation and experimentation. It proves that the proposed cost-effective converter possesses a distinct merit for potential implementation in high power applications, such as electric ship propulsion systems, microgrid converters, motor drives, and so on.

6. Comparison

To further demonstrate the merit of the proposed three-phase four-leg inverter, a quantitative comparison with the conventional eight-IGBTs VSI is conducted and discussed. For a fair comparison, the converter ratings are unified as the power level of 2.88 MW, whereas the DC voltage and current are set to 1600 V and 1800 A. The specifications of IGBT, thyristor, and diode can be tabulated in Table 4.

Table 4. Specifications of Switches.

Item	IGBT Module (Single Switch)	IGBT Module (Dual Switch)	Thyristor	Diode
Model	FZ1800R16KF4	FF1800R17IP5	Y60KPE	ZP2000A
Cost (USD)	550	965	50	30
Size (H × W × D, cm)	3.81 × 19.0 × 14.0	3.8 × 23.4 × 8.9	6.0 × 15 × 5.0	3.2 × 9.9 × 9.9
Weight (kg)	2.31	1.4	0.85	0.52
I_r (Amps)	1800	1800	1800	2000
V_r (Volts)	1600	1700	1800	5000

First, the number of switches for the proposed converter and the conventional three-phase four-leg inverter can be determined according to Figure 1. The numbers of single switch IGBT module, dual switch IGBT module, thyristor and diode for the proposed converter and conventional converter are 0, 4, 0, 0 and 1, 1, 6, 12, respectively. Subsequently, size and cost comparison can be calculated. The size and weight are first compared with the specific data. Then, their cost is quantitatively compared and discussed.

The estimated data of the proposed and conventional inverters, namely, the size, weight and cost are summarized in Table 5. It can be observed that the proposed inverter has a definite advantage in terms of lower cost, although it suffers from its relatively complicated structure and larger size. Approximately USD 1094 can be saved by one three-phase four-leg inverter for the power level of a 2.88 MW system, which is appreciated for the demand side. Therefore, the proposed inverter has great potential for mega-watt level cost-sensitive applications.

Table 5. Comparison between Proposed and Conventional Inverter.

Item	Proposed Inverter	Conventional Inverter
Overall size (cm ³)	8268.4	3165.56
Overall weight (kg)	15.05	5.6
Cost (USD)	2766	3860

7. Conclusions

In this paper, a new integrated IGBT-thyristor three-phase four-leg VSI is proposed, analyzed and evaluated, specifically for mega-watt level applications. As compared with traditional four-leg inverters, the proposed inverter achieves a distinct advantage of higher cost-effectiveness. The operation principle of the proposed inverter is investigated and discussed. The inverter output voltage in $\alpha\beta\gamma$ coordinate of each segment is also presented. Moreover, the current control strategy based on carrier-based PWM with PR controllers and the PCM is developed and analyzed. Demonstration results of simulation and experimentation for closed-loop current control are accomplished, which verifies the functionality of the proposed inverter under balanced and unbalanced load conditions.

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