A Digitally Controlled Power Converter for an Electrostatic Precipitator

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Abstract: Electrostatic precipitators (ESPs) are devices used in industry to eliminate polluting particles in gases. In order to supply them, an interface must be included between the three-phase main line and the required high DC voltage of tens of kilovolts. This paper describes an 80-kW power supply for such an application. Its structure is based on the series parallel resonant converter with a capacitor as output filter (PRC-LCC), which can adequately cope with the parasitic elements of the step-up transformer involved. The physical implementation of the prototype includes the use of silicon carbide—SiC—semiconductors, which provide better switching capabilities than their traditional silicon—Si—counterparts. As a result, a new control strategy results as a better alternative in which the resonant current is maintained in phase with the first harmonic of the inverter voltage. Although this operation mode imposes hard switching in one of the inverter legs, it minimizes the reactive energy that circulates through the resonant tank, the resonant current amplitude itself and the switching losses. Overall efficiency of the converter benefits from this. These ideas are supported mathematically using the steady state and dynamic models of the topology. They are confirmed with experimental measurements that include waveforms, Bode plots and thermal behavior. The experimental setup delivers 80 kW with an estimated efficiency of 98%.

Keywords: electrostatic precipitator; silicon carbide; digital control

1. Introduction

ESPs have been industrially used to eliminate polluting particles in gases since the beginning of the 20th century [1–4]. They are durable, relatively simple to maintain, cost-effective and present a high collection efficiency, typically 80% per step. ESPs have found application in power generation plants, steelworks, cement-free building materials, chemical process factories, incinerators, etc. Thus, by using three steps placed in series, it is possible to reach an efficiency in particle elimination above 99%. Its mode of operation is as follows: A very high DC voltage of 45–150 kV negative is applied to a wire located in the center of the precipitator, known as a discharge electrode. The outer walls of the precipitator, called the collector electrode, are grounded to zero potential. The gas to be purified is injected through the precipitator. The electric field around the wire reaches high enough values to cause a discharge crown, ionizing the gas around it and injecting electrons. Negative electrons and ions are accelerated by the electric field to the collector electrode. By collision and ion capture, particles suspended in the gas are charged and also deposited by the electric field in the collector electrode. The gas then exits the precipitator free of impurities. Since particles larger than 10 μm in diameter absorb several times more load than those smaller than 1 μm, the electrical forces are much lower in the latter. As the particles begin to settle into the collector, the thickness of the material layer

in the collector increases. As a consequence, the electric field decreases, so it is necessary to periodically clean the collector surfaces. The material falls and collects at the bottom.

The complete filtrate is divided into several sections that are sequentially crossed by the gas. Each of them is controlled by a different voltage source and can be considered an independent precipitator. Depending on the physical proportions of each section and the power and voltage levels applied, different harvesting efficiencies are achieved in each section. They are generally optimized for dust collection of different sizes. The sum of the individual performances gives the final total performance figure for the system. For it to reach 99% the precipitator must have three or more sections.

They must be supplied by using a DC power source that provides around 100 kV and 100 kW to the ESP electrodes. The design of such power sources commonly relies on low-frequency phase regulators [5]. A typical structure includes thyristors, low frequency transformers working at 50–60 Hz, and a rectifier bridge at the output. A coil in series limits the current peaks in the input when a short circuit occurs at the output. These short circuits are frequent (up to 90 per minute) due to the dielectric rupture of the gas flowing through the ESP electrodes. In this sort of DC power sources, the triggering of the thyristors regulates the average voltage level at the electrodes. One of the problems associated to this technique is the very large low-frequency ripple it gives rise to [6], which makes the change to High Frequency Switched Mode Power Supplies (HF-SMPS) become a very attractive solution for ESPs. Some of the advantages are:

- Reduction of weight and volume due to the use of high frequency in the step-up transformer.
- Decrease of the volume of oil in the tank containing the high-voltage equipment, i.e., the transformer and the rectifier output.
- Better performance from the point of view of the input network because of its three-phase connection and its higher power factor (above 0.9).
- Operation independent of the input frequency.
- Lower ripple at the output voltage for a given specification of the precipitator. This is so because the output capacitance between the electrodes remains the same, whereas the output rectifier frequency experiments a great increment. Additionally, this ripple reduction means an increment in the average output voltage for the same peak (breakdown) in the operating voltage.
- Possibility to supply the ESP with pure DC voltage, or to include different pulses or degrees of intermittency due to the source faster dynamic response.

Despite all these advantages, the construction of high-frequency power sources was not addressed until the last decade, due to problems related to the design of equipment involving high current levels [7,8]. Nowadays, its use is still incipient [5] with limitations in voltage (less than 80 kV) and current (less than 1 A). With the advantages provided by HF-SMPS, the ESP itself may evolve to operate with new voltage waveforms that are more convenient from the process point of view. New operating capabilities can provide greater purification efficiency. The effect of these new sources is even more evident in cases where the phenomenon of "back corona" appears. This phenomenon, generally linked to high-resistivity impurities [9], takes place when the potential drop across the dust layer is so large that corona discharges begin to appear in the gas trapped within the dust layer.

In [10,11] a series-parallel resonant tank (SPRC) and IGBTs as the switch are used to implement the ESP. In this paper, a series-parallel resonant converter (PRC-LCC) as HF-SMPS is proposed and studied for ESPs. Additionally, a "new" control strategy is also proposed that minimizes reactive energy through the resonant tank and improves the switching losses by using SiC MOSFETs. Two versions of the inverter (Si IGBTs vs. SiC MOSFETS) have been assembled in order to compare their features. Their output voltage and power are regulated by means of only one control variable: the duty cycle, *d*. The design of the closed-loop operation is based on the topology small signal model developed.

2. The Model for the Series-Parallel Topology

2.1. Power Stage

There are several resonant topologies described in the literature [12–15] that use LCC resonant tanks, i.e., LLC resonant converter [16], soft switching technology [17] and a secondary-side resonant converter [18]. But the series-parallel resonant converter (PRC-LCC) with an inductive output filter is especially well suited for the type of application considered in this paper [19]. This topology has, however, one drawback in our case: it is not easy to design the inductor in the output filter when the output voltage is very high. Thus, for the sake of simplicity, many high-output DC voltage applications use a PRC-LCC resonant topology with only a capacitor as output filter, as shown in Figure 1 [20–23]. The price to pay for this simplification in the assembly is a more complicated performance of the topology, since the use of a purely capacitive filter results in discontinuous-conduction-mode operation. Nevertheless, this is not much of a problem, for the behavior of this topology has already been described and developed by means of different mathematical models for a half-bridge [20,24] where several topologies are compared, for a PRC-LCC topology [21,23,25,26]; for high voltage pulse loads [22] and full bridge Zero Current Switching Pulse Wide Modulation (ZCS PWM) application in [27]. Other models have been developed in [28–31] for LCC-type parallel resonant converter.
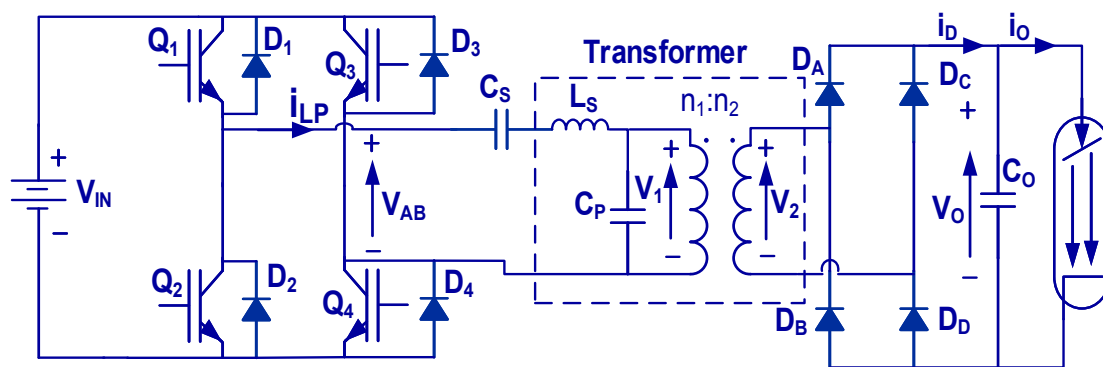

Figure 1. Series–parallel resonant topology, PRC-LCC, with a capacitor as output filter.

In the optimal current control traditionally used (Figure 2a), the current through the resonant tank, i_L, is high because it has a reactive component, due to the fact that it is not in phase with the input voltage to the tank, V_{AB}. On the other hand, the switching current of the switches Q_3–Q_4 is much greater than that in switches Q_1–Q_2, and, therefore, so are the switching losses.

In the centered current control (Figure 2b), the resonant current, i_L, is smaller than the one obtained with the optimal current control, since this current is in phase with the input voltage, V_{AB}. This allows conduction losses to be reduced. On the other hand, for high duty cycles, the switching currents will be similar in both legs of the inverter, and smaller than those produced in the optimal current control (Figure 2a); these results in lower switching losses. In this paper, the control mode used sets a switching frequency that guarantees that the inverter is working in the centered current mode.

(a)

(**b**)
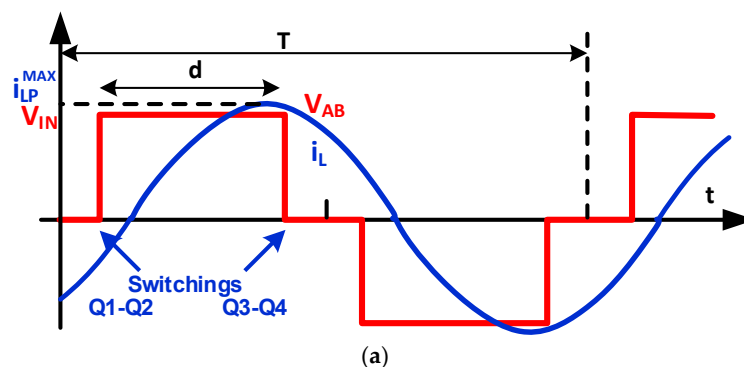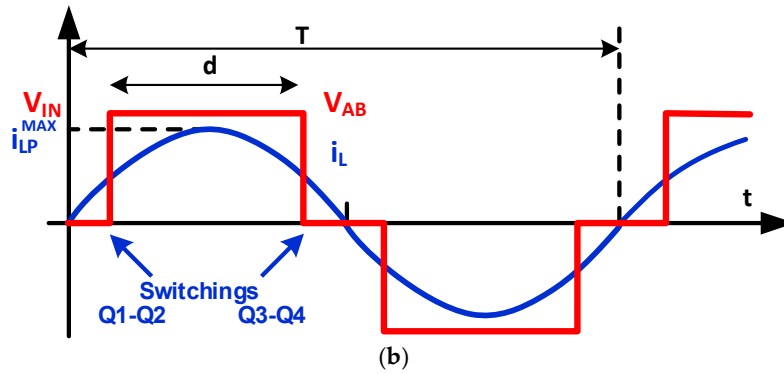
Figure 2. Waveforms for (**a**) Optimum switching control and (**b**) Centered-current control.

2.2. Large-Signal Model and Steady-State Condition

Not all the models describing the performance of a PRC-LCC with capacitive output filter are equally easy to work with [32]. In some cases, different operation regions are identified in the performance of the topology. Each of these regions is adequately modeled, but the only way to identify the operation region the converter that is working is by means of a trial-and-error procedure. This is not practical to carry out a full analysis of the converter, mainly because the adequate set of equations to be used is not known at the beginning of the calculation.

There is one model, however, that succeeds in describing the full performance of the topology throughout its continuous conduction mode using a single set of equations [25,33]. This model can be used for large-signal, small-signal and steady-state analysis. Focusing on the latter, a simple equivalent circuit can be used to represent steady-state performance (Figure 3); reference [32] provides the details on how to obtain such an equivalent circuit. This steady-state model is better suited than those defining different operation regions, for it results in a set of equations that can be used for the whole range of operation (at steady state); these equations can also be adapted to any control mode.

Any practical application provides the specification of the input DC voltage, V_{IN}, the output DC voltage, V_O, and the output power, P_O. On the other side, after assembling the power supply, the values for all the circuit components (r, L_S, C_S, C_P, and R) are known [25,33]. The equivalent load of the converter, R, is derived from the output voltage and output power specifications, and its value is typically considered to be constant.

An impedance analyzer may measure the other parameters of the topology: r is the parasitic resistance of the circuit; C_S is a serial capacitor; L_S and C_P are, respectively, the parasitic inductance and capacitance of the step-up transformer. All those parameters are referred to primary by using the transformer turns ratio. With these data, the mathematical model provides a method to calculate a suitable value for the control parameters.
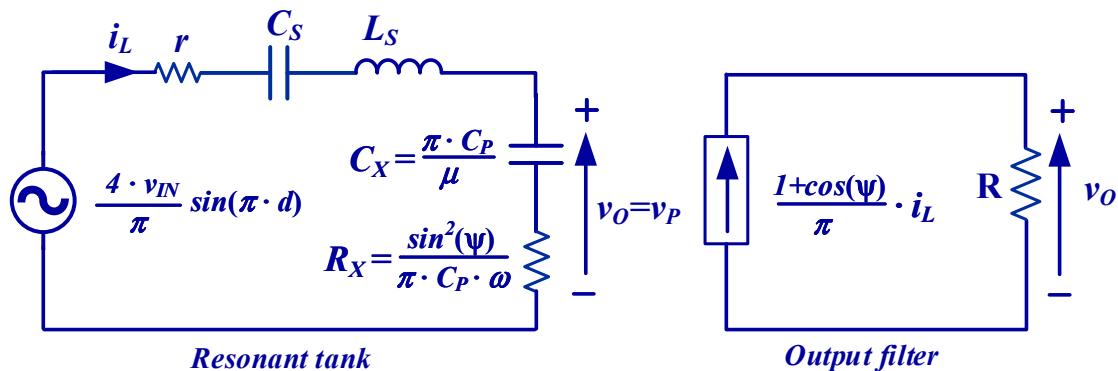
Figure 3. Equivalent circuit of the topology according to [25,33]. Waveforms are expressed as amplitudes.

In Figure 3, C_X and R_X depend on μ, which is simply a function of the clamping angle Ψ (1) used for the sake of compactness. The clamping angle, Ψ, varies between 0 and π radians and has a physical meaning: it represents the part of the period where none of the output rectifying diodes is on (see Figure 4). During this period, C_P provides all of the resonant current, i_L, while experiencing a voltage variation from $-V_O$ to $+V_O$ (or vice versa). These conditions provide the way to calculate Ψ (2) [31]. Since R and C_P are previously known, only ω_S needs to be obtained in order to derive the value of the clamping angle:

$$\mu = \psi - \sin(\psi) \cdot \cos(\psi) \tag{1}$$

$$cos(\psi) = \frac{\pi - 2 \cdot R \cdot C_P \cdot \omega_S}{\pi + 2 \cdot R \cdot C_P \cdot \omega_S} \tag{2}$$

Figure 3 shows two differentiated circuits. The one on the left represents the topology resonant tank, where several components are connected in series whose impedance is:

$$Z_{REAL} = r + R_X \tag{3}$$

$$Z_{IMAG} = \omega L_S - \frac{C_S + C_X}{\omega C_S \cdot C_X} \tag{4}$$

$$Z = \sqrt{Z_{REAL}^2 + Z_{IMAG}^2} \tag{5}$$

The control method must maintain the sinusoidal current centered with respect to the inverter voltage. This means that the first harmonic term of the voltage and the resonant current must be in phase, $\varphi = 0$ (Figure 4). This condition is met if the imaginary part of the resonant network is null ($Z_{IMAG} = 0$) for the switching frequency, f_S. Since Z_{IMAG} is defined in (5), it can be solved for f_S as shown in (6). However, it must be noted that f_S depends on C_X, and, thus, on Ψ:

$$f_S = \frac{\omega_S}{2 \cdot \pi} = \frac{1}{2 \cdot \pi} \cdot \sqrt{\frac{C_S + C_X}{L_S \cdot C_S \cdot C_X}} \tag{6}$$

The procedure described so far has resulted in two equations, (2) and (6), with only two unknown variables, Ψ and ω_S. There are different ways to calculate the value of these unknowns. One possibility is using a look-up table. Other possibility consists in applying recursive methods. When using the latter option, a value for Ψ is inserted in (6) so as to obtain ω_S; then (2) is used to check whether the value thus obtained is correct and, after some iteration, the solution is found.
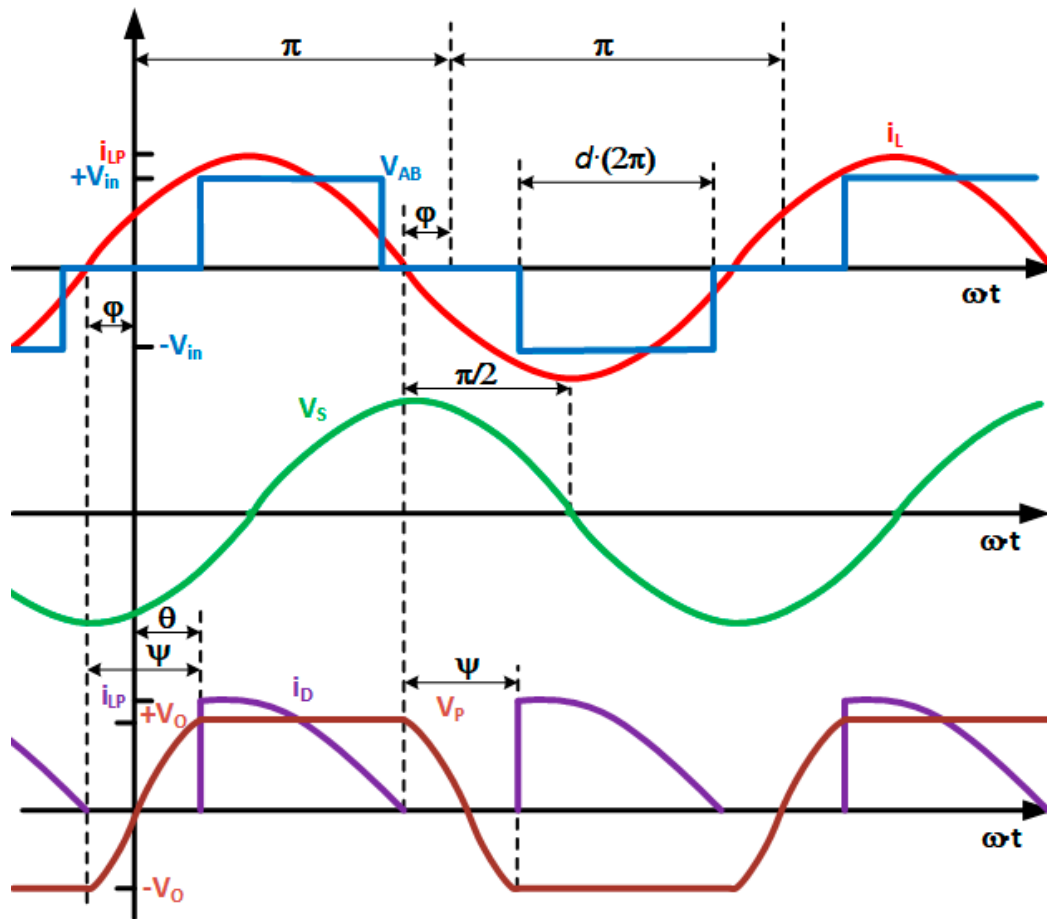
Figure 4. Main waveforms of the topology. V_{AB} is the input voltage of the resonant tank. i_{LP} is the current of the resonant tank. V_S is the voltage of the series inductance. V_P is the voltage of the parallel capacitor C_P. i_D is the current through the output diodes. φ is the delay between input voltage V_{AB} and resonant current i_{LP}.

Now that f_S and Ψ are known, the impedance of the resonant network is obtained through (3), since:

$$\left| Z \right| = Z_{REAL} = r + R_X \tag{7}$$

In the resonant tank of Figure 3, it makes sense to consider the energy balance in the circuit. Most of the power is transferred from the power source to resistor R_X. This power on R_X ideally equals the output power, P_O. Hence, (8) provides an expression for the amplitude of the resonant current, i_L^{Max}.

$$P_O = \frac{v_O^2}{R} = R_X \cdot \left(\frac{i_L^{Max}}{\sqrt{2}} \right)^2 \tag{8}$$

Now, Kirchhoff's law is applied to obtain the required input voltage (9).

$$i_L^{Max} = \frac{v_{AB}^{Max}}{\left| Z \right|} \tag{9}$$

Finally, the duty cycle is calculated from the relationship between the DC input voltage, V_{IN}, defined in Figure 1, and the first harmonic term of the output voltage of the converter, V_{AB}, as in (10):

$$v_{AB}^{Max} = \frac{4 \cdot v_{IN}}{\pi} \cdot \sin(\pi \cdot d) \tag{10}$$

By following this procedure, the control parameters (duty cycle and frequency) can be obtained for any required operation point.

2.3. Centered-Current Operating Point

Overall losses have been estimated on real prototypes considering two different types of switches: IGBT (FF300R12KS4) and SiC MOSFET (CAS300M12BM2).

The working conditions in the prototypes tested were:

- V_{IN} = 800 V, V_O = 80 kV (1000 V in the primary side) and P_O = 80 kW (R = 12.5 Ω in the primary side).
- Transformer parameters: n$_1$/n$_2$ = 1/80, L_S = 62.7 µH, C_P = 219 nF (see Figure 5). A series capacitor C_S = 408 nF completes the topology.

| (a) | (b) |
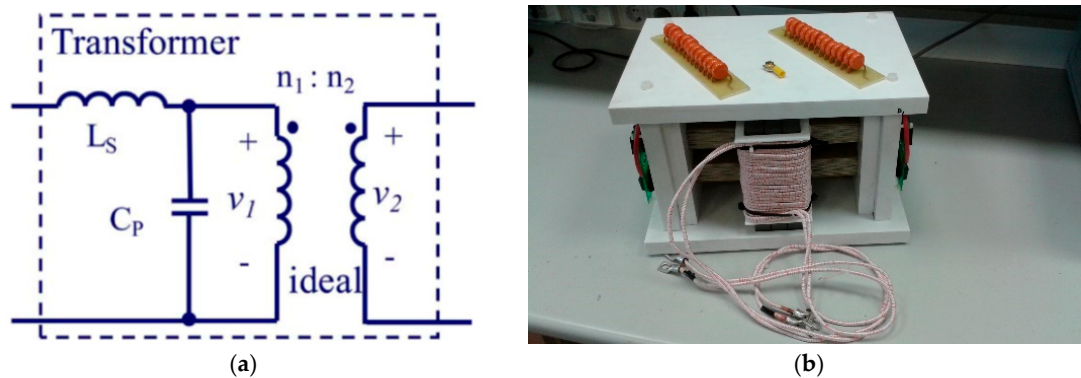
Figure 5. High-voltage transformer (**b**) and simplified equivalent circuit (**a**) of the step-up transformer.

Once the switching frequency has been decided and the converter is working on the centered-current mode, the duty cycle (*d*) is used to regulate the output voltage (V_O). This control scheme is referred to as centered-current control. By using this control mode, each of the legs of the inverter has a different switching pattern. One of them, Q$_1$–Q$_2$, experiences hard-switching (Figure 6), whereas the other one, Q$_3$–Q$_4$, goes through zero voltage switching (ZVS) thanks to the conduction of the diodes in parallel (Figure 7).

In order to calculate switching losses, it is necessary to know the value of the actual switching current through the semiconductors, I_S, the switching frequency, f_S, the input voltage, V_{IN}, and the switching energies in the semiconductors when operating at nominal voltage and current (V_N = 600 V and I_N = 300 A in this case).

Since this paper considers two different types of semiconductors, the energies to use in the calculation of the switching losses are:

- IGBT: $E_{ON(IGBT)}$, $E_{OFF(IGBT)}$
- IGBT diode: $E_{REC(DIGBT)}$
- MOSFET SiC: $E_{ON(MOS)}$, $E_{OFF(MOS)}$
- MOSFET SiC diode: $E_{REC(DMOS)}$

As indicated in Figure 6, switch Q$_4$ turns on with no losses, but there are switching losses in Q$_3$ when it is turned off. Leg Q$_1$–Q$_2$ performs differently (Figure 7): Q$_1$ turns OFF with no losses, because the diode in parallel, D$_1$, is ON; switching losses appear when Q$_2$ turns ON and diode D$_1$ is forced OFF. The formula to estimate these losses is given by (11):

$$P_{SW} = E_{ON,EOFF\ or\ EREC} \cdot \frac{V_{IN}}{V_N} \cdot \frac{I_S}{I_N} \cdot f_S \tag{11}$$

Conduction losses can be calculated by applying Equation (12). The magnitudes included in this expression are:

(1) The average, I_{AVG}, and RMS, I_{RMS}, values of the current circulating through the switches.
(2) The forward voltage drop, V_D, or the ON resistance, R_{CD}, of the semiconductor:

- IGBT: $V_{CESAT(IGBT)}$, $R_{CESAT(IGBT)}$
- IGBT diode: $V_{F(IGBT)}$, $R_{D(IGBT)}$
- SiC MOSFET: $R_{DS(MOS)}$

$$P_C = R_{CD} \cdot I_{RMS}^2 + V_D \cdot I_{AVG} \tag{12}$$

One important matter to consider is the importance of the diodes. When using IGBTs, the diodes in anti-parallel are ON during a sizeable part of the switching period, whereas with SiC MOSFETs they are only ON during the dead times of the legs, when no switch is ON.

In the theoretical analysis, the current and voltage levels in the inverter have been obtained from the topology steady-state model. Later, the theoretical values will be proven to be similar to experimental ones.
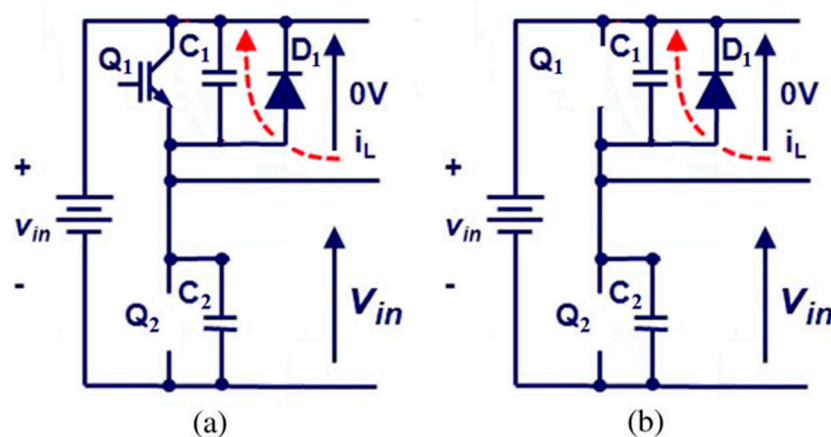
Figure 6. (**a**) Initially Q₁ is ON and Q₂ is OFF. In this case, Q₁ is ON but current flows through D₁; (**b**) during switching, Q₁ switches OFF before Q₂ switches ON. C₁ and C₂ continue to have 0 V and V_{IN} respectively across their terminals. When Q₂ is turned ON, diode D₁ will be forced OFF, C₁ will be charged up to V_{IN} and C₂ will be fully discharged.
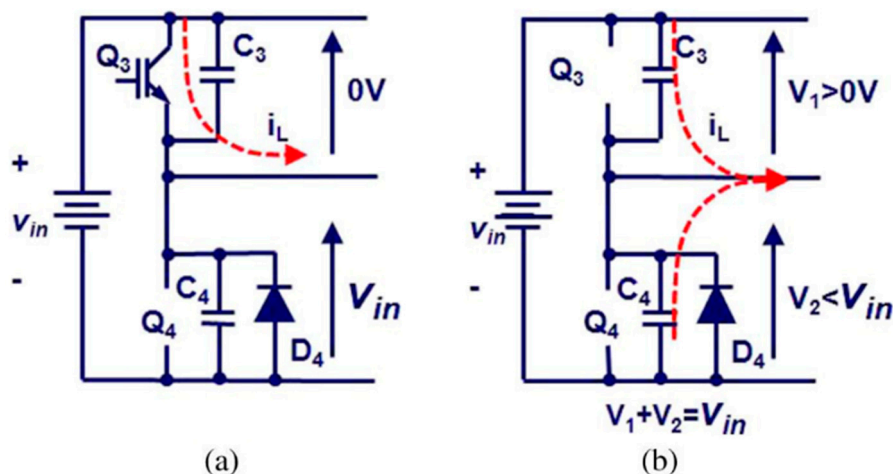
Figure 7. This figure shows the switching process for leg Q₃–Q₄. (**a**) Initially Q₃ is ON and Q₄ is OFF; In this case (**b**), Q₄ switches ON with zero voltage, because the diode in parallel D₄ is conducting. Thus, no turn-on losses are expected in Q₄. However, they appear during the OFF transition of Q₃.

The operating point has been calculated using Equations (1)–(10) at nominal conditions:

- V_{IN} = 800 V, V_O = 80 kV (1000 V in the primary side) and P_O = 80 kW (R = 12.5 Ω in the primary side).

The values obtained for the experimental operating point are as follows:

- Amplitude of the resonant current i_{PL} = 171 A, switching current for leg Q_1–Q_2 I_S = 52.5 A, switching current for leg Q_3–Q_4 I_S = 78.7 A, switching frequency f_S = 37.7 kHz and duty cycle d = 0.388.

The losses in the switches haven been obtained through calculation, using Equations (11) and (12), the values previously obtained for the nominal operating point and the parameters provided by the manufacturers in their datasheets.

- IGBT: $E_{ON(IGBT)}$ = 36 mJ, $E_{OFF(IGBT)}$ = 18 mJ
- IGBT diode: $E_{REC(DIGBT)}$ = 13 mJ
- MOSFET SiC: $E_{ON(MOS)}$ = 8.75 mJ, $E_{OFF(MOS)}$ = 5.95 mJ
- MOSFET SiC diode: $E_{REC(MOS)}$ = 1.92 mJ
- IGBT: $V_{CESAT(IGBT)}$ = 1.2 V, $R_{CESAT(IGBT)}$ = 5.75 mΩ
- IGBT diode: $V_{F(IGBT)}$ = 1.5 V, $R_{D(IGBT)}$ = 1.6 mΩ
- SiC MOSFET: $R_{DS(MOS)}$ = 5 mΩ

The estimated total losses for a full bridge, Table 1, made with IGBTs are 2.54 kW in total: 1.71 kW associated to leg Q_1–Q_2 and 836 W coming from leg Q_3–Q_4. This level of losses requires that two inverters be parallelized in order to share them. If SiC MOSFETs are used instead, losses in the inverter are reduced to 740 W, with P_{Q1-Q2} = 503 W and P_{Q3-Q4} = 237 W, below 1% the total delivered power.

Table 1. Power Dissipation in a Full Bridge at nominal conditions. P_{OUT} = 80 kW, V_{IN} = 800 V, V_O = 1000 V.

|	P_{OUT} = 80 kW	V_{IN} = 800 V	V_O = 1000 V	
Power	**Q₁–Q₂**	**Q₃–Q₄**	**Total**	**η_{FB}**
IGBT	1.71 kW	836 W	2.547 kW	96.9%
MOSFET	503 W	237 W	740 W	99%

2.4. Small Signal Model

The Bode diagram of the inverter expresses the dynamic relationship between the controlled variable, the output voltage, and the control parameter, the duty cycle (13)

$$G(s) = \widetilde{V}_0 / \widetilde{d} \tag{13}$$

Transfer function, $G(s)$, has been obtained by modifying the small-signal model of the topology presented in [25] so as to include the control strategy in the mathematical equations. This strategy sets a constant switching frequency so that the resonant current is centered with respect to the inverter voltage, Figure 8. The duty cycle, d, controls the output voltage V_O.

The mathematical model was implemented using MATLAB (R2015b, MathWorks, Boston, MA, USA) Equation (14), which allowed the theoretical Bode diagram of the converter to be plotted (blue line in Figure 9).

$$G(s) = 201.2 \cdot 10^9 \cdot \frac{(s + 137 \cdot 10^3) \cdot}{(s + 1.3 \cdot 10^3) \cdot (s + 44.8 \cdot 10^3) \cdot (s + 118.8 \cdot 10^3)} \cdot \frac{(s^2 - s \cdot 58.7 \cdot 10^3 + 61.8 \cdot 10^9)}{(s^2 + s \cdot 46 \cdot 10^3 + 209.4 \cdot 10^9)} \tag{14}$$
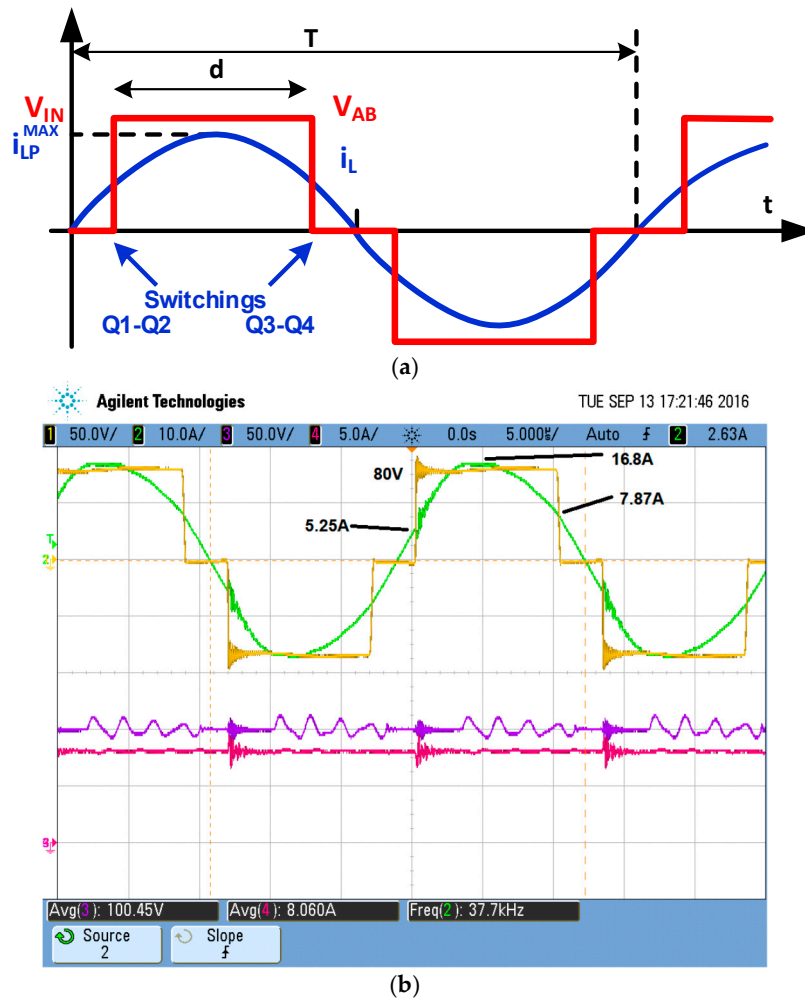
Figure 8. (**a**) Theoretical waveforms of V_{AB} (red) and i_{PL} (blue); (**b**) Experimental waveforms of V_{AB} (yellow) and i_{PL} (green) scaled to V_{IN} = 80 V, V_O = 100 V and P_O = 800 W.

A scaled prototype, Figure 10, was assembled to validate the theoretical Bode plot. It is a 10:1 version, in voltage and current, of the final power supply: V_{IN} = 80 V, V_O = 100 V, f_S = 38 kHz, R = 12.5 Ω, C_O = 96 μF and P_O = 800 W. All the variables have been transferred to the primary of the transformer. Transformer parasitics, L_S and C_P, have been implemented using discrete components. In this case, an analogue circuit implements the phase-shifted control. This gain must be considered when comparing experimental measurement and theoretical prediction.

Figure 9 also shows the experimental small signal behavior of the prototype (in orange). Data are captured by means of a differential probe and a data acquisition card as explained in [34]. The difference between the mathematical calculation and the experimental measurement is not significant. It is important to remember that any theoretical small signal model should be valid up to one tenth of the switching frequency, i.e., up to 4 kHz in this case.

(**a**)

(b)
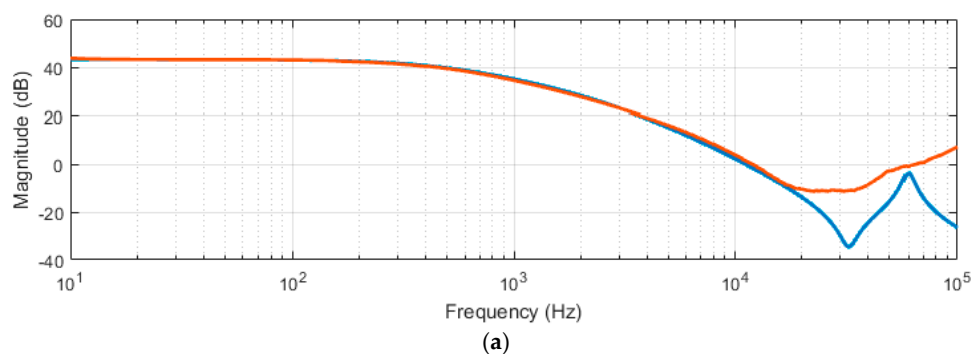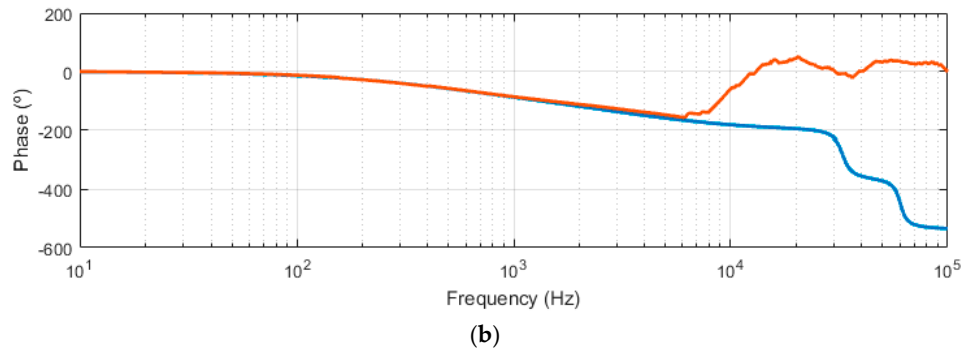
Figure 9. Experimental (orange) and theoretical (blue) Bode plots for the power source operating on scaled output voltage and power using centered-current control. (**a**) Magnitude in (dB) and (**b**) phase in degrees.
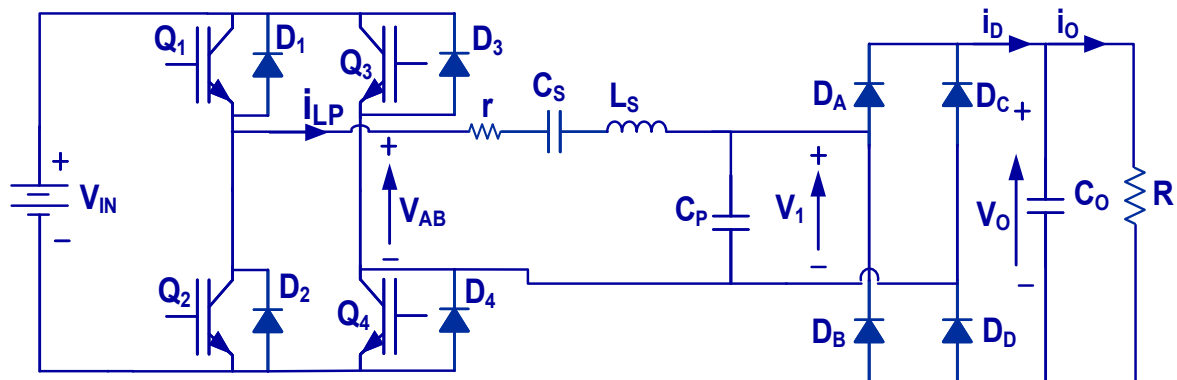
Figure 10. Experimental converter used to obtain the Bode diagram and the corresponding waveforms. The transformer has been replaced by discrete L_S and C_P parts.

The authors in a previous work [33] performed the control of the converter with an analog control, $C(j\omega)$. In this work, the design of the digital feedback loop [35,36] is based on classical control theory and small signal analysis (Figure 11). Other techniques based in digitally controlled power converter based on DSP [10] could be used always. All the transfer functions used have been discretized using the ZOH approximation with $T_S = 1/f_S$. Since the output voltage, V_O in Figure 10, is floating, a differential amplifier is used to feedback the output voltage, $H(z)$. The Bode diagram of the inverter is $G(z)$. Its differential gain is $31.25 \cdot 10^{-6}$ and it presents a high-frequency pole at 4 kHz to eliminate noise. The regulator, $C(z)$, introduces a proportional integral action, PI, (15). The pole at the origin guarantees the absence of a position error. The regulator's gain is set to provide enough phase margin, 64.5 degrees, and a bandwidth of 502 Hz. Altogether, this decision avoids dangerous oscillations in the output voltage (Figure 12):
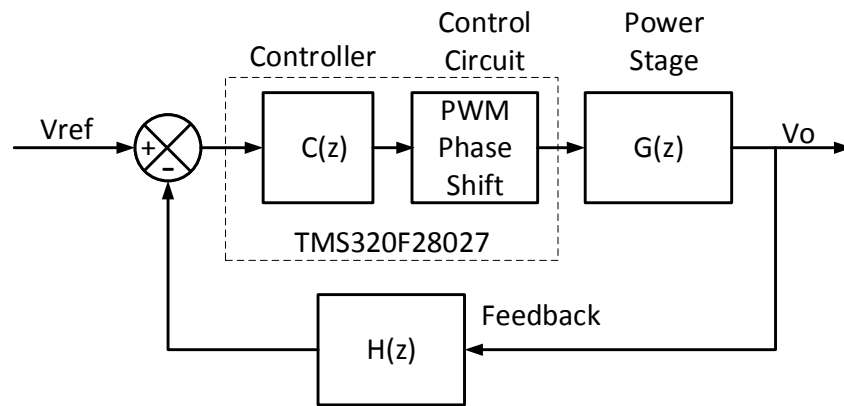
$$C(z) = 0.8873 \cdot \frac{(z - 0.926)}{z - 1} \tag{15}$$

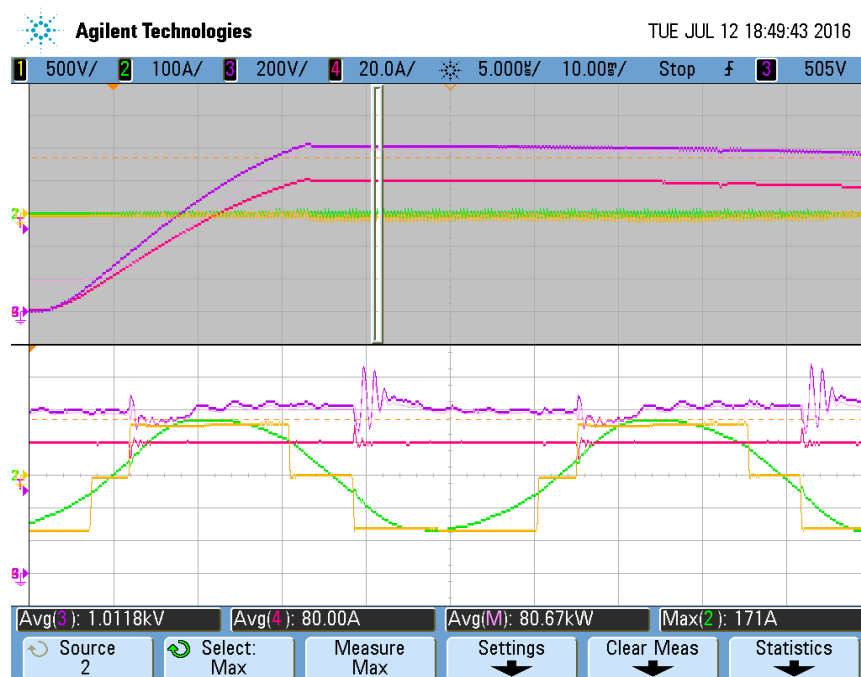**Figure 11.** Digital Feedback system block diagram.

Figure 12. Experimental waveforms. V_{AB} (yellow), i_{PL} (green), V_O (magenta). Bottom: Zoom of the top waveform.

3. Experimental Results

The converter has been tested experimentally as shown in Figure 12. Actual waveforms and their values match theoretical ones. Figure 13 shows a picture of the test bench. A TMS320F28027 digital microcontroller (Copyright © 2010, Texas Instruments Incorporated, Dallas, TX, USA) is used to implement the phase-shift control and the digital regulator $C(z)$.

It must be noted that the power switches, the output rectifier, D_A–D_D, and a three-phase input rectifier have been installed on the heatsink shown in the figure (the three-phase rectifier together with a filter capacitor allows voltage V_{IN} to be obtained from the three-phase mains). The temperature of the heatsink will increase due to the losses in the switches and in both rectifiers. The nominal conditions are:

- V_{IN} = 800 V, V_O = 1000 V and P_O = 80 kW (R = 12.5 Ω on the primary side and C_O = 96 μF). Resonant current amplitude i_{PL} = 171 A, duty cycle d = 0.358, switching frequency f_S = 37.8 kHz.
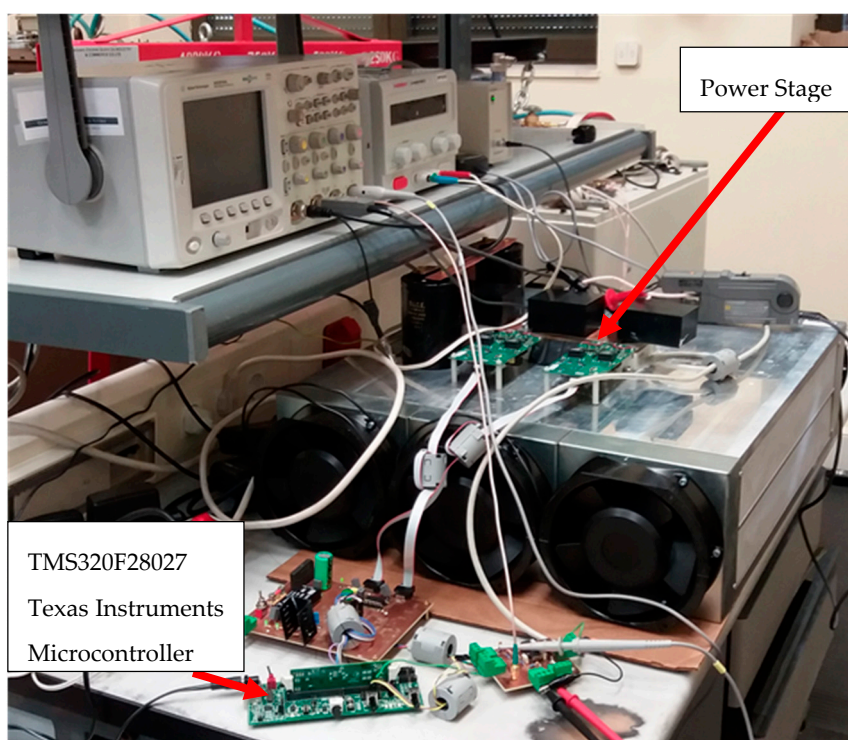
Figure 13. Converter Test Bench with digital control.

In a first batch of tests, the 800 V–80 kW V_{IN} input source was implemented by means of an electrolytic capacitor bank of 84 mF. The capacitor discharges from a maximum value (V_{IN} = 825 V) to a minimum value (V_{IN} = 720 V) as seen in Figure 12. The regulation works perfectly without appreciable overvoltage at the start-up.

3.1. Thermal Analisys

The losses in the experimental prototype are evaluated and compared with theoretical values. Measurements are taken on the case of the switches and on the heatsink near them. Additionally, the temperature profile, using both types of semiconductors, is analyzed with a thermal camera [37,38]. In this case, the mains are used as input voltage.

3.1.1. Thermal Analysis for P_O = 5 kW

Thermal measurements of the converter for P_O = 5 kW have been made under the following conditions:

- V_{IN} = 300 V, V_O = 255 V, P_O = 5 kW.
- Si-IGBTs and SiC-MOSFETs as switches. Non-forced ventilation. Reference of the heatsink (R_{thha} = 0.063 °K/W) RG40160N87/500AFR.

The operating point of the converter, Figure 14, is in this case:

- Amplitude of the resonant current i_{PL} = 43.8 A, switching current for leg (Q_1–Q_2) I_S = 28.7 A, switching current for leg (Q_3–Q_4) I_S = 38.7 A, switching frequency f_S = 37.7 kHz and duty cycle d = 0.22.
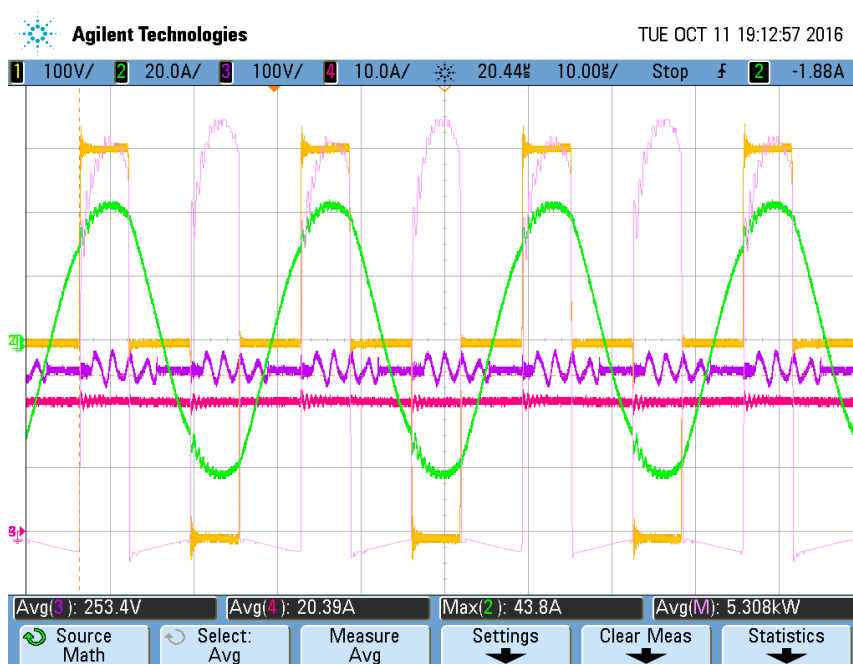
Figure 14. Experimental waveforms for V_{AB} (yellow) and i_{PL} (green), with V_{in} = 300 V, V_O = 250 V and P_O = 5 kW.

Figures 15 and 16 show the temperature increment vs. time. In these figures, AR01 represents the measurement area considered for leg Q_3–Q_4, AR02 is that associated to leg Q_1–Q_2, and AR03 is the heatsink. The temperatures measured after 15 min are shown in Table 2. It can be clearly observed how the temperature in the SiC MOSFETs is lower than that in the Si IGBTs.
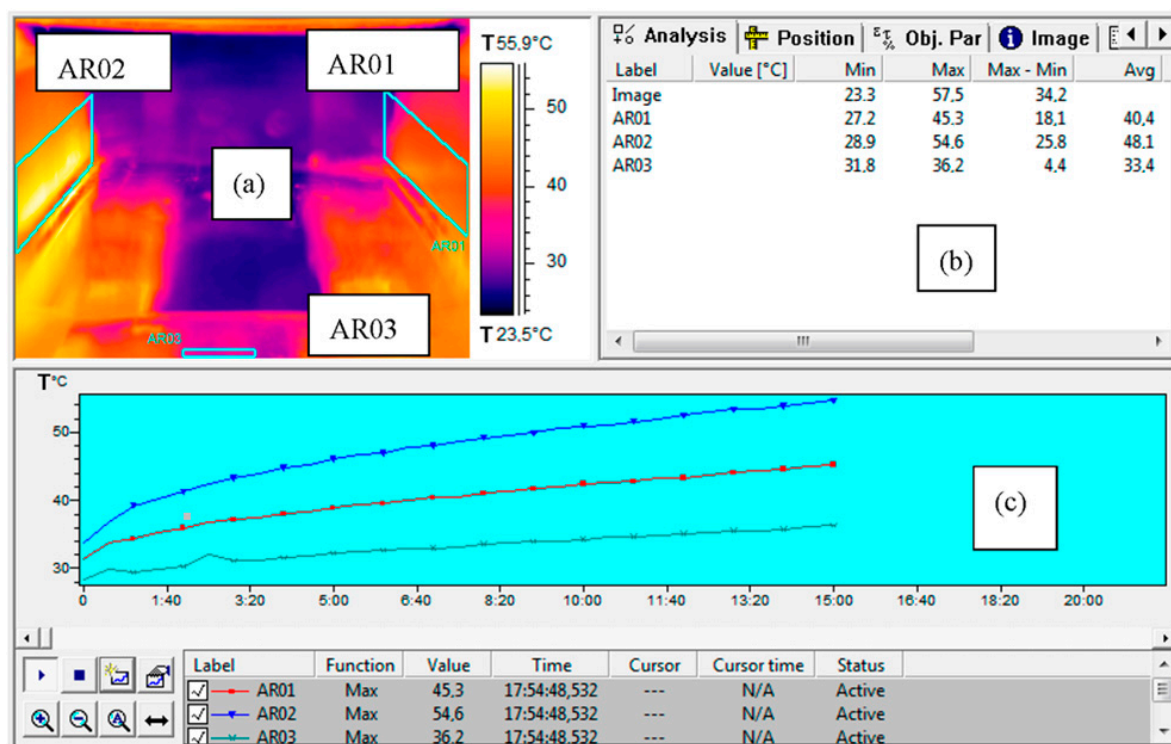
Figure 15. Temperature Measurement (5 kW) of each leg using IGBTs FF300R12KS4. (**a**) Infrared image of power stage; (**b**) Maximum, minimum and difference values measured in each AR0x zone; (**c**) Temperature evolution in each leg and heatsink; blue: AR02 (Q_1–Q_2); red: AR01 (Q_3–Q_4); green: AR03 (heatsink).
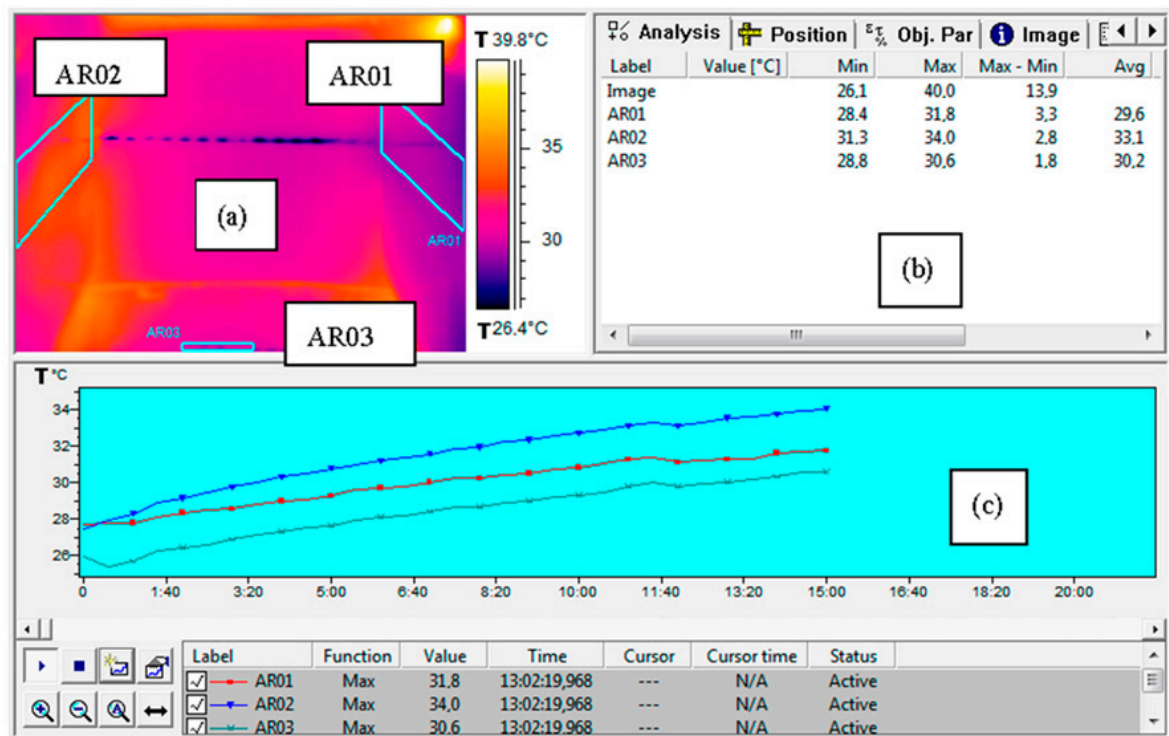
Figure 16. Temperature Measurement (5 kW) of each leg using MOSFETs CAS300M12BM2. (**a**) Infrared image of power stage; (**b**) Maximum, minimum and difference values measured in each AR0x zone; (**c**) Temperature evolution in each leg and heatsink; blue: AR02 (Q_1–Q_2); red: AR01 (Q_3–Q_4); green: AR03 (heatsink).

It can also be observed that leg Q_1–Q_2, which experiences hard switching, is hotter than leg Q_3–Q_4, where ZVS takes place. As expected, it was not possible to complete the full power test with IGBTs: thermal problems made advisable not to go beyond 5 kW.

Table 2. Temperature Measurements for P_O = 5 kW in SiC MOSFET and Si IGBT after 15 min.

P_O = 5 kW V_{IN} = 300 V		V_O = 250 V	
Temperature	$T_{Q1–Q2}$	$T_{Q3–Q4}$	T_{Heatsink}
IGBT	54.6 °C	45.3 °C	36.2 °C
MOSFET	34 °C	31.8 °C	30.6 °C

3.1.2. Thermal Analysis for P_O = 20 kW

The thermal measurement of the converter for P_O = 20 kW has been made under the following conditions:

- V_{IN} = 400 V, V_O = 500 V, P_O = 20 kW
- SiC-MOSFETs. Non-forced ventilation. Reference of the heatsink (R_{thha} = 0.063 °K/W) RG40160N87/500AFR.

The operating point of the converter, Figure 17, in this case is:

- Amplitude of the resonant current i_{PL} = 84 A, switching current for leg Q_1–Q_2 I_S = 23 A, switching current for leg Q_3–Q_4 I_S = 34 A, switching frequency f_S = 37.7 kHz and duty cycle d = 0.385.
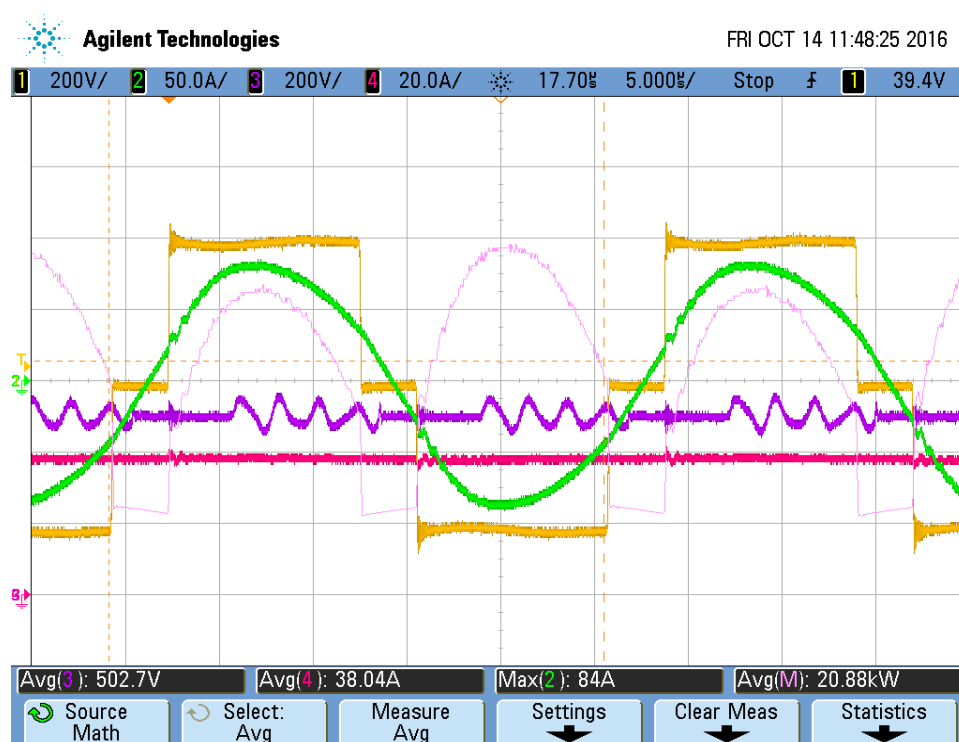
Figure 17. Experimental waveforms for V_{AB} (yellow) and i_{PL} (green), with V_{in} = 400 V, V_O = 500 V and P_O = 20 kW.

Figure 18 shows the temperature increment vs. time when the converter is assembled with SiC MOSFETs. AR01 represents the measurement area considered for leg Q_3–Q_4, AR02 is that associated to leg Q_1–Q_2, and AR03 is the heatsink. The temperatures measured after 15 min are shown in Table 3.
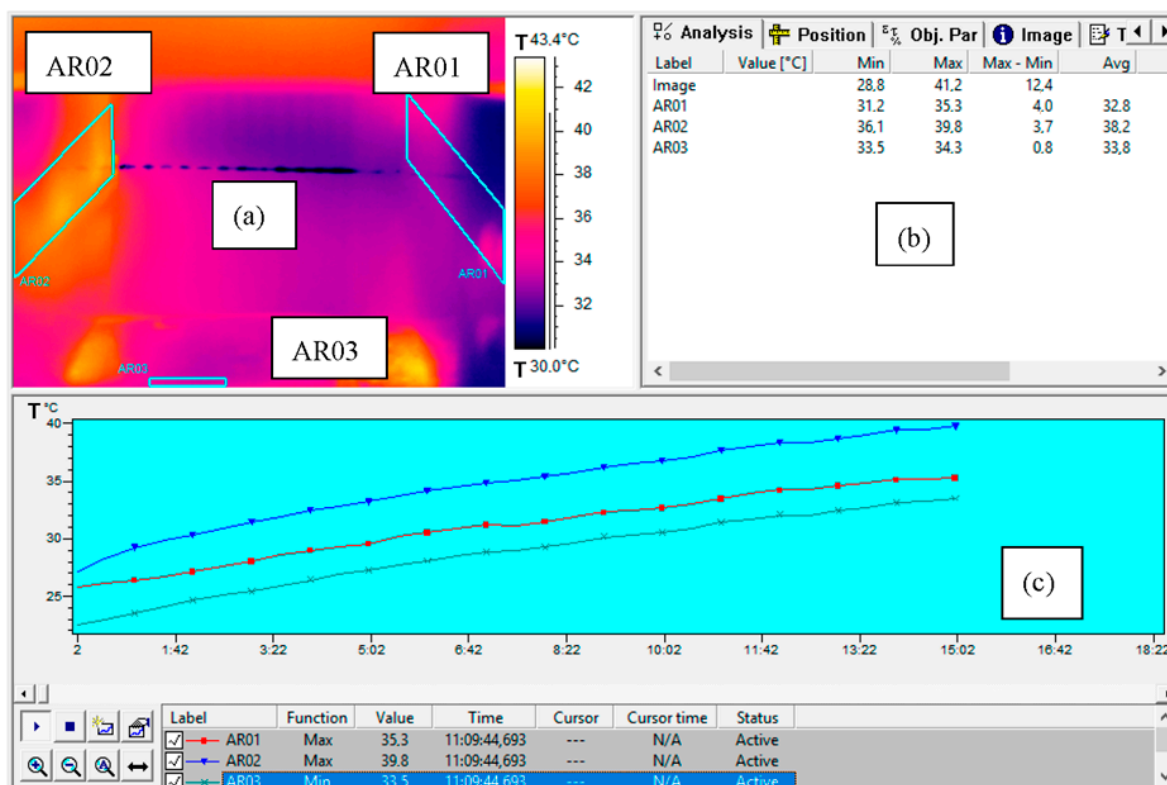
Figure 18. Temperature Measurement (20 kW) of each leg using MOSFETs CAS300M12BM2. (**a**) Infrared image of power stage; (**b**) Maximum, minimum and difference values measured in each

AR0x zone; (**c**) Temperature evolution in each leg and heatsink; blue: AR02 (Q_1–Q_2); red: AR01 (Q_3–Q_4); green: AR03 (heatsink).

Table 3. Temperature Measurements for P_O = 20 kW in SiC MOSFET after 15 min.

P_O = 20 kW	V_{IN} = 400 V	V_O = 500 V	
Temperature	T_{Q1-Q2}	T_{Q3-Q4}	$T_{Heatsink}$
MOSFET	39.9 °C	35.3 °C	34.3 °C

Table 4 shows that the temperature increment in the switches has been moderate. In fact, the dissipation in the semiconductors is mostly due to switching losses: they depend on the input voltage and the current value at the time of switching. Notice that, at 20 kW, the supply voltage is higher than the one corresponding to P_O = 5 kW, whereas the switching current is lower; thus, overall increment of losses is far from being proportional to the delivered power.

Table 4. Temperature Measurements for SiC MOSFET and Si IGBT after 15 min for 5 kW and 20 kW.

P_{OUT} = 20 kW	V_{IN} = 400 V	V_O = 500 V	
Temperature	T_{Q1-Q2}	T_{Q3-Q4}	$T_{Heatsink}$
MOSFET	39.9 °C	35.3 °C	34.3 °C
P_{OUT} = 5 kW	V_{IN} = 300 V	V_O = 250 V	
IGBT	54.6 °C	45.3 °C	36.2 °C
MOSFET	34 °C	31.8 °C	30.6 °C

Summary of the temperatures reached by the switches and heatsinks for the indicated operating points after 15 min and for the switches used.

3.1.3. Thermal Analysis to Estimate the Steady-State Temperature

Temperature variation in the converter has been measured using SiC MOSFET switches for a time interval of 3 h, so that it is possible to estimate the steady-state temperature value.

Thermal measurements of the converter for P_O = 20 kW have been made under the following conditions:

- V_{IN} = 400 V, V_O = 500 V, P_O = 20 kW
- SiC-MOSFETs. Non-forced ventilation. Reference of the heatsink (R_{thha} = 0.063 °K/W) RG40160N87/500AFR.

The operating point of the converter, Figure 17, in this case is:

- Amplitude of the resonant current i_{PL} = 84 A, switching current for leg Q_1–Q_2 I_S = 23 A, switching current for leg Q_3–Q_4 I_S = 34 A, switching frequency f_S = 37.7 kHz and duty cycle d = 0.385.

An exponential approximation has been used in order to estimate the temperature in the inverter's steady state, since this state has not been reached during the measurement process (Figure 19). The maximum temperature for the semiconductors and the heatsink in steady state are: T_{Q1-Q2} = 65 °C, T_{Q3-Q4} = 60 °C and T_h = 56 °C. In the case of the heatsink, the temperature rise is the result of the losses of the three-phase rectifier, the output rectifier and the inverter switches.

The temperature that would have reached the hottest element within each leg, T_j, has been calculated using Equations (16)–(18) and compared to that measured in the experimental results. The following values have been obtained: $T_{j(Q1,Q2)}$ = 61.7 °C, $T_{j(Q3,Q4)}$ = 58.9 °C and T_h = 56.8 °C. These calculations are consistent with the experiments.
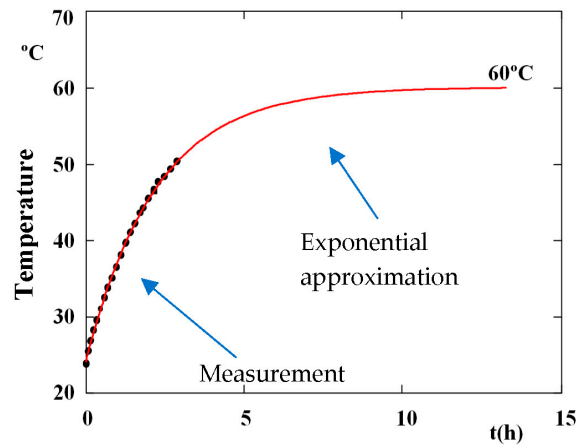
(**a**) Q_3–Q_4 temperature in °C. Time in hours.
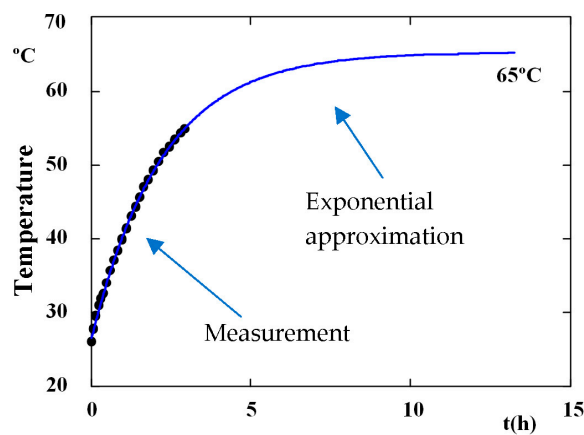
(**b**) Q_1–Q_2 temperature in °C. Time in hours.
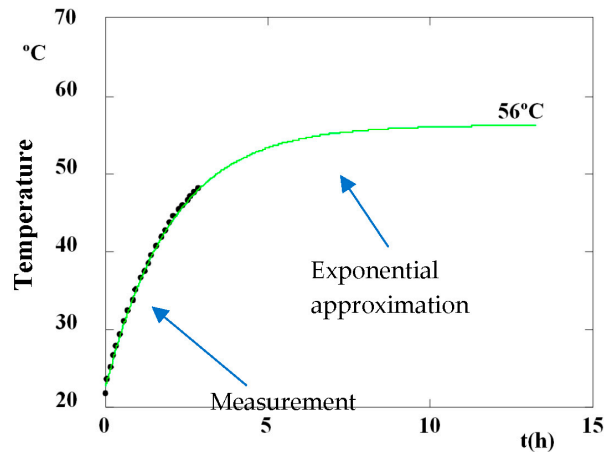
(**c**) Heatsink temperature in °C. Time in hours.

Figure 19. Measurement of temperature in °C (20 kW) for each leg and for the heatsink using MOSFET CAS300M12BM2 for a time interval of 3 h (dots). Exponential approximations are also included for the temperature (**a**) in Q_3–Q_4 (blue), (**b**) Q_1–Q_2 (red) and (**c**) heatsink (green).

$T_{j(Q1,Q2)}$ or $T_{j(Q3,Q4)}$ are the temperatures at the junction of the switch, T_H is the heatsink temperature and T_A is the ambient temperature (all of them expressed in degrees Celsius). R_{th} values have been obtained from the datasheets, the power dissipated in one leg is P_{Q1-Q2}; the one dissipated in one switch is $P_{(Q1,Q2)}$ that dissipated in the three-phase rectifier, P_{RecT}; and the power loss in the output rectifier, P_{RecO}. The expressions used for the calculations are (16)–(18):

$$T_{j(Q1,Q2)} = T_h + R_{thch} \cdot P_{Q1-Q2} + R_{thjc(Q1,Q2)} \cdot P_{(Q1,Q2)} \tag{16}$$

$$T_{j(Q3,Q4)} = T_h + R_{thch} \cdot P_{Q3-Q4} + R_{thjc(Q3,Q4)} \cdot P_{(Q3,Q4)} \tag{17}$$

$$T_h = R_{thha} \cdot (P_{Q1-Q2} + P_{Q3-Q4} + P_{\text{Re}cT} + P_{\text{Re}cO}) + T_A \tag{18}$$

The use of IGBTs is not recommended, since the temperatures reached by leg Q_1–Q_2 exceed 50 °C in only 15 min at 5 kW. On the other hand, temperature reaches only 40 °C at 20 kW with SIC MOSFET.

3.1.4. Power Loss Comparison

Table 5 shows a summary of the estimated power losses in the complete bridge for three different output powers, P_O: 80 kW, 20 kW and 5 kW. In all the cases, efficiency close to 99% is achieved when using SiC MOSFET as switches.

**Table 5.** Theoretical Power Dissipation in Full Bridge topology.

	P_{OUT} = 80 kW	V_{IN} = 800 V	V_O = 1000 V	
Power	**Q₁–Q₂**	**Q₃–Q₄**	**Total**	η_{FB}
IGBT	1.71 kW	836 W	2.547 kW	96.9%
MOSFET	503 W	237 W	740 W	99%
	P_{OUT} = 20 kW	V_{IN} = 400 V	V_O = 500 V	
IGBT	515 W	239 W	755 W	96.3%
MOSFET	107 W	47 W	154 W	99.2%
	P_{OUT} = 5 kW	V_{IN} = 300 V	V_O = 250 V	
IGBT	407 W	166 W	573 W	89.7%
MOSFET	70 W	28 W	98 W	98%

3.2. High-Voltage Test

The authors tested in a previous work the inverter operating at low output voltage, without including the high-voltage transformer, and using analog control circuitry [33]. In the present work, the converter has been experimentally tested including the high-voltage transformer too [39–41], Figure 5. The results obtained allow a good operation of the converter to be verified, as shown in Figure 20. The original analog control circuitry has been replaced by a digital control circuit based on the TMS320F28027 microcontroller.

The operating point of the converter in Figure 20 is:

- V_{IN} = 385 V, V_O = 40.55 kV (1:10,000 ratio) and P_O = 22.11 kW. Resonant current amplitude i_{PL} = 94 A, duty cycle d = 0.43, switching frequency f_S = 37.8 kHz.
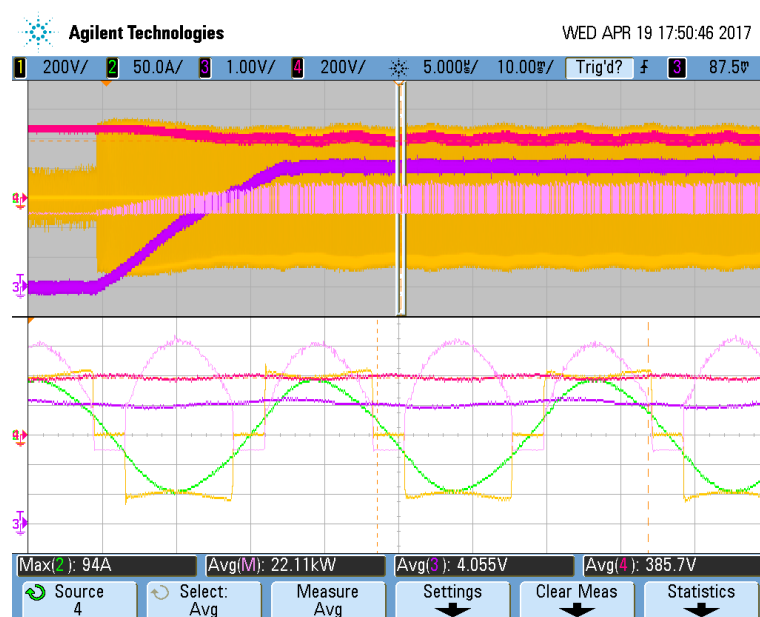
Figure 20. Experimental waveforms for V_{AB} (yellow) and i_{PL} (green), with V_{IN} = 385 V (red), V_O = 40 kV (magenta) and P_O = 22 kW.

4. Discussion

The study demonstrates that the use of SiC MOSFETs is an important improvement in high-power, high-voltage DC/DC converters for electrostatic precipitators. Lower switching losses (as compared to their IGBT-counterpart) lead to an efficiency in the prototype that is several points higher, both at high and low output power levels. Moreover, the switching characteristics of the MOSFETs influence the control strategy of the whole converter. With IGBTs, it was very important to ensure that the antiparallel diode was always ON before turning the main switch ON. However, with the new MOSFETs, preserving zero voltage switching is no longer so important. The mathematical models and the experimental measurements demonstrate that hard switching at 40 kHz is a good option. This gives rise to a new concept of "good behavior" in the inverter. The best way to reduce losses and current amplitude is to center the resonant current in the switching period, i.e., to make the phase between the current and the first harmonic of the inverter voltage zero. Instantaneous waveforms, thermal measurement and power balance in a full-scale prototype support the study with experimental evidence.

The control method has some limitations:

The converter is designed to operate at a constant frequency, therefore, it will be necessary to implement a variable frequency control to keep it in phase with the voltage when the load changes, controlling the mode centered in the current. The converter does not should to work with low duty cycles, since both legs would be switching with higher current values and thus will be increased the losses in the switches. This can occur for a constant load with low output voltages. A decrease in the load will produce an increase in the switching frequency to maintain the current in phase and, therefore, an increase in losses.

On the other hand, the architecture of the control has been digitally implemented. The small signal model of the topology is a good basis to support the design. A simple linear structure for the feedback is demonstrated to be valid. The transient response is fast enough, avoiding any overvoltage at the output. This is quite relevant, since, otherwise, the isolation in the step-up transformer could be under risk. Again, the experiments in the prototype verify the theoretical study, supporting the whole control scheme.

5. Conclusions

In this paper, a new centered-current control that allows reactive energy and, therefore, the current in the resonant tank to be minimized, thus reducing conduction losses, is proposed. Likewise, by means of this control mode, it is possible to reduce switching losses, since switching operations take place at low current. To improve the commutations, SiC MOSFETs have been used instead of Si IGBTs, which resulted in an efficiency of 98% in the power stage. A dynamic model has been proposed that allows a digital regulator to be calculated for a bandwidth of 500 Hz, typically enough for this type of application. This converter has been tested experimentally at nominal values and at high output voltage, with no appreciable over voltages having been observed with the selected regulator.

In order to complete the design of this converter it will be necessary to enhance the following goals in the future:

- Allow the digital control of the converter to adjust its frequency taking into account that the load *R* will be modified due to the conditions of the contaminated gases. Up to now, the constant *R* load has been considered.
- Implement a regulator that allows the rapid recovery of the output voltage in case of short-circuits, due to the effect of the back corona.
- Perform tests in the production plant where we have agreements with companies. In our case Arcelor-Mittal, a company dedicated to steel production in Asturias, Spain.

Author Contributions: This paper is part of a research carried out by Pedro J. Villegas, and Juan A. Martín-Ramos, Juan Díaz and Juan Á. Martínez, whereas Miguel J. Prieto and Alberto M. Pernía assisted with thermal measurements and prototype development.

Conflicts of Interest: The authors declare no conflict of interest.

Abbreviations

AR01	Thermal measurement surface for Q_3, Q_3 leg
AR02	Thermal measurement surface for Q_1, Q_2 leg
AR03	Thermal measurement surface for heatsink
C_P	Parasitic capacitance of the transformer
C_S	Serial Capacitance of the topology
C_X	Equivalent capacitor in large signal model
$C(z)$	Control (z) transference function
d	duty cycle
D_A–D_D	Output diodes
D_1–D_4	Diodes in anti-parallel of switches
E_{OFF}	Turn OFF Energy
E_{ON}	Turn ON energy
E_{REC}	Diode Recovery Energy
ESP	Electrostatic Precipitators
$G(s)$	Power stage (s) transference function
$G(z)$	Power stage (z) transference function
f_S	Switching frequency
$H(z)$	Feedback (z) transference function
HF-SMPS	High Frequency Switching Mode Power Supply
i_D	Current through the output diodes
IGBT	Insulated Gate Bipolar Transistor
i_{PL}	Current of the resonant tank
I_{AVG}	Average current of the semiconductors
I_N	Nominal Current of the switches (300 A on the datasheets)
I_{RMS}	RMS current of the semiconductors

I_S	Switching current
L_S	Parasitic Inductance of the transformer
MOSFETs	Metal Oxide Semiconductor Field Effect Transistors
n_1 and n_2	Numbers of turns in the primary, n_1, and secondary, n_2, of transformer
P_O	Output power of the converter
$P_{(Qx,Qy)}$	Power dissipated in each semiconductor
P_{Qx-Qy}	Power dissipated in one leg
P_{RecT}	Power dissipated in tri-phase main power supply rectifier
P_{RecO}	Power dissipated in output rectifier
PRC-LCC	Series-Parallel Resonant Converter with an inductive output filter
Q_1–Q_4	Switches in the converter
R	Equivalent load of the converter
R_{CD}	Conduction resistance of IGBT
R_{CESAT}	Collector-Emitter saturation resistor
R_D	Diode resistance
R_{DS}	Drain-Source resistance
R_{thch}	Thermal resistance between case and heatsink
R_{thha}	Thermal resistance between heatsink and ambient
R_{thjc}	Thermal resistance between junction and case
R_X	Equivalent resistor in large-signal model
r	Equivalent resistance of the circuit
t	Time
Si	Silicon
SiC	Silicon Carbide
T	Period
T_j	Junction Temperature
T_h	Heatsink Temperature
T_A	Ambient Temperature
V_{CESAT}	Collector-Emitter saturation voltage
V_D	Voltage drop in the semiconductors
V_{IN}	Input DC voltage of the converter
V_N	Nominal voltage of the switches (600 V on the datasheets)
V_O	Output DC voltage of the converter
V_{AB}	Input voltage of the resonant tank
V_S	Voltage across the series inductance
V_P	Voltage across the parallel capacitor, C_P
ZCS	Zero-current switching
ZVS	Zero-voltage switching
ZOH	First order z conversion
φ	Delay between input voltage, V_{AB}, and resonant current, i_{LP}
Ψ	Output diodes clamping angle
ω_s	Pulsating frequency

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