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A Digital Hysteresis Current Control for Half-Bridge Inverters with Constrained Switching Frequency

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Received: 7 September 2017; Accepted: 12 October 2017; Published: 14 October 2017

Abstract: This paper proposes a new robustly adaptive hysteresis current digital control algorithm for half-bridge inverters, which plays an important role in electric power, and in various applications in electronic systems. The proposed control algorithm is assumed to be implemented on a high-speed Field Programmable Gate Array (FPGA) circuit, using measured data with high sampling frequency. The hysteresis current band is computed in each switching modulation period based on both the current error and the negative half switching period during the previous modulation period, in addition to the conventionally used voltages measured at computation instants. The proposed control algorithm is derived by solving the optimization problem—where the switching frequency is always constrained at below the desired constant frequency—which is not guaranteed by the conventional method. The optimization problem also keeps the output current stable around the reference, and minimizes power loss. Simulation results show good performances of the proposed algorithm compared with the conventional one.

Keywords: half-bridge inverters; digital control; hysteresis current control; switching frequency; optimization

1. Introduction

Nowadays, inverters and their controllers play an important role in the enabling of a wider proliferation of renewable energy generation [1,2], the realization of new grid concepts with high efficiency [3,4], and various applications in electronic systems [5,6]. Among various current control techniques developed over last few decades, there are three major classes of control scheme: sine-triangle Pulse Width Modulation (PWM), predictive dead-beat, and hysteresis current control. While the asynchronous sine-triangle PWM is a popular technique to modulate current error, it requires a PI (Proportional-Integral) regulator and often results in unavoidable delays. The predictive dead-beat control technique tends to give good performance in terms of response and accuracy. However, this technique is highly dependent on the accuracy of the predictive model and is complicated to implement [7]. Hysteresis current control, on the other hand, is simpler to implement and does not have such drawbacks. It has a fast dynamic response, and does not require any information about the system parameters, which enhances its robustness [5,8]. For this reason, it finds applications in a large variety of switching inverters.

The basic implementation of hysteresis current control is based on the switching signal that is derived by comparing the actual current and the reference current so that the current error is kept within the tolerance current band. In classical hysteresis current controllers, the hysteresis current band is normally fixed to a certain value, which makes the switching frequency vary in order to contain the current ripple within the band. This leads to unwanted heavy interference among the phases in the three-phase system [9]. In order to overcome this problem, an adaptive hysteresis

current control technique has been developed and used in many applications [10–12]. In this technique, the hysteresis current band is not fixed, but controlled adaptively in each switching modulation period, and based on the measured output voltage values and the desired constant switching frequency [13].

Digital hysteresis current control usually requires a sufficiently high sampling frequency to control the switch devices with accurate switching time [14,15]. The ripple current varies during each switching modulation at a very fast rate, which is inversely proportional to the output inductance and proportional to the difference between the dc and output voltages. Because, during the sampling interval, the hysteresis current band could not be observed until the arrival of the next data sample, the low sampling frequency may lead to a large ripple current overshoot from the hysteresis current band. A high sampling frequency at the MHz level seems to be quite high for conventional Digital Signal Processors (DSP) and microcontrollers, which are employed in most power electronic applications at present. Additionally, such a high sampling frequency is beyond the scope of the Field Programmable Gate Array (FPGA) circuit, which has a high-speed clock and is becoming more and more popular in inverter control [16–18].

In many applications, the high switching frequency has several advantages including lower current ripple, faster transient response, and effective size reduction for the inverter circuit [19–21]. In some cases, the switching devices are operated near the highest possible switching frequency, for example when the controller is redesigned for an existing device, or in order to reduce the price of the inverters. For instance, when a motor is accelerated from a standstill to rated speed, an inverter is usually designed to operate near its highest possible switching frequency in order to achieve a low current distortion [22]. In these cases, if the switching devices are forced to change their on-off states at a frequency beyond their limit, especially under the influence of noise, short-circuit fault can occur and may lead to breakage of the switching device [23]. Therefore, it is important to properly control the hysteresis current band so that the frequency of the switching device does not exceed its highest possible switching frequency. However, the switching frequency fluctuation controlled by the conventional method is not guaranteed to never exceed this limit, especially with noise. The conventional method of computing a hysteresis current band uses only the measured voltage values at the instant when the switches start a new modulation period [13,24]. The present study proposes a new digital hysteresis current control algorithm that takes the feedback information from the preceding modulation period into account, keeping the switching frequency constant and always below the highest possible switching frequency of the switching device, even when noise is present. The controller is assumed to be using an FPGA while the sampling interval is at the MHz level.

This paper is organized as follows. Section 2 presents a conventional method of using the fixed band hysteresis current. In Section 3, a conventional adaptive hysteresis current control is described and its disadvantages are explained. Then, a new robustly-adaptive hysteresis current control algorithm is proposed in Section 4. In Section 5, the simulation results are shown to demonstrate that the proposed method has better performance than the conventional method. Conclusions are given in Section 6.

2. Classical Fixed Band Hysteresis Current Control

Consider a single-phase half-bridge inverter circuit, where the output is connected to a grid ac voltage v_g as in Figure 1. The dc voltage is supplied by two constant and balanced dc sources, each of which has a value of V_{dc}. Parameters L, C, and R present the output inductance, current ripple filter, and load respectively. The inverter output current i_L is controlled by the switching devices S_1 and S_2 to track a given reference current i_{ref}. The ripple component of the output current i_L is filtered by the current ripple filter, and the grid current i_o is derived without a ripple component.

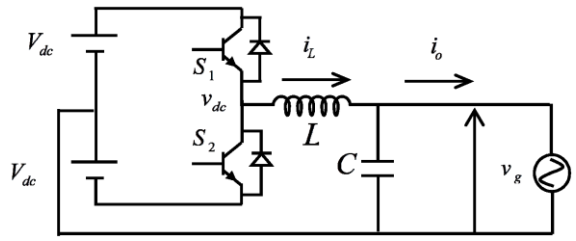

Figure 1. Single-phase half-bridge inverter circuit.

Figure 2 shows the structure of the digital control system. The measured output voltages, and currents are sampled by analog/digital converters, and used for computing on/off pulses of switches S_1 and S_2. The states of the switches and the corresponding inputs and outputs of the inverter are shown in Table 1.

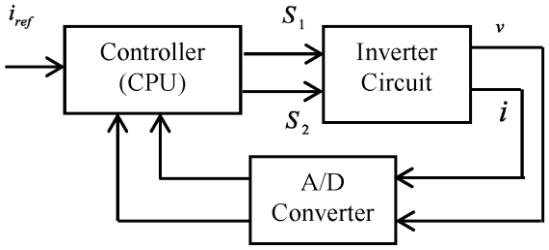

Figure 2. Structure of the digital control system.

Table 1. States of switches and corresponding outputs.

Half Period	S_1	S_2	Input Voltage v_{dc}	Output Current i_L
Positive	On	Off	V_{dc}	Increase
Negative	Off	On	$-V_{dc}$	Decrease

In the classical fixed band hysteresis current control, the tolerance current band is fixed to a certain value Δi_b [25]. While the measured output current i_L is between the upper and lower limits, no switching occurs. When the measured output current crosses above the upper limit of the hysteresis band $\left(i_{ref}+\Delta i_b\right)$, the switch S_1 is turned off, the switch S_2 is turned on and the current starts to decay. In contrast, when the measured current crosses below the lower limit of the hysteresis band $\left(i_{ref}-\Delta i_b\right)$, the switch S_1 is turned on, the switch S_2 is turned off and the current starts to increase (Figure 3).

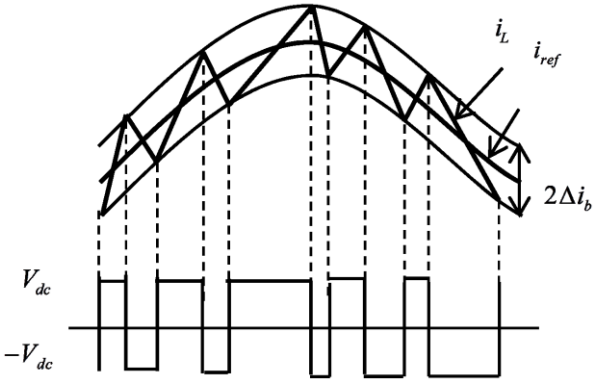

Figure 3. Fixed band hysteresis current control.

The hysteresis current band value is directly proportional to the current ripple and inversely proportional to the switching frequency. Thus, increasing the value of the hysteresis current band will increase the current ripple while a decrease in the band will increase the switching losses. In analog controllers, the current ripple is always kept exactly within the hysteresis band. However, in digital controllers, the hysteresis control is shown to be effective only if the current band is chosen to satisfy the following condition [5]:

$$\Delta i_b > \max\left(\frac{di_{ref}}{dt}\right)\frac{1}{f_{sp}}, \tag{1}$$

where f_{sp} is the sampling frequency. The maximum switching frequency $f_{sw\_\max}$ should be smaller than half the sampling frequency f_{sp}, i.e. :

$$f_{sw\_\max} \le \frac{1}{2} f_{sp}. \tag{2}$$

3. Conventional Adaptive Hysteresis Current Control

3.1. Algorithm of the Convention Adaptive Hysteresis Current Control

The above mentioned fixed band hysteresis control has many advantages: its simplicity, its fast and stable response, and its independence from system parameters. However, a disadvantage is that the switching frequency needs to vary in order to keep the peak-to-peak current ripple controlled at all points on the fundamental frequency wave [10]. In order to solve this problem, the adaptive hysteresis current control technique has been presented in the literature [7, 26]. In this technique, the hysteresis current band is not fixed, but controlled adaptively in each switching modulation period, based on the measured output voltage values and the desired constant switching frequency. The adaptive hysteresis current control is employed as shown below.

Define the current error $\Delta i(t)$ as:

$$\Delta i(t) = i_L(t) - i_{ref}(t), \tag{3}$$

where $i_L(t)$, and $i_{ref}(t)$ are the inverter output and the reference currents, respectively, at instant t. Consider the instant t_0, when the output current i_L tends to cross the lower hysteresis band, and the switch S_1 is switched on. The current error at t_0 is $\Delta i(t_0)$ (Figure 4). Assume that the switch S_1 is switched on during $[t_0, t_1)$, and is switched off during $[t_1, t_2)$ intervals. These intervals are called positive and negative half switching periods respectively.

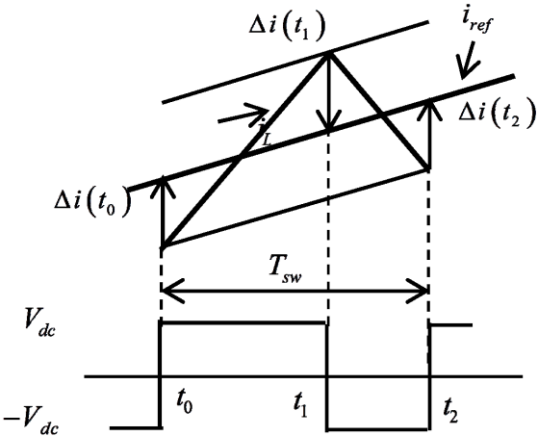

Figure 4. Conventional adaptive hysteresis current control.

The output current dynamic equation can be written as:

$$\frac{di_L(t)}{dt} = \frac{v_{dc}(t) - v_g(t)}{L} \tag{4}$$

for $t_0 \le t \le t_2$, where v_g is the instantaneous grid voltage, L is the output inductance, and $v_{dc}(t)$ is the inverter dc voltage, and can be elaborated as:

$$v_{dc}(t) = \begin{cases} V_{dc} & if\ S_1\ is\ On \\ -V_{dc} & if\ S_1\ is\ Off \end{cases}. \tag{5}$$

Define the output current slopes in the on and off periods by $\dot{I}_{on}$, and $\dot{I}_{off}$ respectively. Assuming that the output voltage is slowly varying during the switching modulation period $[t_0, t_2]$, the output current slopes (4) can be expressed as:

$$\dot{I}_{on} = \frac{di_L(t)}{dt} = \frac{V_{dc} - v_g(t_0)}{L} \tag{6}$$

for $t \in [t_0, t_1)$, and:

$$\dot{I}_{off} = \frac{di_L(t)}{dt} = \frac{-V_{dc} - v_g(t_0)}{L} \tag{7}$$

for $t \in [t_1, t_2)$.

The current errors in the positive and negative half switching periods are given as:

$$\begin{aligned} \Delta i(t_1) &= i_L(t_1) - i_{ref}(t_1) \\ &= i_{ref}(t_0) + \Delta i(t_0) + \dot{I}_{on} T_{on} - i_{ref}(t_1), \end{aligned} \tag{8}$$

$$\begin{aligned} \Delta i(t_2) &= i_L(t_2) - i_{ref}(t_2) \\ &= i_{ref}(t_0) + \Delta i(t_0) + \left(\dot{I}_{on} T_{on} + \dot{I}_{off} T_{off}\right) - i_{ref}(t_2). \end{aligned} \tag{9}$$

where T_{on} and T_{off} are the on and off periods of switch S_1, given as:

$$T_{on} = t_1 - t_0 \tag{10}$$

$$T_{off} = t_2 - t_1 \tag{11}$$

The reference current $i_{ref}(t)$ is slowly varying during the modulation period, such that it can be approximated as:

$$i_{ref}(t_1) = i_{ref}(t_0) + \dot{I}_{ref}(t_0) T_{on}, \tag{12}$$

$$i_{ref}(t_2) = i_{ref}(t_0) + \dot{I}_{ref}(t_0)\left(T_{on} + T_{off}\right), \tag{13}$$

where:

$$\dot{I}_{ref}(t_0) = \left.\frac{di_{ref}(t)}{dt}\right|_{t=t_0} \tag{14}$$

By substituting Equations (12) and (13) into Equations (8) and (9), one can write the current errors $\Delta i(t_1)$, and $\Delta i(t_2)$ as:

$$\Delta i(t_1) = \Delta i(t_0) + \dot{I}'_{on} T_{on} \tag{15}$$

$$\Delta i(t_2) = \Delta i(t_0) + \dot{I}'_{on} T_{on} + \dot{I}'_{off} T_{off} = \Delta i(t_1) + \dot{I}'_{off} T_{off} \tag{16}$$

where $\dot{I}'_{on}$ and $\dot{I}'_{off}$ are the current error slopes in positive and negative half switching periods, given as:

$$\dot{I}'_{on} = \dot{I}_{on} - \dot{I}_{ref}(t_0) = \frac{V_{dc} - v_g(t_0)}{L} - \dot{I}_{ref}(t_0), \tag{17}$$

$$\dot{I}'_{off} = \dot{I}_{off} - \dot{I}_{ref}(t_0) = \frac{-V_{dc} - v_g(t_0)}{L} - \dot{I}_{ref}(t_0) \tag{18}$$

Let f_{sw} be the desired constant switching frequency. In the conventional adaptive hysteresis current control method, the hysteresis current band $\Delta i_b(t_0)$ is derived by using the following conditions:

$$\Delta i(t_1) - \Delta i(t_0) = 2\Delta i_b(t_0) \tag{19}$$

$$\Delta i(t_2) - \Delta i(t_1) = -2\Delta i_b(t_0), \tag{20}$$

$$T_{on} + T_{off} = T_{sw}, \tag{21}$$

where $T_{sw} = 1/f_{sw}$ is the desired constant switching period. Substituting Equations (19)–(21) into Equations (15) and (16), we can derive the hysteresis current band as:

$$\Delta i_b(t_0) = \frac{1}{2}\frac{\dot{I}_{on}\dot{I}_{off}}{\dot{I}_{off} - \dot{I}_{on}} T_{sw} \tag{22}$$

By substituting Equations (17) and (18) into Equation (22), the hysteresis band in Equation (22) can also be written in the form of [26] :

$$\Delta i_b(t_0) = \frac{V_{dc} T_{sw}}{4L}\left(1 - m^2(t_0)\right), \tag{23}$$

where:

$$m(t_0) = \frac{1}{V_{dc}}\left(v_g(t) + L\dot{I}_{ref}(t)\right) \tag{24}$$

3.2. Disadvantages of Conventional Adaptive Hysteresis Current Control

Consider the case where the inverter needs to be controlled so that the operating switching frequency is always strictly equal to or lower than a constant frequency, which may be the highest possible switching frequency of the switching devices.

The conventional adaptive hysteresis current control described in Section 3.1 has been shown to be able to improve on the disadvantage of the fixed band hysteresis current control of the varying switching frequency [8]. However, when the inverter is operated under the effect of noise or disturbances, this conventional method does not guarantee a stable response and constant switching frequency as, for example, in the following problems.

Problem 1. *If the negative half switching period of switch* S_1 *in the previous modulation period is* T_{off_pre}*, as shown in Figure 5, then:*

$$T_{off\_pre} = t_0 - t_{-1} \tag{25}$$

While the operating switching frequency can be defined from both the time periods $T_{on} + T_{off}$ and $T_{off\_pre} + T_{on}$, the calculation of the conventional hysteresis current band only guarantees that modulation period $T_{on} + T_{off}$ is equal to the desired constant switching period T_{sw}, as in Equation (21). If the noise or disturbances to voltage and current make the negative half switching period

T_{off_pre} in the previous modulation shorter than the calculated value, then the operating switching frequency of the conventional method may exceed the highest possible switching frequency of the switching devices.

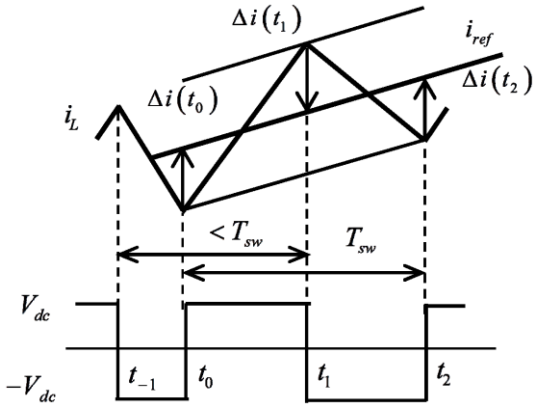

Figure 5. Conventional adaptive hysteresis current control does not guarantee that the operating switching frequency will be lower than the desired constant frequency.

Problem 2. *In order to keep the average value of the output current equal to the reference current in each switching modulation, the hysteresis current band should be computed so that:*

$$-\Delta i(t_1) = \Delta i(t_2) = -\Delta i_b \tag{26}$$

However, the hysteresis current band computed by the conventional method, as in Equations (19) and (20), in general, does not satisfy the Condition (26), except in the case of the ideal condition shown by the dashed line in Figure 6, where the current error at instant t_0 is identical to the computed hysteresis current band Δi_b, i.e. :

$$\Delta i(t_0) = -\Delta i_b \tag{27}$$

When the Condition (27) is not satisfied, the average value of the output current during a switching modulation period deviates from the reference current, which may lead to an unstable response as shown in Figure 6 by the solid line.

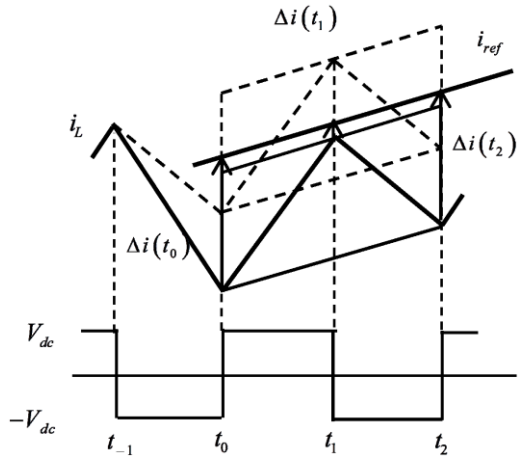

Figure 6. Conventional adaptive hysteresis current control does not guarantee the stability of the response current.

4. Proposed Robustly Adaptive Hysteresis Current Control

Consider the instant t_0, when the output current crosses to pass the lower limit of the hysteresis band $i_{ref} + \Delta i(t_0)$ and the switch S_1 starts to be switched on as shown in Figure 7. The negative half switching period of switch S_1 in the previous modulation period T_{off_pre} is:

$$T_{off\_pre} = t_0 - t_{-1}. \tag{28}$$

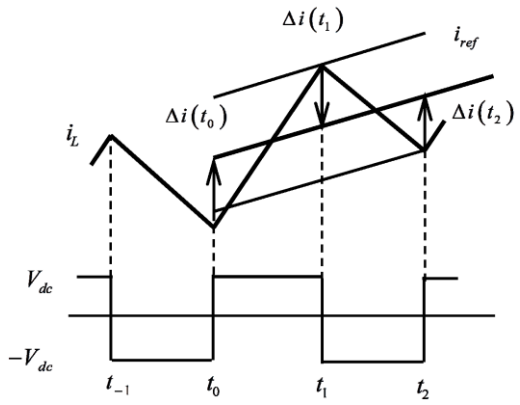

Figure 7. Proposed adaptive hysteresis current control.

In order to solve the problem of unstable switching frequency of the conventional adaptive hysteresis current control mentioned in Section 3, this study proposes a new hysteresis current band computation method by setting an optimization problem as:

$$\begin{aligned}
&(i) \quad T_{off-pre} + T_{on} \geq T_{sw}, \\
&(ii) \quad T_{on} + T_{off} \geq T_{sw}, \\
&(iii) \quad \Delta i_b = \Delta i(t_1) = -\Delta i(t_2), \\
&(iv) \quad \Delta i_b \geq \Delta i_{conv}, \\
&\underset{\Delta i}{\text{minimize}} \; J = \left(\Delta i(t_1)\right)^2 + \left(\Delta i(t_2)\right)^2,
\end{aligned} \tag{29}$$

where Δi_{conv} is the hysteresis current band computed by the conventional method as in Equation (22), and J is the objective function.

Constraint conditions (*i*) and (*ii*) in Equation (29) maintain the operating switching frequency to always be equal to or smaller than the desired instant switching frequency. Condition (*iii*) keeps the average value of the output current identical to the reference current during the switching modulation period. Condition (*iv*) keeps the output current from deviating from the reference current. The objective function J represents the power loss from the inverter in each switching modulation period. The hysteresis current band is computed such that the power loss J is minimized.

Equations (15) and (16) can be written as:

$$T_{on} = \frac{1}{\dot{I}'_{on}}\left(\Delta i(t_1) - \Delta i(t_0)\right), \tag{30}$$

$$T_{off} = \frac{1}{\dot{I}'_{off}}\left(\Delta i(t_2) - \Delta i(t_1)\right) \tag{31}$$

Substituting Equations (30) and (31) into Equation (29), the optimization problem (29) can be written as:

$$\begin{aligned}
&(i)\quad \Delta i(t_1) \geq \dot{I}'_{on}\left(T_{sw} - T_{off-pre}\right) + \Delta i(t_0),\\
&(ii)\quad \left(1 - \frac{\dot{I}_{on}}{\dot{I}_{off}}\right)\Delta i(t_1) + \frac{\dot{I}_{on}}{\dot{I}_{off}}\Delta i(t_2) \geq \dot{I}_{on}T_{sw} + \Delta i(t_0),\\
&(iii)\ \Delta i(t_1) = -\Delta i(t_2) = \Delta i\\
&(iv)\ \ \Delta i \geq \Delta i_{conv},\\
&\underset{\Delta i}{\text{minimize}}\ J = \left(\Delta i(t_1)\right)^2 + \left(\Delta i(t_2)\right)^2
\end{aligned} \tag{32}$$

The constraints in the optimization problem given in Equation (32) are linear. They can be solved by using the graphical method for minimization problems [27], as below. The feasible region representing constraint conditions (*i*–*iv*) can be represented by the dark area on the phase-plane $\left(\Delta i(t_1), \Delta i(t_2)\right)$ as in Figure 8. The objective function J is represented by the distance from the original phase-plane to the point $\left(\Delta i(t_1), \Delta i(t_2)\right)$. Thus, the optimal solution for Problem (32) is the point $\left(\Delta i(t_1)_s, \Delta i(t_2)_s\right)$ on the feasible region, which is closest to the original point. The solution can be derived as:

$$\Delta i_{opt} = \max\left(\Delta i_{conv}, \Delta i_A, \Delta i_B\right), \tag{33}$$

where Δi_A, Δi_B, Δi_{conv} are the points which satisfy pair constraint conditions (*i*, *iii*), (*ii*, *iii*), (*iv*, *iii*), respectively, and are given by:

$$\Delta i_A = \dot{I}_{on}\left(T_{sw} - T_{off-pre}\right) + \Delta i(t_0), \tag{34}$$

$$\Delta i_B = \frac{\dot{I}_{on}T_{sw} + \Delta i(t_0)}{1 - 2\dot{I}_{on}/\dot{I}_{off}}, \tag{35}$$

$$\Delta i_{conv} = \frac{1}{2}\frac{\dot{I}_{on}\dot{I}_{off}}{\dot{I}_{off} - \dot{I}_{on}}T_{sw} \tag{36}$$

When the optimal solution is at Δi_A, it means that, for example under the effect of noise, the negative half switching period T_{off_pre} in the previous switching modulation was smaller than the regular value (Problem 1 in Section 3) and the hysteresis current band needs to be broadened to satisfy condition (i) in Equation (29). When the optimal solution is at Δi_B, it means that the average output current deviated from the reference current (Problem 2 in Section 3) and the hysteresis current band needs to be broadened to satisfy condition (*ii*) in Equation (29). When the optimal solution is at Δi_{conv}, it means that the conditions (*i*) and (*ii*) are satisfied and the hysteresis current band should be brought to the steady state as in the conventional method.

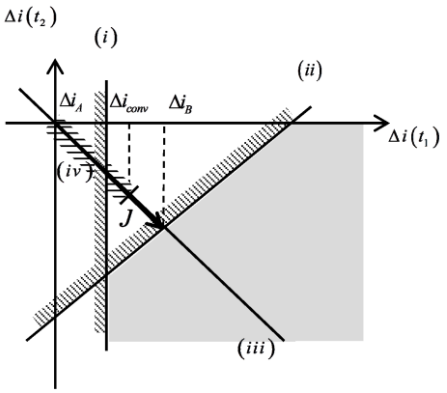

Figure 8. Domain and optimal solution for the hysteresis current band.

Remark 1. *In an ideal state, where the effect of noise is sufficiently small, the proposed method gives the same hysteresis current band as the conventional adaptive hysteresis current control method.*

5. Simulation Results

Simulations have been carried out to assess the performance of the proposed method as compared with the conventional method [13] using the Matlab-Simscape Power System. A single-phase half-bridge inverter was employed with the following parameters: an output inductance of $L = 1\,\text{mH}$ and a filter capacitor of $C = 10\ \mu\text{F}$. The switching transistors in the inverter circuit were modeled by the Insulated Gate Bipolar Transistor (IGBT) block in the Matlab-Simscape(R2016a, MathWorks, Natick, MA, USA) Power System. The IGBTs have internal and snubber resistances of 1 mΩ and 1 kΩ, respectively. The inverter was connected to the dc voltage source $V_{dc} = 175\,\text{V}$, and the ac voltage of the grid was $v_g = 100\sqrt{2}\sin(100\pi t)\,\text{V}$. The sampling frequency of the analog/digital converters was $f_{sp} = 2\,\text{MHz}$. The reference current was set at $i_{ref} = 10\sin(100\pi t)\,\text{A}$. The noise in the measured current, which may have come from the current sensor or the analog/digital converter, was assumed to be white noise with a variance of 0.01 A. Figures 9–11 show the operating switching frequencies and the output currents of the proposed and conventional methods compared with the reference current for the desired constant switching frequency f_{sw} at 40 kHz, 20 kHz, and 10 kHz respectively. The upper sub-figures show a part of the current hysteresis response. Regarding the desired constant switching frequencies, both methods yielded hysteresis output currents that were similar to the reference current. However, the operating switching frequency of the conventional method oscillated and went over the desired constant switching frequency. On the other hand, the proposed method yielded a switching frequency that was more stable than that of the conventional method and was always maintained at equal to or lower than the desired constant switching frequency. All the Figures also show that the hysteresis current band increased when the desired constant switching frequency was increased.

The power efficiency of the inverter has been calculated, taking into account hysteresis current loss. Table 2 shows the power efficiencies of the proposed and conventional methods with the tested switching frequencies. The efficiencies of both methods decreased when the switching frequency was decreased. It can be seen that the proposed method performed better than the conventional method in terms of power efficiency in all cases.

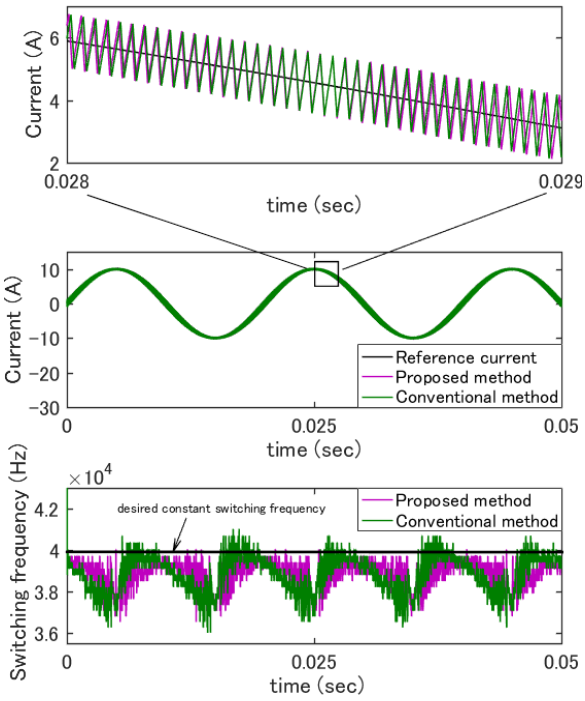

Figure 9. Current and switching period of the proposed method and conventional method for the desired switching frequency at 40 kHz.

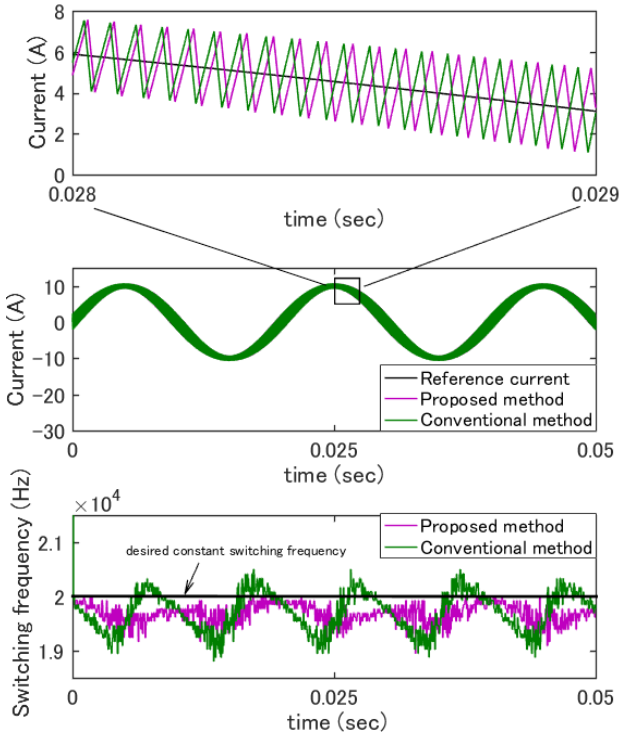

Figure 10. Current and switching period of the proposed method and conventional method for the desired switching frequency at 20 kHz.

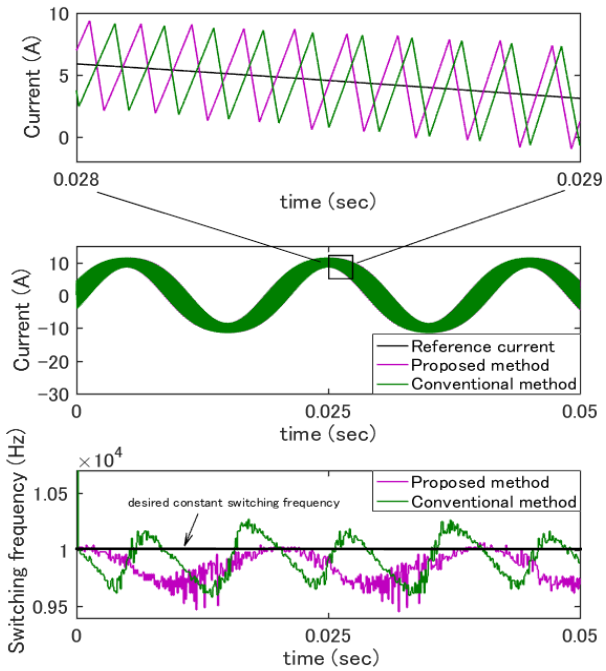

Figure 11. Current and switching period of the proposed method and conventional method for the desired switching frequency at 10 kHz.

Table 2. Power efficiency with various switching frequencies (%).

Switching frequency	$f_{sw} = 10$ kHz	$f_{sw} = 20$ kHz	$f_{sw} = 40$ kHz
Proposed method	97.1	98.4	99.3
Conventional method	95.2	97.2	98.5

6. Conclusions

A new digital hysteresis current control algorithm for single-phase half-bridge inverters has been proposed. By taking advantage of digital controls, the hysteresis current band is computed in each switching modulation period based on both the negative half switching period and the current error during the previous switching modulation period, in addition to the usual measured voltage value at the instant of computing. The hysteresis current control, with its simplicity and its fast and stable response, may be implemented on high-speed FPGA boards with a high sampling frequency. The proposed algorithm for computing the hysteresis current band is derived by solving the optimization problem where (i) the switching frequency is stable and always maintained at equal to or lower than the desired constant frequency, (ii) the output current is kept stable around the reference current, and (iii) the power loss is minimized. Although the proposed control method has not been evaluated in experiments, the theoretical numerical and simulation results show good performance of the proposed algorithm compared with those of the conventional method. The proposed method is expected to contribute to the control theory of high-speed FPGA-based hysteresis current control.

Author Contributions: Triet Nguyen-Van, Rikiya Abe, Kenji Tanaka performed and discussed the research; Triet Nguyen-Van carried out the simulations, analyzed the data, and wrote the paper.

Conflicts of Interest: The authors declare no conflict of interest.

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