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Seamless Grid Synchronization of a Proportional+Resonant Control-Based Voltage Controller Considering Non-Linear Loads under Islanded Mode

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Abstract: This paper proposes the grid synchronization method of inverter using a quasi Proportional+Multi Resonant (P+MR) control-based voltage controller a stationary reference frame. The inverter supplies a non-linear load under the islanded mode. In islanded mode, the inverter is defined as a voltage source to supply the full local load demand without a connection to the grid. On the other hand, if the grid is restored from a previous fault or the strategic islanding is unnecessary, the inverter needs to be synchronized with the phase of the grid before the transfer from islanded mode to grid-connected mode. When the system is modeled and controlled based on the stationary reference frame control, the AC reference voltage, which has a constant voltage and frequency in islanded mode, is substituted to the AC grid voltage. Significant error can occur due to the large phase differences between the phase of reference and that of the measured value. This error also can cause severe voltage dynamic problems. In addition, if any nonlinear local load is connected to the output of the inverter, it becomes more serious due to the harmonics generated from the loads. In this paper, the PR control under a stationary reference frame is used for voltage control under islanded mode considering the harmonic effects from the nonlinear load. The seamless grid synchronization method based on this PR control is proposed to solve the aforementioned problems. The validity of the proposed seamless grid synchronization method is verified through PSiM simulations and experimental results.

Keywords: nonlinear load; PR control; stationary reference frame; islanded mode; grid synchronization; voltage control; harmonic compensation

1. Introduction

A distributed generator (DG) fed by an inverter is connected to the grid through a LCL filter to attenuate the current harmonics as shown in Figure 1. In this grid-connected mode, the inverter output current should be controlled to supply power to the grid within the allowable distortion range of current [1]. In the event of any grid faults or intentional switchover, the inverter has to operate as a voltage source to supply power to the local load under islanded mode [2].However, the transient performance of the inverter output voltage control is limited due to the characteristics of the non-zero output impedance of the inverter, the accurate voltage regulation becomes more difficult when the nonlinear or unbalanced load is connected to the inverter [2–5]. The design of a multi loop voltage controller has been studied conventionally to improve the dynamic response of the inverter [6–17], and different types of controllers for harmonics compensation, such as Proportional+Integral (PI), Proportional+Resonant (PR) and repetitive based methods, etc., have been proposed [4–13]. Among these controllers, the harmonic compensation method using the

Proportional+Multi Resonant (P+MR) controller has attracted attention because it is simpler to implement than the PI-based harmonics compensation method and the positive and negative sequence components can be controlled simultaneously by one controller [13,14]. In [2,4,12], the durability of the P+MR controller was improved by modifying it as a quasi-PR control form, which has an extremely large gain at the target frequency. Therefore, the allowable band of the control frequency was extended, and it was possible to compensate for the specific order of harmonics with high stability in spite of the frequency change due to sudden load changes or limited component tolerance [13,14].

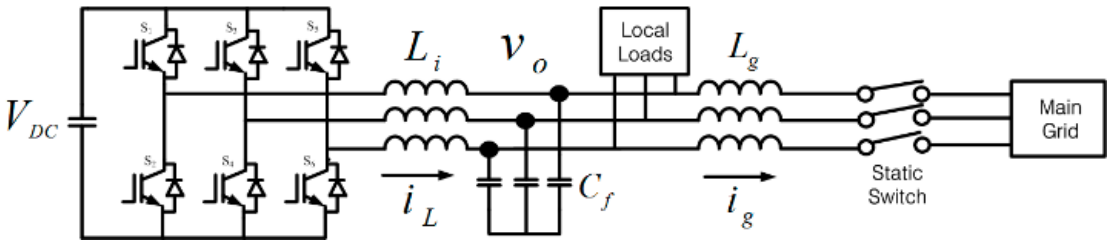


Figure 1. System configuration of grid-connected inverter with LCL filter and local loads.

When the grid fault is recovered or the strategic islanding is no longer required, the inverter operation is switched from the islanded mode to the grid-connected mode. During this transition, the phase of the inverter output voltage is to be synchronized with the phase of the grid voltage, and the Phase Locked Loop (PLL) has been usually used for synchronization [15–19]. The PI-based grid synchronization technique was implemented in [10,20] as the partial study of indirect current control based inverter operation which includes the inner filter capacitor voltage loop. The vector diagram-based capacitor voltage reference calculation method was proposed in [20], but the vector diagram- based reference calculation is difficult to implement, especially under non-linear load conditions. In [10], the PI-based grid synchronization technique was proposed to realize the direct load voltage control, but the grid synchronization was still difficult under the non-linear load connection. Because this PI control was based on the fundamental frequency, it could not compensate the harmonics properly. The addition of PI-based harmonics compensation terms was not also preferred due to the complexity of implementation [12]. A PR-based grid synchronization method was proposed in [11], but it considered only the linear resistive local load. Therefore, if the grid voltage was injected directly to the reference voltage without an additional technique for grid synchronization, it might cause a serious voltage transient. This is because an unexpected large voltage error was generated at the point of phase synchronization due to the phase difference between the grid voltage and the inverter voltage under the stationary reference frame. On the other hand, the fixed *d-q* variable assigning technique, which the inner current reference was assigned as a fixed average value according to the local load amount, was proposed [11]. In [11], the output of PR voltage loop was disabled and the *abc-dq* transformation was needed temporarily for grid synchronization to assign the fixed *d-q* value to the inner current reference. However, this method still had two drawbacks as follows: Firstly, it had some limitation to adapt the harmonics compensation during the grid synchronization because the acquisition of fixed average value for harmonics term was quite difficult, and secondly, it did not respond adaptably to the frequent load changes which the relatively different *d-q* assigned values were necessary to the amount of load.

This paper adopts the quasi-P+MR control-based inverter voltage control for grid synchronization under the islanded mode so that harmonics compensation can be easily implemented as aforementioned. The reference voltage modification technique is also proposed instead of using the fixed *d-q* variable technique to solve the problems in [11] with the non-linear load connection. The contributions of this paper are as follows: firstly, the angular frequency of the PLL is limited by an additional limiter. With this limited angular frequency, the injected reference voltage can be newly generated without assigning directly a grid voltage to the voltage reference. Therefore, the phase

of generated voltage reference can be smoothly synchronized with the phase of grid. The mutual compatibility between the phase angle of PLL and the allowed controllable frequency range of resonant controller has been considered carefully. Secondly, the total harmonic distortion (THD) performance of load voltage and the transient response to the load change can be improved by the well-designed control parameters. Therefore, the seamless grid synchronization and good voltage quality can be obtained simultaneously by the proposed method. Finally, the proposed method is evaluated by the comparison with the results of existing works through the case studies, and the validity of the proposed algorithm is verified through the PSiM simulations and laboratory-scale experiments.

2. Quasi P+MR Based Harmonic Compensation Method under Islanded Mode

2.1. Quasi P+MR Based Harmonic Compensation Method

The harmonic components or negative sequence components are generated when the AC power supplies power to a nonlinear or unbalanced load [3]. The output voltage is then distorted by these generated current harmonics. The PI controller-based harmonics compensation has been proposed [21]. This method, however, was quite complicated because it required both positive and negative component controllers and many separate digital filters proportional to the number of compensated specific harmonics. In addition, the accurate phase information of the fundamental and harmonic components of the distorted output voltage for the *dq* transformation are necessary. This means that the PI-based control with a harmonics compensation term requires a high performance PLL to analyze the information on both the fundamental component and harmonic components [19]. On the other hand, in the case of PR-based control in the stationary reference frame, it filters the specific harmonic frequency component autonomously without correct phase information. Therefore, the harmonics compensation can be implemented simply through the use of a P+MR resonant voltage controller.

The basic equation for a quasi P+MR controller is given in Equation (1), which has $\omega_{n,cut}$ adding the low pass term to an ideal PR equation. This includes the s term in the nominator of the resonant controller. Hence, it has a larger phase margin and guarantees better dynamic performance than that without an s term [14,22]:

$$H_{P+MR} = K_P + \frac{K_i \omega_{1.cut} s}{s^2 + 2\omega_{1.cut} s + \omega_o^2} + \sum_{n=3,5,7th} \frac{K_{i.n} \omega_{n.cut} s}{s^2 + 2\omega_{n.cut} s + (n\omega_o)^2} \quad (1)$$

where $K_{i.n}$ $\omega_{n.cut}$ is the resonant gain of the voltage controller for the nth frequency. The P+MR controller has a large gain in the order of harmonics to compensate for the harmonics generated from the unbalanced and nonlinear loads. Therefore, the 1st, 3rd, 5th, and 7th harmonics can be compensated for by the P+MR voltage controller under islanded mode. In this paper, the inner proportional current controller was added to enhance the system transient dynamics at the instant of a load change or initial starting. In this case, the proportional current loop causes a significant phase shift at the operating frequency. Therefore, the large voltage loop controller gain is essential to compensate for the phase shift and to guarantee a negligible steady state error [4,12].

Figure 2 shows the configuration of the P+MR voltage controller, which includes the inner proportional current control loop. As shown in the figure, all controllers are based on the αβ reference frame.

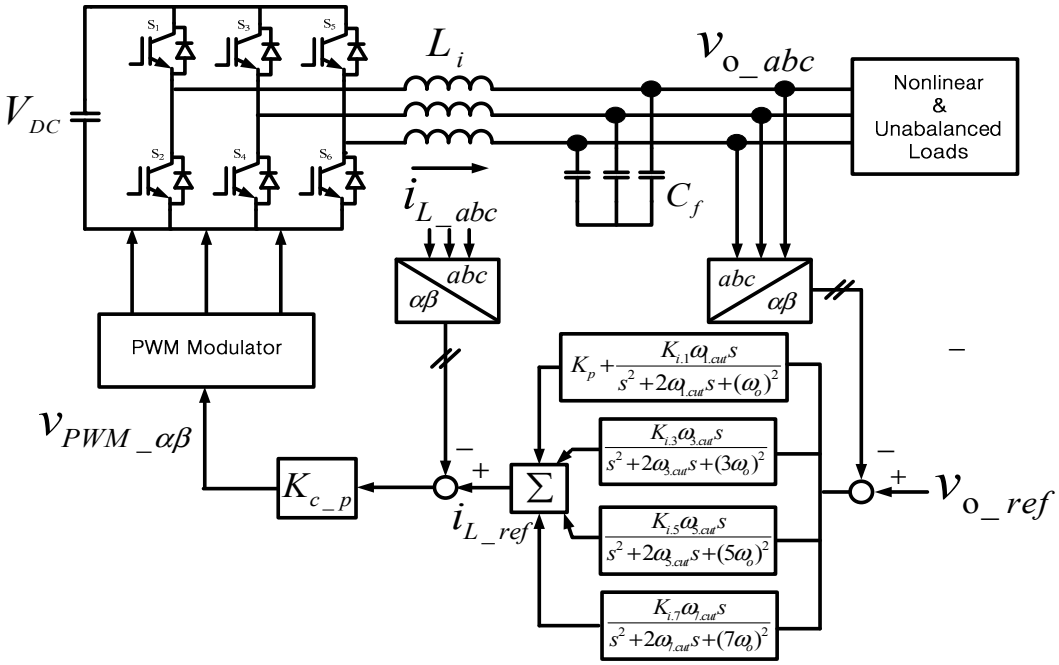


Figure 2. Configuration of P+MR controller in islanded mode.

2.2. Design of Outer Voltage Loop with Inner Current Loop for SSI Mode

2.2.1. Design of Inner Current Loop

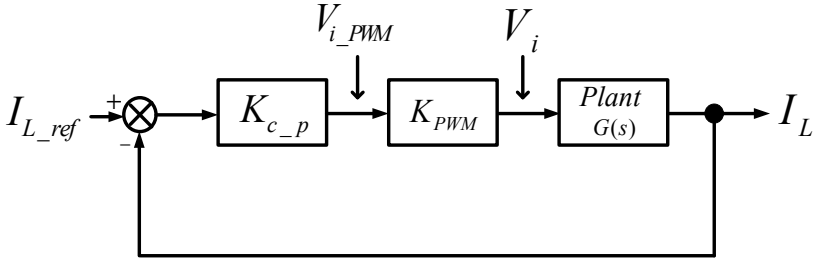
Figure 3a presents a block diagram of the inner current controller, where K_{c_p} and K_{pwm} represent the proportional gain of the current controller and the pulse-width modulation (PWM) gain of the inverter, respectively. $G(s)$ represents the LC filter transfer function when the output current, I_o, is assumed to be a disturbance, which can be described in Equation (2):

$$G(s) = \frac{I_L(s)}{V_i(s)} = \frac{sC}{s^2LC+1} \tag{2}$$

Substituting Equation (2), the closed transfer function of the current controller can be expressed as Equation (3):

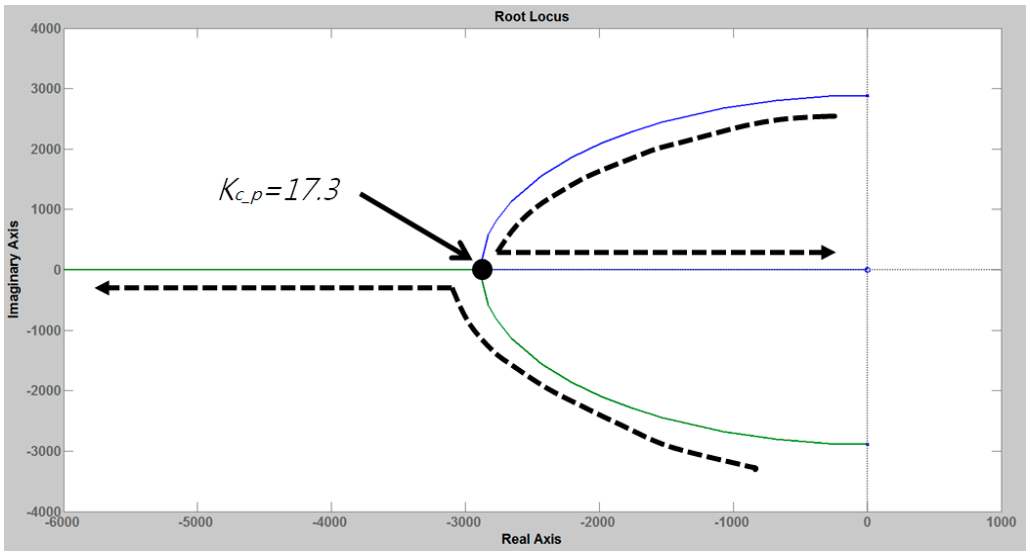
$$\frac{I_L(s)}{I_{L\_ref}(s)} = \frac{sK_{c\_p}K_{PWM}C_f}{s^2L_iC_f + sK_{c\_p}K_{PWM}C_f + 1} \tag{3}$$

Figure 3b shows the root locus from Equation (3) according to various K_{c_p} when K_{pwm} is assumed to be '1'. As shown in this figure, all oscillation characteristics can be eliminated entirely for $K_{c\_p} \geq 17.3$ [2].



(**a**)

Figure 3. *Cont.*



(**b**)

Figure 3. Block diagram and root locus of the inner current control loop: (**a**) block diagram; (**b**) root locus.

2.2.2. Design of Cut-Off Frequency, $\omega_{n.cut}$

The output frequency changing problem under islanded mode is not as serious as that in grid-connected mode because the voltage reference is fixed during the operation of a microgrid under islanded mode and the frequency change under islanded mode occurs intermittently within a stable operating frequency range. Although droop control is used to share the output power of the inverters by changing the voltage and frequency intentionally, this changeable frequency range is within the stable boundary by a constant voltage and frequency. Therefore, in islanded mode, the practical PR control form with $\omega_{n.cut}$, as shown in Equation (1), is sufficient to meet the stable output voltage regulation for both transient and steady-state of islanded mode [12] (note that [23,24] investigated the adaptive frequency control mainly for a steady state operation. In the present study, however, it is not considered because these authors only considered the transient dynamics under islanded mode of which the operating frequency is fixed at 60 Hz).

The cut-off frequency for the fundamental component, $\omega_{1.cut}$, and that for the harmonic frequency components, $\omega_{n.cut}$, can be designed using the following equations [12]:

$$\zeta = \frac{\omega_{n.cut}}{n\omega_o} \tag{4}$$

$$\omega_{5.cut} = 5 \cdot \omega_{1.cut} \tag{5}$$

$$\omega_{7.cut} = 7 \cdot \omega_{1.cut} \tag{6}$$

The damping factor, σ, and the cutoff frequencies of the PR controller are defined by Equations (4)–(6). The cutoff frequencies of the harmonic terms defined as Equations (5) and (6) need to meet the same damping ratio for the cutoff frequencies of the harmonic terms as that for the fundamental frequency. In this paper, the fundamental cutoff frequency, $\omega_{1.cut}$, was designed to cover ±1.6% of the frequency variation. Therefore, $\omega_{1.cut}$ can be designed as $\omega_{1.cut} = 2\pi \times 60 \times 1.6\% \approx 6$ r ad/s [25].

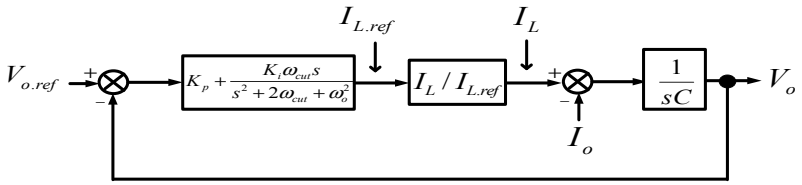
2.2.3. Selection of PR Voltage Control Gain

Figure 4a shows the closed loop block diagram of fundamental component voltage control. From Figure 4a, the characteristic equation of the voltage loop can be obtained as follows:

$$\frac{V_o}{V_{o.ref}} = \frac{s^2K_pK_{c.p} + s(2K_pK_{c.p}\omega_{cut} + K_iK_{c.p}) + K_pK_{c.p}\omega_o^2}{s^4LC + s^3(K_{c.p}C + 2LC\omega_{cut}) + s^2(2\omega_{cut}K_{c.p}C + K_pK_{c.p} + LC\omega_o^2 + 1) + s(K_{c.p}C\omega_o^2 + K_iK_{c.p} + (K_pK_{c.p} + 1)2\omega_{cut}) + (K_pK_{c.p} + 1)\omega_o^2} \quad (7)$$

$$(K_i.\omega_{cut} \approx K_i, K_{PWM} \approx 1)$$

The bandwidth of the outer voltage loop is determined mainly by the proportional gain, K_p. Hence, $k_{i.1}\cdot\omega_{1.cut}$ can be assumed to be '0' for the selection of the proportional gain, K_p. Figure 4b shows the root locus in accordance with various K_p values from the characteristic equation (Equation (7)). As shown in the figure, the damping ratio is 0.707 when K_p reaches 0.0577.



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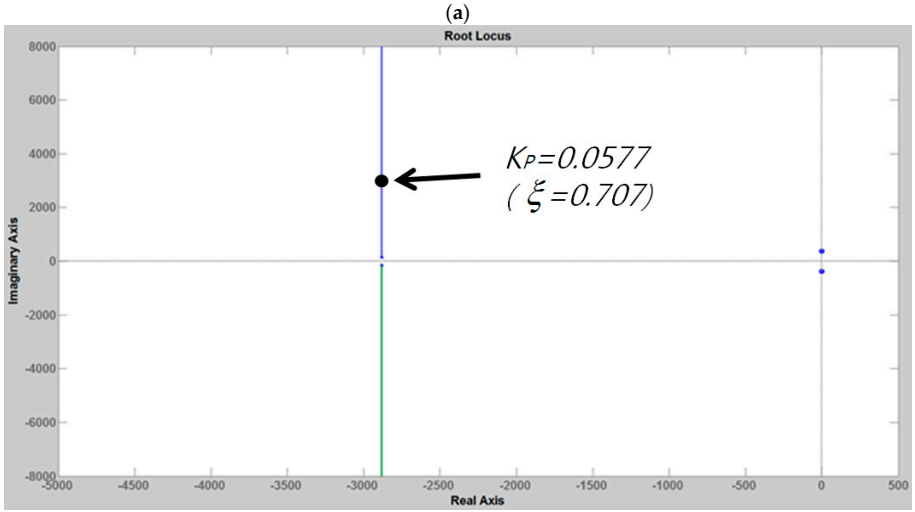

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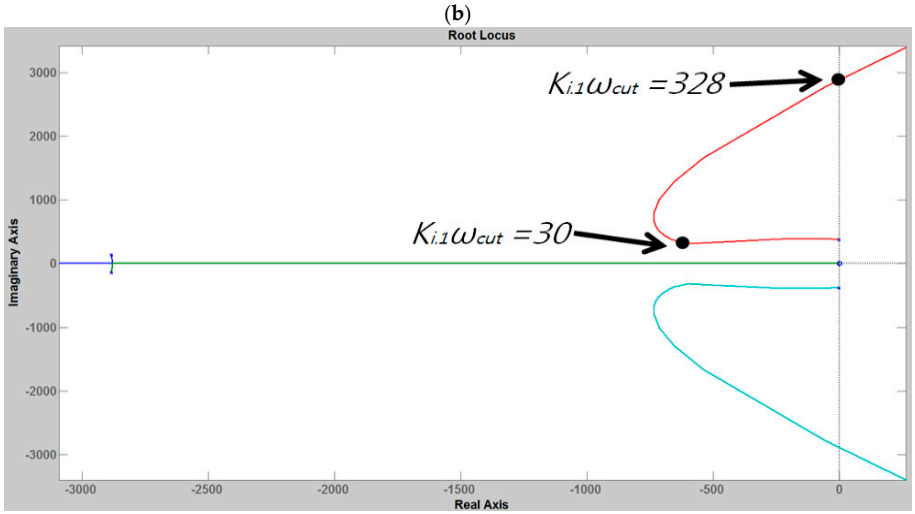
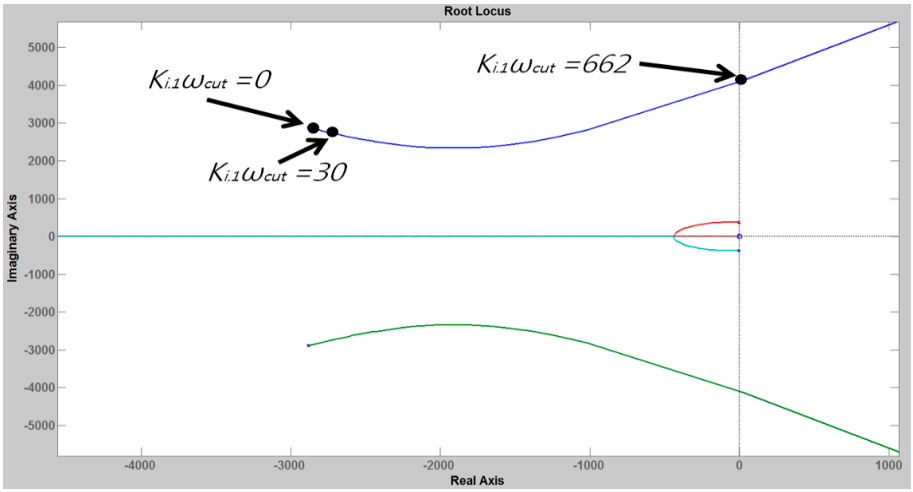


(**c**)

Figure 4. *Cont.*



(**d**)

Figure 4. Block diagram and root locus of the inner current control loop: (**a**) outer voltage loop block diagram; (**b**) root locus for K_p variations under $K_{i.1}\cdot\omega_{1.cut} = 0$; (**c**) root locus for $K_{i.1}\cdot\omega_{1.cut}$ variation under $K_p = 0$; (**d**) root locus for $K_{i.1}\cdot\omega_{1.cut}$ variations under $K_p = 0.0577$.

In this paper, K_p was selected as 0.0577, which satisfies both the system stability and proper transition response for harmonics compensation. Figure 4c,d show the root locus for various $k_{i.1}\cdot\omega_{1.cut}$ when $K_p = 0$ and 0.0577, respectively. As shown in Figure 4c, it has the largest damping ratio when $k_{i.1}\cdot\omega_{1.cut}$ is 30. Therefore, $k_{i.1}\cdot\omega_{1.cut}$ was selected as 30. To check the validity of $k_{i.1}\cdot\omega_{1.cut}$, the full model, which includes the K_p value, was considered in Figure 4d. As shown in this figure, the system damping ratios are almost 0.707 in the range of $k_{i.1}\cdot\omega_{1.cut}$ values from 0 to 30. Therefore, K_p mainly affects the transient response of the controller. Figure 5 shows the Bode plot of the open loop with P+MR-based voltage control. If the resonant gains for harmonics compensation are small, there is no satisfactory harmonics compensation. On the other hand, if the resonant gains are too large, it will become unstable as the phase margin is less than 0°. Therefore, $k_{i.5,7}\cdot\omega_{5,7.cut}$ was selected to be 20, of which the phase margin becomes approximately 45° to meet both the system stability and harmonics compensation.

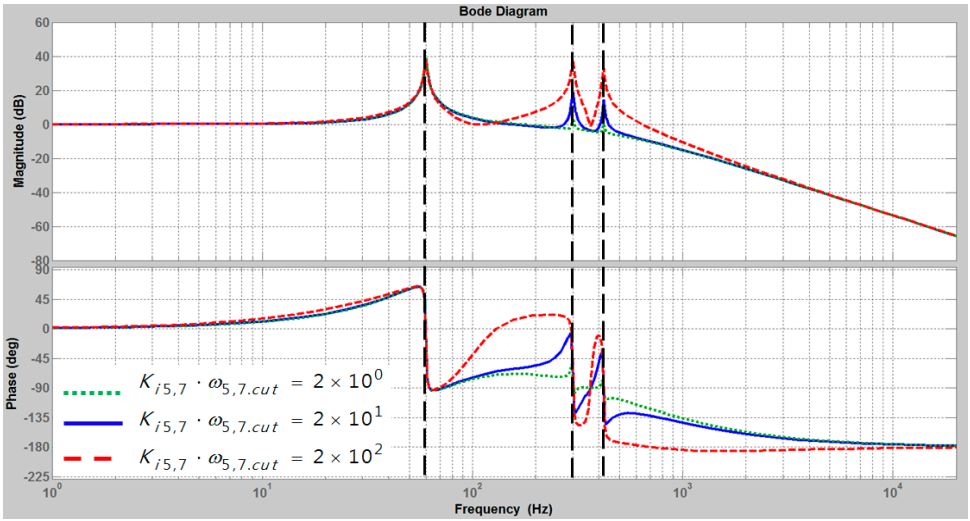


Figure 5. Bode plot of the P+MR based voltage controller with harmonics compensation: $K_p = 0.0577$, $K_{i.1}\cdot\omega_{1.cut} = 30$, $K_{i.5,7}\cdot\omega_{5,7.cut} = 20$.

3. Proposed Scheme with Case Study for Seamless Grid Synchronization

3.1. Analysis and Design of Proposed Scheme for Grid Synchronization

When the grid fault is recovered or the strategic islanding is no longer necessary, the quasi P+MR-based inverter needs to change the operation from the islanded mode to the grid-connected mode. For the mode transfer of the mode change, the phase of the inverter output voltage has to be synchronized with the phase of the grid before this transition. The grid voltage was used conventionally as the reference voltage, V_{o_ref}, as shown in Figure 2. However, this causes a serious voltage transient because the large voltage error can be generated at the point of phase synchronization as shown in Figure 6 due to the phase difference between the grid voltage and the inverter voltage under the stationary reference frame. The transient performance of the PR-based voltage controller is affected strongly by the frequency change as the control gain at the changed error frequency is relatively small compared to that near the center frequency, which is one of the drawbacks of using the PR-based control. To cope with this issue, the fixed *d-q* variable assigning technique, which the inner current reference was assigned as a fixed average value according to the local load amount, was proposed as shown in Figure 7 [11].

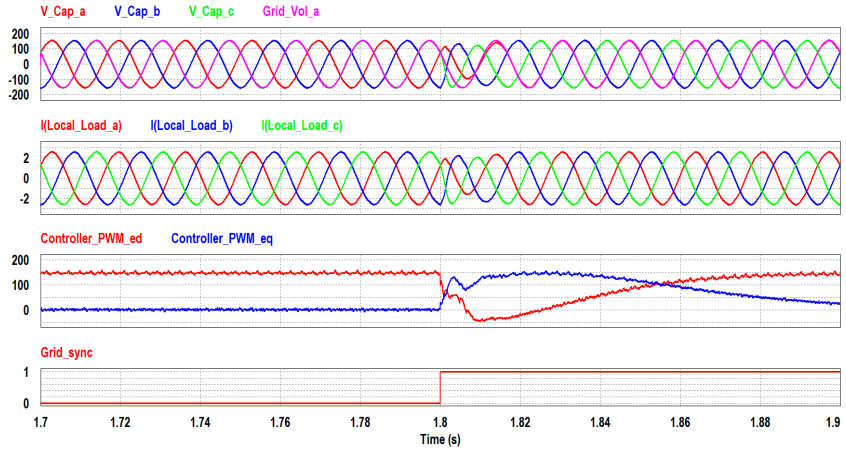


Figure 6. Simulation results with a direct grid injection to the reference voltage. (From top to bottom: Measured three phase inverter output voltages and a phase grid voltage, three phase local load currents, PWM *d-q* controller outputs, and GS status signal).

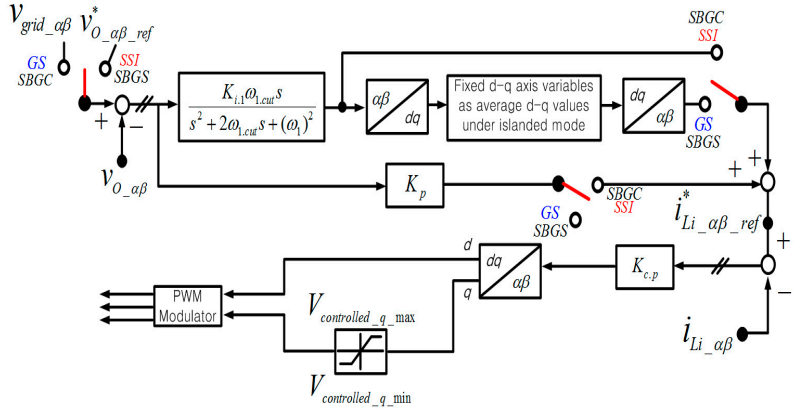


Figure 7. Block diagram of multi loop output voltage control-based grid synchronization method in [11] (Islanded mode changes from SSI (Steady State of Islanded mode) ⟶ SBGS (Standby mode for Grid Synchronization) ⟶ GS (Grid Synchronization) ⟶ SBGC (Standby mode for Grid Connection)).

Figure 8 shows the ideal waveforms of grid synchronization mode, which consists of Steady State of Islanded mode (SSI), Standby mode for Grid Synchronization (SBGS), Grid Synchronization mode (GS), and Standby mode for Grid Connection (SBGC) [11]. When the inverter is transferred from the SSI to the SBGS, the fixed *d-q* variable technique is activated to restrain the serious transient caused by the voltage error. The output of PR voltage loop is disabled and the $\alpha\beta$-*dq* transformation is needed temporarily to assign the fixed average *d-q* values as the inner current reference. As the GS mode starts, the voltage reference toggle switch also moves from SSI to GS to apply the grid voltage directly. After achieving the grid synchronization completely, the mode is changed to SBGC. In this mode, the disabled PR control output under SBGS and GS is returned to enable the control output. As last, it is ready to transfer the mode to GC seamlessly. However, this method still has two drawbacks. Firstly, it has some limitation to adapt the harmonics compensation during the grid synchronization because the acquisition of fixed average value for harmonics term is quite difficult. In addition, even though the 5th and 7th harmonics resonant controllers are enabled during GS, the bad transient performance can also occur because of the control mismatch between the allowable control frequency range of harmonics resonant controllers and the frequency change of voltage error due to the significant instantaneous voltage control error. Secondly, it does not respond adaptably to the frequent load changes which the relatively different *d-q* assigned values are necessary to the amount of load. Therefore, the load voltage magnitude error can occur during the period of grid synchronization. In other words, it is quite difficult to realize the seamless mode transfer while simultaneously satisfying harmonics compensation and load change adaptation.

In order to solve the above-described problems, the following must be considered. The directly injected grid voltage as the reference of voltage loop needs to be changed gradually to provide a smooth transition, and the phase angle is to be limited to prevent the large momentary frequency change considering the compatibility with the allowable range of control frequency depending on the cut-off frequency, $\omega_{\_(1.cut)}$ of the resonant controller.

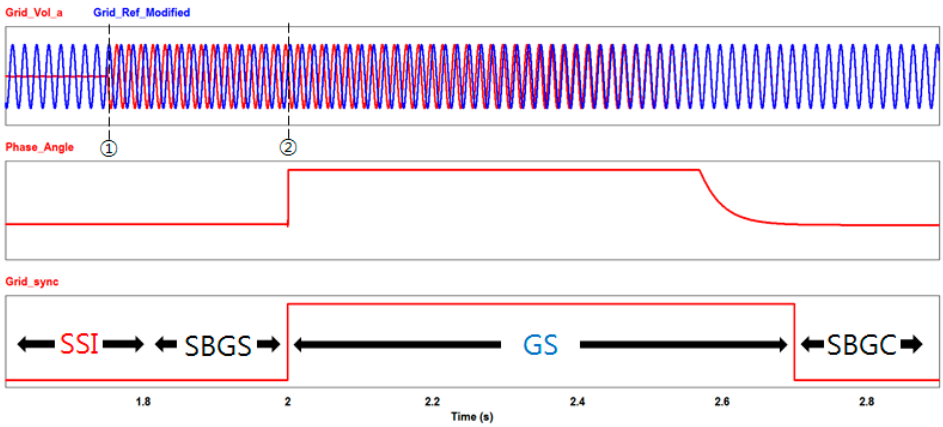


Figure 8. Ideal waveforms of grid synchronization mode (Top: Measured grid voltage and modified grid voltage. Mid: Phase angle during islanded mode. Bottom: GS status signal. ① Grid has been restored, and ② grid synchronization mode starts).

Figure 9 shows the block diagram of the proposed P+MR-based output voltage control scheme. As shown in this Figure, the mode selector toggling switch is much simpler than that in Figure 7. Unlike the previous method, the P+MR voltage controller is configured to operate during the whole islanded mode to cope with the unexpected load change adaptively. Under SSI, the rated voltage and frequency are assigned as the voltage reference value. As the grid is restored, the mode is changed from SSI to SBGS, but there is no change for control in this proposed method. Hence, it is no longer necessary to worry about the deterioration of the transient characteristic during the mode change. In the mode of GS, the phase angle of PLL is limited within the tuned threshold value, and the voltage

reference is generated with the modified angular frequency to change the voltage reference smoothly to the grid voltage for seamless grid synchronization. Figure 10 presents the detailed consideration for this compatibility between the cut-off frequency of quasi PR control and the min-max threshold values of the PLL limiter. As shown in this figure, the absolute gain at the operating frequency of 60 Hz, i.e., approximately 377 rad/s, is '2.56' when $\omega_{\_(1.cut)}$ is 6 rad/s. The absolute gains at 371 and 383 rad/s, which are ±6 rad/s of 377 rad/s, are all '1.81'. Here, this '1.81' is '$1/\sqrt{2}$' times as large as '2.56' because 371 and 383 rad/s are the threshold angular frequencies of the operating frequency due to the bandwidth using 6 rad/s $\omega_{\_(1.cut)}$ of quasi PR control. This means that only the signal between 371 and 383 rad/s is adoptable for stable control performance under the predesigned theoretical criteria. As shown in Figure 8, the phase angle of modified voltage reference can be gradually changed to the phase angle of grid voltage considering with operating frequency limit, which is compatible with the allowable frequency range of resonant controller. Therefore, it is possible to add the harmonics compensation terms of resonant controller in GS because the proper angular frequency threshold value is considered with the allowable control range of resonant controller and so the degradation of transient characteristic does not occur due to the smoothly changed voltage reference. After the phase tracking is complete, the grid voltage can be directly injected to the voltage reference by changing the toggle switch from GS to SBGC.

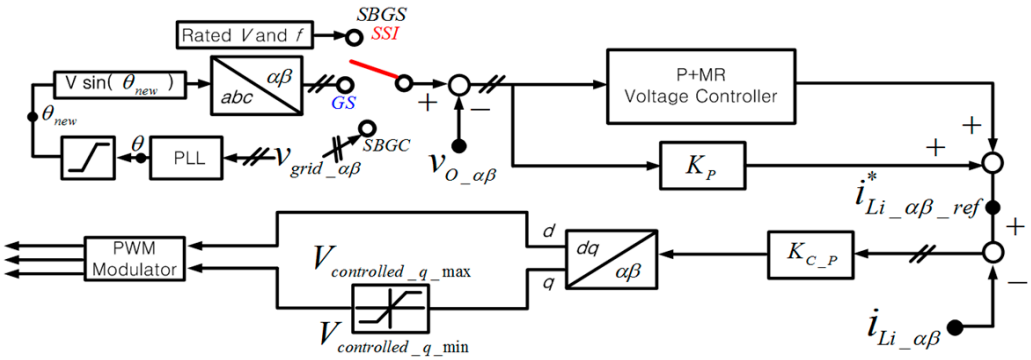


Figure 9. Block diagram of proposed P + MR based multi loop output voltage control scheme.

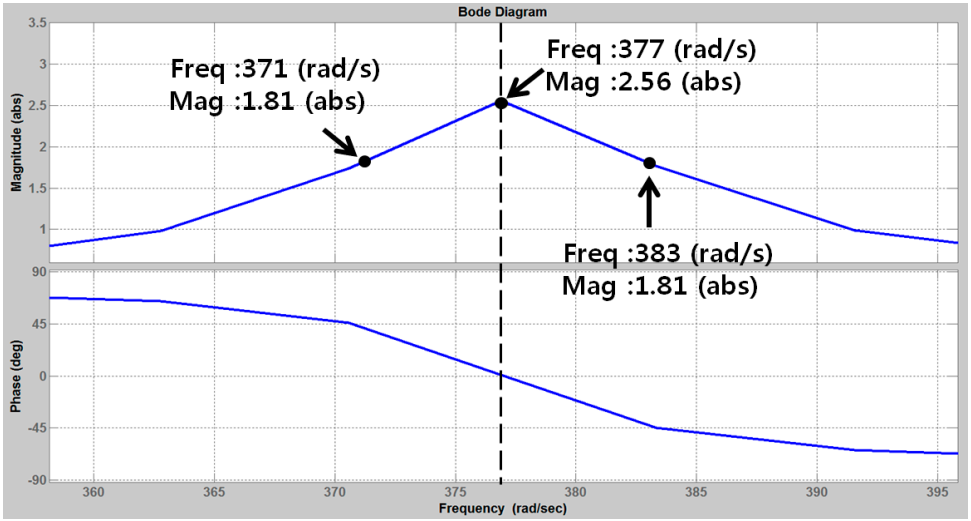


Figure 10. Consideration of the compatibility between the bandwidth of quasi PR control and min-max threshold values of the PLL limiter: Zoom in Bode plot of the quasi PR transfer function near the operating frequency.

In conclusion, this proposed method can realize the seamless mode transfer with harmonics compensation. Besides, it can respond adaptively to the frequent load changes as the P + MR voltage control output is enabled continuously during GS mode. It will be verified through the following case studies.

3.2. Case Study for Grid Synchronization

Four different cases of grid synchronization under the PR-based stationary reference frame were studied, and all cases were compared and evaluated through simulations and experiments for the transient characteristics, THD, grid synchronization speed, and implementation difficulty.

3.2.1. Case Study I

For Case study I, the linear resistive load was connected to the inverter, and the fixed dq variable technique-based grid synchronization method in Figure 7 is used. The outputs of both 5th and 7th harmonics resonant controller were fixed to '0' which has the same effect as removing the PR control. The significant error may occur when the GS mode starts, but the output voltage magnitude is transferred smoothly to the grid voltage with high synchronization speed because the output of fundamental resonant controller is fixed by the grid synchronization technique, as shown in Figure 7.

3.2.2. Case Study II

For Case study II, the inverter supplies a diode rectifier-type non-linear load instead of the linear resistive load in Case I. Therefore, 5th and 7th harmonic currents are inserted to the line, which degrades the inverter output voltage quality at the same time. The grid synchronization method in Figure 7 is still used, as in the Case study I, and both the 5th and 7th harmonics resonant controller outputs are also fixed to '0'. Therefore, the THD performance of controlled voltage will not be degraded even though the non-linear load connection does not affect the transient characteristic of grid synchronization.

3.2.3. Case Study III

For Case study III, the nonlinear load is used, as in Case study II. The grid synchronization method in Figure 7 is also used, but the 5th and 7th harmonic resonant controllers are enabled differently from Case II. Therefore, the outputs of the 5th and 7th harmonics resonant terms should not fixed as '0' anymore and become a part of the inner current reference. Especially for the simulation condition, after 0.05 s from starting the GS mode operation, the addition of load change event will be planned for 0.1 s. After 0.1 s, it is returned as the initial load value so that the fixed *d-q* axis variable technique in Figure 7 resulted in load voltage regulation mismatch due to the unexpected load changes.

3.2.4. Case Study IV

For Case study IV, the non-linear load is also connected, as in Case studies II and III, but the grid synchronization method in Figure 9 will be used instead of the fixed *d-q* variable technique in Figure 7. As mentioned in Section 3.1, the seamless grid synchronization can be realized using the smooth reference changing technique and PLL limiter selection considering the cut-off frequency, $\omega_{1.cut}$ of the quasi PR control. To evaluate the performance under load changes in simulation, after 0.5 s from the start of the GS mode operation, the load change event also occurs in common with the Case study III to analyze the positive effect by enabling the P+MR-based output voltage control loop for the GS mode through the proposed Case study IV. After grid synchronization is complete, the mode changes to the SBGC mode and the grid voltage is injected directly into the voltage reference to track the grid voltage directly.

4. Simulation Results

In this study, the performance of the controller for four cases is analyzed through a PSiM simulation as shown in Figures 11–15. The grid synchronization mode in all simulations begins at 1.8 s. Table 1 lists the simulation and experimental parameters in this paper.

Table 1. Simulation and Experimental Parameters.

Parameters		Value	Unit
Rated Active Power		500	W
DC Link Voltage		400	V
Rated Output Voltage		155	V_{peak}
Switching Frequency		5	kHz
Filter Capacitor, C_f		40 (Y)	μF
Inverter Side Inductor, L_i		3	mH
PR Control Gain	P gain of Voltage Controller (K_p)	0.0577	Ω^{-1}
	P gain of Current Controller(K_{c_p})	17.3	Ω
	Resonant Gain (1st)	30	Ω^{-1}
	Resonant Gain (5,7th)	20	Ω^{-1}
	Cut-off Frequency ($\omega_{1,5,7.cut}$)	6, 30, 42	rad/s

Figure 11 shows the simulation results in Case I. The grid is restored at 1.7 s and the grid synchronization is started from 1.8 s to track the phase of grid voltage. In this case, the linear local load is connected and the conventional fixed *d-q* variable technique in [11] is used to realize the seamless grid synchronization. As shown in this figure, it realizes the seamless grid synchronization performance with the fast synchronization speed. On the other hand, the voltage waveform is slightly distorted because the fixed *d-q* variable technique is applied which makes the output of fundamental frequency resonant controller disabled.

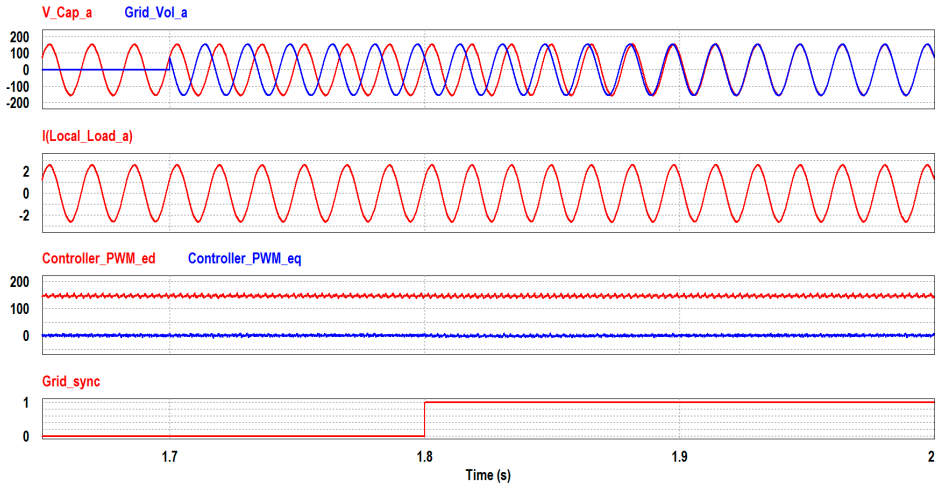


Figure 11. Simulation results in Case I. (SBGS ⟶ GS Mode) (From top to bottom: Measured *a*-phase inverter output voltage and grid voltage, *a*-phase local load current, PWM *d-q* controller outputs, and GS status signal).

Figure 12 shows the simulation results in Case II. The local linear load is only replaced by the rectifier type of non-linear load for Case I. As shown in this figure, the seamless grid synchronization can be realized quickly, but the voltage waveform is much more distorted by the harmonic currents generated from the non-linear load. It is because the fixed *d-q* variable technique in [11] does not include any fixed harmonic component prediction. This fixed harmonic component prediction is

much more complicated than only using the fixed fundamental frequency component prediction. Even though the fixed *d-q* variable prediction for harmonic component is added, it cannot cope with the frequent load changes due to the use of fixed controller parameter value for assigning the inner inductor side current reference.

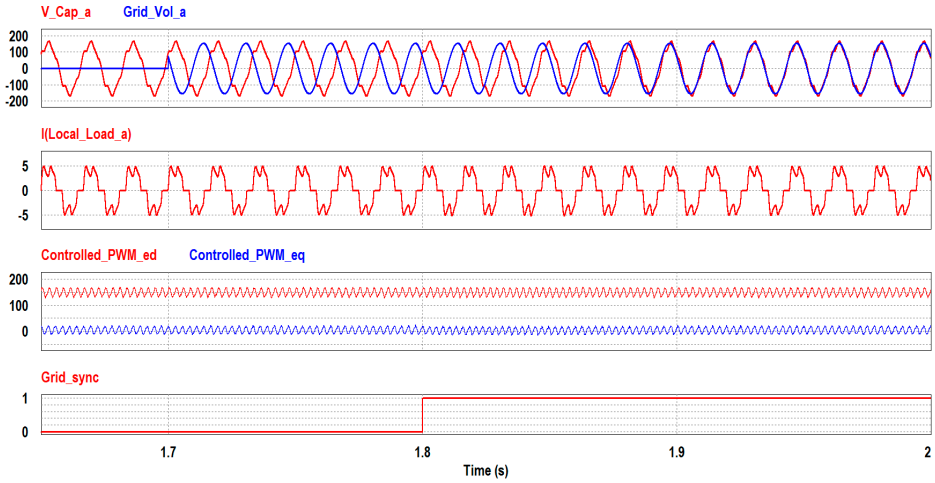


Figure 12. Simulation results in Case II. (SBGS ⟶ GS Mode) (From top to bottom: Measured a phase inverter output voltage and grid voltage, phase local load current, PWM *d-q* controller outputs, and GS status signal).

Figure 13 shows the simulation results of Case III. The harmonic compensation for 5th and 7th harmonics is applied to the fixed *d-q* variable technique instead of the fixed *d-q* variable prediction for 5th and 7th to solve the above-mentioned problem under the load change. As shown in this figure, the output voltage waveform is more improved than that of Case II due to the harmonic compensation. However, the transient characteristics of both waveforms of the output voltage and current are worse than that of Case II. This is because the significant voltage control error caused by the large phase difference between the grid voltage and the load voltage cannot be compatible with the allowable control range of voltage resonant control as mentioned in Figure 9.

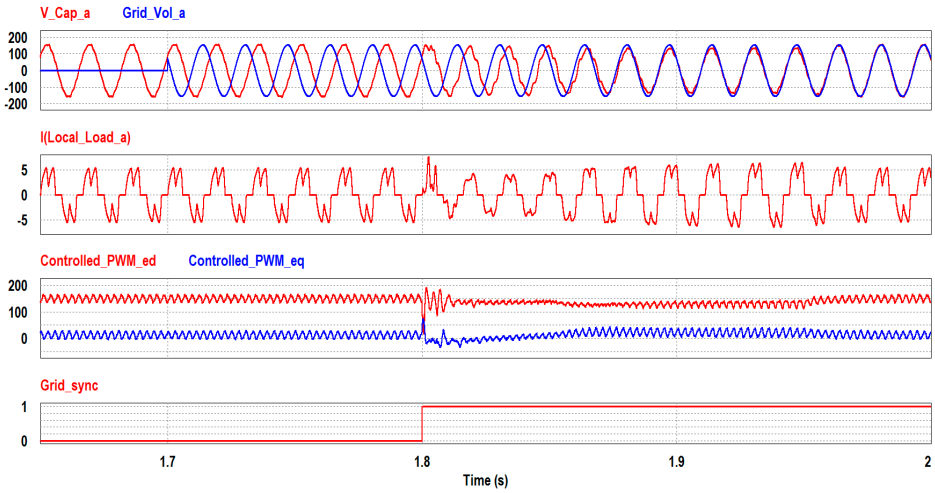


Figure 13. Simulation results in Case III. (SBGS ⟶ GS Mode) (From top to bottom: Measured *a*-phase inverter output voltage and grid voltage, *a*-phase local load current, PWM *d-q* controller outputs, and GS status signal).

Figure 14 shows the simulation results in Case IV. The instantaneous angular frequency of PLL is limited for the smooth change of voltage reference during the grid synchronization. As shown in this figure, its synchronization speed is three or four times slower than that of other cases although the seamless grid synchronization is realized with good THD performance. Nevertheless, the stability is improved with the limited angular frequency, 383 rad/s, which was chosen after considering the 6 rad/s cut-off frequency of the quasi resonant control, $\omega_{n.cut}$. However, the high speed grid synchronization is not always preferred because it can affect the poor influence to the local load due to the unrated high operating frequency.

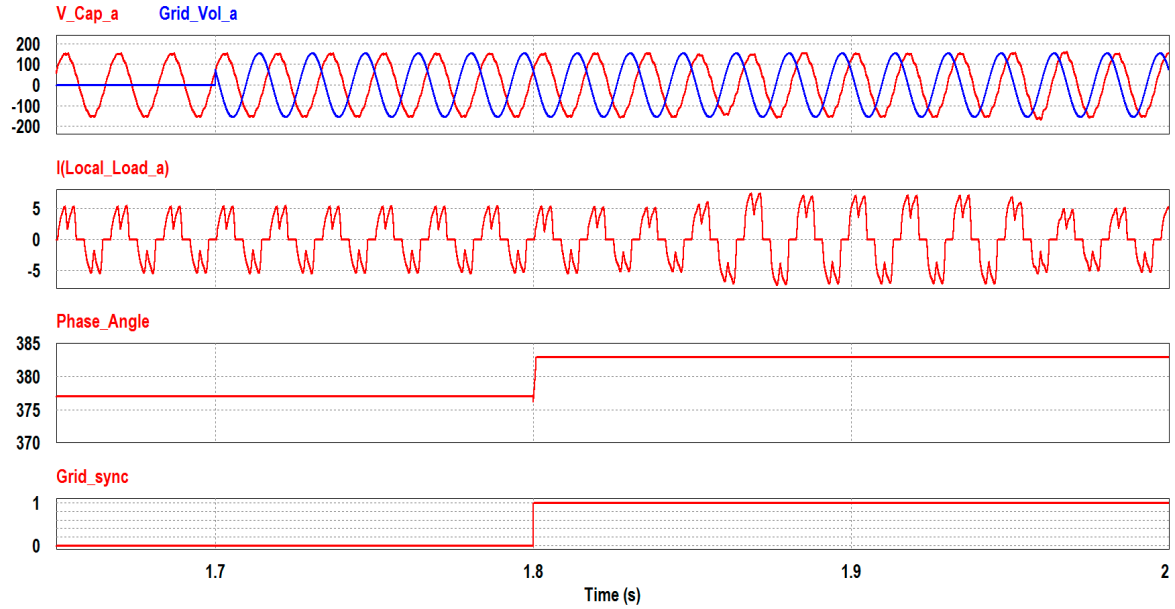
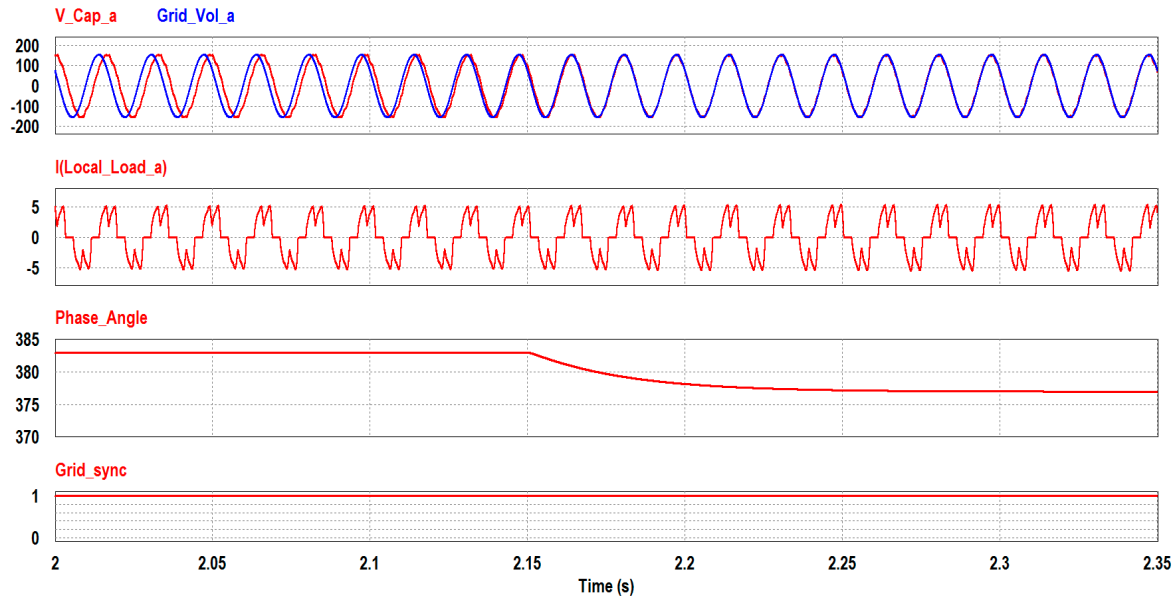
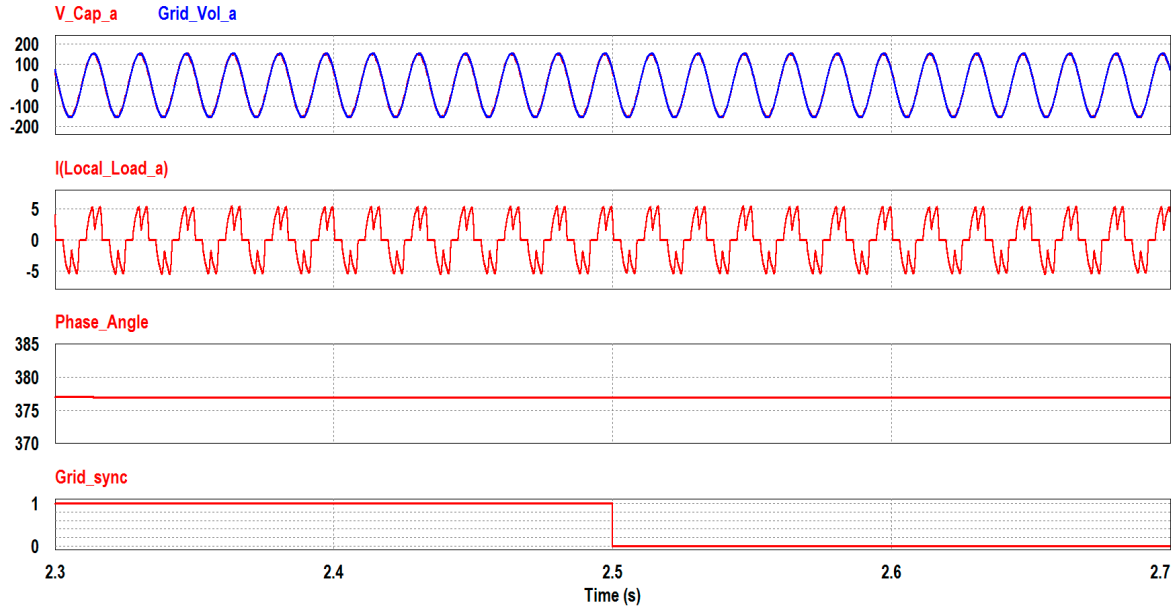


Figure 14. Simulation results in Case IV. (SBGS ⟶ GS Mode) (From top to bottom: Measured *a*-phase inverter output voltage and grid voltage, *a*-phase local load current, instantaneous angular frequency of output voltage, and GS status signal).



(**a**)

Figure 15. *Cont.*



(**b**)

Figure 15. Simulation results when mode changes from GS to SBGC in Case IV: (**a**) Grid synchronization, (**b**) mode change from GS to SBGC. (From top to bottom: Measured *a*-phase inverter output voltage and grid voltage, *a*-phase local load current, instantaneous angular frequency of output voltage, and GS status signal).

Figure 15 shows the simulation results when the mode changed from GS to SBGC in Case IV. In this sequence change, the instantaneous angular frequency is applied to the current grid voltage directly. The output voltage and load current were kept stable without any transients when the inverter begins to be operated under SBGC mode at 2.5 s. When the grid synchronization starts, the worst case is to be '180°' phase angle difference between the grid voltage and the load voltage, so it could be synchronized within approximately 0.5235 s under 6 rad/s limitation of the PLL output. Therefore, the period of GS mode is determined to be '0.7 s' considering the unexpected factor for phase matching in the simulation and experiment.

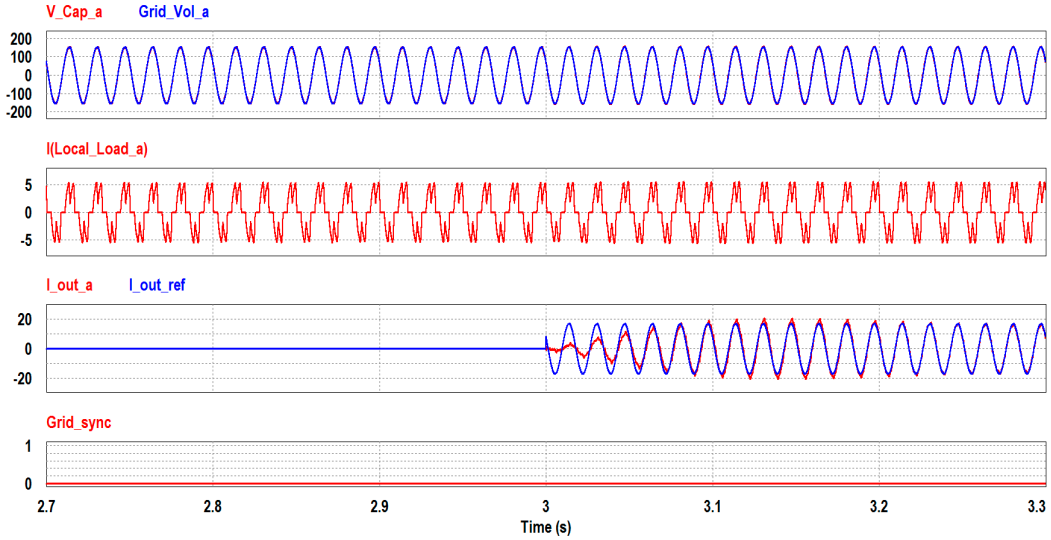


Figure 16. Simulation results when the mode changes from SBGC to GC (Grid Connected mode) in Case IV. (From top to bottom: Measured *a*-phase inverter output voltage and grid voltage, *a*-phase local load current, grid current, and GS status signal).

Figure 16 shows the simulation results when the mode changed from SBGC to GC in Case IV. At 3 s, the mode is changed from SBGC to GC by turning on the static switch between the main grid and the inverter filter capacitor. The reference grid current, I_{out_ref}, is increased with the rated current reference magnitude as 17 A. Here, the grid current control loop is added to the predesigned output voltage loop as an outer loop to accomplish the indirect current control, which can make the seamless mode transfer possible between the grid-connected and islanded mode. As shown in this figure, the seamless mode transfer to the grid connected mode is realized with maintaining the good dynamic performance for harmonic compensation.

Figure 17 shows the simulation results without and with resonant harmonic compensation under SSI, respectively. The THD is improved from 8% to 2.7% when the harmonic compensation is enabled with the rated frequency under SSI.

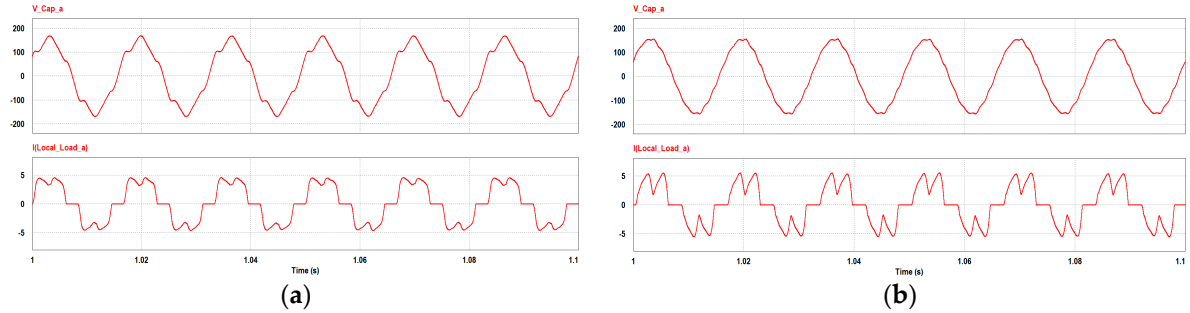


Figure 17. Simulation results during SSI mode: (**a**) Without harmonic compensation; **(b)** with harmonic compensation. (From top to bottom: Measured *a*-phase inverter output voltage, *a*-phase local load current, instantaneous angular frequency of output voltage, and GS status signal).

5. Experimental Results

Figure 18 shows the configuration of the experimental setup. The parameters are same as those used in the simulation as shown in Table 1. The inverter is connected to the grid through the LCL filter and the rectifier type of non-linear load is installed at the filter output capacitor. The control system is implemented by TMS320f28335digital signal processor. The output load voltage, V_o, the inverter side inductor current, I_L, and the grid voltage, V_g, are measured as the feedback variables of DSP controller for the operation of islanded mode.

Figure 19 shows the experimental results in SSI mode without or with harmonic compensation to evaluate the harmonic compensation performance of well-designed quasi P + MR control. The 5th and 7th harmonics are reduced considerably, and the THD performance is improved from 7.3% to 2.9%. It is similar aspect with the simulation results in Figure 17 of which THDs are 8% and 2.7% under SSI mode, respectively.

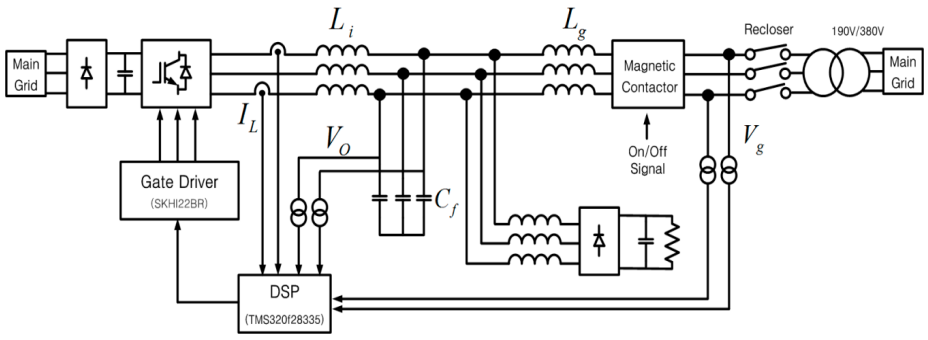
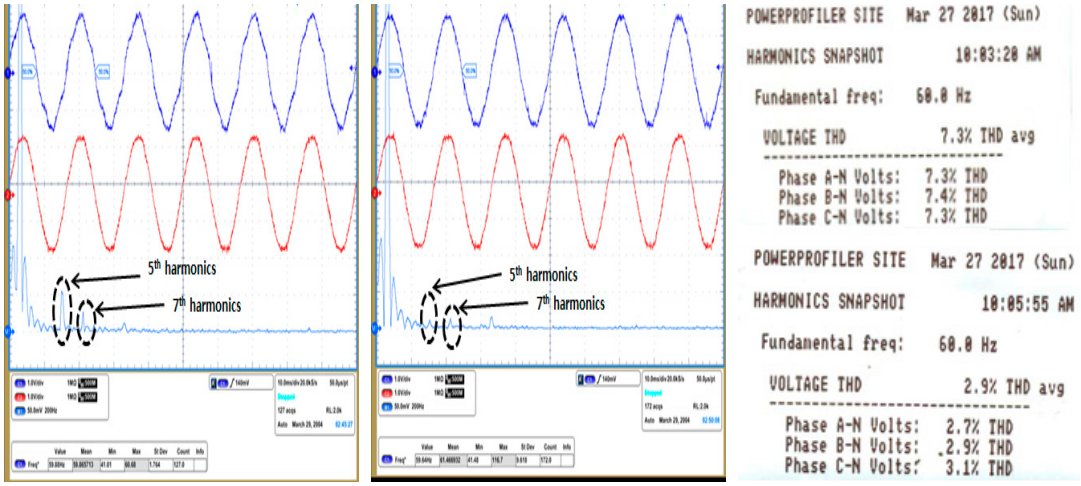


Figure 18. Configuration of experimental setup.



(**a**) (**b**) (**c**)

Figure 19. Experimental results: (**a**) without harmonic compensation; (**b**) with harmonic compensation, (From top to bottom: measured *a*-phase inverter output voltage and grid voltage, and FFT of the inverter output voltage); and (**c**) THD analyses.

Figure 20 shows the experimental results in Case I. The linear local load is connected and the conventional fixed *d*-*q* axis variable technique is applied to realize the seamless grid synchronization. With the grid synchronization signal, the seamless grid synchronization is realized with the conventional fixed *d*-*q* axis variable technique in three cycles. The load voltage waveform is good enough as far as the linear local load is connected.

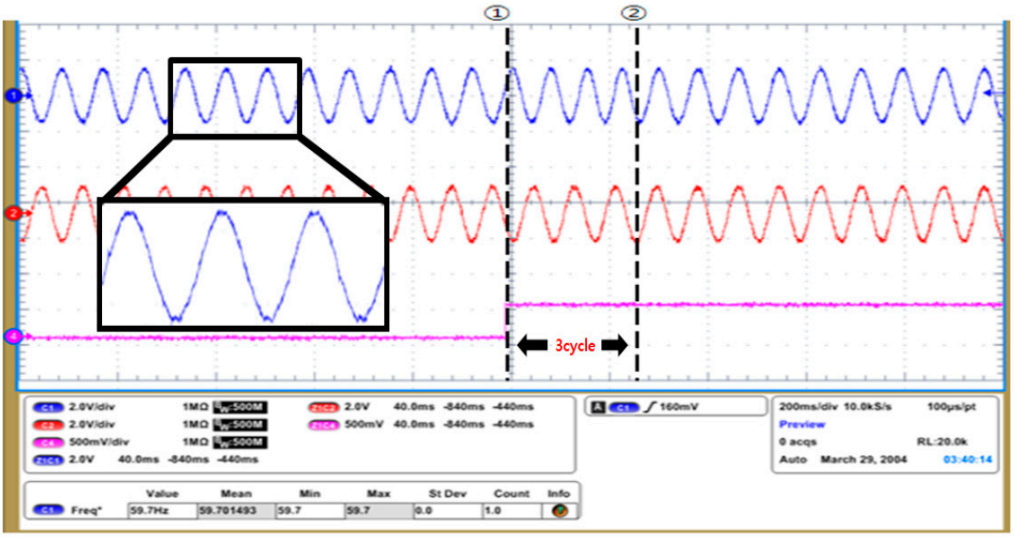


Figure 20. Experimental results in Case I (SBGS ⟶ GS Mode). (From top to bottom: Measured *a*-phase inverter output voltage and grid voltage (200 V/div), and GS status signal (0 or 1)) (①: starting point of synchronization. ②: finalized point of synchronization).

Figure 21 shows the experimental results of Case II. The local linear load is only replaced by the rectifier type of non-linear load under the fixed *d*-*q* axis variable technique. As shown in this figure, the load voltage waveform is distorted by the current harmonics, because the fixed *d*-*q* variable technique is applied without additional harmonics compensation term in spite of the non-linear load. However, the seamless grid synchronization can be realized with the fast synchronization speed.

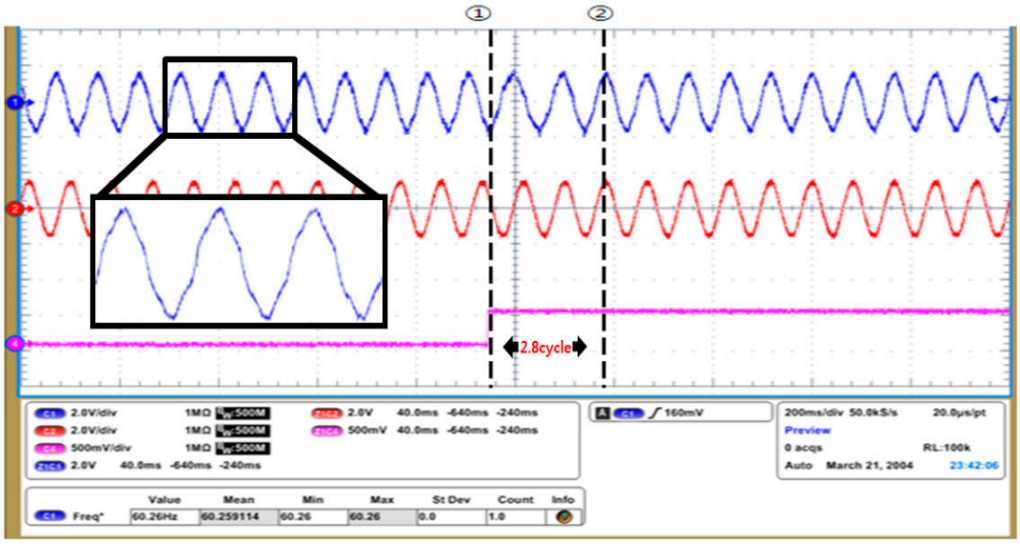


Figure 21. Experimental results in Case II. (SBGS⟶GS Mode) (From top to bottom: Measured *a*-phase inverter output voltage and grid voltage (200 V/div), and GS status signal (0 or 1)), (①: starting point of synchronization. ②: finalized point of synchronization).

Figure 22 shows the experimental results of Case III. Here, 5th and 7th harmonic compensation terms are added to the conventional fixed *d-q* variable technique under the whole islanded mode operation which consists of SSI, SBGS, GS, and SBGC modes. As shown in this figure, the waveform of load voltage is improved due to the addition of harmonics compensation term. However, the transient characteristics are degraded, because the added 5th and 7th resonant controllers can be affected by the significant voltage error in the controller due to the unexpected large phase differences between the grid voltage and the current load voltage. This can be improved by applying the limitation method of angular frequency in PLL, but it still cannot cope with the frequent load change t as mentioned in Figure 13.

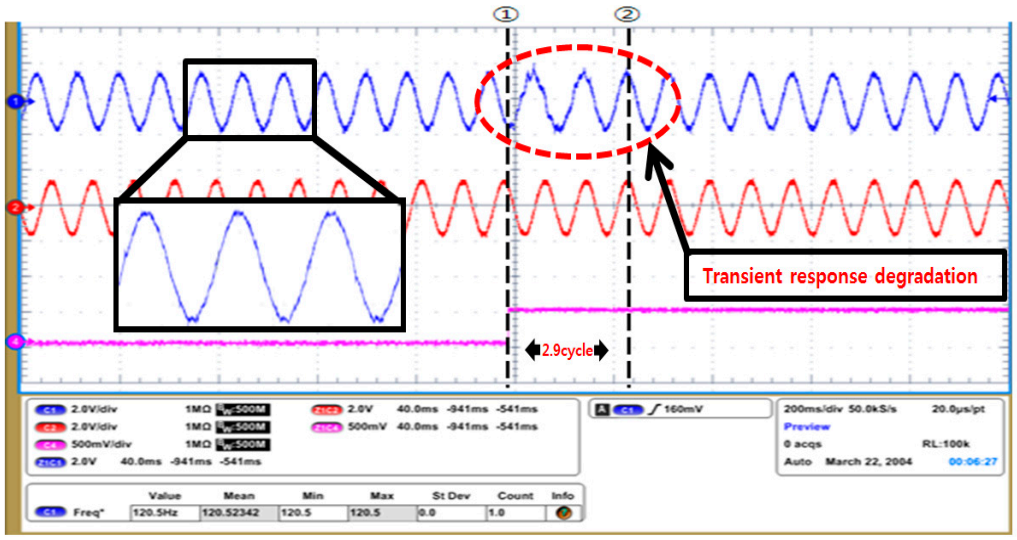


Figure 22. Experimental results in Case III. (SBGS⟶GS Mode) (From top to bottom: Measured *a*-phase inverter output voltage and grid voltage (200 V/div), GS status signal (0 or 1)), (①: starting point of synchronization. ②: finalized point of synchronization).

The experimental results of Case IV with the proposed method are shown in Figure 23. The synchronization speed is lower than those of other cases, but it realizes the seamless grid synchronization without any degradation of the transient response and the low THD performance despite the non-linear load connection. Although the synchronization speed is slower than that of Case III, it is still within the satisfactory level practically considering the recommended slew rate of UPS, 6 Hz/s.

Figure 24 shows the experimental results when the mode changes from GS to SBGC in Case IV. As shown Figure 9, the mode can be transferred simply by toggling the control switch. As shown in this figure, there is no transient during the mode changes from GS to SBGC because the phase difference between the grid voltage and the current load voltage has been already reduced by the proposed grid synchronization technique.

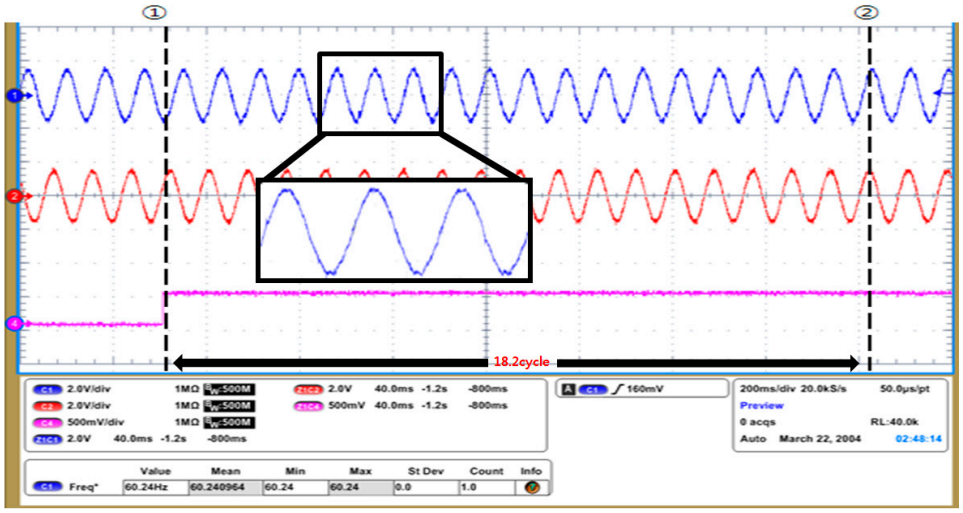


Figure 23. Experimental results in Case IV. (SBGS⟶GS Mode) (From top to bottom: Measured *a*-phase inverter output voltage and grid voltage (200 V/div), and status signal (0 or 1)), (①: starting point of synchronization. ②: finalized point of synchronization).

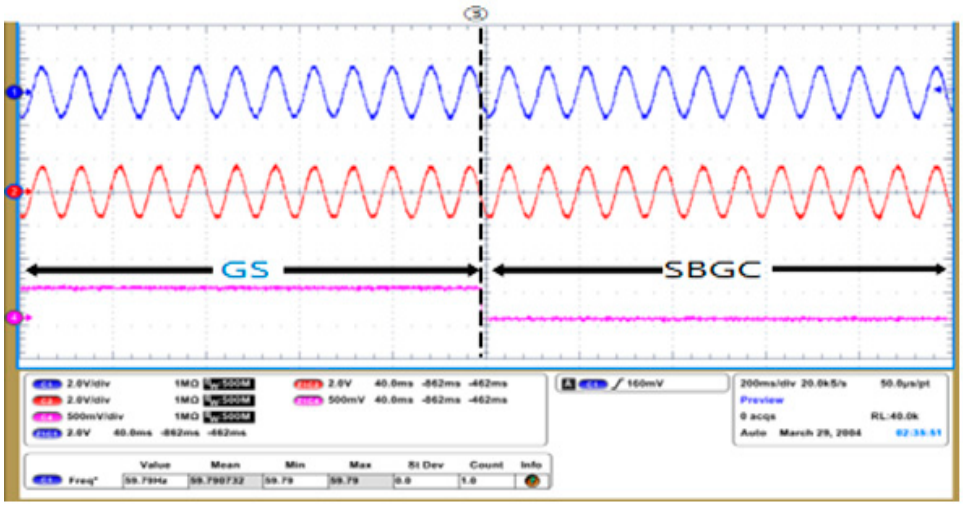


Figure 24. Experimental results when the mode changes from GS to SBGC in Case IV. (From top to bottom: Measured *a*-phase inverter output voltage and grid voltage (200 V/div), and GS status signal (0 or 1)), (③: GS mode complete).

Table 2 shows the summary of the case study results from the simulation and experiment. As shown in this table, the proposed control algorithm is well verified to meet the performance for THD and transient response with an acceptable synchronization speed.

Table 2. Summary of results from the simulation and experiment.

Performance Features	Linear Local Load	Non-Linear Local Load		
	Case I	**Case II**	**Case III**	**Case IV**
Control Scheme	Same as Figure 7	Same as Figure 7	Figure 3 with enabling 5th & 7th resonant terms	Same as Figure 9
Quality of Transient Dynamic	Good	Good	Bad	Good
Synchronization Speed	Fast	Fast	Fast	Slightly Inferior
THD Performance	Slightly inferior	Bad	Slightly inferior	Good
Difficulties of Implementation	Little complex	Little complex	Little complex	Easier than other cases

6. Conclusions

This paper proposes the grid synchronization method of inverter using a quasi P+MR-based multi loop voltage controller under a stationary reference frame. The inverter supplies a non-linear load under the islanded mode. This proposed method can realize the seamless mode transfer with harmonics compensation considering the compatibility with allowable frequency range of resonant control. Besides, it can respond adaptively to the frequent load changes as the P+MR voltage control output is enabled continuously during the grid synchronization period. And also, the above results can be achieved without any high performance of PLL by using the stationary reference frame. It will be verified through the following case studies. Finally, the proposed grid synchronization method is verified through the PSiM simulations and laboratory-scaled experimental results for four different case studies.

In order to realize the overall seamless mode transfer under both grid-connected and islanded mode, this proposed quasi P+MR based voltage controller can be extended to the indirect current control by adding the grid current loop as an outer loop for further research. In addition, the cut off frequency design of quasi resonant controller is also to be investigated to cope with unexpected frequency change under the weak grid condition.

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Author Contributions: Kyungbae Lim designed the study, implemented the simulations and experiments. Jaeho Choi advised the data analyses and edited the manuscript.

Conflicts of Interest: The authors declare no conflict of interest.

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