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A New Successive Time Balancing Time-to-Digital Conversion Method

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Abstract: This paper presents a new self-clocked time-to-digital conversion method based on a binary successive approximation (SA) algorithm. Its novelty consists in combining fully clockless operation with direct conversion of the measured time interval. The lack of any reference clock makes the presented method potentially predisposed to low-power solutions. Furthermore, its circuit representation is extremely simple, thereby the ability to direct conversion of time intervals is not burdened by a significant amount of components. The method is intended to measure relatively long time intervals, i.e., hundreds of microseconds. Therefore, it is suitable for e.g., biomedical applications using time-mode signal processing.

Keywords: successive approximation; analog-to-digital conversion; asynchronous time-to-digital conversion; self-clocked method; clockless circuit

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1. Introduction

One of the key requirements for modern systems is minimizing energy consumption (low-power electronics). This factor is especially important in systems such as biomedical applications, environmental sensor networks, or commercial mobile devices [1–5]. Regardless of this tendency, since the beginning of the CMOS technology development, the aim has always been to increase the efficiency of the systems by reducing the size of the transistors. For decades, the combination of these two above-mentioned trends has caused the necessity of the gradual supply voltage reduction [6,7].

Digital electronics benefit from the CMOS technological improvements in terms of die area and switching speed [6–11]. On the other hand, unfortunately, analog circuit design becomes more and more challenging, because aggressively decreasing voltage headroom and declining transistor threshold voltage deteriorate the signal-to-noise ratio [9–11]. This is relevant issue, for instance, for what concerns the dynamic range of analog-to-digital converters (ADCs) [9]. Assuming the same number of bits, a lower power supply means a smaller voltage range per bit.

In reference to this issue, in the last several years, alternative methods of signal processing were proposed, such as time-mode signal processing (TMSP) [6,10,11]. In this technique, instead of processing the information in the conventional, vertical form (voltage domain), the operations are handled horizontally (time domain) using variable time intervals.

Analog-to-digital conversion using TMSP can be achieved by relatively simple two-stage action (Figure 1). Firstly, by encoding the voltage values x(t) into time intervals y(t), and secondly, by converting them to the appropriate digital words z(t). The migration from the voltage domain to the time domain can be performed, for example, by the time encoding machine (TEM) or the level-crossing sampling technique [12–16]. Such an approach transforms the analog signal to a quasi-digital waveform (voltage quantization, time-length variability) which not only eliminates the shrinking headroom voltage problem, but also

provides resistance to undesirable noise and distortion [6,7]. The time intervals generated in this way are then converted to digital words using a time-to-digital converter (TDC).

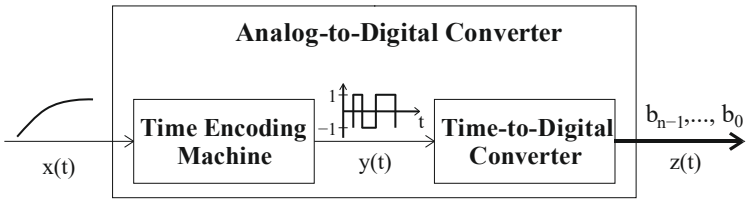

Figure 1. Analog-to-digital conversion implemented using TMSP.

Depending on the target application, the parameters of both TEMs and TDCs must be carefully chosen to meet specific requirements imposed by the signals that occur in the system. The TEM can be implemented in a few different ways, i.e., as an Asynchronous Sigma-Delta Modulator (ASDM) or as a Spiking Neuron (SN) circuit [17–23]. A characteristic feature of all TEMs is that they are fully-asynchronous analog circuits designed with an extremely low number of components. It directly translates into advantages such as the low power consumption and the low occupied area, making the TEMs suitable for sensor systems, i.e., pixels of event-based vision cameras [9,24]. However, contrary to the asynchronous operation of TEMs, the conventional TDC solutions require a reference clock which is used for the measurement itself, for the control operations, or both [25,26]. Unfortunately, this is one of the main factors contributing to power consumption [6,12]. For some applications where low-power operation is a crucial design factor, eliminating the clock signal may significantly reduce the energy demand. Therefore, the fully asynchronous time conversion method, which is described in this paper, is suitable for such low-power applications [27,28]. Additionally, it solves the direct conversion problem in the time domain which is described below.

Because of its irreversibility, time does not fit the typical conversion methods commonly used in the voltage domain. A specific moment of an ongoing time interval cannot be directly restored in the same manner as the voltage (current, charge, etc.), which can be decreased, because it is impossible to turn back time. In reference to this issue, preconversion-based time-processing methods are commonly used [10,28–30]. They include the prior conversion of the measured time interval to different, decremental physical quantities (i.e., charge), which is then converted to the right digital word. Unfortunately, the preconversion itself is associated, i.a., with the use of additional elements, increased energy consumption, and obviously with additional measurement errors which leads to increased uncertainty of the final result.

The time-to-digital conversion method presented in this paper is based on the binary successive approximation variant which allows converting the time intervals directly, so it is preconversion-free by default [27,28]. In general, there are three binary successive approximation (SA) variants that are adopted in the analog-to-digital conversion: Oscillating Successive Approximation (OSA), Monotonic Successive Approximation (MSA), and Full–Scale Monotonic Successive Approximation (FSMSA) [31]. Each of them has specific properties that are particularly manifested in the issue of direct conversion of time.

The first one—OSA—does not allow for direct time conversion [31]. In this approach, a reference equivalent R of the measured input value S is created (e.g., time interval), based on which the output bits are evaluated (Figure 2a). The equivalent R is created with the use of predetermined binary-scaled reference elements. At each step, the equivalent R is compared to the measured input value S and, based on the result, an appropriate bit is evaluated. If the equivalent is smaller than the measured input value ($R < S$), the currently tested bit is set to one and the equivalent R is increased by adding the next reference element to it. Otherwise ($R > S$), the bit is set to zero and the equivalent is decreased by replacing the most recently added reference element with a smaller one. The above operations cause the measured input value to be approximated alternatively, upwards and downwards, causing

an oscillatory character (OSA) [31,32]. The necessary reduction of the equivalent R in case of overestimation (R > S) makes the OSA inapplicable as a direct time conversion approach. This is due to the fact that in time conversion the reference elements are time intervals. If the time corresponding to the reference time interval (reference element) has elapsed, it is impossible to return to the moment when the reference time interval started measuring time [31]. This time interval has passed and cannot be turned back in the same way as the voltage or charge can be decreased. Despite this disadvantage, the OSA is by far the most commonly used successive approximation variant and by this, often mistakenly considered to be the only one.

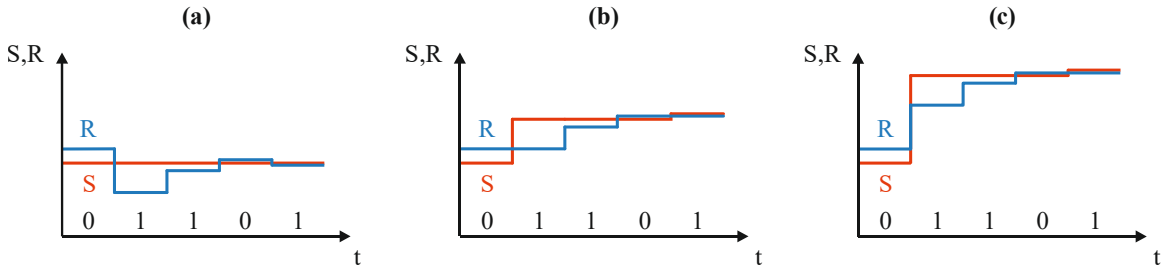

Figure 2. Exemplary waveforms of the successive approximation algorithms: (**a**) Oscillating Successive Approximation (OSA); (**b**) Monotonic Successive Approximation; (**c**) Full-Scale Monotonic Successive Approximation.

The alternative variant—MSA—has the ability to perform direct conversion of time [31,32]. In this algorithm, the output bits are evaluated based on the successive balancing of the input value S by the binary-scaled reference elements (Figure 2b). In the first step, the measured input value S is compared to the reference R which is equal to the biggest reference element. At each next step, the subsequent reference element is added to this value (S or R) which currently is smaller. In this algorithm, no matter the relationship between the signal S and the reference R values, the compensation is always handled by the addition operation [31]. Thus, the direct time conversion can be successfully implemented using MSA, since the reference elements removal operations (time returning operation) do not occur.

The FSMSA variant also has the ability to produce a direct time conversion, but in comparison to the MSA, it requires twice the number of reference elements—one set for the value R and one for the value S [31,33]. In this case, the digital equivalent of the value S is evaluated on the basis of successive comparisons with monotonically increasing reference value R. The reference value R growth pattern is always the same, regardless of the measured value S. It is created by adding subsequent reference elements at each step of the conversion process. If the value S is smaller than the value R, the overestimation is compensated by adding an identical reference element to the value S that caused the overestimation. After that, the relationship between the values S and R changes and the value S is again greater than the value R [31]. The bit evaluation in this case is similar to the OSA and the MSA. If the value S is smaller than the value R, the bit is set to 0. Otherwise, the bit is set to 1. The FSMSA is rarely applied. One of its few examples of use is [33].

The necessity of using additional reference elements for value S leads to increased energy consumption, making the FSMSA relatively inefficient. This is the second reason (aside from the direct time conversion capability) why the time conversion method presented in this paper is based on the MSA variant rather than the others. It has been named Successive Time Balancing Time-to-Digital Conversion (STB-TDC).

In this paper, the STB-TDC technique is described, with a particular emphasis on time irreversibility. Firstly, a simplified, intuitive model is introduced. It shows how the proposed time conversion method handles the problem of inevitable timelapse. The inherent property of time is its natural, continuous lapse. Neither reversal, stoppage, nor prediction of the measured time interval length is possible. Thus, in direct time conversion,

the adopted method has to provide information about the current length of the measured time interval at every moment during the conversion. Only then is the method capable of making correct decisions without any intervening delays which are a source of the additional error. Considering this fact, the continuous timelapse phenomenon must be accurately reflected during the direct time conversion process. The STB-TDC method is based on the well-known SA variant (Monotonic Successive Approximation). Nevertheless, the way it handles the continuous lapse of time is unique and by this it is necessary to describe [27,28]. After this introduction, the circuit representation of the STB-TDC is described along with the processing method relating to the specific elements. Next, the simulation results of the ideal STB-TDC circuit are presented. Finally, the physical implementation of the Successive Time Balancing time-to-digital converter using UMC 0.18 µm technology is presented. The ideal model and the layout implementation are designed using Cadence Virtuoso EDA with the preliminary assumptions imposed in advance by the target technology.

2. Idea of the Successive Time Balancing Method

The STB-TDC conversion scheme, as well as the bits evaluation, can be accurately illustrated as a building process of two columns: the signal column *S* and the reference column *R*.

The building components are limited to a single set of n binary-scaled, empty reference tanks $C_{n-1}, \ldots, C_0$ (in real circuits these are capacitors). The capacities of the reference tanks are defined as $C_k = 2^k C_0$, for $k = 0, \ldots, n-1$. In any other consideration, the reference tanks are identical.

The columns S and R are constructed by appropriately stacking the reference tanks $C_{n-1}, \ldots, C_0$, one on top of another. For every column-building process, the reference tanks are used in the same descending order, starting from the biggest one, C_{n-1}.

Each column has assigned a pump (current source) of constant and equal throughput: I_S and I_R, for the signal column S and the reference column R, respectively (Figure 3). The pumps I_S and I_R are used to uniformly (constant throughput) fill the subsequent reference tanks with liquid (charge), one after another. Thus, the time required to fill the k-th tank C_k is always proportional to its capacity C_k.

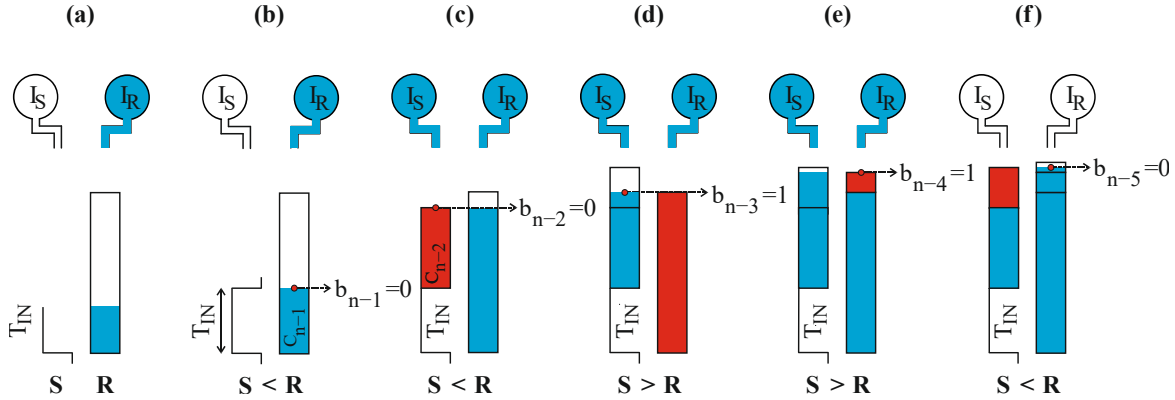

Figure 3. STB-TDC method conversion steps: (**a**) the initial step of the column R building; (**b**,**c**) the initial step of the column S building; (**c**,**d**) adding subsequent tank to the column S; (**d**,**e**) adding subsequent tank to the column R; (**f**) finished conversion process.

The conversion process begins with the occurrence of the front edge of the measured pulse T_{IN}. At the same moment, the building process of the reference column R begins (Figure 3a). Firstly, the biggest tank C_{n-1} is placed on the column R. Simultaneously, the pump I_R is turned on to start filling the biggest tank C_{n-1} with a constant flow rate. The rising liquid level reflects the timelapse of the constantly increasing time interval T_{IN}.

The building process of the signal column S starts when the rear edge of the time interval T_{IN} appears (Figure 3b,c). Similarly to the building process of the column R, at that moment the biggest reference tank C_k from the empty ones is used (in this example C_{n-2}). However, it is placed at the height equal to the length of the time interval T_{IN}. Instantly after that, the signal pump I_S starts filling the newly connected reference tank C_k with a constant flow rate.

All next steps of the conversion process are designated by the moments in time when the filling process of any reference tank is finished. In these moments, two crucial conversion operations are made. Firstly, the appropriate bit is evaluated (corresponding to the specific tank), and secondly, the decision about adding the subsequent, still unused reference tank is made. Following the above, evaluation of the bits $b_{n-1}, \ldots, b_0$ can be described as follows:

- If the tank C_k has been attached to the column S and during its filling process, the filling of a new tank on the (opposite) column R was started, the bit b_k is set to logic one: $b_k = 1$ (Figure 3d).
- If the tank C_k has been attached to the column R and during its filling process, the filling of a new tank on the (opposite) column *S* was not started, the bit b_k is set to logic one: $b_k = 1$ (Figure 3e).
- In any other case, the bit b_k is set to logic zero: $b_k = 0$ (Figure 3b,c,f).

The above operations are repeated until the moment when, after filling the tank C_k, there are no empty ones left that could be used to extend the column (S or R) height (Figure 3f). In the case of the reference tank C_0, the bit b_0 is evaluated as if there were another reference tank, C_{-1}, which would start filling at the moment when the filling of the reference tank C_0 is finished (Figure 3f).

By looking at the conversion process results statically (omitting the filling), it can be noted that the T_{IN} can be treated as a tank of an initially unknown height. From that perspective, it is successively approximated with the use of preliminary defined reference tanks $C_{n-1}, \ldots, C_0$ in a similar way as an unknown voltage is determined with a set of voltage references in conventional successive approximation ADCs. In addition, the heights of the columns S and R are equal with the accuracy of C_0. Because of that, the measured time interval T_{IN} can be evaluated as the difference of the reference elements accumulated on each column.

What is also clearly visible here is the applied variant of the binary successive approximation method (Monotonic Successive Approximation) and its properties [31]. During the conversion process, there is no situation in which it would be necessary to remove any reference tank C_k (i.e., subtract reference time interval). This property fits the direct time conversion very well because turning back on time is obviously impossible.

3. The STB Time-to-Digital Converter Circuit

Described in the previous section, the column-building model illustrates how the STB-TDC method handles the phenomenon of an inherent and continuous timelapse. However, the model does not present the second greatest advantage of the STB-TDC which is fully asynchronous, self-clocked conversion. In order to show how the particular subcircuits cooperate with each other without any reference clock, it is necessary to migrate from the simplified model to the circuit implementation.

3.1. General Architecture of the STB-TDC

The conversion flow diagram and the complete schematic diagram of the STB time-to-digital converter are presented in Figures 4 and 5, respectively. The fundamental building blocks are: one set of binary-scaled capacitors $C_{n-1}, \ldots, C_0$, two current sources I_R, I_S, two comparators K_R, K_S, a reference voltage source V_{REF}, a set of analog switches units $SW_{n-1}, \ldots, SW_0$ and an asynchronous state machine ASM, which controls the operation of the entire converter (Figure 5).

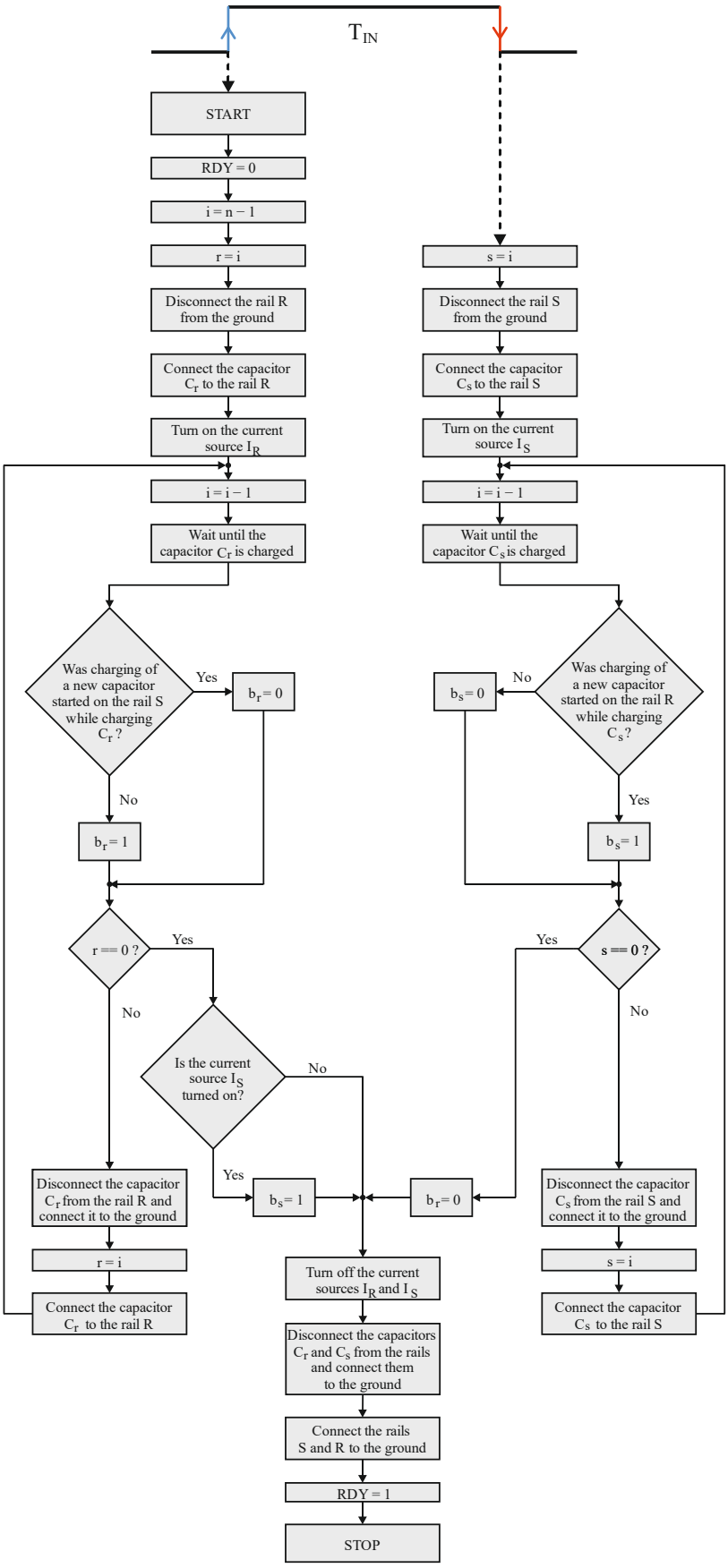

Figure 4. The flow diagram of the Asynchronous State Machine.

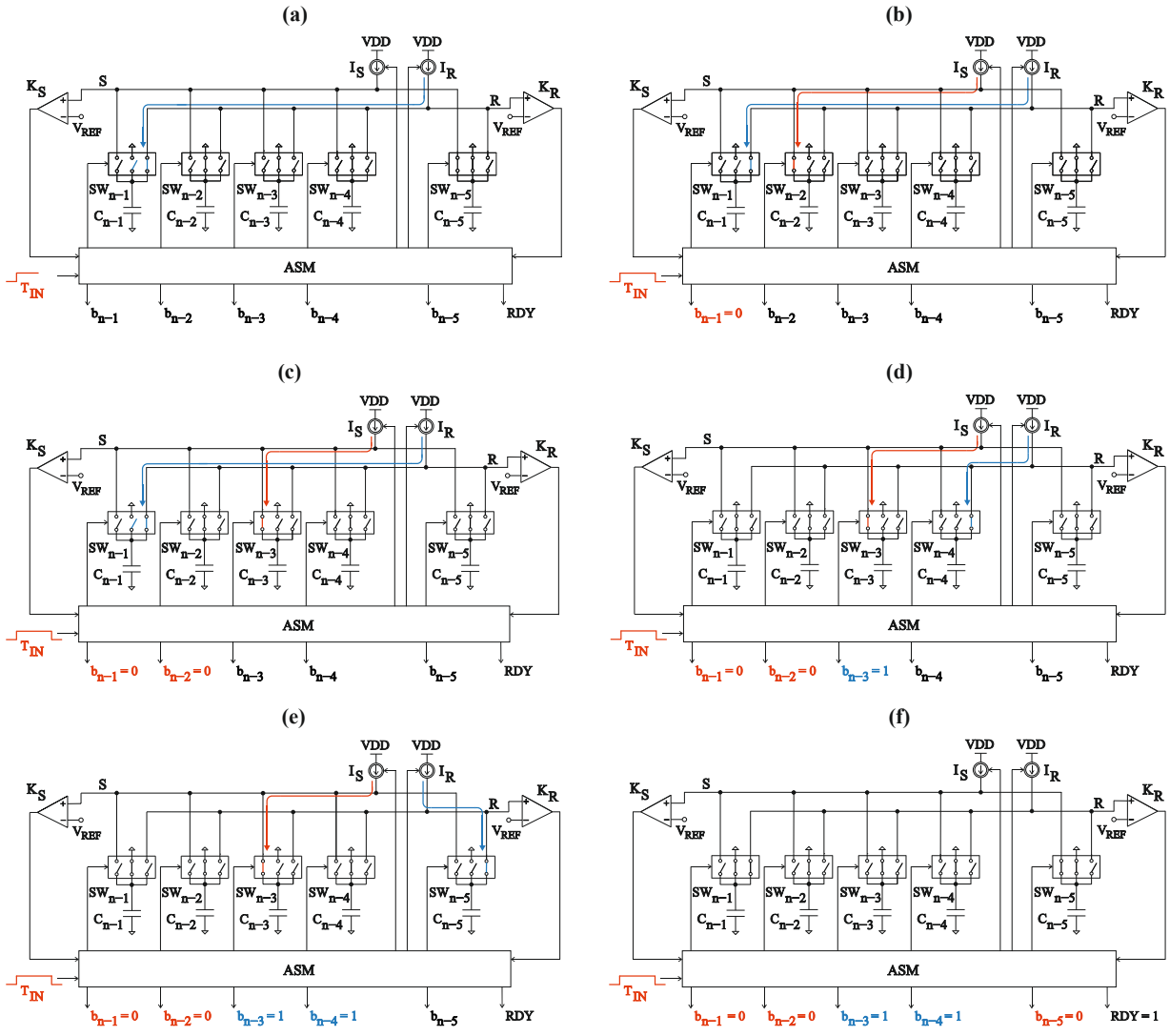

Figure 5. Exemplary states during the STB conversion: (**a**) detection of the rising edge of the measured time interval; (**b**) detection of the falling edge of the measured time interval; (**c**) simultaneous disconnecting the capacitor C_{n-2} from the rail S and connecting the capacitor C_{n-3} to this rail; (**d**) simultaneous disconnecting the capacitor C_{n-1} from the rail R and connecting the capacitor C_{n-4} to this rail; (**e**) simultaneous disconnecting the capacitor C_{n-4} from the rail R and connecting the capacitor C_{n-5} to this rail; (**f**) conversion process finished.

In comparison to the column-building model, there are two rails: S and R, which directly correspond to the signal column S and the reference column R (Figure 3). The reference tanks have been replaced by the binary-scaled capacitors $C_{n-1}, \ldots, C_0$ defined as $C_k = 2^k C_0$, for $k = 0, 1, \ldots, n-1$.

Each capacitor C_k is related to a corresponding bit b_k, which is evaluated during the conversion process. The capacitors are sequentially connected, one by one, to the rails (S or R) in such a way that one is replaced by another. Thus, at any step of the conversion process, no more than one capacitor is connected to a given rail. Also, with the connection of the capacitor C_k to the specific rail, a simultaneous disconnection of the previously connected one is made.

Each capacitor C_k has a set of switches SW_k associated with it. This set comprises three single switches which allow setting the capacitor C_k in one of the three configurations: connected to the rail S, connected to the rail R, or connected to the ground. Initially, all

capacitors are connected to the ground and at an appropriate step of the conversion the ASM makes the decision when and where the specific capacitor C_k should be connected.

The pumps I_R and I_S have been replaced by the current sources: I_R and I_S which are digitally switched on and off. They provide constant current flow to the specific capacitors which are currently used. The charging capacitor with a constant current flow was presented in the column model as filling an appropriate reference tank (Figure 3).

The comparators K_R and K_S are assigned to the rails in the same way as the current sources I_R and I_S. The purpose of the comparators is to sense the moment when the voltage across a currently charging capacitor reaches the level set by the reference voltage V_{REF}. When such an event occurs, the comparator indicates it to the asynchronous state machine ASM which then firstly determines the appropriate bit value, and secondly makes the decision which capacitor should be connected to the specific rail (S or R). Of course, the target rail is always the one on which the charging has just finished.

The asynchronous state machine ASM is a fully clockless control circuit. Neither external (global) nor internal (local) clock signal is required for its proper operation. The only signals it is driven by are the edges of the measured time interval T_{IN} and the event signals generated by the comparators K_R, K_S, so basically, the ASM is an event-driven circuit [34]. This is actually where the self-clocked property of the STB comes from. The devices that are directly under the control of the ASM are the switches $SW_{n-1}, \ldots, SW_0$, and the current sources I_R and I_S. During the conversion process, the ASM connects subsequent capacitors, one by one, to the rail (S or R) via the appropriate switch SW_k which is assigned to the chosen capacitor. In addition, it turns on the current source: I_R with the T_{IN} front edge and I_S with the rear edge occurrence. The conversion process flow diagram of the ASM is presented in Figure 4.

3.2. Conversion Process

During the relaxation state, while waiting for the time interval T_{IN}, both R and S rails are grounded, which prevents the accumulation of random charges that could disturb the conversion accuracy. For this purpose, the switches SW_{n-1} and SW_0 are used, respectively, for the reference rail R and the signal rail S.

The conversion starts with the front edge of the measured time interval T_{IN} (Figure 5a). At this moment two actions are performed. Firstly, the triggered ASM simultaneously disconnects the reference rail R from the ground and connects the biggest capacitor C_{n-1} to the reference rail R via the switch SW_{n-1}. Secondly, the constant current source I_R is turned on causing the linear increase of the capacitor C_{n-1} voltage as well as the reference rail R voltage (Figure 6).

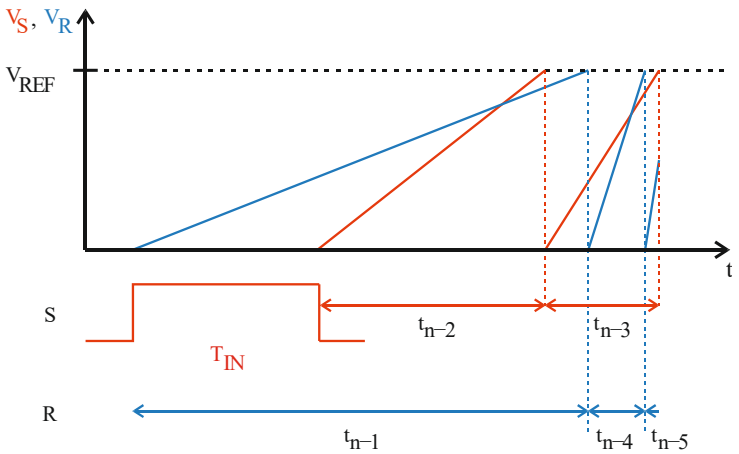

Figure 6. Voltage waveforms of the rails R (blue color) and S (red color).

With the rear edge of the measured input value T_{IN}, two operations are performed. Firstly, the biggest capacitor C_k ($k < n - 1$) from the group of the empty ones $C_k, \ldots, C_0$ is

connected to the signal rail *S* via the appropriate switch SW_k. Immediately after that, the constant current source I_S is turned on, which causes the voltage across the capacitor C_k and the signal rail S to increase linearly (Figure 5b).

When the voltage across the charging capacitor reaches reference level V_{REF}, the relevant comparator (K_S or K_R) triggers the ASM, which performs two operations. The first of them is evaluating the appropriate bit associated with the capacitor that was the most lately connected to any rail. Of course, it does not necessarily have to be the capacitor that has just finished charging and caused the specific comparator to trigger.

The output digital word evaluation can be described as follows:

- If the capacitor C_k is connected to the signal rail S, and during the time it is being charged, the charging of a new capacitor on the (opposite) rail R was started, the bit b_k is set to logic one: $b_k = 1$ (Figure 5c,d).
- If the capacitor C_k is connected to the reference rail R, and during the time it is being charged, the charging of a new capacitor on the (opposite) rail S was not started, the bit b_k is set to logic one: $b_k = 1$ (Figure 5d,e).
- In any other cases, bit b_k is set to logic zero: $b_k = 0$ (Figure 5a,b,f).

As mentioned before, the exception to the above rules is bit b_0, because it is associated with the capacitor C_0 which is connected to one of the rails as the last in the sequence. Thus, in this case, the bit value is determined as if there were another, capacitor C_{-1} that would be used in the processing (Figure 5f).

The second operation after the capacitor C_k reaches the V_{REF} is simultaneously disconnecting the fully charged capacitor C_k from the rail, connecting it to the ground, and connecting the subsequent capacitor from the empty ones (supposing that there is at least one left). Obviously, it does not necessarily have to be the subsequent capacitor C_{k-1} as it could have been used on the opposite rail already. If there are no capacitors left, the conversion process is finished. The procedure of connecting, charging, and disconnecting the capacitors is repeated until all of them are used (Figure 5f). The duration of the capacitors switching operation is negligibly short, so the current sources I_R,I_S are not turned off when the fully charged capacitor C_k is replaced by a smaller one.

Here the self-clocked mechanism is clearly visible. Once triggered, ASM decides about replacing the charged capacitor with an empty one. This newly connected capacitor will become a source that triggers the ASM in one of the later conversion steps.

When the conversion process is completed, the signal RDY is set to the logic one, indicating that the bits determination process is complete (Figure 5f). Simultaneously, the current sources are turned off and the rails are connected to the ground via the switches. The bits $b_{n-1}, \ldots, b_0$ in the digital output word are latched until the front edge of the next time interval T_{IN} occurs and triggers the conversion process.

4. The STB-TDC Circuit Simulations

The proposed conversion method has been verified in the Cadence® Virtuoso environment (version IC6.1.8) by simulating the circuit application (TDC) on the schematic level. The analog parts were designed using ideal elements (comparators, current sources, analog switches, and capacitors) from the default analogLib library. The functionality of the asynchronous state machine ASM was implemented in Verilog-A which is a subset of Verilog-AMS Hardware Description Language. The use of Verilog-A was necessary to fully control the capacitors' switching sequence and thus prevent the occurrence of false phenomena associated with the use of ideal elements. Since the whole circuit is relatively simple (Figure 5), it was assumed that, overall, it can be supplied using a 1.8 V power source.

The STB method does not strictly dictate the number of used capacitors. As each capacitor C_k refers to one bit b_k, for the purpose of the simulation eight capacitors $C_7, \ldots, C_0$ were used to achieve 8-bit resolution. At such a simplified level of the STB converter the technological aspects can be totally omitted because all the elements are ideal. Still, already at this stage certain parameters should be selected in such a way that they are

achievable in the physical semiconductor implementation. The target technology is UMC 0.18 µm which in combination with the purpose of measuring relatively long time intervals (microseconds) leads to the conclusion that for the good circuit matching and high resistance to technological variations, the analog elements should be relatively large in size [35,36]. Following the above, the smallest capacitor C_0 was set to 500 fF. The reference voltage V_{REF}, to which the capacitors $C_7, \ldots, C_0$ are linearly charged, has been set to 1.2 V, which is around the typical value for the real bandgap voltage reference circuits [37–42].

The current sources I_R, I_S were set to provide a constant current flow of 1 µA. Thus, the minimum time interval that can be resolved equals to $t_0 = \frac{V_{REF} \cdot C_0}{I_{R(S)}} = 600$ ns, which directly leads to the full-scale range of 153.6 µs.

The verification of the STB converter was carried out using Virtuoso Analog Design Environment XL tool. As the state machine, ASM behavior was handled with Verilog-A, it imposed mixed-signal simulation. Figure 7 presents the result of a single simulation for the measured time interval T_{IN} of 31.9 µs which is converted to the digital word 00110101.

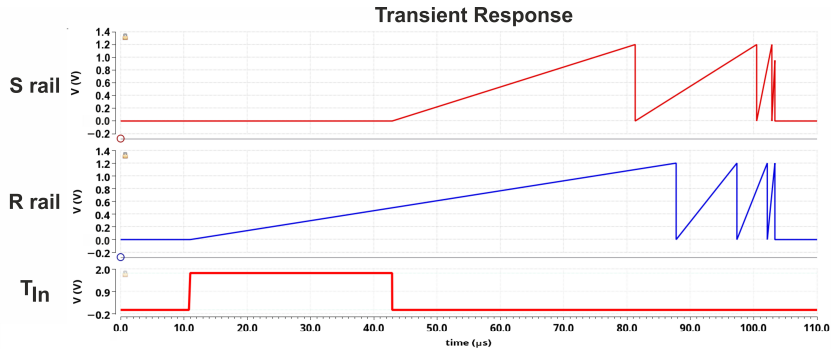

Figure 7. The conversion of input time interval T_{IN} = 31.9 µs.

As shown, the STB converter starts the direct time approximation process as soon as the front edge of the measured time interval T_{IN} appears and there is no preconversion process used. The charges generated by the current sources I_R, I_S cause the linear increase of the voltage across subsequent capacitors $C_7, \ldots, C_0$ (one by one). The characteristic, sudden voltage drops indicate the moment of replacing a fully-charged capacitor with another one—not yet used.

The transfer characteristic shown in Figure 8 has been plotted based on 3080 different lengths of T_{IN} in the range from 1 ns to 154 µs with a step of 50 ns. As expected, the results show that at this level of complexity the STB converter is fully error-free and completely coincides with the ideal characteristics of analog-to-digital conversion. This proves that STB-TDC can be successfully used as a direct time-to-digital conversion method and no additional reference clock is needed. The self-clocking mechanism is indeed sufficient to achieve the appropriate quality of conversion.

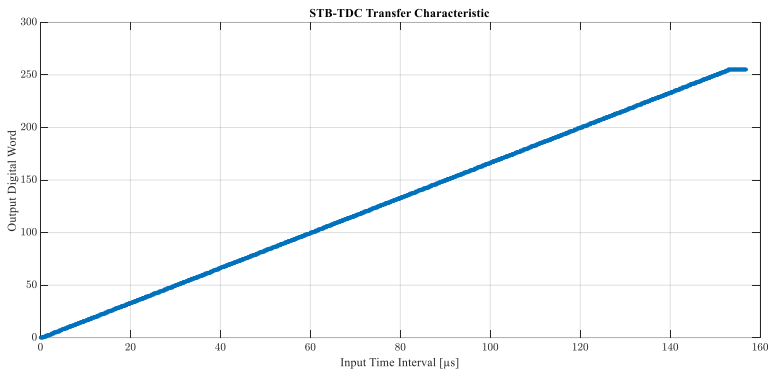

Figure 8. Transfer characteristic of the STB time-to-digital converter based on 3080 measurement points.

5. The STB-TDC Physical Implementation

The topologies of analog subcircuits used in the implementation of the STB-TDC prototype are presented in Figure 9. The current sources I_S, I_R, shown in Figure 9a, were implemented as the cascode current sources which, by default, provide resistance to the temperature variation, process variation, and channel length modulation effect [43–46]. In addition, the high-swing modification was applied. It allows the increase of the V_{REF} value to which capacitor C_k can be charged without causing the current sources to deviate from the assumed value. For the comparators K_S, K_R, shown in Figure 9b, a simple topology has been used which does not require any additional biasing voltage sources [44,47]. Due to the completely clockless design of the STB-TDC, there is no auxiliary reference clock signal. The asynchrony of the comparators K_S, K_R means that their propagation time depends on the rate of voltage change on the monitored rail. Its parameters have been selected in such a way as not to disturb the binary ratio of charging times of subsequent capacitors. Each of the three switches comprised in a single switch SW_k has been implemented as a transmission gate (Figure 9c). For 8-bit STB-TDC there are 8 transmission gates (16 transistors) connected to each rail which significantly increases its parasitic capacitance. Therefore, the minimum transistor sizes offered by the UMC 0.18 µm CMOS technology were used for the transistors in transmission gates. The bandgap reference voltage V_{REF} presented in Figure 9d is based on mutual compensation of PTAT-CTAT (proportional to absolute temperature—complementary to absolute temperature) structure [43–46].

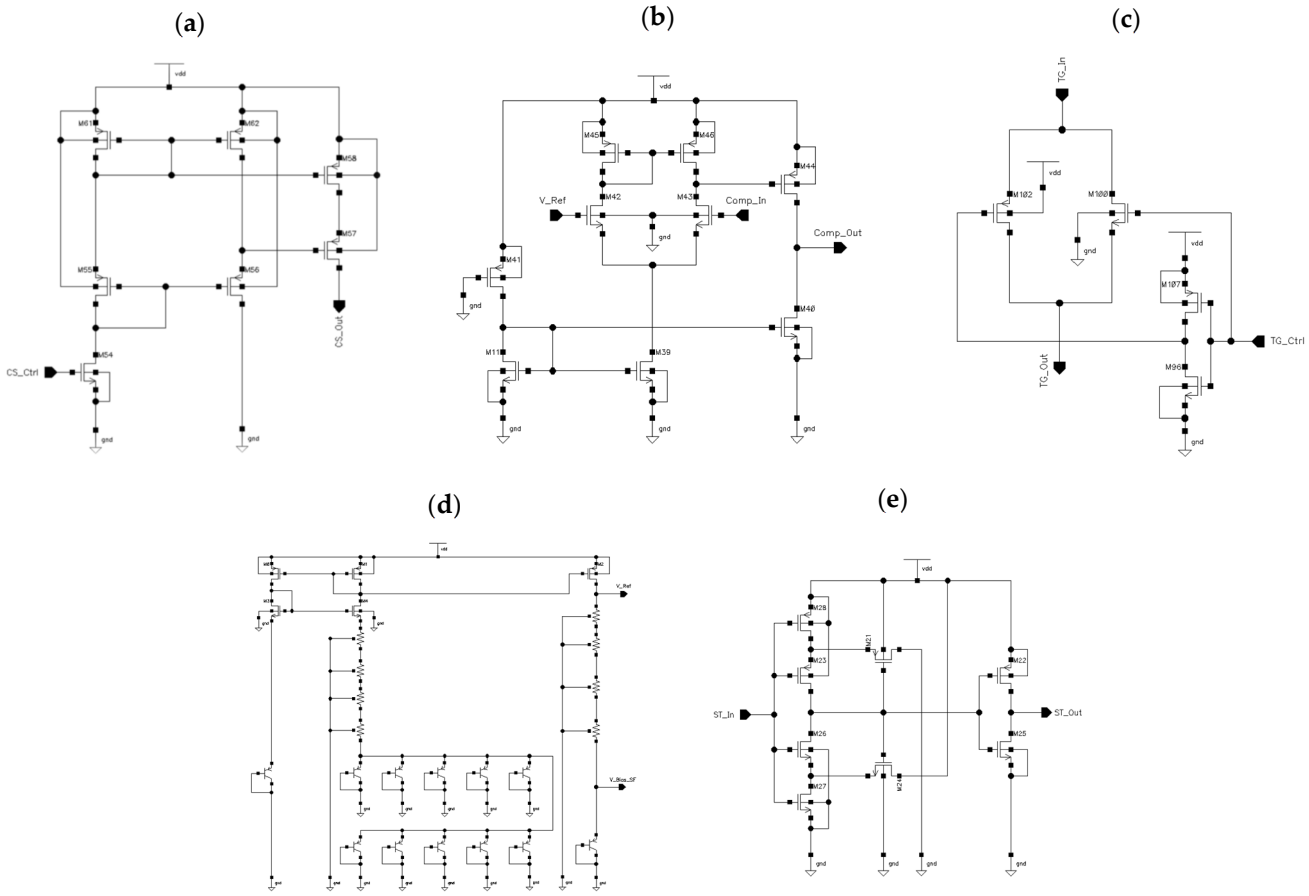

Figure 9. The analog components of the STB-TDC: (**a**) current source I_S, I_R; (**b**) comparator K_S, K_R; (**c**) one of the three switches comprised in SW_k; (**d**) bandgap reference voltage V_{REF}; (**e**) Schmitt trigger.

In addition to the above described components, a few circuits have been applied. For instance, a non-inverting Schmitt trigger, shown in Figure 9e, has been connected to the

output of each comparator to increase the slope of the edges of the signals entering the ASM [48,49]. In addition, a mutex (mutual exclusion) has been used to avoid the situation of simultaneous appearance of output signals from the comparators K_R, K_S at the input of the ASM. Proper resolution between the signals is absolutely necessary because the circuits related to the individual rails S, R operate independently of each other.

The presented analog circuits can be controlled by a fully asynchronous state machine. As shown, they can be implemented as relatively simple structures. Therefore, they are suitable for direct cooperation with TEM circuits creating time-based ADC conversion system (Figure 1).

The layout of the first 8-bit STB-TDC prototype is presented in Figure 10. It was designed using UMC 0.18 µm 1P6M CMOS technology. Including the wire bonding pads, the total occupied area equals 1.45 mm^2 with the aspect ratio of approx. 1.14. The power supply domains for the analog circuits and the digital asynchronous state machine have been physically separated, but both of the domains are dedicated for 1.8 V as it was assumed. The circuit requires two input digital ports: T_{IN}, RESET; nine output digital ports: $b_7, \ldots, b_0$, RDY; two power supply ports: VDD, VDDA; and one port for the ground connection: GND which is common for all the components across the chip. Each signal path has been equipped with additional buffers and basic antistatic protection.

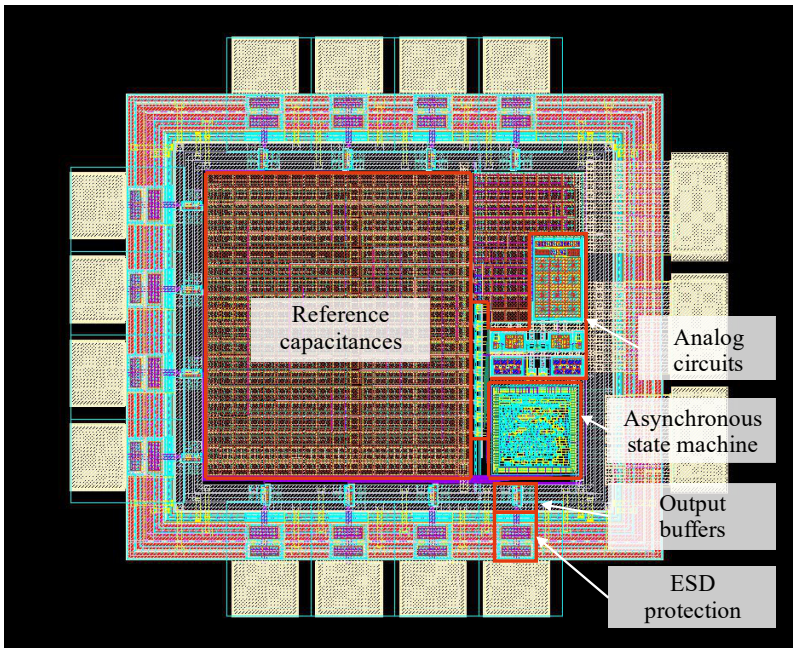

Figure 10. The STB Time-to-Digital Converter layout.

The unit capacitor C_0 has been set to 499.5 fF and the entire reference capacitors matrix was designed using it. The reference capacitors have been arranged based on common centroid algorithm in order to minimize the systematic mismatch. In addition, dummy capacitors have been added around the reference capacitors so that all capacitances have the same neighborhood. Overall, the matrix occupies 0.305 mm^2 and it is the largest component.

The ASM, presented in Figure 11a, has been implemented in Verilog-HDL and synthesized using Genus Synthesis Solution. In the final netlist 359 logic elements from the dedicated library were included to form a fully clockless, event-driven state machine. The physical implementation PnR (place and route) was carried out using the Innovus Implementation System. In order to ensure proper filtration, capacitive filler cells were used. The area of the ASM is 0.03 mm^2, however, it should be noted that most of it are the above-mentioned filler cells.

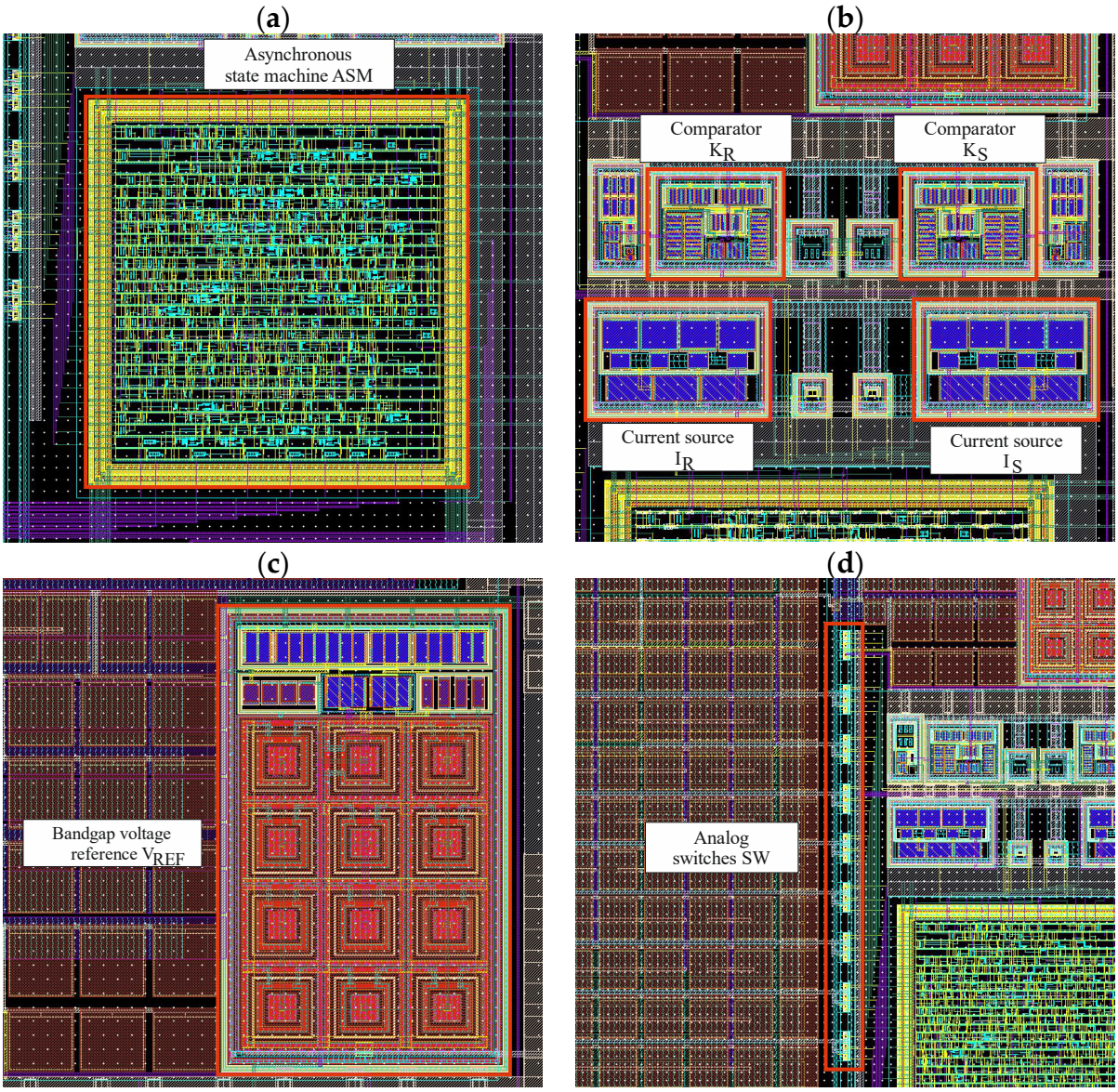

Figure 11. STB-TDC layout subparts: (**a**) asynchronous state machine; (**b**) comparators and current sources; (**c**) bandgap reference voltage; (**d**) analog switches.

The analog circuits are presented in Figure 11b–d. In total, 188 CMOS transistors were used (excluding dummy transistors) to design the whole analog part of the STB-TDC. During the design of each individual components, efforts were made to maintain layout symmetry. The summary area of all the analog circuits is 0.037 mm^2, most of which is occupied by the bandgap voltage reference as it contains a set of emitter diodes made of PNP transistors.

The post-layout verification of the STB-TDC has been performed in the same way as the verification of the ideal model. Based on the acquired data, selected time-to-digital parameters have been analyzed.

Figure 12 presents the final transfer characteristic of the proposed 8-bit STB-TDC design. Comparing the physical implementation to the ideal model, current sources I_R, I_S and bandgap reference voltage V_{REF} values were slightly changed, which resulted in a change of the LSB and therefore in the transfer characteristic. The proposed solution is able to convert the measured time intervals T_{IN} up to 135.66 µs with the LSB of 532 ns. The transfer characteristic is monotone and none of the output codes are missing.

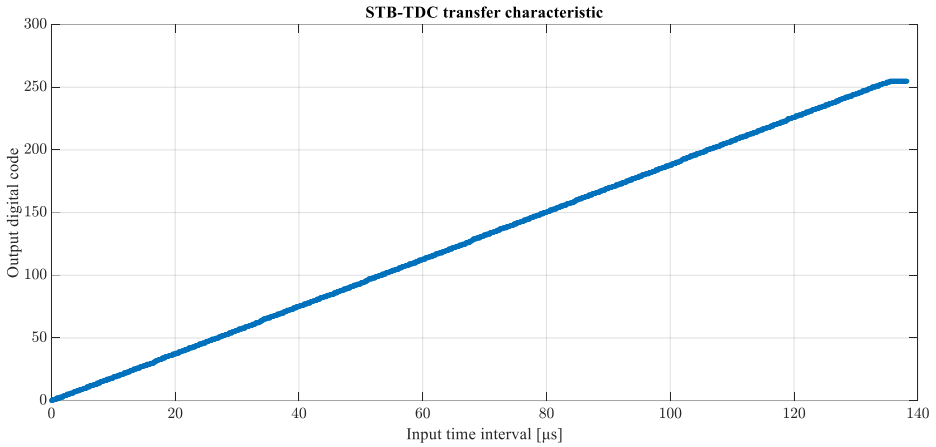

Figure 12. Transfer characteristic of the STB-TDC post-extraction circuit.

The differential and integral nonlinearity (DNL, INL) plots are shown in Figures 13 and 14. Maximum positive and negative differential nonlinearity errors equal, respectively, 0.25 LSB and −0.6 LSB. The latter occurs for the output digital code transition from 127 to 128. Maximum positive and negative integral nonlinearity equal, respectively, 0.71 LSB and −0.5 LSB.

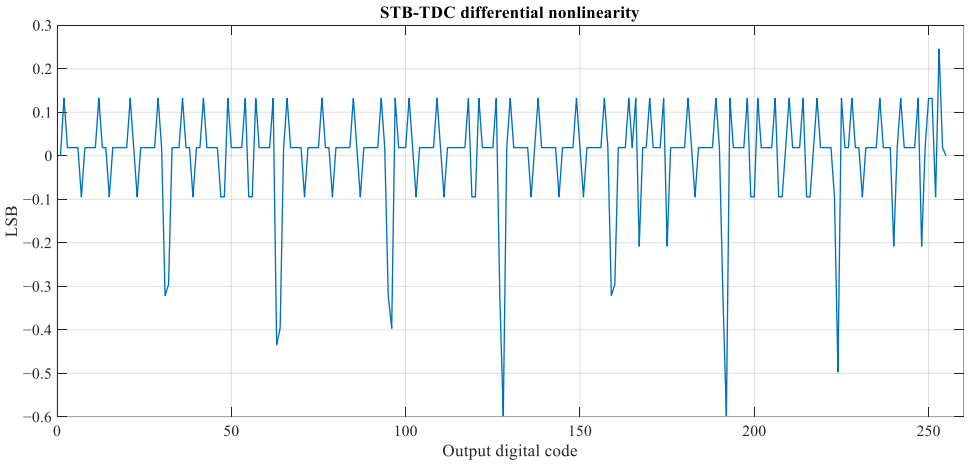

Figure 13. Differential nonlinearity of the STB-TDC post-extraction circuit.

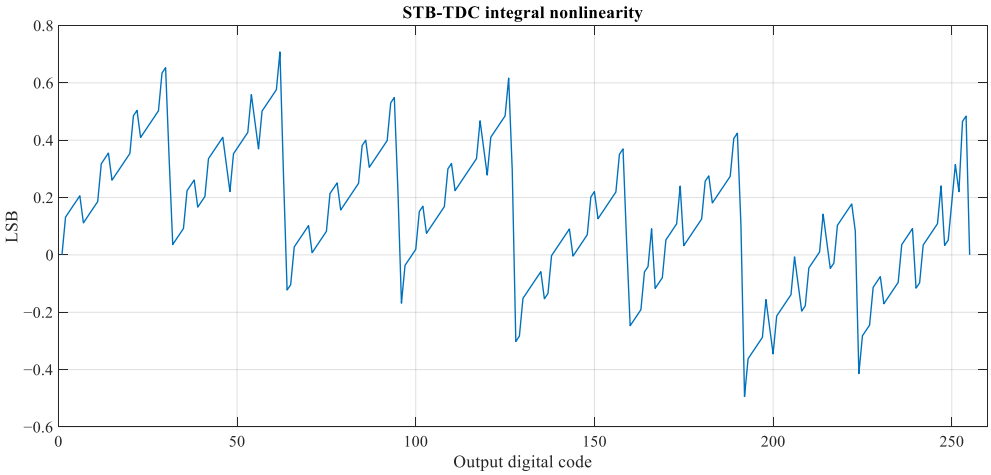

Figure 14. Integral nonlinearity of the STB-TDC post-extraction circuit.

The average consumed current equals 445 µA, which, after taking into account the power supply of 1.8 V, determines the average power consumption of 801 µW. The above-described parameters are summarized in the Table 1.

Table 1. The STB-TDC physical implementation parameters.

Parameter	Value
CMOS process	UMC 0.18 µm
Power supply	1.8 V
Occupied area	1.45 mm^2
Unit capacitance C0	499.5 fF
LSB	532 ns
Full-scale range	135.66 µs
Maximum DNL	+0.25 LSB, −0.6 LSB
Maximum INL	+0.71 LSB, −0.5 LSB
Average power consumption	801 µW

6. Conclusions

In this paper, a new time-to-digital conversion method based on the binary successive approximation has been presented. Its main advantage consists in a fully clockless operating method with the simultaneous ability to direct conversion of the measured time intervals without the necessity of any preconversion. The introduction of the method was carried out gradually. Firstly, the simplified column-building model has been presented, in which the ability to direct conversion was emphasized. Secondly, the operation of the TDC circuit model has been described, wherein additionally, a fully clockless conversion is clearly visible. Next, the STB-TDC ideal model, followed by the physical implementation using UMC 0.18 µm technology have been presented. Finally, the simulations results as well as the time-to-digital conversion parameters have been shown, which proves that the STB-TDC method can be successfully used for time interval measurement.

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