



Article A Compact and Efficient Boost Converter in a 28 nm CMOS with 90 mV Self-Startup and Maximum Output Voltage Tracking ZCS for Thermoelectric Energy Harvesting

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Abstract: There are increasing demands for the Internet of Things (IoT), wearable electronics, and medical implants. Wearable devices provide various important daily applications by monitoring real-life human activities. They demand low-cost autonomous operation in a miniaturized form factor, which is challenging to realize using a rechargeable battery. One promising energy source is thermoelectric generators (TEGs), considered the only way to generate a small amount of electric power for the autonomous operation of wearable devices. In this work, we propose a compact and efficient converter system for energy harvesting from TEGs. The system consists of an 83.7% efficient boost converter and a 90 mV self-startup, sharing a single inductor. Innovated techniques are applied to adaptive maximum power point tracking (A-MPPT) and indirect zero current switching (I-ZCS) controllers for efficient operation. The startup circuit is realized using a gain-boosted tri-state buffer, which achieves 69.8% improved gain at the input $V_{\rm IN} = 200$ mV compared to the conventional approach. To extract the maximum power, we use an A-MPPT controller based on a simple capacitive divider, achieving 95.2% tracking efficiency. To address the challenge of realizing accurate voltage or current sensors, we propose an I-ZCS controller based on a new concept of maximum output voltage tracking (MOVT). The integrated circuit (IC) is fabricated using a 28 nm CMOS in a compact chip area of 0.03 mm^2 . The compact size, which has not been obtained with previous designs, is suitable for wearable device applications. Measured results show successful startup operation at an ultralow input, $V_{\rm IN}$ = 90 mV. A peak conversion efficiency of 85.9% is achieved for the output of 1.07 mW.

Keywords: thermoelectric generator; wearable electronics; boost converter; maximum power point tracking; zero current switching; self-startup

1. Introduction

Recent interest in renewable energy sources is significantly increasing with rising environmental pollution and energy costs. Extensive research has been conducted to explore new methods to conserve power and harvest clean energy. Because of the increasing number of low-power devices such as the Internet of Things (IoT), wearable electronics, and medical implants, energy harvesting from renewable sources is an urgent research topic [1]. Among them, wearable devices provide important daily applications by monitoring various human activities. Diverse examples of wearable devices have been proposed, which include electronic skin, wristbands, watches, smart clothing, virtual reality (VR) headsets, and artificial intelligence (AI) hearing aids [2]. These devices demand low-cost autonomous operation with miniaturized form factors; the demands are challenging to satisfy using a rechargeable batteries. One promising energy source for wearable electronics is thermoelectric generators (TEGs), which convert an omnipresent temperature gradient into electrical energy via the Seebeck effect [3,4]. It is considered that TEGs are the only way to generate a small amount of electric power for the autonomous operation of wearable



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Copyright: © 2023 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (https:// creativecommons.org/licenses/by/ 4.0/). devices. Because energy conversion can be performed using a solid-state material without moving elements, TEGs are suitable for long-term operation. Under a relatively small temperature gradient, however, TEG generates a low source voltage (V_S), which cannot be used to supply the devices directly. For example, commercially available TEGs generate V_S between 10 mV and 30 mV for a 1 °C temperature difference [5]. Therefore, a DC-DC converter is required to boost the input to a suitable output.

Various techniques have been explored to realize efficient DC-DC converters using maximum power point tracking (MPPT) methods [6–9]. The authors of [6] configure the switching frequency based on the internal resistor (R_S) of the TEG and the inductor value. However, the frequency of the on-chip clock generator can fluctuate due to process, voltage, and temperature (PVT) variations. This necessitates an adaptive MPPT controller based on a voltage-controlled oscillator (VCO) to tune the switching frequency [7]. The work conducted in [8] utilizes a hill-climbing MPPT controller that senses the output current of the converter, which charges algorithm capacitors to track V_S for handling the input range from 5 μ W to 10 mW. The work conducted in [9] uses transformer-based methods for a dual-stage boost converter to increase conversion efficiency to 81.5%.

The switched capacitor (SC)-based approach offers the advantage of on-chip integration and low-voltage operation [10–12]. The gate-boosted charge pump operates with an input voltage of 100 mV [10]. Another work [11] utilized a voltage doubler as a negative charge pump to reduce the on-resistance of the load-side switch. Additionally, a fully integrated SC converter used a 220 mV input to generate a 1.9 V output [12]. However, previous works have the drawback of large system sizes; for example, the algorithm capacitor in [8] requires a 7.6 mm² silicon area. Other works have bulky implementations, such as a transformer of 1.8 mm² size [9], a sizeable on-chip capacitor of 2.31 mm² [10], and three inductors [13]. The SC-based converter shows relatively low efficiencies, for example, 33% [10], 52% [11], and 37.4% [12].

Because V_S can be smaller than the threshold voltage (V_{TH}) of transistors, a selfstartup method is required for the initial step-up of the supply voltage. The startup temporarily provides power for the main converter until it can be self-sustained. Various methods have been investigated. These methods include using a mechanical switch to initiate the converter [6], utilizing an off-chip transformer [9], using on-chip inductors [10], and pre-charging the output capacitor using an external battery [14]. However, these techniques often demand bulky implementations, which can be impractical for low-cost sensor nodes and IoT applications. The works [15,16] use the switched branches for inductor sharing between the startup and main converter; however, the switching increases the system complexity.

The discontinuous conduction mode (DCM), commonly used for low-power DC-DC converters, should suppress the reverse current through the inductor. The high-side switch is opened when the inductor current I_{IND} is close to zero for zero current switching (ZCS). One method to implement ZCS is using a diode [17]; however, this approach is unsuitable for low-voltage design due to diode voltage drop. For efficiency reasons, a transistor switch is typically used with a ZCS controller. A previous work on a ZCS controller used a comparator to detect the voltage [18]. Another approach is to use digital circuits to detect current zero crossing indirectly using the inductor voltage [19]. The digital quantization of inductor voltage needs to select fine pulse width for the ZCS operation. However, the linear scaling used to modulate the pulse width becomes inefficient for low V_{IN} . To handle the issue, a fine delay stage is used [20], which sets the pulse width suitable to open the high-side switch; however, the ZCS controller uses an external supply to realize fine delay. In addition, appropriate measurement delay is not addressed [21].

To overcome the issues mentioned above, we propose a compact and efficient DC-DC converter system realized in the 28 nm CMOS technology. The integrated system consists of an 85.9% efficient boost converter and a 90 mV self-startup, sharing a single inductor. Innovated techniques are applied to adaptive MPPT (A-MPPT) and indirect ZCS (I-ZCS) controllers for efficient operation. The startup circuit is realized using a ring-oscillator-

based charge pump, which enhances gain using a tri-state buffer for ultralow voltage operation. The tri-state buffer achieves a 69.8% gain improvement over a single buffer at $V_{\rm IN}$ = 200 mV. To extract the maximum power, we use an A-MPPT controller based on a simple capacitive divider for fractional open circuit voltage (FOCV) operation. To address the challenges of realizing accurate voltage or current sensors, we propose an I-ZCS controller based on maximum output voltage tracking (MOVT). The fabricated integrated circuit (IC) is realized in a compact chip area of 0.03 mm². The compact size, which has not been obtained with previous designs, is suitable for wearable device applications. The measured results show a peak tracking efficiency of 95.2% and a conversion efficiency of 85.9%. The end-to-end efficiency of 83.7% is achieved using $R_{\rm S}$ = 8 Ω and $V_{\rm S}$ = 280 mV.

This paper is organized as follows. Section 2 describes the system design. Section 3 presents the circuit implementation. Section 4 presents the measured results, and Section 5 draws the conclusion.

2. System Design

2.1. Proposed System

Figure 1 shows the block diagram of the proposed system. It mainly consists of a boost converter and a self-startup circuit. The boost converter includes an A-MPPT controller, an I-ZCS controller, a voltage detector (VD), an oscillator, and four power switches (M_{N1} , M_{N2} , M_{P1} , and M_{P2}). M_{N1} , used for self-startup, is a low threshold voltage (LVT) transistor. High threshold voltage (HVT) transistors are used for the switches of the boost converter (M_{N2} , M_{P1} , and M_{P2}), which reduces the leakage current compared to the standard threshold voltage (SVT) transistor. Super-low threshold voltage (SLVT) transistors are used for the startup circuit to reduce the minimum input V_{IN} to the system. The oscillator consists of a ramp generator, pulse generator, biasing resistor R_{OSC} , and capacitor C_{OSC} . The ramp voltage V_{RAMP} is compared with a reference V_{REF} to generate the clock signal Φ_{OSC} for the A-MPPT controller. The TEG is modeled using V_S and R_S . An input capacitor C_{IN} is used to buffer the converter's input V_{IN} . A single inductor $L = 100 \ \mu\text{H}$ is shared between the startup and boost converter without extra switches.



Figure 1. Block diagram of the proposed system.

Figure 2 shows the waveform of the converter. When V_{IN} is supplied to the startup circuit, it generates an output pulse $\Phi_{S,OUT}$ (= Φ_{N1}) for M_{N1} . During the on-time of M_{N1} , L is charged when V_{IN} is as low as 90 mV. During the off-time of M_{N1} , stored energy in L keeps charging the storage capacitor C_{DD} through M_{P1} . During the startup, the supply voltage V_{DD} gradually increases to 700 mV. The VD monitors V_{DD} . When V_{DD} reaches 700 mV, it generates the disable signal V_{DIS} , which stops the oscillation of the startup circuit and enables the boost converter. The boost converter raises the tens of mV generated by

the TEG to the output V_{OUT} level required to power IoT devices. To extract the maximum power from the TEG, the A-MPPT controller continuously adjusts the on-time of the pulse Φ_{N2} for M_{N2} . Then, the input impedance R_{IN} is adjusted to match R_S , and the maximum power point (MPP) voltage V_{MPP} tracks half of V_S . The I-ZCS controller provides the pulse Φ_{P2} to control the on-time of M_{P2} when *L* discharges. The M_{P2} is turned off at a suitable time to prevent the current backflow from V_{OUT} .



Figure 2. Waveforms of the converter operation.

2.2. Self-Startup Circuit

Ring oscillators are widely used to generate the clock for the startup circuit; however, the operation is limited mainly by two reasons. Firstly, when V_{DD} reduces, it is difficult to sustain the oscillation with the decreased gain of the inverter. Secondly, the output swing needed to drive the subsequent stage is reduced. These limitations can significantly impede the low-voltage startup [22].

Figure 3 shows the proposed self-startup circuit using a gain-boosted tri-state buffer. It consists of six stages, in which the output of the fifth stage is feedback to the first stage. The inset shows the schematic of the unit stage. It comprises two inverters, INV1 (transistors N₁ and P₁) and INV2 (transistors N₂ and P₂). They are realized using SLVT transistors to reduce the startup voltage further. The INV2 works as a tri-state buffer, which provides additional gain to reduce the input for the startup. V_{EN} is enabled by the input, and the startup circuit generates $\Phi_{\text{S,OUT}}$. When disabled, it keeps a high impedance state. The voltage gain A_{V1} of a single inverter can be expressed [22] as

$$A_{\rm V1} \cong \frac{g_{\rm m,eff1}}{g_{\rm ds,N1} + g_{\rm ds,P1}} = \frac{g_{\rm m,N1} + g_{\rm m,P1}}{g_{\rm ds,N1} + g_{\rm ds,P1}} \tag{1}$$

where the effective transconductance $g_{m,eff1}$ is the transconductance sum of N₁ and P₁. The $g_{ds,N1}$ and $g_{ds,P1}$ are the output conductance of N₁ and P₁, respectively. In the proposed gain-boosted buffer, the input $V_{Buf,in}$ is fed to the gate of the two inverters. The buffer output $V_{Buf,out}$ is taken from the output of INV2. The output of INV1 is connected to the source of the P₂, which is amplified by the gain ($A_{V1}V_{IN}$) of INV1. Then, it is increased to (1 + A_{V1}) V_{IN} . Because $A_{V1} > 1$, $V_{Buf,in}$ is amplified by the effective transconductance $g_{m,eff2}$ of the tri-state buffer, which can be written as

$$g_{m,eff2} \cong (1 + A_{V1})g_{m,P2} + g_{m,N2}$$
 (2)

where $g_{m,P2}$, and $g_{m,N2}$ are the transconductance of P₂ and N₂, respectively. Using a similar method to that used to derive Equation (1), we obtain the gain A_{V2} of the gain-boosted buffer as

$$A_{\rm V2} \cong \frac{g_{\rm m,eff2}}{g_{\rm ds,P2} + g_{\rm ds,N2}} = \frac{(1 + A_{\rm V1})g_{\rm m,P2} + g_{\rm m,N2}}{g_{\rm ds,P2} + g_{\rm ds,N2}}$$
(3)

where $g_{ds,N2}$, and $g_{ds,P2}$ are the output conductance of N₂ and P₂, respectively. The result shows an enhanced gain of the tri-state buffer.



Figure 3. Schematic of the proposed self-startup circuit using the gain-boosted tri-state buffer. $C_{S1} = 100$ fF; $C_{S2} = 1.5$ pF.

Figure 4a shows the transfer characteristics of the single- and tri-state buffers for three V_{IN} . The tri-state buffer shows steeper slopes, indicating increased gain. The gain is calculated by taking the derivative of $V_{Buf,out}$. Figure 4b shows the gain comparison using $V_{IN} = 100$ mV. The result indicates that the tri-state buffer achieves a 21.2% gain improvement. Figure 4c,d show the gain comparison using $V_{IN} = 150$ mV and $V_{IN} = 200$ mV, respectively. The results show that the tri-state buffer increases the gain by 41.1% and 69.8%, making it an attractive approach for low-voltage startups.



Figure 4. (a) Transfer characteristics of the single inverter and the gain-boosted tri-state buffer. Gain comparison at three input values of (b) V_{IN} = 100 mV, (c) V_{IN} = 150 mV, and (d) V_{IN} = 200 mV.

2.3. Loss Analysis for Startup

Figure 5 shows the equivalent circuit of the startup for loss analysis. The resistive power loss $P_{R,startup}$ of the startup circuit can be expressed as

$$P_{\rm R,startup} \cong \frac{R_0 V_{\rm IN}^2}{\left(R_{\rm IN} + R_0\right)^2} = \frac{\left(R_{\rm IND} + R_{\rm N1}\right) V_{\rm IN}^2}{\left(R_{\rm IN} + R_{\rm IND} + R_{\rm N1}\right)^2} \tag{4}$$

where R_0 consists of the inductor parasitic resistance R_{IND} (= 120 m Ω) and the resistance R_{N1} of M_{N1} . The switching loss $P_{SW,startup}$ can be expressed as

$$P_{\text{SW,startup}} \cong \frac{1}{2} C_{\text{G,N1}} V_{\text{G,N1}}^2 f_{\text{St}}$$
(5)

where f_{St} is the switching frequency of the startup circuit. $V_{G,N1}$ and $C_{G,N1}$ are the gate voltage and capacitance of M_{N1} , respectively. The power consumption $P_{Q,startup}$ of the startup circuit is 60 nW using $V_S = 150$ mV and $R_S = 18 \Omega$. The total loss $P_{T,startup}$ is the sum of $P_{R,startup}$, $P_{SW,startup}$, and $P_{Q,startup}$. Using the input power P_{IN} , we obtain the efficiency $\eta_{startup}$ of the startup circuit as

$$\gamma_{\text{startup}} = \frac{P_{\text{IN}} - P_{\text{T,startup}}}{P_{\text{IN}}}$$
(6)



1

Figure 5. Equivalent circuit of the startup circuit for loss analysis.

Figure 6a shows the calculated loss of the startup circuit as a function of V_{IN} . $P_{R,startup}$ increases with V_{IN} , and $P_{SW,startup}$ is negligible compared to $P_{R,startup}$ with a relatively low $f_{St} \approx 40$ kHz. Figure 6b shows that $\eta_{startup}$ decreases when V_{IN} increases for a given R_{IN} . Figure 6c shows that $P_{R,startup}$ decreases slightly with R_{IN} , which is mainly determined by V_{IN} . Figure 6d shows that $\eta_{startup}$ increases with R_{IN} while decreasing with V_{IN} , which is attributed to increased $P_{R,startup}$. In summary, increasing V_{IN} leads to elevated $P_{R,startup}$ and reduced $\eta_{startup}$. Increasing R_{IN} results in reduced $P_{R,startup}$ and improved $\eta_{startup}$.



Figure 6. Cont.



Figure 6. Calculated loss and efficiency of the startup circuit: (a) power loss, (b) efficiency as a function of V_{IN} for different R_{IN} , (c) conduction loss, and (d) efficiency as a function of R_{IN} for different V_{IN} .

2.4. Loss Analysis for Boost Converter

Figure 7 shows the equivalent circuit of the converter for loss analysis. The resistive power loss $P_{R,boost}$ of the boost converter can be written as

$$P_{\rm R,boost} = \left(\overline{I_{\rm CHA}}\right)^2 (R_{\rm IND} + R_{\rm N2}) + \left(\overline{I_{\rm DIS}}\right)^2 (R_{\rm IND} + R_{\rm P2}) \tag{7}$$

where I_{CHA} is the average inductor charging current when M_{N2} is on, and I_{DIS} is the average discharging current when M_{P2} is on $(M_{N2}$ is off). R_{N2} and R_{P2} are the on-resistances of M_{N2} and M_{P2} , respectively. In the typical boost converter, we can neglect the loss of M_{P2} with the condition of $(\overline{I_{CHA}} \gg \overline{I_{DIS}})$. The switching loss $P_{SW,boost}$ can be expressed as

$$P_{\rm SW,boost} = \frac{1}{2} \Big[(C_{\rm G,N2} + C_{\rm PAR}) V_{\rm DD}^2 + C_{\rm G,P2} (V_{\rm OUT} - V_{\rm TH,P2})^2 \Big] f_{\rm S} \cong \frac{1}{2} (C_{\rm G,N2} + C_{\rm G,P2} + C_{\rm PAR}) V_{\rm DD}^2 f_{\rm S}$$
(8)

where f_S is the switching frequency, and we use the approximated relationship of $V_{DD} \approx (V_{OUT} - V_{TH,P2})$. Here, $V_{TH,P2} = 0.52$ V is the threshold voltage of M_{P2}. $C_{G,N2}$ and $C_{G,P2}$ are the gate capacitance of M_{N2} and M_{P2}, respectively. $C_{PAR} = 21$ pF is the parasitic capacitance. We obtain $P_{SW,boost} = 200$ nW using $f_S = 8$ kHz, and $V_{DD} = 0.9$ V. The quiescent power $P_{Q,boost}$ of the boost converter is 420 nW. The total power loss $P_{T,boost}$ of the boost converter is the sum of $P_{R,boost}$, $P_{SW,boost}$, and $P_{Q,boost}$. The synchronization and leakage losses are neglected to simplify the analysis. Then, we obtain the end-to-end efficiency η_{EE} of the boost converter as

$$\eta_{\rm EE} = \frac{P_{\rm OUT}}{P_{\rm Max}} = \frac{P_{\rm Max} - P_{\rm T, boost}}{P_{\rm Max}} \tag{9}$$

where $P_{\text{Max}} = (V_{\text{S}})^2/(4R_{\text{S}})$ is the maximum available power from the source, and $P_{\text{OUT}} = (V_{\text{OUT}})^2/R_{\text{L}}$ is the output power with the load resistance R_{L} .



Figure 7. Equivalent circuit of the boost converter for loss analysis. $C_{IN} = 20 \text{ nF}$, $R_{IND} = 0.12 \Omega$, $C_L = 0.5 \mu$ F, and $R_L = 500 \text{ k}\Omega$.

Figure 8 shows the calculated η_{EE} as a function of R_{S} for different V_{S} using the switch parameters shown in Table 1. When R_{S} is reduced, increased $\overline{I_{\text{CHA}}}$ and $P_{\text{R,boost}}$ reduces η_{EE} . The η_{EE} improves with increasing R_{S} for a given V_{S} . For $R_{\text{S}} = 8 \Omega$ and $V_{\text{S}} = 300 \text{ mV}$, η_{EE} increases to 89.3%. Beyond the maximum point, increasing R_{S} reduces η_{EE} by the decreased P_{Max} .



Figure 8. Calculated efficiency of the converter as a function of *V*_S and *R*_S.

Table 1. Parameters of the power switches.

Power Switch	On-Resistance	Gate Capacitance	Size (W/L)
M _{N1}	$R_{ m N1}=0.40~\Omega$	$C_{G,N1} = 45.2 \text{ pF}$	2048 µm/35 nm
M _{N2}	$R_{\rm N2} = 0.18 \ \Omega$	$C_{G,N2} = 15.4 \text{ pF}$	2048 µm/35 nm
M _{P2}	$R_{\rm P2}=0.45\;\Omega$	$C_{G,P2} = 9.1 \text{ pF}$	4096 µm/35 nm

3. Implementation

3.1. Adaptive MPPT Controller

Figure 9a shows the schematic of the A-MPPT controller. It consists of a capacitorbased FOCV sampler, a comparator CM1, a counter, a programmable delay controller (PDC), and logic gates. In the FOCV technique, $V_{\text{MPP}} \approx (\alpha_{\text{MPP}}V_{\text{OC}})$ is obtained using the sampled open-circuit voltage $V_{\text{OC}} (\approx V_{\text{S}})$ and a source-dependent coefficient α_{MPP} , where $\alpha_{\text{MPP}} = 0.5$ is used for the TEG. The capacitive divider (C_{M1} and C_{M2}) generates V_{MPP} . When Φ_1 is high (Φ_2 is low), switch M_{M1} is turned on, and V_{OC} is stored in C_{M2} . When Φ_2 is high (Φ_1 is low), switch M_{M2} is turned on. The stored charge in C_{M2} is shared with C_{M1} . Then, the voltage V_{MPP} across C_{M2} becomes half of V_{OC} . CM1 compares V_{IN} against V_{MPP} , which decides the direction of the up/down counter. The counter output sets the delay of the PDC, and the on-time t_{N2} of Φ_{N2} is adjusted by the capacitor array in the PDC.

The R_{IN} of the DCM operation can be expressed [9] as

$$R_{\rm IN} = \frac{2L}{t_{\rm N2}^2 f_{\rm S}} \tag{10}$$

where we vary t_{N2} to adjust R_{IN} while keeping f_S constant. To facilitate the MPPT operation, the oscillator frequency f_{OSC} , which is higher than f_S , is used to update t_{N2} . This method is different from a previous approach [23], which adjusts t_{N2} after evaluating V_{MPP} rather than choosing between different V_{MPP} values. Figure 9b shows the simulated waveforms of the MPPT operation. In the beginning, V_{IN} increases to V_{OC} by the sampling operation. Using the output of CM1, the A-MPPT controller adjusts t_{N2} to vary R_{IN} for tracking the V_{IN} changes occurring between two consecutive V_{MPP} values. The A-MPPT controller consumes 430 nW at V_{DD} = 900 mV.



Figure 9. (a) Schematic of the A-MPPT controller; (b) simulated waveforms. $C_D = 80$ fF; $C_{M1} = C_{M2} = 1$ nF.

Figure 10 shows the flowchart further explaining the MPPT operation. The operation is based on the approximately linear relationship between V_{OC} and V_{MPP} . By leveraging this relationship, t_{N2} is adjusted to control R_{IN} and V_{IN} . In the case of ($V_{IN} < V_{MPP}$), t_{N2} is decreased to increase R_{IN} and V_{IN} . Conversely, t_{N2} increases to reduce R_{IN} . The proposed approach is simple since it requires measurements of only V_{OC} , even during temperature variations. Figure 11 shows the schematic of CM1. It is based on a PMOS differential input pair and is biased, using $I_{BIAS} = 5$ nA. The power consumption of CM1 is 40 nW at $V_{DD} = 0.9$ V.



Figure 10. Flowchart of the MPPT operation.



Figure 11. Schematic of the comparator.

3.2. Indirect ZCS Controller

Figure 12a shows the schematic of the I-ZCS controller. It comprises a comparator CM2, a counter, a PDC, sampling capacitors ($C_{1,2,3}$), and logic gates. The CM2 compares the current average output $V_{OUT,AVG}(n)$ against the previous output $V_{OUT,AVG}(n-1)$, which is obtained via the low pass filter (R_Z , C_Z). The CM2 outputs the up/down signal $\Phi_{U/D}$ for the counter, followed by the PDC that generates the adjustable delay Φ_{P2} for M_{P2} . Using the 6-b output Φ_{6b} , PDC either increases or decreases the on-time t_{P2} of Φ_{P2} . The PDC used for the I-ZCS controller has a similar structure to the one used in the A-MPPT controller. The Φ_{N2} is input to the PDC to set the starting reference for Φ_{P2} since the on-time of Φ_{N2} is used for inductor charging, while the on-time of Φ_{P2} is used for inductor discharging. At the end of discharging, the ZCS operation is performed.



Figure 12. (a) Schematic of the I-ZCS controller; (b) logic operation. $C_Z = 5$ fF; $R_Z = 36$ k Ω ; $C_1 = C_2 = C_3 = 16$ fF.

Using the waveform of I_{IND} , we can derive the expression for the change Δt_P in terms of output change $\Delta V_{OUT} = [V_{OUT,AVG}(n) - V_{OUT,AVG}(n-1)]$ as

$$|\Delta t_{\rm P2}| \cong \left(\frac{L}{t_{\rm N2}R_{\rm OUT}f_{\rm S}}\right) \frac{|\Delta V_{\rm OUT}|}{V_{\rm OUT}} \tag{11}$$

where Δt_{P2} is the difference between the current $t_{P2}(n)$ and the previous $t_{P2}(n-1)$. The derivation of the above relation is shown in Appendix A. The nomenclature used for the acronyms and symbols of this paper are listed in Appendix B. The working principle of the I-ZCS controller is based on MOVT. V_{OUT} is maximized when optimal t_{P2} is set for ZCS. In either case, when I_{IND} falls to zero before or after M_{P2} is switched off, the non-optimal ZCS operation reduces V_{OUT} ; when there is perfect inductor zero crossing, V_{OUT} is maximized. One advantage of an I-ZCS operation is that no I_{IND} sensor is needed. The t_{N2} of Φ_{N2} is determined by the A-MPPT controller, depending on the source impedance R_S . The t_{N2} does not have a direct effect on the I-ZCS controller since it is independently determined before the ZCS operation.

Waveforms for explaining I-ZCS operation are also shown. When $V_{OUT,AVG}(n)$ is greater than $V_{OUT,AVG}(n-1)$, the positive difference ($\Delta V_{OUT} > 0$) performs down-counting with low $\Phi_{U/D}$. The PDC reduces the number of active delay capacitance, decreasing the pulse width of t_{P2} . Conversely, the opposite condition ($\Delta V_{OUT} < 0$) performs up-counting to increase t_{P2} . Then, $\Phi_{U/D}$ switches between high and low until it reaches the steady state, when V_{OUT} is maximized by optimal ZCS operation. One drawback of this approach is that V_{OUT} is not fully regulated, which can be handled using additional regulators commonly used for various power supplies.

Figure 12b shows the logic operation to generate $V_{OUT,AVG}(n-1)$. After Φ_{N2} is turned off, Φ_{P2} turns on M_{P2} . The output Φ_Q is kept high until Φ_{P2} becomes high. With a high transition of Φ_{P2} , the output Φ_Q of the J/K flip-flop becomes low. When Φ_{P2} becomes low, Φ_{NOR} becomes high, which allows C_2 to be charged from C_1 . When Φ_{NOR} changes to low due to the rising Φ_{P2} , the voltage V_{C2} across C_2 is transferred to C_3 , generating $V_{OUT,AVG}$ (n-1). Figure 13 shows the simulated results of the I-ZCS controller. During the on-time of Φ_{N2} , I_{IND} increases. When Φ_{N2} turns off and Φ_{P2} turns on, I_{IND} decreases. The result shows that Φ_{P2} accurately switches off when the zero crossing of I_{IND} occurs. When I_{IND} reaches zero, M_{P2} turns off, initiating the DCM period indicated by T_{DCM} . The result shows the successful operation of the proposed I-ZCS controller.



Figure 13. Simulated waveforms of the I-ZCS controller.

4. Measured Results

Figure 14a shows the micrograph of the converter IC fabricated using a 28 nm CMOS process in an area of 0.03 mm². The IC is mounted on a test board using the chip-on-board (COB) technique. Figure 14b shows the experimental setup for the converter characteriza-

tion. A digital meter (DMM6500) is used for measuring the current. The DC power supply emulates the TEG source from 0.1 V to 0.4 V. The commercial TEG source is also used for testing [24].



Figure 14. (a) Micrograph of the fabricated converter IC; (b) experimental setup.

Figure 15 shows the measured waveform of the oscillator. When V_{RAMP} is higher than $V_{\text{REF}} = 600 \text{ mV}$, Φ_{OSC} is triggered high. The measured frequency of Φ_{OSC} is 44.4 kHz. Figure 16a shows the measured transient result of the self-startup. Using $V_{\text{IN}} = 250 \text{ mV}$ and $R_{\text{S}} = 20 \Omega$, V_{DD} is increased to 700 mV, which is enough to enable the boost converter. The steady state is reached after 2 sec. Using the commercial TEG having $V_{\text{IN}} = 200 \text{ mV}$, V_{DD} is increased to 600 mV, and the steady state is reached after 5 sec. These results demonstrate the successful operation of the self-startup. We further characterize the startup circuit using reduced V_{IN} . Figure 16b shows the measured result, in which $V_{\text{IN}} = 90 \text{ mV}$ is increased to $V_{\text{DD}} = 650 \text{ mV}$. The result shows that the gain-boosted tri-state buffer effectively reduces the minimum startup voltage.



Figure 15. Measured waveforms of the oscillator. $C_{OSC} = 22 \text{ pF. } R_{OSC} = 100 \text{ k}\Omega$ is used to set the bias current of the oscillator.



Figure 16. (a) Measured waveforms of the self-startup circuit using a power supply (left) and a commercial TEG (right). (b) Measured waveforms of the self-startup for $V_{\rm IN}$ = 90 mV. $R_{\rm S}$ = 30 Ω ; $C_{\rm IN}$ = 0.47 μ F.

Figure 17 shows the measured waveforms of the converter. The experiment is performed using $V_{IN} = 250 \text{ mV}$ and $R_S = 20 \Omega$. When Φ_{N2} is high, *L* is charged. When Φ_{N2} is triggered to low, the energy stored in *L* is transferred to the output. When V_{IND} reaches the ground, Φ_{P2} becomes high to turn off M_{P2} via the I-ZCS controller. The ringing is caused by the *LC* resonance when M_{P2} is turned off. Overall capacitance, including C_L , forms resonance with *L*, and the amplitude is decayed by the path loss.



Figure 17. Measured waveforms of the boost converter. C_{IN} = 0.47 $\mu F\!$

Figure 18a shows the measured tracking efficiency $\eta_{\text{MPPT}} = (P_{\text{IN}}/P_{\text{Max}})$ as a function of V_S. The results show that $\eta_{\text{MPPT}} > 93\%$ is achieved in the V_S range from 135 mV to 300 mV, with the peak η_{MPPT} of 95.2%. Figure 18b shows the measured conversion efficiency $\eta_{\text{CONV}} = (P_{\text{OUT}}/P_{\text{IN}})$ as a function of P_{OUT} . P_{OUT} is changed from 77 µW to 1.28 mW by varying R_{L} . The peak $\eta_{\text{CONV}} = 85.9\%$ is achieved for $P_{\text{OUT}} = 1.07$ mW. Figure 19 shows the measured $\eta_{\text{EE}} = (P_{\text{OUT}}/P_{\text{Max}})$ of the converter as a function of V_{S} for different R_{S} . Because P_{Max}

is reduced, η_{EE} decreases with increasing R_{S} . The result shows that peak η_{EE} = 83.7% is achieved using R_{S} = 8 Ω and V_{S} = 280 mV.



Figure 18. (a) Measured tracking efficiency of the converter; (b) measured conversion efficiency of the converter. V_{IN} = 200 mV; R_S = 18 Ω .



Figure 19. Measured end-to-end efficiency of the converter as a function of V_S for different R_S . $R_L = 4.7 \text{ k}\Omega$.

Table 2 shows the comparison with previous works using the boost converter for energy harvesting [25–32]. Our approach introduces a novel technique for self-startup using the tri-state buffer, distinguishing it from the studies conducted in [26,29], which relied on a single buffer. Notably, the proposed self-startup circuit achieves a minimum startup voltage of 90 mV, outperforming all the works except [30]. Furthermore, our proposed A-MPPT and I-ZCS controllers achieve a relatively high conversion efficiency of 85.9%. In comparison, the efficiencies observed in [25,28,32] are 74.5%, 75.0%, and 25.0%, respectively. In addition, our compact design has the smallest chip area (0.03 mm²) among the works, including ICs implemented using the same technology node of a 28 nm CMOS [31,32]. The result shows that our work effectively handles the previous issue of bulky implementations. Consequently, our research provides practical and efficient solutions for low-cost wearable electronics and IoT applications.

	[25]	[26]	[27]	[28]	[29]	[30]	[31]	[32]	This Work
Process	65 nm	180 nm	180 nm	180 nm	180 nm	180 nm	28 nm	28 nm	28 nm
Energy source	TEG	TEG, PV	TEG	TEG, PZ	TEG	PV	TEG, PV, BFC, Battery	TEG, RF	TEG
Туре	Boost	Buck-Boost	Boost	Boost	Boost	Boost	Buck-Boost	Boost	Boost
Startup technique	OSC + CP	Ring OSC + CP	СР	_	Ring OSC + CP	СР	Battery	LC OSC	Tri-state buffer, Ring OSC
Minimum startup voltage	210 mV	370 mV	500 mV	100 mV	129 mV	80 mV	-	110 mV	90 mV
ZCS technique	Dynamic comp.	gate comparators	One shot pulse gen.	Latched comp.	D-F/F	Comparator, D-F/F	Digital calibration	_	* MOVT
MPPT technique	FOCV	FOCV	⁺ AIR	⁺⁺ DPR	OCV	⁺⁺⁺ SRFG	FOCV	++++ ASF	FOCV
η_{CONV}	74.5% @ P _{OUT} = 229 μW	_	_	75.0% @ P _{OUT} = 450 μW	_	89.0% @ P _{OUT} = 0.12 mW	89.0% @ P _{OUT} = 20 mW	25.0% @ P _{OUT} = 0.52 mW	85.9% @ P _{OUT} = 1.07 mW
$\eta_{\rm EE}$	71.5% @ V _{IN} = 240 mV	82.1% @ V _{IN} = 600 mV	82.0% @ V _{IN} = 600 mV	_	84.0% @ V _{IN} = 260 mV	86.0% @ V _{IN} = 260 mV	_	10.0% @ N/A	83.7% @ V _{IN} = 280 mV
V _{OUT}	0.86–1.4 V	1.2 V	1–1.2 V	3–4 V	0.8 V	1.2 V	0.4–1.4 V	_	1.4 V
Area (mm ²)	4.57	1.23	1.1	1.5	1.62	1.5	0.5	0.46	0.03

 Table 2. Performance comparison.

* Maximum output voltage tracking; [†] Adaptive input ripple; ⁺⁺ Double pile-up resonance; ⁺⁺⁺ Self-controlled resonant frequency generator; ⁺⁺⁺⁺ Adaptive switching frequency.

5. Conclusions

In this paper, we propose a compact and efficient boost converter in a 28 nm CMOS for thermoelectric energy harvesting. For self-startup, we use a gain-boosted tri-state buffer in a ring oscillator to achieve a 90 mV minimum startup. A comparison with the single inverter shows that the proposed tri-state buffer achieves a 69.8% improvement in the DC gain. To extract the maximum power from the TEG, we use a FOCV-based A-MPPT controller. To remove the current sensor required by the conventional approach, we propose an I-ZCS controller to achieve an efficient DCM operation. The converter is fabricated in a 28 nm COMS process realized in a compact area of 0.03 mm². The measured data show a successful I-ZCS operation using the proposed MOVT technique. Using the A-MPPT controller, the converter achieves a peak tracking efficiency of 95.2%. The converter delivers the output power of 1.07 mW with a peak conversion efficiency of 85.9%. Using the proposed techniques, TEG energy harvesting can be realized in a compact system. These characteristics are suitable for various applications, including wearable electronics, medical implants, and IoT devices.

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Appendix A

Figure A1 shows the inductor current I_{IND} waveform of the boost converter. The I_{IND} is the sum of I_{CHA} during t_{N2} and I_{DIS} during t_{P2} . Assuming V_{IN} slowly varies during the conversion, the voltage difference across L for I_{CHA} can be expressed as

$$V_{\rm IN} - 0 = L \frac{dI_{\rm IND}}{dt} \cong L \frac{I_{\rm P}}{t_{\rm N2}} \tag{A1}$$

where $I_P \approx V_{IN}(t_{N2}/L)$ denotes the peak current. Using the voltage across the inductor at t_{P2} , we obtain another expression for the peak current I_P :

$$I_{\rm P} = \frac{(V_{\rm OUT} - V_{\rm IN})t_{\rm P2}}{L}$$
(A2)



Figure A1. Inductor current waveform of the boost converter.

$$A_2 = \frac{1}{2} t_{\rm P2} I_{\rm P} = \frac{1}{2L} t_{\rm P2}^2 (V_{\rm OUT} - V_{\rm IN})$$
(A3)

Then, the output current *I*_{OUT} can be expressed as

$$I_{\rm OUT} = \frac{t_{\rm P2}^2}{2L} (V_{\rm OUT} - V_{\rm IN}) f_{\rm S}$$
(A4)

where f_S is the switching frequency. Using the I_{OUT} expression of (A4), we obtain the output resistance R_{OUT} as

$$R_{\rm OUT} = \frac{V_{\rm OUT}}{(V_{\rm OUT} - V_{\rm IN})f_S} \frac{2L}{t_{\rm P2}^2}$$
(A5)

Rearranging (A5) for t_{P2} , we obtain

$$t_{\rm P2}^2 = \frac{2L}{R_{\rm OUT} f_{\rm S}} \frac{V_{\rm OUT}}{(V_{\rm OUT} - V_{\rm IN})} \tag{A6}$$

For the present state, we use the discharging time as $t_{P2}(n)$ and the average output as $V_{OUT,AVG}(n)$. Similarly, for the previous state, we use $t_{P2}(n-1)$ and $V_{OUT,AVG}(n-1)$. Then, we obtain

$$t_{\rm P2}^2(n) = \frac{2L}{R_{\rm OUT}f_{\rm S}} \frac{V_{\rm OUT,AVG}(n)}{(V_{\rm OUT,AVG}(n) - V_{\rm IN})}$$
(A7)

$$t_{\rm P2}^2(n-1) = \frac{2L}{R_{\rm OUT}f_{\rm S}} \frac{V_{\rm OUT,AVG}(n-1)}{(V_{\rm OUT,AVG}(n-1) - V_{\rm IN})}$$
(A8)

Subtracting (A8) from (A7), we obtain

$$t_{P2}^{2}(n) - t_{P2}^{2}(n-1) = 2t_{P2} \times \Delta t_{P2} = \left[\frac{V_{OUT,AVG}(n)}{V_{OUT,AVG}(n) - V_{IN}} - \frac{V_{OUT,AVG}(n-1)}{V_{OUT,AVG}(n-1) - V_{IN}}\right] \frac{2L}{R_{OUT}f_{S}}$$
(A9)

where $\Delta t_{P2} = t_{P2}(n) - t_{P2}(n-1)$. Assuming $V_{OUT}(n) \approx V_{OUT,AVG}(n-1)$ under a small-signal operation and $(V_{OUT} \gg V_{IN})$ for the boost converter, we can simplify (A9) as

$$2t_{\rm P2} \times \Delta t_{\rm P2} = -\Delta V_{\rm OUT} \left(\frac{2L}{R_{\rm OUT} f_{\rm S}}\right) \left(\frac{V_{\rm IN}}{V_{\rm OUT}^2}\right) \tag{A10}$$

where $\Delta V_{\text{OUT}} = V_{\text{OUT,AVG}}(n) - V_{\text{OUT,AVG}}(n-1)$. Using (A1) and (A2), we obtain the expression for t_{P2} as

$$t_{\rm P2} = t_{\rm N2} \frac{V_{\rm IN}}{V_{\rm OUT} - V_{\rm IN}} \cong t_{\rm N2} \frac{V_{\rm IN}}{V_{\rm OUT}}$$
 (A11)

Using (A10) and (A11), we obtain

$$\Delta t_{P2} = -\frac{\Delta V_{OUT}}{2t_{P2}} \left(\frac{2L}{R_{OUT}f_{S}}\right) \left(\frac{V_{IN}}{V_{OUT}^{2}}\right) = -\Delta V_{OUT} \left(\frac{L}{R_{OUT}f_{S}}\right) \left(\frac{V_{IN}}{V_{OUT}^{2}}\right) \frac{V_{OUT}}{t_{N2}V_{IN}}$$

$$= -\left(\frac{L}{t_{N2}R_{OUT}f_{S}}\right) \frac{\Delta V_{OUT}}{V_{OUT}}.$$
(A12)

The nomenclature used	in this paper are listed below.
Symbol	Definition
A-MPPT	Adaptive maximum power point tracking
DCM	Discontinuous conduction mode
FOCV	Fractional open circuit voltage
I-ZCS	Indirect zero current switching
MOVT	Maximum output voltage tracking
MPPT	Maximum power point tracking
PDC	Programmable delay controller
ZCS	Zero current switching
VD	Voltage detector
LVT	Low threshold voltage
HVT	High threshold voltage
SVT	Standard threshold voltage
SLVT	Super-low threshold voltage
SC	Switched capacitor
I _{IND}	Inductor current
V _{TH}	Threshold voltage
$A_{\rm V1}$	Voltage gain of a single inverter
$A_{\rm V2}$	Voltage gain of the gain-boosted buffer
P _{R,startup}	Resistive power loss of startup circuit
P _{SW,startup}	Switching loss of startup circuit
P _{Q,startup}	Power consumption of startup circuit
P _{R,boost}	Resistive power loss of boost converter
P _{SW,boost}	Switching loss of boost converter
P _{Q,boost}	Power consumption of boost converter
$V_{\rm OUT,AVG}(n)$	Current average output voltage
$V_{\text{OUT,AVG}}(n-1)$	Previous average output voltage

Appendix B

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