

## Article

# 0.3-V Voltage-Mode Versatile First-Order Analog Filter Using Multiple-Input DDTAs

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**Abstract:** This paper presents a versatile first-order analog filter using differential difference transconductance amplifiers (DDTAs). The DDTA employs the bulk-driven (BD) multiple-input MOS transistors technique (MI-MOST) operating in the subthreshold region. This results in low-voltage and low-power operational capability. Therefore, the DDTA, designed using 130 nm CMOS technology from UMC in the Cadence environment, operates with 0.3 V and consumes 357.4 nW. Unlike previous works, the proposed versatile first-order analog filter provides first-order transfer functions of low-pass, high-pass, and all-pass filters within a single topology. The non-inverting, inverting, and voltage gain of the transfer functions are available for all filters. Furthermore, the proposed structure provides high-input and low-output impedance, which is required for voltage-mode circuits. The pole frequency and voltage gain of the filters can be electronically controlled. The total harmonic distortion of the low-pass filter was calculated as  $-39.97$  dB with an applied sine wave input signal of  $50$  mV<sub>pp</sub>@  $50$  Hz. The proposed filter has been used to realize a quadrature oscillator to confirm the advantages of the new structure.

**Keywords:** differential difference transconductance amplifier; analog filter; voltage-mode circuit; low-voltage low-power circuit



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## 1. Introduction

The second-generation current conveyor (CCII) was introduced in [1] as a single active building block, namely containing a voltage follower between the y- and x-terminals and a current follower between the x- and z-terminals. To increase the performance of the CCII for handling differential input signals, a differential difference current conveyor (DDCC) was proposed [2]. A DDCC includes the advantages of both CCII and the differential difference amplifier (DDA) [3] within a single circuit. One such advantage is a high input impedance and arithmetic operation capability, which is valuable for voltage-mode circuits. However, the circuits based on DDCCs lack electronic tuning capability. Thus, the next phase of development of DDCCs has been to obtain electronic tuning capability, for example, as a differential difference current conveyor transconductance amplifier (DDCCTA) [4], differential difference transconductance amplifier (DDTA) [5], or differential voltage current conveyor transconductance amplifier (DVCCTA) [6]. Recently, the DDTA has been designed to operate with a low power supply and low power consumption and has been successfully utilized for various applications with analog filters [7–12].

First-order filters are single-pole circuits that are widely used in signal processing. There are three filtering functions to realize first-order transfer functions: low-pass (LP),

high-pass (HP), and all-pass (AP) filters. The first-order LP and HP filters can be used as subcircuits to realize high-order filters [13–16], while the first-order AP filters are an important block of high-quality (Q) band-pass (BP) filters [17], sinusoidal oscillators [18], time delays [19], group-delay or phase equalizers [20].

Universal first-order filters are topologies that can realize the first-order transfer functions of LP, HP, AP filters into a single circuit. There are many universal first-order filters available in open literature [21–55]. Nowadays, the topic of the first-order universal filter is an interesting area for research. Considering the input and output signals of universal first-order filters in [21–55], these topologies can be classified as current-mode (CM) filters [21–35], voltage-mode (VM) filters [36–51], mixed-mode (MM) filters [52–55]. Focusing on the CM filters, the circuits in [21,29] offer maximum first-order transfer functions of LP, HP, AP filters. With a suitable choice of the output currents, the filters in [21,29] offer both non-inverting and inverting transfer functions of LP, HP, AP filters, thus obtaining six transfer functions. However, the gain of the transfer functions cannot be controlled. Considering the VM filters in [36–51], the filters in [41,43–46] offer the voltage gain of the transfer functions, but these filters can control the gain only for a few transfer functions, such as LP and HP filters.

The MM filters are topologies that offer four types of transfer functions in a single circuit: VM, CM, trans-admittance mode (TAM), and trans-impedance mode (TIM). Considering MM filters in [52–55], the filters in [52–54] offer four types of transfer functions (CM, VM, TIM, TAM), but each type offers only three transfer functions of LP, HP, and AP filters.

In this work, a voltage-mode versatile first-order analog filter based on DDTA as an active element is presented. The work shows that the multiple-input DDTA (MI-DDTA) can offer an easy choice for voltage-mode first-order filters. The MI-DDTAs with 0.3 V and 357.4 nW consumption were used, with the bulk-driven (BD) technique of multiple-input MOS transistors (MI-MOST) operating in the subthreshold region. Unlike previous works, the proposed versatile first-order analog filter can realize both non-inverting and inverting transfer functions of LP, HP, and AP filters in a single circuit. In addition, the voltage gain of all transfer functions can be controlled. The proposed structure provides high-input and low-output impedance, which is ideal for voltage-mode circuits. Furthermore, both the pole frequency and voltage gain of all filters can be controlled electronically. The proposed filter has been used to realize a quadrature oscillator to confirm the advantages of the new structure.

## 2. Proposed Circuit

### 2.1. CMOS Structure of the Multiple-Input DDTA

Figure 1 shows the electrical symbol of the DDTA. The *y*- and *o*-terminals possess a high impedance level, while the *w*-terminal possesses a low impedance level. The addition and subtraction voltages at the *w*-terminal ( $V_w$ ) are transformed to a current at the *o*-terminal by the transconductance  $g_m$ . The port characteristic of the DDTA can be expressed as:

$$\left. \begin{aligned} V_w &= V_{+1} + V_{+2} - V_{-1} - V_{-2} \\ I_o &= g_m V_w \end{aligned} \right\} \quad (1)$$

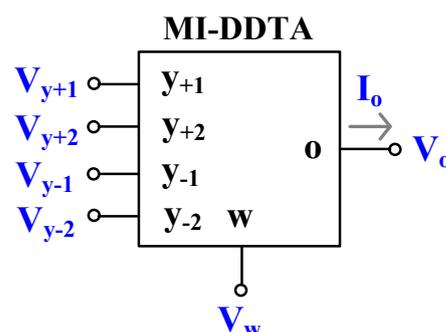


Figure 1. Electrical symbol of the MI-DDTA.

The CMOS structure of the LV LP DDTA was first presented in [10]. The circuit, as shown in Figure 2, consists of two main blocks: a differential-difference current conveyor (DDCC) and a transconductance amplifier (TA). The DDCC can be considered as a two-stage amplifier with a differential difference input stage ( $M_1$ – $M_8$ ) and a second stage based on the transistor ( $M_{10}$ ) operating in a common source configuration. The capacitance  $C_C$  is used for frequency compensation. The input stage of the DDCC is based on a bulk-driven non-tailed differential pair with partial positive feedback [56,57]. The non-tailed architecture allows operation at very low supply voltages, while providing good common-mode and power supply rejection ratios (CMRR and PSRR, respectively) [56,57]. The BD technique achieves a large common-mode range, which is usually rail-to-rail. In order to improve the voltage gain of the differential amplifier, partial positive feedback (PPF) is introduced by the cross-coupled pair of transistors,  $M_7$  and  $M_8$ . The transistors generate negative conductances, which partially compensate for the total conductances at the gate/drain nodes of  $M_{2A}$  and  $M_{2B}$ , thus increasing the voltage gain of the whole input stage. The differential difference capability is realized using an MI-BD technique, i.e., using an additional capacitive voltage summing circuit. A particular realization of the MI-BD transistors is shown in Figure 3. The capacitors ( $C_{Bi}$ ) form a voltage divider/voltage summing circuit. In a passband, their impedances are much lower than the resistances of the large resistors ( $R_{MOS}$ ). The resistors are realized as an anti-parallel connection of two minimum-size MOS transistors operating in a cut-off region (Figure 3c), which are used to provide proper biasing of the bulk terminals of the input MOS transistors for DC. This solution provides differential difference capability without using a second transistor pair, thus saving dissipation power and simplifying the overall structure. The voltage  $V_w$  can then be expressed as:

$$V_w = \frac{A_v}{1 + A_v} (V_{+1} + V_{+2} - V_{-1} - V_{-2}) \quad (2)$$

where the open-loop gain  $A_v$  can be expressed as:

$$A_v = \beta \cdot \frac{2g_{mb1}}{1 - m} (r_{ds1} || r_{ds6}) g_{m10} (r_{ds9} || r_{ds10}) \quad (3)$$

where  $\beta$  is the voltage gain of the input capacitive divider. Assuming equal capacitances,  $C_{Bi}$  is equal to 1/3, and  $m = g_{m7,8}/g_{m2A,B}$  is the coefficient associated with PPF. Note that for stable operation, the value of  $m$  should always be less than unity. In the proposed design,  $m = 0.75$ .

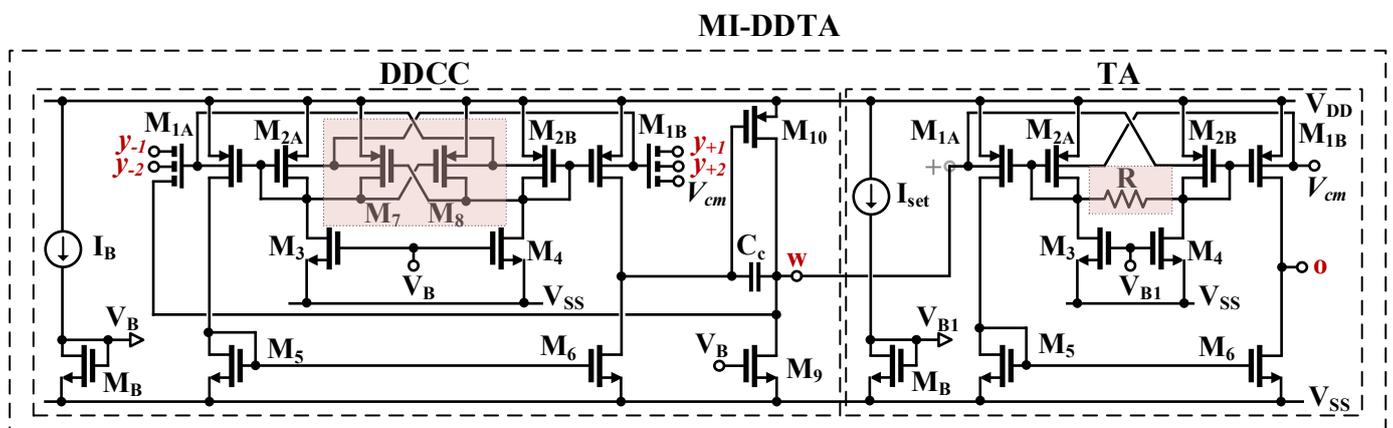


Figure 2. CMOS implementation of the MI-DDTA.

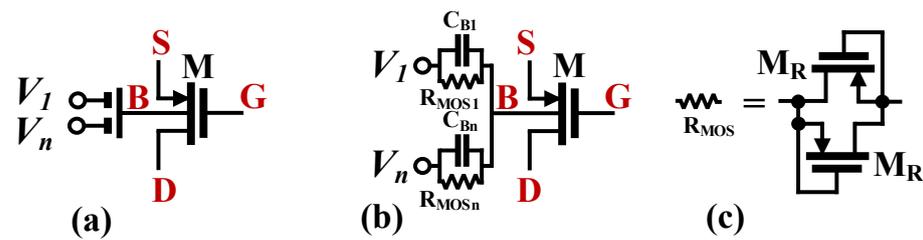


Figure 3. MI-BD MOST: (a) symbol, (b) realization, (c) possible implementation of  $R_{MOS}$ .

The output resistance of the DDCC, seen from the  $w$  terminal, can be expressed as:

$$r_{outW} = \frac{1}{\beta \cdot \frac{2g_{mb1}}{1-m} (r_{ds1} || r_{ds6}) g_{m10}} \quad (4)$$

and is typically 20–30 times lower than  $1/g_{m10}$ .

The second block of the proposed DDTA, namely the transconductance amplifier, was originally proposed and verified experimentally in [58]. The circuit can be seen as a non-tailed differential pair ( $M_1$ – $M_6$ ), with an additional linearization resistor  $R$ . Assuming  $M_1 = M_2$ , the circuit transconductance can be expressed as [58]:

$$g_m = 2g_{mb1,2} \frac{R + \frac{1}{g_{m1,2}}}{R + \frac{2}{g_{m1,2}}} \quad (5)$$

The circuit shows optimum linearity when the following condition is satisfied [58]:

$$R = \frac{1}{g_{m1,2}} \quad (6)$$

However, the circuit linearity remains good even for relatively large differences between  $R$  and  $1/g_{m1,2}$ . This enables the tuning of the transconductance of the TA with the biasing current  $I_{set}$ . The voltage gain of the TA can be expressed as:

$$A_{VTA} = g_m (r_{ds1} || r_{ds6}) \quad (7)$$

Due to the non-cascode structure, its value is relatively low but sufficient for the proposed application.

## 2.2. Proposed Voltage-Mode First-Order Versatile Analog Filter

Figure 4 shows the proposed voltage-mode first-order analog filter employing two MI-DDTAs, one grounded capacitor  $C_1$  and one grounded resistor,  $R_1$ . The  $V_{in1}$ ,  $V_{in2}$ ,  $V_{in3}$ , and  $V_{in4}$  are the input voltages, while  $V_{o1}$  and  $V_{o2}$  are the output voltages. The inputs,  $V_{in1}$ ,  $V_{in2}$ ,  $V_{in3}$ , and  $V_{in4}$ , are applied via the high-impedance level (y-terminal) of the MI-DDTA, while the output  $V_{o1}$  is available at the low-impedance level (w-terminal) of the MI-DDTA. Thus, the proposed filter possesses high-input and low-output impedances.

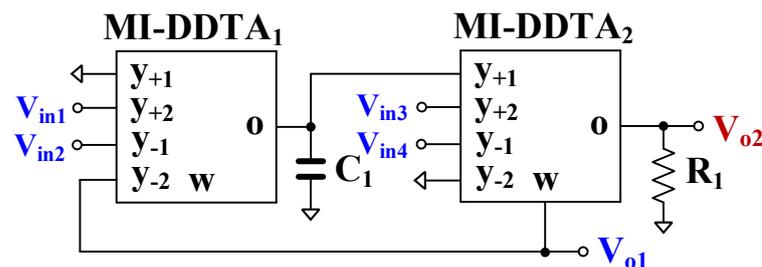


Figure 4. Proposed voltage-mode first-order universal analog filter.

From Figure 4, using (1) and nodal analysis, the outputs  $V_{o1}$  and  $V_{o2}$  can be expressed, respectively, as:

$$V_{o1} = \frac{sC_1(V_{in3} - V_{in4}) + g_{m1}(V_{in1} - V_{in2})}{sC_1 + g_{m1}} \quad (8)$$

$$V_{o2} = g_{m2}R_1 \left( \frac{sC_1(V_{in3} - V_{in4}) + g_{m1}(V_{in1} - V_{in2})}{sC_1 + g_{m1}} \right) \quad (9)$$

The LP, HP, AP filtering functions can be obtained by suitably applying the input voltages to the circuit. The variant filtering functions of first-order filters are shown in Table 1. It is obvious that the non-inverting and inverting transfer functions of LP, HP, AP filters can be obtained in a single circuit without the need for an inverted input signal. The voltage gain of all transfer functions is obtained at the output  $V_{o2}$ , which can be controlled by  $g_{m2}R_1$ . The electronic tuning capability is obtained by varying  $g_{m2}$ . However, since this output node does not have a low-impedance level, a buffer circuit may be required if a low-impedance load is connected.

**Table 1.** Obtaining variant filtering functions of the first-order analog filter.

Filtering Function		Input	Transfer Function	
LP	Non-inverting	$V_{in1} = V_{in}$	$\frac{V_{o1}}{V_{in}} = \frac{g_{m1}}{sC_1 + g_{m1}}$	$\frac{V_{o2}}{V_{in}} = g_{m2}R_1 \left( \frac{g_{m1}}{sC_1 + g_{m1}} \right)$
	Inverting	$V_{in2} = V_{in}$	$\frac{V_{o1}}{V_{in}} = -\frac{g_{m1}}{sC_1 + g_{m1}}$	$\frac{V_{o2}}{V_{in}} = -g_{m2}R_1 \left( \frac{g_{m1}}{sC_1 + g_{m1}} \right)$
HP	Non-inverting	$V_{in3} = V_{in}$	$\frac{V_{o1}}{V_{in}} = \frac{sC_1}{sC_1 + g_{m1}}$	$\frac{V_{o2}}{V_{in}} = g_{m2}R_1 \left( \frac{sC_1}{sC_1 + g_{m1}} \right)$
	Inverting	$V_{in4} = V_{in}$	$\frac{V_{o1}}{V_{in}} = -\frac{sC_1}{sC_1 + g_{m1}}$	$\frac{V_{o2}}{V_{in}} = -g_{m2}R_1 \left( \frac{sC_1}{sC_1 + g_{m1}} \right)$
AP	Non-inverting (Phase lag)	$V_{in2} = V_{in3} = V_{in}$	$\frac{V_{o1}}{V_{in}} = \frac{sC_1 - g_{m1}}{sC_1 + g_{m1}}$	$\frac{V_{o2}}{V_{in}} = g_{m2}R_1 \left( \frac{sC_1 - g_{m1}}{sC_1 + g_{m1}} \right)$
	Inverting (Phase lead)	$V_{in1} = V_{in4} = V_{in}$	$\frac{V_{o1}}{V_{in}} = -\frac{sC_1 - g_{m1}}{sC_1 + g_{m1}}$	$\frac{V_{o2}}{V_{in}} = -g_{m2}R_1 \left( \frac{sC_1 - g_{m1}}{sC_1 + g_{m1}} \right)$

The pole frequency of all transfer functions can be expressed by:

$$\omega_o = \frac{g_{m1}}{C_1} \quad (10)$$

The pole frequency can be controlled by  $g_{m1}$ . Therefore, the voltage gain and the pole frequency can be electronically controlled.

### 2.3. Non-Ideality Analysis

The non-ideal characteristics of MI-DDTA can be considered as [11]:

$$\left. \begin{aligned} V_w &= \beta_{+1j}V_{+1} + \beta_{+2j}V_{+2} - \beta_{-1j}V_{-1} - \beta_{-2j}V_{-2} \\ I_o &= g_{mnj}V_w \end{aligned} \right\} \quad (11)$$

where, for the  $j$ -th DDTA,  $\beta_{+1j}$  is the voltage gain between  $V_{+1}$  and  $V_w$ ,  $\beta_{+2j}$  is the voltage gain between  $V_{+2}$  and  $V_w$ ,  $\beta_{-1j}$  is the voltage gain between  $V_{-1}$ , and  $V_w$ ,  $\beta_{-2j}$  is the voltage gain between  $V_{-2}$  and  $V_w$ , of  $j$ -th DDTA, and  $g_{mnj}$  is the non-ideal transconductance of the  $j$ -th MI-DDTA. Ideally, the voltage gains,  $\beta_{+1}$ ,  $\beta_{-2}$ ,  $\beta_{-1}$ ,  $\beta_{+2}$ , are equal to unity. However, these voltage gains may slightly deviate from ideality and affect the transfer functions of the proposed filter.

For the DDTA operating near the cut-off frequency,  $g_{mnj}$  can be approximated by [11]:

$$g_{mnj} = g_{mj}(1 - \mu_j s) \quad (12)$$

where  $\mu_j = 1/\omega_{gj}$ , and  $\omega_{gj}$  denotes the first pole of the  $j$ -th MI-DDTA.

Using (11), (8) and (9) can be rewritten, respectively as:

$$V_{o1} = \frac{sC_1(\beta_{+22}V_{in3} - \beta_{-12}V_{in4}) + g_{mn1}(\beta_{+21}\beta_{+12}V_{in1} - \beta_{-11}\beta_{+12}V_{in2})}{sC_1 + \beta_{-21}\beta_{+12}g_{mn1}} \quad (13)$$

$$V_{o2} = g_{mn2}R_1 \left( \frac{sC_1(\beta_{+22}V_{in3} - \beta_{-12}V_{in4}) + g_{mn1}(\beta_{+21}\beta_{+12}V_{in1} - \beta_{-11}\beta_{+12}V_{in2})}{sC_1 + \beta_{-21}\beta_{+12}g_{mn1}} \right) \quad (14)$$

The non-ideal transfer functions of LP, HP, AP filters can be expressed by:

$$\frac{V_{o1}}{V_{in1}} = \frac{\beta_{+21}\beta_{+12}g_{mn1}}{sC_1 + \beta_{-21}\beta_{+12}g_{mn1}} \quad (15)$$

$$\frac{V_{o1}}{V_{in2}} = -\frac{\beta_{-11}\beta_{+12}g_{mn1}}{sC_1 + \beta_{-21}\beta_{+12}g_{mn1}} \quad (16)$$

$$\frac{V_{o1}}{V_{in3}} = \frac{sC_1\beta_{+22}}{sC_1 + \beta_{-21}\beta_{+12}g_{mn1}} \quad (17)$$

$$\frac{V_{o1}}{V_{in4}} = -\frac{sC_1\beta_{-12}}{sC_1 + \beta_{-21}\beta_{+12}g_{mn1}} \quad (18)$$

Letting  $V_{in2} = V_{in3} = V_{in}$ , we obtain:

$$\frac{V_{o1}}{V_{in}} = \frac{sC_1\beta_{+22} - \beta_{-11}\beta_{+12}g_{mn1}}{sC_1 + \beta_{-21}\beta_{+12}g_{mn1}} \quad (19)$$

Letting  $V_{in1} = V_{in4} = V_{in}$ , we obtain:

$$\frac{V_{o1}}{V_{in}} = -\frac{sC_1\beta_{-12} - \beta_{+21}\beta_{+12}g_{mn1}}{sC_1 + \beta_{-21}\beta_{+12}g_{mn1}} \quad (20)$$

Using (12), the denominator of all transfer functions ( $D(s)$ ) can be expressed by:

$$D(s) = sC_1 \left( 1 - \frac{\beta_{-21}\beta_{+12}\mu_1 g_{m1}}{C_1} \right) + \beta_{-21}\beta_{+12}g_{m1} \quad (21)$$

The non-ideal transconductance can be made negligible by satisfying:

$$\frac{\beta_{-21}\beta_{+12}\mu_1 g_{m1}}{C_1} \ll 1 \quad (22)$$

If the non-ideal behavior of the DDTA operating at a high frequency is also considered, the parallel connection of parasitic resistance ( $R_o$ ) and parasitic capacitance ( $C_o$ ) at the o-terminal should be taken in account ( $R_o // C_o$ ) [43]. In consideration of the non-ideal behavior of the DDTA given by  $R_o // C_o$ , the pole frequency of Figure 4 obtained from (21), while satisfying (22), can be determined by:

$$\omega_{on} = \frac{\beta_{-21}\beta_{+12}g_{m1}}{C'_1} \quad (23)$$

where  $C'_1 = C_1 + C_{o1}$  and  $R_{o1} \gg 1/g_{m1}$ ,  $C_{o1}$  and  $R_{o1}$  are the parasitic capacitance and resistance at the o-terminal of MI-DDTA<sub>1</sub>.

### 3. Application Example

To demonstrate the advantages of the proposed versatile filter, two first-order AP filters, namely non-inverting and inverting AP filters based on the same topology, have been used to realize a sinusoidal oscillator as shown in Figure 5.

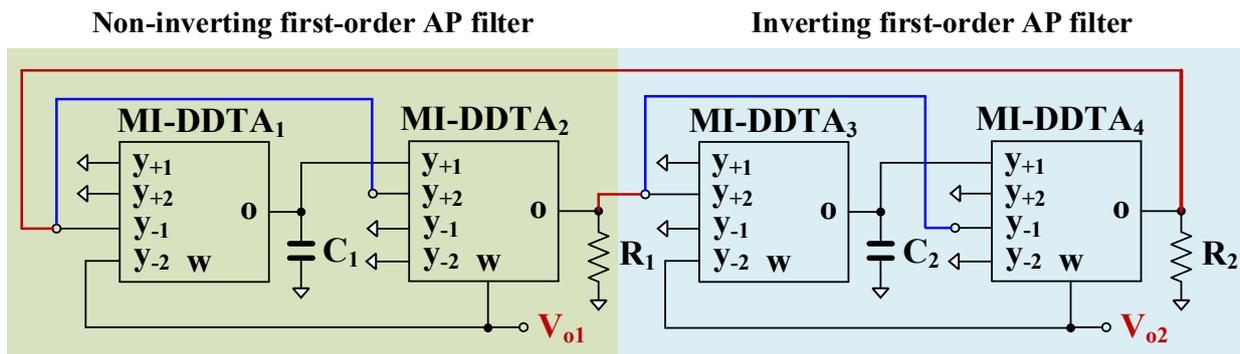


Figure 5. Proposed sinusoidal oscillator using first-order AP filters.

Using Table 1 and the row for AP filters, the loop gain (LG) of the oscillator can be given as:

$$LG(s) = -g_{m2}R_1g_{m4}R_2 \left( \frac{sC_1 - g_{m1}}{sC_1 + g_{m1}} \right) \left( \frac{sC_1 - g_{m3}}{sC_1 + g_{m3}} \right) \quad (24)$$

Letting  $g_{m1} = g_{m3} = g_{mf}$ ,  $C_1 = C_2 = C_f$ , and  $LG = 1$ , the characteristics of the oscillator can be expressed by:

$$g_{m2}R_1g_{m4}R_2 \left( \frac{sC_f - g_{mf}}{sC_f + g_{mf}} \right)^2 = 0 \quad (25)$$

The condition of oscillation (CO) can be given by:

$$g_{m2}R_1g_{m4}R_2 = 1 \quad (26)$$

The frequency of oscillation (FO) can be given as:

$$\omega_o = \left( \frac{g_{mf}}{C_f} \right) \tan\left(\frac{\pi}{4}\right) \quad (27)$$

From (15) and (26), the CO can be controlled electronically by  $g_{m2}$  and/or  $g_{m4}$  and the FO can be controlled electronically by  $g_{mf}$ .

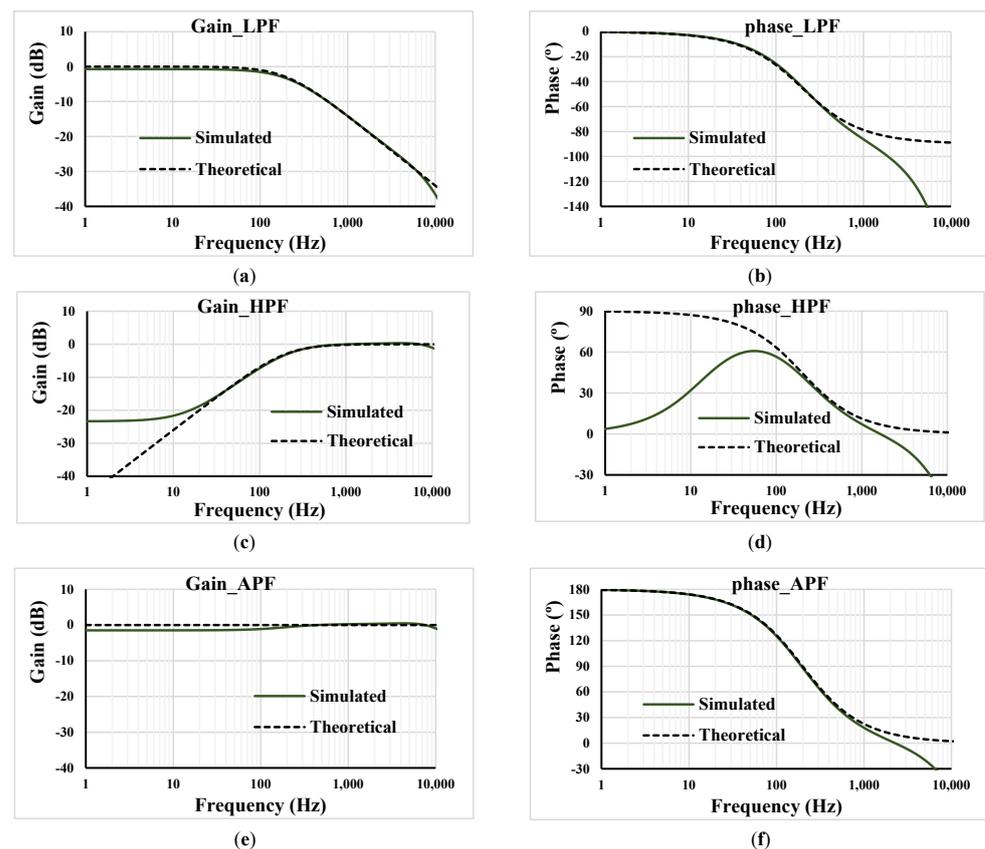
#### 4. Simulation Results

The circuit was designed and simulated using the Cadence Virtuoso Analog Design Environment with 130 nm using UMC CMOS technology. The transistor's aspect ratio and the values of passive devices are shown in Table 2. The voltage supply was 0.3 V ( $\pm 0.15$  V), the bias current of the DDCC  $I_B = 50$  nA, and the nominal value of the setting current of the TA  $I_{set} = 0.5$   $\mu$ A. The nominal power consumption of the DDTA was 357.4 nW. The input and compensation capacitors were highly linear metal–isolator–metal capacitors (MIM). The linear resistor's  $R$  was a high-resistance poly-resistor. Intensive simulation results of the standalone MI-DDTA including Monte Carlo analysis (MC) and process, voltage, and temperature (PVT) corners were presented in detail in [10]. The open-loop gain of the DDCC (i.e., without the unity gain feedback) was simulated as 73.9 dB and the phase margin was 56.2° for 20 pF load capacitor. The low-frequency gain for  $V_w/V_{y+1}$  ( $=V_w/V_{y+2}$ ) and  $V_w/V_{y-1}$  ( $=V_w/V_{y-2}$ ) is 14 mdB and 57.29 mdB while the  $-3$  dB bandwidth is 22.24 kHz and 22.23 kHz, respectively. The simulated DC transfer characteristics of the DDCC show rail-to-rail operation capability. The simulated gain and phase characteristics for the TA with  $I_{set} = 0.5$   $\mu$ A and 20 pF load capacitance show that the low DC gain is 23.2 dB and the bandwidth is 19.65 kHz, while the phase error is 3.8° [10]. The DC characteristic of the output current and the transconductance of the TA versus fully differential input voltage for  $I_{set} = 0.125$   $\mu$ A, 0.25  $\mu$ A, 0.5  $\mu$ A confirms a rail-to-rail operation with high linearity.

**Table 2.** Transistor aspect ratios of the MI-DDTA.

Device	W/L ( $\mu\text{m}/\mu\text{m}$ )
$M_{1A}, M_{2A}, M_{1B}, M_{2B}$	20/3
$M_7, M_8$	15/3
$M_3-M_6, M_B$	10/3
$M_9$	$6 \times 10/3$
$M_{10}$	$6 \times 20/3$
$M_R$	5/3
MIM capacitor: $C_B = 0.2 \text{ pF}, C_c = 4 \text{ pF}$	
Poly-resistor $R = 90 \text{ k}\Omega$	

Figure 6 shows the simulated and theoretical frequency characteristics of the gain and phase of the proposed voltage-mode first-order universal filter from Figure 4 with  $R_1 = 400 \text{ k}\Omega$ , capacitor  $C_1 = 2 \text{ nF}$  and setting current  $I_{\text{set}1} = I_{\text{set}2} = 0.5 \mu\text{A}$  ( $g_m = 2.5 \mu\text{S}$ ). The designed cut-off frequency of 197.4 Hz was very close to the simulated frequency of 195.6 Hz.

**Figure 6.** Frequency characteristics of the gain and phase: (a,b) LPF; (c,d) HPF; (e,f) APF.

In order to confirm the electronic tuneability of the filter, the frequency characteristics of the gain and phase were repeated for  $C_1 = 2 \text{ nF}$ ,  $R_1 = 400 \text{ k}\Omega$ ,  $I_{\text{set}2} = 0.5 \mu\text{A}$ , and different  $I_{\text{set}1} = (0.3, 0.4, 0.5, 0.6, 0.7) \mu\text{A}$ . The cut-off frequency was 120.8 Hz, 158.8 Hz, 195.6 Hz, 231.8 Hz, 260.7 Hz, respectively, as depicted in Figure 7.

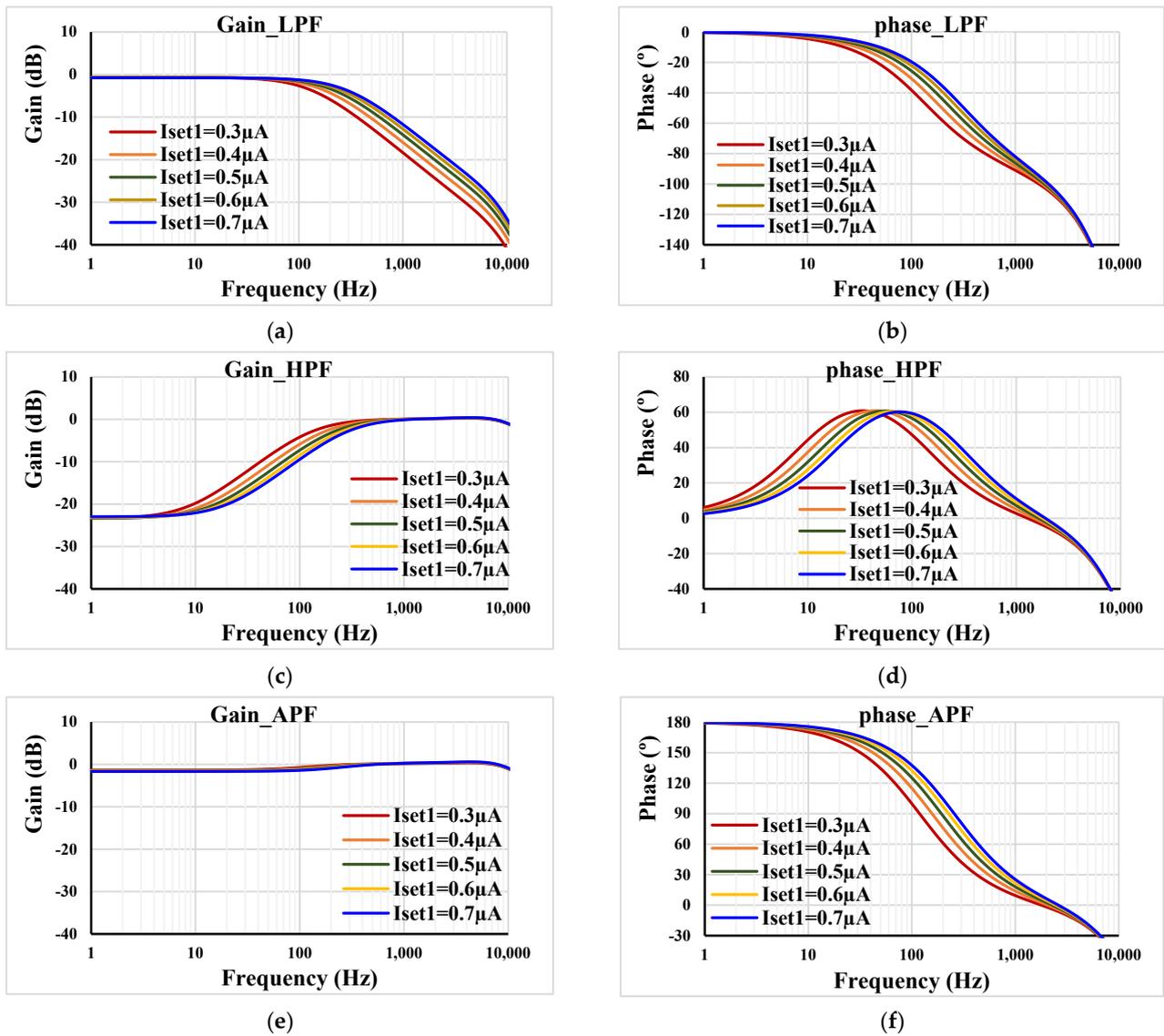


Figure 7. Frequency responses of the gain and phase: (a,b) LPF; (c,d) HPF; (e,f) APF with different  $I_{set1}$ .

Figure 8 shows the frequency characteristics of the gain and phase for  $C_1 = 2$  nF,  $R_1 = 400$  k $\Omega$ ,  $I_{set1} = 0.5$   $\mu A$ , and different  $I_{set2} = (0.4, 0.5, 0.6, 0.7, 0.8, 0.9)$   $\mu A$ . The gain was in range of  $-3$  dB to 3.3 dB, which confirms the electronic tunability of the filter gain. When the value of the resistor was changed to  $R_1 = 800$  k $\Omega$ , the gain was in range of  $-3$  dB to 8 dB.

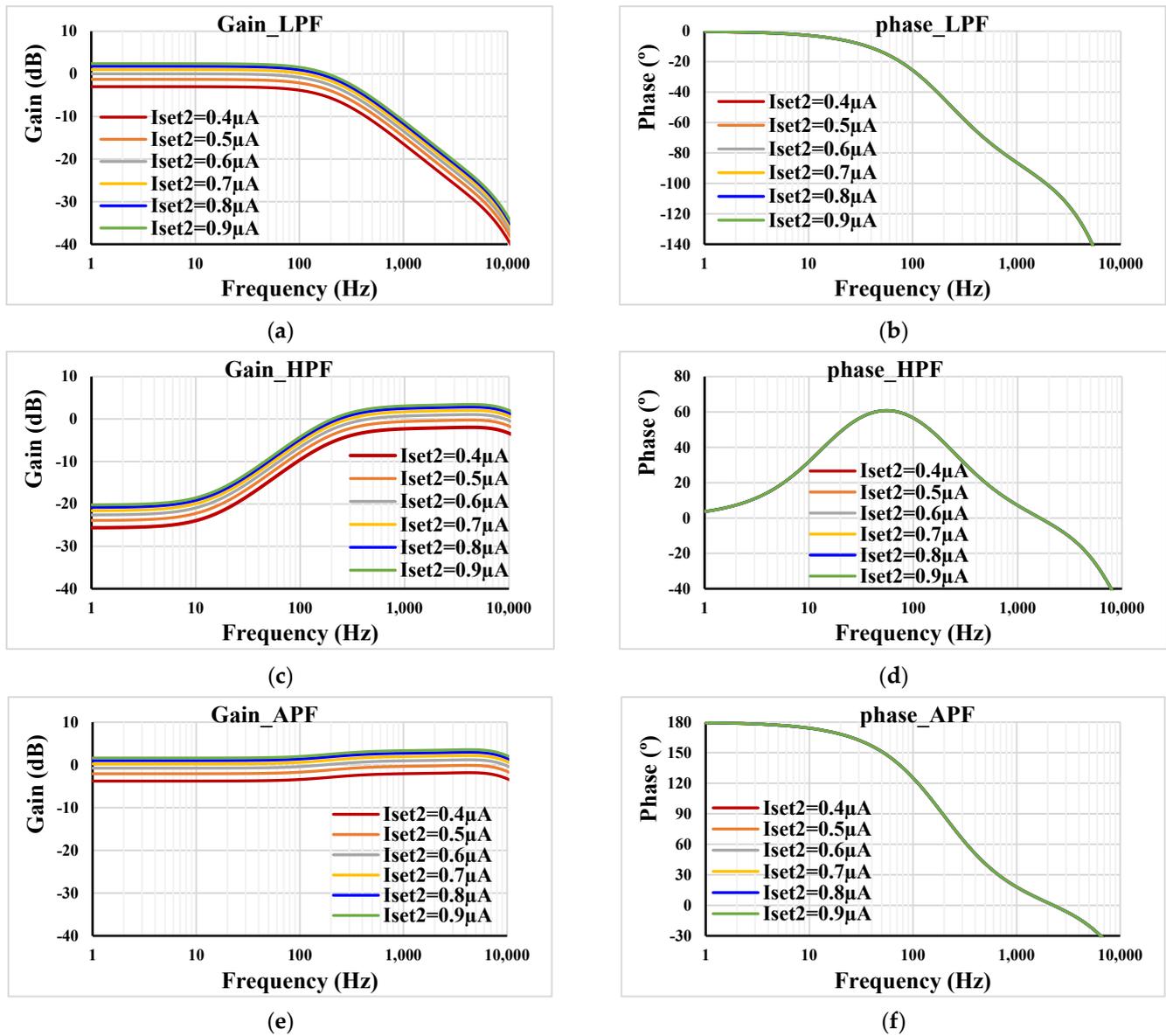
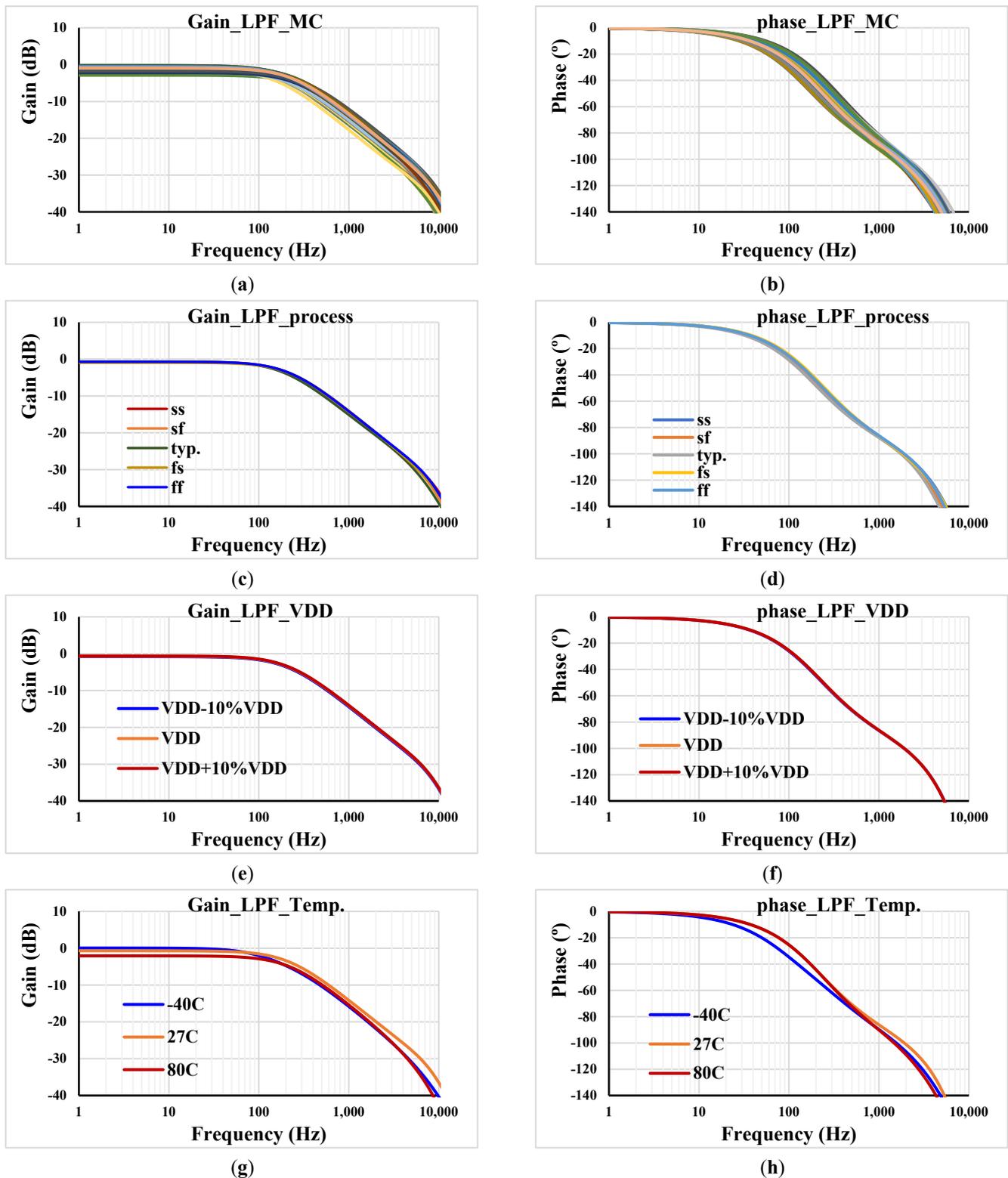


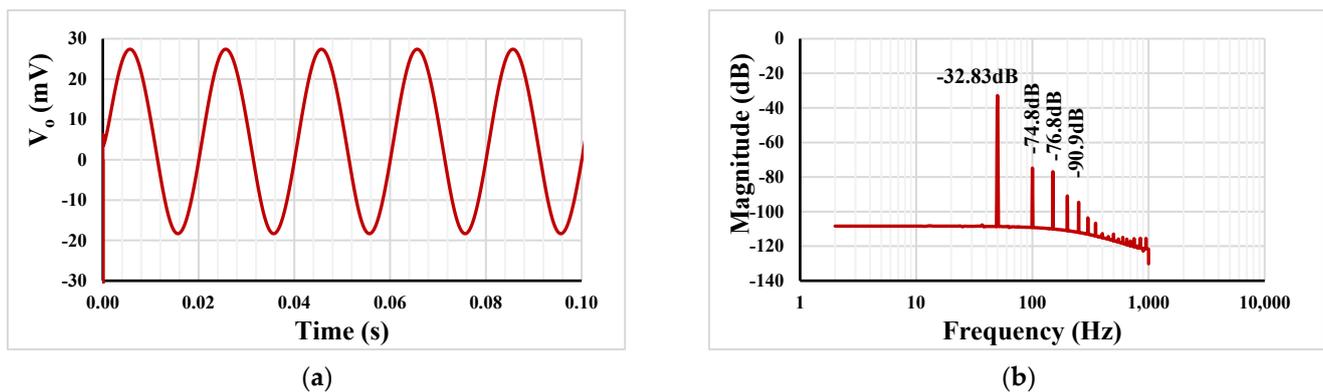
Figure 8. Frequency responses of the gain and phase: (a,b) LPF; (c,d) HPF; (e,f) APF with different  $I_{set2}$ .

Figure 9 shows the frequency characteristics of the gain and phase of the LPF for  $C_1 = 2 \text{ nF}$ ,  $R_1 = 400 \text{ k}\Omega$ , and  $I_{set1,2} = 0.5 \mu\text{A}$ . The Monte Carlo analysis, including process and mismatch variation and 200 runs, is shown in (a,b). The gain of the LPF at low frequency was in the range of  $-2.87 \text{ dB}$  to  $-0.243 \text{ dB}$  and the cut-off frequency was in the range of  $158.48 \text{ Hz}$  to  $335.26 \text{ Hz}$ . The slow–slow (ss), slow–fast (sf), fast–slow (fs) and fast–fast (ff) processes are shown in (c,d). Finally, (e,f) shows the voltage supply corners,  $V_{DD} \pm 10\%V_{DD}$ , and (g,h) shows the temperature corners  $-40 \text{ }^\circ\text{C}$  and  $80 \text{ }^\circ\text{C}$ . As is evident, the curves are almost overlapped, with a slight variation in the temperature corner analysis. This is suspected to be due to the subthreshold region operation that is known to be sensitive to temperature. The deviation of the cut-off frequency can be readjusted by the setting current.



**Figure 9.** Frequency responses of the gain and phase for LPF: (a,b) MC; (c,d) process corners; (e,f) voltage corners and (g,h) temperature corners.

Figure 10a shows the transient response of the LPF with  $R_1 = 400 \text{ k}\Omega$ , capacitor  $C_1 = 2 \text{ nF}$ , the setting current  $I_{\text{set}1} = I_{\text{set}2} = 0.5 \text{ }\mu\text{A}$ , and the applied sine wave input signal  $50 \text{ mV}_{\text{pp}} @ 50 \text{ Hz}$ . The spectrum of the output signal  $V_o$  using fast Fourier transform (FFT) is shown in (b). The total harmonic distortion was calculated as  $-39.97 \text{ dB}$  (1.024%).



**Figure 10.** The transient response of the LPF (a) and the spectrum of the  $V_o$  using FFT (b).

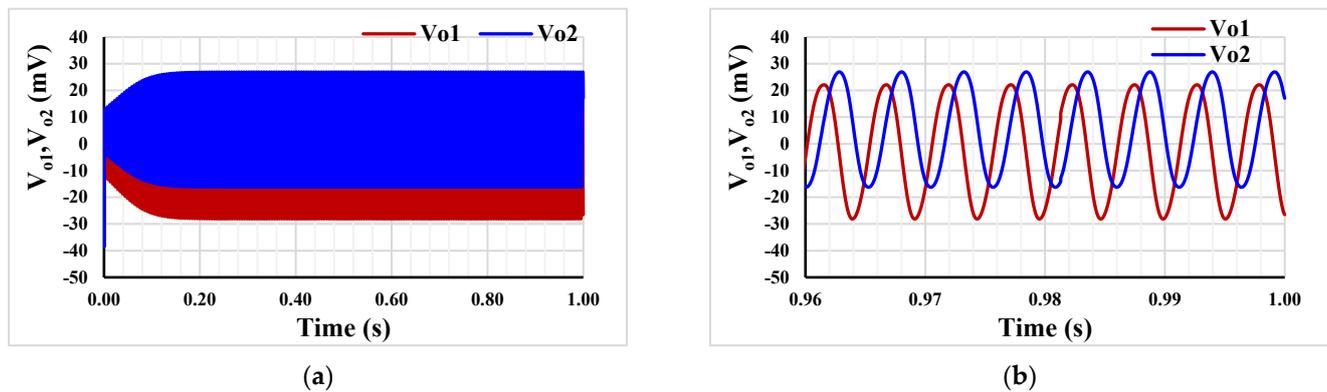
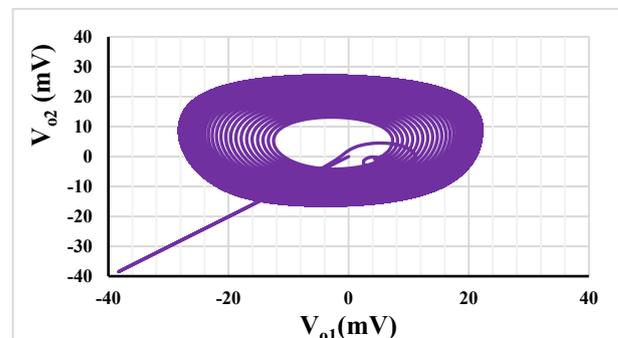
The comparison between the proposed versatile first-order filter and some previous works is shown in Table 3. Recently published filters, such as the CM filter in [29], the VM filters in [44,46,51,59], or the MM filter in [54], have been selected for comparison. The proposed filter offers six transfer functions similar to [29], but the proposed filter can control the voltage gain of the transfer functions. Moreover, the CM filter in [29] uses multiple-output ICCII, which has a high-power consumption. Compared with [44,46,51,59], the proposed filter exhibits rich filtering functions, and the gain of all transfer functions can be controlled. The MM filter in [54] offers nine transfer functions through CM, VM, TAM, and TIM filters, but each filter offers only three transfer functions of LP, HP, and AP filters, whereas the proposed VM filter offers six transfer functions of LP, HP, and AP filters. The filters using a single active device in [44,46,54] apply the input voltage signal via a capacitor or resistor, which is not ideal for voltage-mode circuits and integrated circuits. In comparison, the proposed filter has high-input and low-output impedance. Finally, compared with all filters in [29,44,46,51,54,59], the proposed filter unequivocally offers the lowest power supply and power consumption, which is served by the low-voltage low-power MI-DDTA. The comparison table also includes a figure of merit (FoM) =  $P_{\text{diss}} / (N) f_o$ , where  $P_{\text{diss}}$  is the power dissipation,  $N$  is the filter order (number of poles), and  $f_o$  is the pole frequency. However, here it is important to note that this FoM is specific to power dissipation, filter order, and pole frequency and does not cover all aspects of filter performance. The proposed filter offers many advantages over other designs due to the multiple-input MOS transistor, which increases the capability of the arithmetic operations of the proposed MI-DDTA without increasing the power consumption such as number of filter functions, high input impedance, electronic parameter control, gain control, and use of grounded passive components, which is the main attractive performance of the proposed filter which cannot be achieved by using two conventional DDTAs.

For the oscillator in Figure 5,  $R_1 = 400 \text{ k}\Omega$ , capacitors  $C_1 = C_2 = 2 \text{ nF}$  and setting current  $I_{\text{set1}} = 0.5 \text{ }\mu\text{A}$  were selected. To start the oscillation,  $R_2 = 500 \text{ k}\Omega$  and  $I_{\text{set2}} = 0.55 \text{ }\mu\text{A}$ . Figure 11a,b show the running oscillation and steady state, respectively. The THD was around 3%. The outputs  $V_{o1}$  and  $V_{o2}$  are in quadrature with a frequency of 192 Hz. Figure 12 shows the relation between  $V_{o1}$  and  $V_{o2}$  that can confirm the quadrature relationship of the output signals.

**Table 3.** Comparison of the proposed design with previous first-order filters.

Features	Proposed	[29] 2017	[44] 2021	[46] 2022	[51] 2022	[54] 2023	[59] 2023
Active and passive elements	2 DDTA, 1 C, 1 R	2 ICCII, 1 C, 1 MOS Figure 4	1 LT1228, 1 C, 2 R	1 VD-DIBA, 1 C, 2 R	2 CFOA, 1 C, 4 R Figure 1d	1 VGA, 1 C, 1 R	2 OTA, 1 C
Realization	CMOS structure (0.13 $\mu\text{m}$ )	CMOS structure (0.13 $\mu\text{m}$ )	Commercial IC (LT1228)	Commercial IC (LT1228, AD830)	Commercial IC (AD844)	CMOS structure (0.18 $\mu\text{m}$ )	CMOS structure (0.18 $\mu\text{m}$ )
Mode operation	VM	CM	VM	VM	VM	MM	VM
Type of filter	MISO	SIMO	MISO	MISO	MISO	MIMO	MISO
Number of filtering functions	6 (LP+, LP-, HP+, HP-, AP+, AP-)	6 (LP+, LP-, HP+, HP-, AP+, AP-)	4 (LP+, HP+, AP+, AP-)	4 (LP-, HP-, AP+, AP-)	3 (LP-, HP+, AP+)	3 (LP+, HP+, AP+)	6 (LP+, LP-, HP+, HP-, AP+, AP-)
High-input impedance	Yes	-	No	No	Yes	No	Yes
Electronic control of parameter $\omega_0$	Yes	Yes	Yes	Yes	No	Yes	Yes
Control of gain	Yes	No	Yes (LP, HP)	Yes (LP, HP)	Yes	No	No
Using grounded capacitor/resistor	Yes	No	No	No	No	No	Yes
Pole frequency (kHz)	0.195	2600	90	159.15	159	1590	0.220
Total harmonic distortion (%)	1.024@50 mVpp	<1.5@90 $\mu\text{A}_{\text{pp}}$	1@200 mVpp	<1@150 mVpp	-	-	0.36@40 mVpp
Supply voltage (V)	0.3	$\pm 0.75$	$\pm 5$	$\pm 5$	$\pm 12$	$\pm 0.9$	0.5
Power dissipation ( $\mu\text{W}$ )	0.7148	4080	57,600	-	-	-	$59.5 \times 10^{-3}$
FoM ( $\mu\text{W}/\text{kHz}$ )	3.66	1.56	640	-	-	-	0.27
Verification of result	Sim.	Sim.	Exp.	Exp.	Exp.	Sim/Exp	Post-layout Sim.

**Note:** VD-DIBA = voltage differencing input buffered amplifier, ICCII = inverting second-generation current conveyors, VGA = voltage differencing gain amplifier, MISO = multiple-input single-output, SIMO = single-input multiple-output, MIMO = multiple-input multiple-output, MM = Mixed-mode, LP+ = non-inverting low-pass filter, LP- = inverting low-pass filter, HP+ = non-inverting high-pass filter, HP- = inverting high-pass filter, AP+ = non-inverting all-pass filter, AP- = inverting all-pass filter.

**Figure 11.** The running oscillation (a) and the steady state (b).**Figure 12.** The quadrature relationship between  $V_{o1}$  and  $V_{o2}$ .

## 5. Conclusions

This work presents the realization of a versatile first-order analog filter that consists of two MI-DDTAs, one grounded capacitor, and one resistor. The proposed filter possesses six transfer functions of LP, HP, and AP filters in a single topology, high-input and low-

output impedance, and electronic control of the gain and the pole frequency of transfer functions. Thanks to the bulk-driven multiple-input MOS transistor technique operating in the subthreshold region, the DDTA works with a 0.3 V of power supply and 357.4 nW of power consumption. In order to confirm the advantages of the new circuit, the proposed first-order filter has been used to realize a sinusoidal oscillator with a frequency of 192 Hz and 3% THD. The filter and oscillator are suitable for low frequency applications such as biomedical applications. The simulation results confirm the performance of the filter.

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