

# In-Situ Monitoring of Reciprocal Charge Transfer and Losses in Graphene-Silicon CCD Pixels

Munir Ali, Yunfan Dong, Jianhang Lv, Hongwei Guo, Muhammad Abid Anwar, Feng Tian, Khurram Shahzad, Wei Liu, Bin Yu \*, Srikrishna Chanakya Bodepudi \* and Yang Xu \*

School of Micro-Nano Electronics, ZJU-Hangzhou Global Scientific and Technological Innovation Center, ZJU-UIUC Joint Institute, State Key Laboratory of Silicon Materials, Zhejiang University, Hangzhou 310027, China

\* Correspondence: yu-bin@zju.edu.cn (B.Y.); bodepudi@zju.edu.cn (S.C.B.); yangxu-isee@zju.edu.cn (Y.X.)

**Abstract:** Charge-coupled devices (CCD) allow imaging by photodetection, charge integration, and serial transfer of the stored charge packets from multiple pixels to the readout node. The functionality of CCD can be extended to the non-destructive and in-situ readout of the integrated charges by replacing metallic electrodes with graphene in the metal-oxide-semiconductors (MOS) structure of a CCD pixel. The electrostatic capacitive coupling of graphene with the substrate allows the Fermi level tuning that reflects the integrated charge density in the depletion well. This work demonstrates the in-situ monitoring of the serial charge transfer and interpixel transfer losses in a reciprocating manner between two adjacent Gr-Si CCD pixels by benefitting the electrostatic and gate-to-gate couplings. We achieved the maximum charge transfer efficiency (CTE) of 92.4%, which is mainly decided by the inter-pixel distance, phase clock amplitudes, switching slopes, and density of surface defects. The discussion on overcoming transfer losses and improving CTE by realizing a graphene-electron multiplication CCD is also presented. The proof of the concept of the in-situ readout of the out-of-plane avalanche in a single Gr-Si CCD pixel is also demonstrated, which can amplify the photo packet in a pre-transfer manner.

**Keywords:** charge-coupled devices; charge transfer; multiplication; graphene

**Citation:** Ali, M.; Dong, Y.; Lv, J.; Guo, H.; Abid Anwar, M.; Tian, F.; Shahzad, K.; Liu, W.; Yu, B.; Bodepudi, S.C.; et al. In-Situ Monitoring of Reciprocal Charge Transfer and Losses in Graphene-Silicon CCD Pixels. *Sensors* **2022**, *22*, 9341. <https://doi.org/10.3390/s22239341>

Academic Editors: Jesper Skottfelt and Roman Sotner

Received: 24 September 2022

Accepted: 24 November 2022

Published: 30 November 2022

**Publisher's Note:** MDPI stays neutral with regard to jurisdictional claims in published maps and institutional affiliations.



**Copyright:** © 2022 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (<https://creativecommons.org/licenses/by/4.0/>).

## 1. Introduction

Photoexcited carrier integration and multiplication play a pivotal role in developing efficient photodetection, especially for weak incident light. Charge-Coupled Devices (CCD) and Complementary Metal-Oxide-Semiconductor (CMOS) are two leading imaging technologies with specific advantages and disadvantages. The attractive factors for using the CCD are its simple metal-oxide-silicon (MOS) photogate detector, which offers high sensitivity, high fill factor, and low noise. For CMOS imagers, the independent pixel structure provides random access, simple clocking, fast parallel readout, natural anti-blooming, and low power consumption [1–4]. Emerging imaging technologies require benefits from both CCD and CMOS architectures. Whereas all major imaging technologies based on CCD and CMOS often suffer from loss of image quality and contrast due to extensive transport and weak charge-to-voltage conversion efficiency.

Graphene can provide absorption tunability that can extend to UV to terahertz band by electrically adjusting the Fermi level without any additional manufacturing cost [5]. Unique properties of graphene open opportunities in various application areas, such as photodetectors, chemical sensors, and metamaterial absorbers that even extend to environmental cleanup functionalities [6–8] and protection units [9]. Graphene-based photodetectors often exhibit responsivity within 100 mA/W [10], resulting from short carrier recombination time (~2 ps) and recombination length (~1 μm), while the charge transport lengths in photodetectors are often extending to hundreds of microns. Thus, collecting

photo-induced carriers before recombination within the graphene channel is still a challenging task [11–13]. One of the approaches to overcome this issue is integrating graphene with conventional device architectures like CCD and CMOS.

Graphene can work as an atomically-thin, transparent, charge-sensing layer that, by leveraging upon the photogating phenomenon through electrostatic capacitive coupling, detects absorption within a thicker adjacent substrate rather than serving as the light-absorbing medium. The changes in the graphene channel conductance can be sensed by the application of a constant bias voltage causing channel current ( $I_{ds}$ ). This current is proportional to the product of carrier density( $n$ ) and mobility( $\mu$ ) of graphene ( $I_{ds} \propto \mu nE$ ). Moreover, graphene's significant ambipolar mobility ( $\sim 10^3 - 10^5 \text{ cm}^2/\text{V.s}$ ) [14] provides a built-in photo gain mechanism that can enhance the detector response. For photo-gated graphene devices, responsivity higher than 1000 A/W has been reported [15–18]. This photo gating of graphene offers a solution to the previously mentioned issue by allowing a hybrid imaging scheme that adopts the benefits of both CCD and CMOS architectures while providing a direct readout of the integrated photoexcited charge and allowing flexible manipulation of the information signal (charge packet).

Previous works have demonstrated the potential of graphene-based CCD schemes for direct readout in a broad wavelength range from X-ray to mid-infrared (MIR) [19–21]. The next crucial step towards large-scale Gr-Si CCD imagers is to realize direct readout of charge multiplication and integration within the charge domain via graphene. A large number of serial transfers in CCD structure at high electric fields sufficient to trigger impact ionization leads to charge amplification within the charge domain before the charge-to-voltage conversion. In this work, we present the proof of concept for in-situ monitoring of the serial charge transfer between adjacent Gr-Si CCD pixels and investigate the potential of this platform to achieve charge multiplication in reciprocating neighboring pixels.

Moreover, the proof of the concept of the in-situ readout of an out-of-the-plane avalanche in silicon absorber through displacement ( $I_g$ ) and graphene channel ( $I_{ds}$ ) currents are explored as well in this work. The Gr-Si CCD pixel is initially dynamically ramped into deep depletion. At this stage, pulsed laser excitation triggers an avalanche effect via photoionization in the device that can be sensed by the two probe techniques discussed above.

## 2. Device Fabrication and Measurements

An n-doped Si/SiO<sub>2</sub> (500  $\mu\text{m}/100 \text{ nm}$ ) substrate with a resistivity of  $(1 - 10) \Omega \cdot \text{cm}$  corresponding to a doping concentration of  $4.5 \times 10^{14} \text{ cm}^{-3}$  to  $4.94 \times 10^{15} \text{ cm}^{-3}$  is used in this work. The SiO<sub>2</sub> layer was patterned using photolithography with successive thermal evaporation (Angstrom Engineering) process to deposit Ti/Au film as the contact pads onto SiO<sub>2</sub>. The respective thicknesses of the Ti and Au metals are 5 and 70 nm. The chemical vapor deposition (CVD) graphene on a copper foil (ACS Materials) is first spin-coated with polymethylmethacrylate (PMMA) (ALLRESIST AR-26, speed = 4000 rpm, time = 60 s) [22]. The copper foil is then dissolved in a CuSO<sub>4</sub> + HCl + H<sub>2</sub>O solution (CuSO<sub>4</sub> + HCl + H<sub>2</sub>O = 10 g: 50 mL: 50 mL) for 5 h. Then the PMMA-coated graphene films are fished into the containers of deionized water and placed there for 2 h [23]. Then these films are transferred onto the top of the silicon wafer covering the pixel area and the metal electrodes.

Furthermore, PMMA was removed with acetone and cleaned with isopropyl alcohol (IPA). It was followed by the graphene patterning into square-shaped pixels, each having an area of  $0.25 \text{ mm}^2$ , using photolithography and oxygen plasma. The photoresist was then removed by acetone and successive cleaning in IPA. Finally, wire bonding connects the top electrode with Au wires. Moreover, by using a Hitachi (Tokyo, Japan) S4800 field-emission microscope at an acceleration voltage of 5 kV, scanning electron microscopy (SEM) images are produced.

A dual-port signal generator provides gate voltage ( $V_{g1}$  and  $V_{g2}$ ) clocks. A power amplifier is used to generate large bias signals. The trans-impedance amplifier is implemented to measure the channel current ( $I_{ds}$ ) of Pixel-1. The 532 nm wavelength laser is used for photo generation in the silicon absorber of the Gr-Si CCD pixel. The laser light is not always ON; instead, it is intermittent, with a frequency of 0.5 Hz having an ON duty of 2.5% for the charge transfer experiment.

### 3. Results and Discussion

#### 3.1. Characterization of the Single Gr-Si CCD Pixel

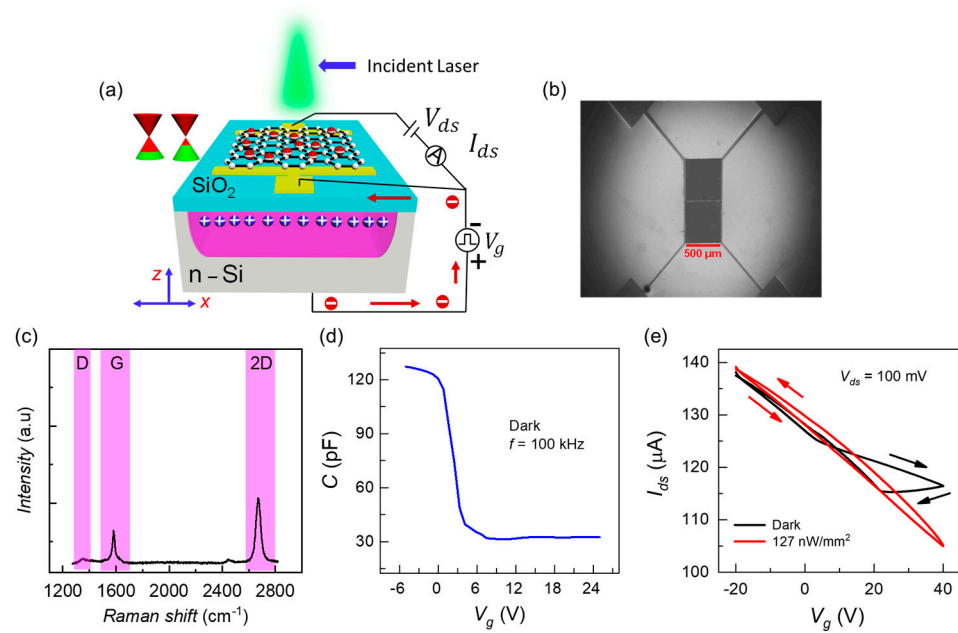
The measurement scheme and essential device characterization of a single Gr-Si CCD pixel are presented in Figure 1. The 3D device schematic and the related electrical circuitry for measurements of  $I_g$  and  $I_{ds}$  are shown in Figure 1a. The scanning electron microscope (SEM) image of the dual Gr-Si CCD pixels platform with each graphene channel having an area of  $500 \times 500 \mu\text{m}^2$  is shown in Figure 1b. Then, the Raman spectra of the graphene layer are shown in Figure 1c, the ratio of  $I_{2D}/I_G$  is larger than two, emphasizing that the employed graphene is a monolayer. The monolayer graphene being highly tunable is a critical ingredient of our study.

The high-frequency capacitance-voltage (HF-CV) characteristics curve in the dark situation for gate voltage varying from  $-5 \text{ V}$  to  $25 \text{ V}$  is shown in Figure 1d. The oxide capacitance ( $C_{ox}$ ) of 126 pF in the accumulation state indicates the strong silicon dioxide layer required for the charge integration process. Before proceeding with the back-and-forth charge transport study, this characterization is essential for each of the Gr-Si CCD pixels.

Several device instabilities have been reported in graphene-based field effect transistors due to differences in graphene Dirac points, and the charge trapping effects in the substrate [24–26]. One such anomaly is the hysteresis in  $I-V$  characteristics [27,28] which originates from the materials involved and the operational environment [29,30]. The charge trapping in the underlying silicon substrate and  $\text{SiO}_2$  can contribute to this unwanted phenomenon. In addition, slow charge trapping at the graphene/ $\text{SiO}_2$  interface produced by the contaminants from the wet transfer of graphene can also contribute to the hysteresis [31–33].

The  $I_{ds}$  vs.  $V_g$  curves during the forward and backward scans to probe the hysteresis effect in a single Gr-Si CCD pixel under dark and light conditions are shown in Figure 1e. A potential well in the silicon is compulsory to enable a Gr-Si CCD pixel for photodetection or to receive the laterally moving carriers. Hence, there are always some losses due to surface defects for the charge packet in the silicon well. Moreover, when surface defects are filled during light exposure, the vertical graphene-oxide-silicon structure behaves as a metal-insulator-metal capacitor. In this case, hysteresis will be mainly due to graphene, which is obvious from Figure 1e for all laser ON conditions. The constant optical illumination is intentionally kept large to cause inversion in the well so that the effect of graphene/ $\text{SiO}_2$  traps on  $I_{ds}$  can be subsided.

At 0 V gating bias, the  $\Delta I_{ds}$  due to hysteresis for all the illumination conditions is approximately  $2 \mu\text{A}$ . Moreover, the nature of Si/ $\text{SiO}_2$  interface trappings and graphene/ $\text{SiO}_2$  interface defects is different as seen from the directions of arrows in the reverse bias scenario of silicon photogate for dark and optical illumination conditions. We used high-quality substrates from the UniversityWafer, Inc. in our experiments. The high-quality thermally grown  $\text{SiO}_2$  of 100 nm thickness does not contain excessive charge trapping.

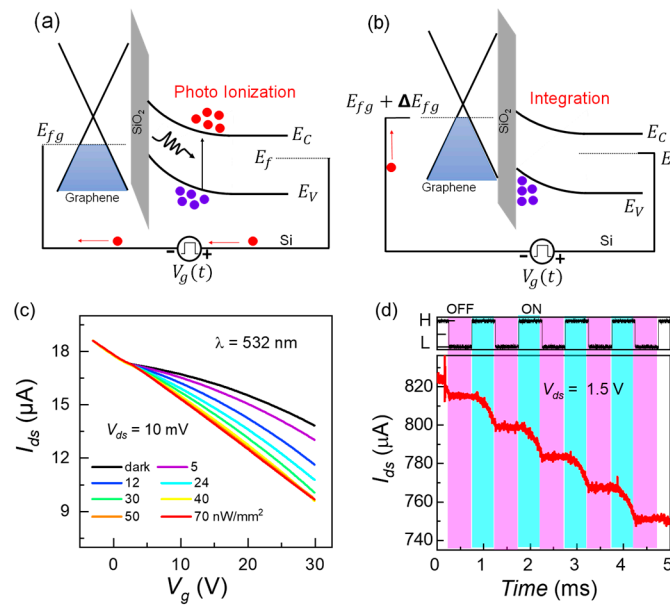


**Figure 1.** (a) A 3D schematic of Gr-Si CCD pixel, electrically connected to measure  $I_{ds}$  and  $I_g$ . The biasing voltage  $V_g$  and constant voltage source  $V_{ds}$  are also included. (b) The SEM image of the two  $500 \times 500 \mu\text{m}^2$  area Gr-Si CCD pixels platform. (c) The Raman spectra characterization shows the implementation of monolayer graphene as  $I_{2D}/I_G > 2$ . (d) The quasi-static C-V measurement at 100 kHz modulation frequency in the dark scenario. (e) By quasi-statically sweeping the voltage  $V_g$ , the contribution of Si/SiO<sub>2</sub> and graphene/SiO<sub>2</sub> trapping states on hysteresis through  $(I_{ds} - V_g)$  are observed within the operating voltages of the work. Both the forward and backward scans in the dark (black arrows) and under illumination (red arrows) are plotted.

These trappings are also not introduced due to excessive electric fields on SiO<sub>2</sub> as our operating fields are within 4 MV/cm. Therefore, defects and trap states at the graphene/SiO<sub>2</sub> interface are the main contributing factors in the hysteresis of channel current rather than the underlying semiconductor substrate. Moreover, graphene/SiO<sub>2</sub> interface trapping states can be controlled by capping the graphene with an Al<sub>2</sub>O<sub>3</sub> dielectric layer [34].

The band diagrams explaining the photoionization event and subsequent charge integration phenomena as the photo-ionized carriers transport to the Si/SiO<sub>2</sub> interface are shown in Figure 2a,b, respectively. The random-access mode, the unique feature enabled by graphene in the CCD structure, is observed by tuning the graphene Fermi level ( $E_{fg}$ ) by the minority carriers accumulated at the underlying Si/SiO<sub>2</sub> interface of a Gr-Si CCD pixel. The integrated holes reflect graphene's conductance variations while the electrons sink into bulk silicon.

Then the plausibility of the charge integration and readout within the single Gr-Si CCD pixel is confirmed through the creation of a potential well by quasi-statically reverse biasing the silicon substrate, followed by a 532 nm constant laser illumination and subsequent real-time sensing of integrated charges through  $I_{ds}$  as shown in the p-type branch of the “V” shaped transfer curve in Figure 2c. For multiple laser intensities, we observed the changes in the Fermi level of graphene indicated by the increase in the slopes of the transfer curves. Here, the  $I_{ds}$  decreased with increased laser power due to the rise in overall photoelectrons transferred to graphene to balance the photo holes in the deep depletion well. The observed photogating effect in the device should mainly come from the photo hole integration in the deep depletion well in silicon rather than the charge trapping in the oxide or the interface [28].



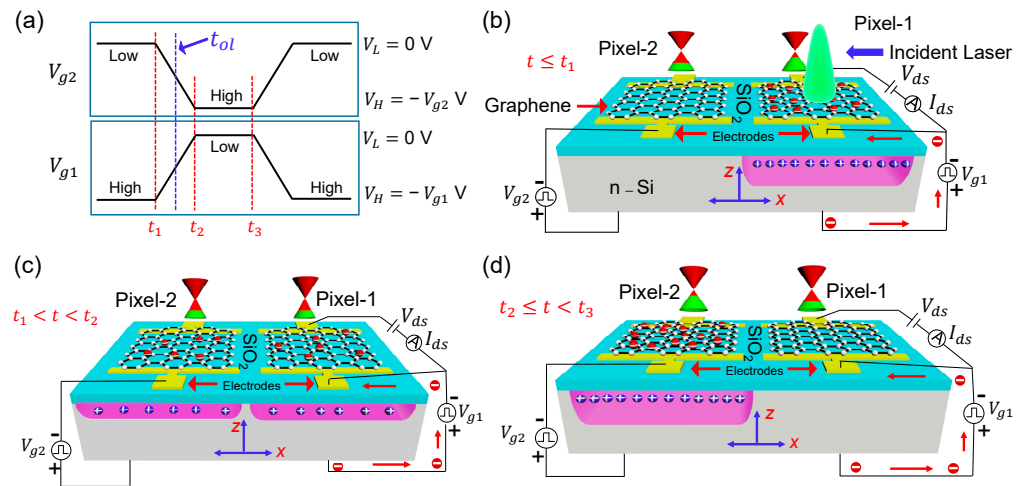
**Figure 2.** (a) Energy band diagram showing the photoionization process in the space charge region; it is equally valid for a constant or pulsed laser illumination. (b) This energy band diagram expresses that electrons drift into the bulk silicon and holes integrate at the Si/SiO<sub>2</sub> interface, causing a change in graphene's Fermi level ( $\Delta E_{fg}$ ). (c) The quasi-static  $I_{ds} - V_g$  curves for multiple constant exposures of 532 nm wavelength laser. (d) The capability of the GCCD pixel for photo-sensing and multi-logic memory applications is illustrated using  $I_{ds}$ . For a square gate bias  $V_g = 33$  V,  $V_{ds} = 1.5$  V, and 532 nm laser pulses, charge integration can be monitored in real time by  $I_{ds} - t$ .

Moreover, due to several output current levels, the Gr-Si CCD pixel can be used as multilevel logic technology, as shown in Figure 2d. A square kind of  $V_g$  signal of 1 kHz frequency and a high voltage level of 33 V is applied to the silicon semiconductor to construct a deep depletion state. Then, a 532 nm pulsed laser (50% duty) is multiply shined as shown in the top panel by black waveform. Charge integration (the stair-like waveform) is monitored in real-time through  $I_{ds}$ .

### 3.2. Back-and-Forth Charge Transfer for Multiplication

Charge multiplication occurs in CCD arrays when the applied gate electric field is large enough for impact ionization. Usually, a single impact ionization event is not strong enough to generate charge carriers to provide a high-quality image. Therefore, multiple impact ionization events are required to create a charge density sufficient to achieve significant image contrast. Back-and-forth serial charge transfer into a potential well is one such strategy for carrier multiplication.

The silicon absorber is the common ground during the charge transfer experiment. At the same time, large negative potentials are applied to the two top graphene gates complementarily to create quantum wells inside the n-type silicon substrate. Crucial temporal points for the back-and-forth charge transfer by the square gating voltages of different switching durations for two consecutive pixels in a single clock cycle are displayed in Figure 3a. The schematics of the dual pixel platform and electrical circuitry to perform serial charge transfer using gate-to-gate-coupling and direct-readout by random-access mode in pixel-1 for three conditions  $t \leq t_1$  ( $V_{g1}$  is high),  $t_1 < t < t_2$  (switching of  $V_{g1}$  and  $V_{g2}$ ), and  $t_2 < t < t_3$  ( $V_{g2}$  is high) are shown in Figure 3b–d, respectively.



**Figure 3.** (a) The temporal dynamics of  $V_{g1}$  and  $V_{g2}$  phasing gate voltages are shown, indicating the crucial moments in the back-and-forth charge transfer experiment. (b–d) The schematics and related electrical circuitry required for the two adjacent Gr-Si CCD pixels for three conditions  $t \leq t_1$  ( $V_{g1}$  is high),  $t_1 < t < t_2$  (switching of  $V_{g1}$  and  $V_{g2}$ ), and  $t_2 < t < t_3$  ( $V_{g2}$  is high) are shown. In-situ sensing of the back-and-forth charge transfer between neighboring pixels can be traced by the channel current  $I_{ds}$ . The charge density in the potential well affects the Fermi level position in graphene.  $V_{g1}$  and  $V_{g2}$  induce potential wells in the adjacent pixels. The fringing electric field produced at the Si/SiO<sub>2</sub> interface in the inter-pixel region drives the charge transfer.

The laser is exposed vertically to the Gr-Si CCD heterostructure from the top for all the optical measurements involved in this work. For the charge transfer experiment, laser light is not always ON; it is intermittent with a frequency of 0.5 Hz having an ON duty of 2.5%. Photoionization and successive charge integration in pixel-1 tunes  $E_{fg}$ , as shown in Figure 3b. The lateral fringing field at the Si/SiO<sub>2</sub> interface in the inter-pixel region is generated during the switching of  $V_{g1}$ , and  $V_{g2}$ . This fringing field drives the carriers in the two-dimensional hole gas (2DHG) of pixel-1 in the x-direction towards the depletion well of Pixel-2.

The scheme in Figure 3c shows an intermediate stage (of integrated photo holes for  $t_1 < t < t_2$ ) corresponding to the switching overlap moment ( $t_{ol} = (t_1 + t_2)/2$ ), where the gates become equipotential. Figure 3d depicts that the entire hole population has been transferred into the quantum well of Pixel-2. Then, Pixel-1 retains its initial dark current state as the electrostatic doping of graphene vanishes. The first largest change of  $I_{ds}$  belongs to holes-integration due to laser illumination. Then for all the charge-receiving events (backward charge transport from pixel-2 to pixel-1),  $\Delta E_{fg}$  will be induced by laterally received carriers instead of photo-ionized carriers. Due to the losses during back-and-forth movement and interface state trapping losses, the overall  $\Delta E_{fg}$  keeps decreasing.

During the photoresponse measurements, the laser is illuminated on a pixel enabled for the readout of the initial photoresponse. In addition, the in-situ readout is limited by the saturation of  $I_{ds}$ , as the maximum number of available states that can be electrostatically doped are limited in graphene. Shining the laser at large intensities generate higher number of photocarriers, leading to the saturation of  $I_{ds}$  in pixel-1 and thus deviates from the linearity of the readout.

### 3.3. Carrier Losses during Back-and-Forth Transfer

Back-and-forth charge transfer between potential wells of adjacent pixels requires suppression of transfer losses such as interface state trapping loss, recombination loss, and losses due to backscattered carriers from the substrate. The interface trap losses can be removed by circulating a background charge [35], and introducing an offset in the driving

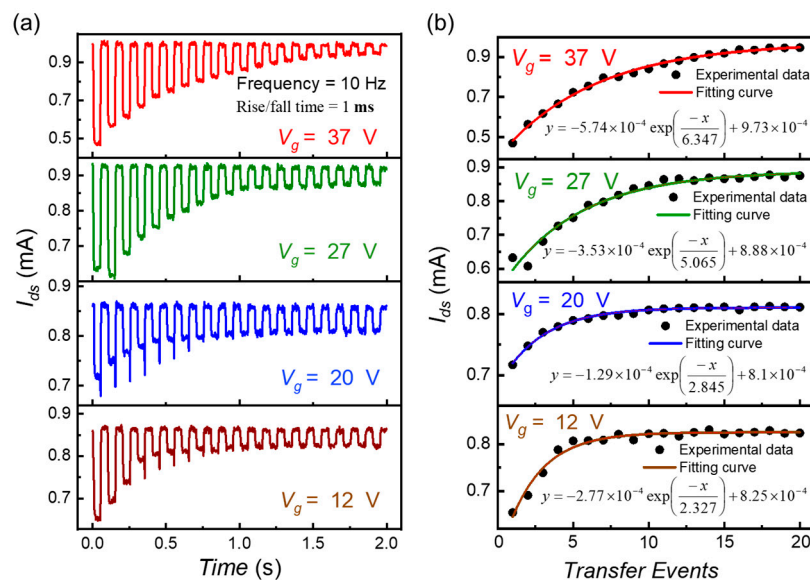


clocks can reduce recombination losses [36]. As we experimented with a slow clock frequency (10 Hz), carrier backscattering at  $t_{ol}$  does not affect measurements [37].

In our adjacent Gr-Si CCD pixels, pixel-1 functions as the photodetector and then, relying upon the random access mode, acts as the sense node (in standard CCDs, the sense node is a complete readout module consisting of many different elements). When the charge has been transferred from Pixel-1 to Pixel-2,  $I_{ds}$  current retains its un-gated level (as no well exists beneath pixel-1, thermal or photo gating of top graphene is no more possible). The pixel-1, while working as the readout element, can sense every second transfer event, i.e., once photoionization happens in the pixel-1 corresponding to the maximum decrease of  $I_{ds}$ , its potential well demolishes for the transfer event from pixel-1 to pixel-2 and then enables again for the backward movement of the charge packet. The initial charge packet was transported twice before the subsequent readout. Moreover,  $I_{ds}$  current for every receiving step (from Pixel-2 to Pixel-1) increases successively, indicating the presence of in-pixel interface state trappings and interpixel transfer losses from the substrate; these losses act twice on the charge packet before every readout.

The fraction of electrons that are successfully moved from one pixel to another is described by the charge transfer efficiency (CTE), while the loss fraction is calculated as  $1 - CTE$ . If  $Q_o$  is the initial integrated charge and  $Q_n$  is the charge that reaches the sense node (pixel-1 in our case) after  $n$  transfers, then  $CTE^n = \frac{Q_n}{Q_o}$ . In our case, for every readout event  $n = 2$ . We measured four  $I_{ds}$  traces for different amplitudes of  $V_{g1}$  and  $V_{g2}$  clock phases, as shown in Figure 3a.

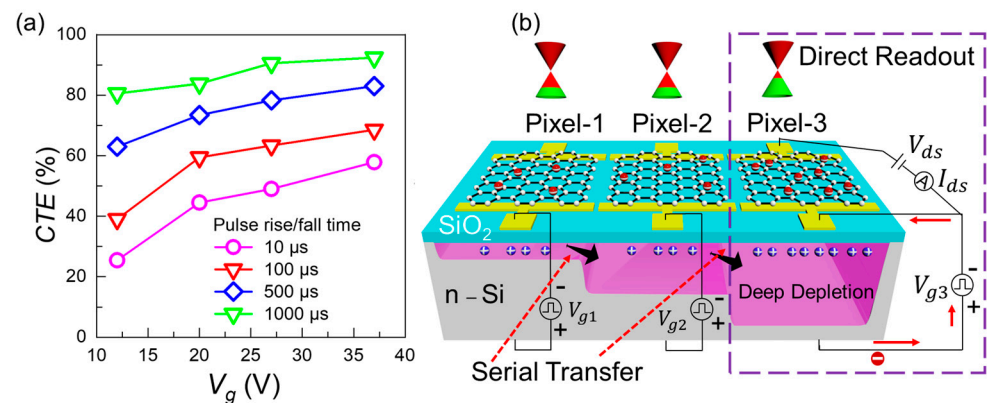
For all the  $I_{ds}$  curves shown in Figure 4a, exponential fittings are plotted in Figure 4b. The decay rates for  $V_{g1}$  and  $V_{g2}$  (12, 20, 27, 37) V are  $1/2.327$ ,  $1/2.845$ ,  $1/5.065$ , and  $1/6.347$ , respectively. Then the corresponding  $CTE^2$  for all four situations are  $e^{-1/2.327}$ ,  $e^{-1/1.845}$ ,  $e^{-1/5.065}$  and  $e^{-1/6.347}$ . The square root will result in 's of 0.806, 0.838, 0.906, and 0.924, respectively.



**Figure 4.** (a) For the back-and-forth charge transfer experiment for two adjacent Gr-Si CCD pixels platform,  $I_{ds}$  is recorded when  $V_{g1}$  and  $V_{g2}$  phases are applied to the two graphene gates. The to and fro transfer of charges is shown for 20 cycles of two input phases. For almost all the amplitudes and switching slopes of two phases, a decaying trend in the initial  $E_{fg}$  of the readout graphene channel is observed. This decay collectively corresponds to the in-pixel defect trappings and recombination losses in the inter-pixel region (b) The  $I_{ds}$  increase with each readout, reducing the net number of charges. The fitting of the  $I_{ds}$  values traces the losses. For four  $V_{g1}$  (12, 20, 27, 37) V and 1 ms switching slopes, exponential fitting successfully highlights the transfer losses. The decaying exponential equations for each measurement situation are also mentioned.

Parasitic capacitance often causes unwanted oscillations at the output of the circuit during the extended frequency operation of electronic devices. Whereas the operational frequencies of  $V_{g1}$  and  $V_{g2}$  reported in this work (10 Hz) are too low to cause any feedback loop. Another possible contribution of parasitic capacitance might originate from the proximity effect based on interpixel distance. However, the dimensions of our individual Gr-Si CCD pixels and corresponding interpixel distance (5  $\mu\text{m}$ ) are long enough to suppress any such proximity effects to cause parasitic capacitance. Therefore, parasitic capacitance is not a dominating factor in our reciprocating charge transfer process.

In Figure 5a, CTE is plotted vs. phase amplitude ( $V_g$ ) for switching durations of (10, 100, 500, and 1000)  $\mu\text{s}$ . The increasing fringing field and slow switching rates result in higher CTE's. For almost all the gate bias values and switching slopes of two phases, a decaying trend in the first  $\Delta E_{fg}$  of the readout graphene is observed. It shows the attenuation of the initial photo charge packet instead of any multiplication. We demonstrate that by exploiting random access and serial transfer modes together, the properties of CCD and CMOS technologies can be overlapped, allowing more flexible operation.



**Figure 5.** (a) CTE is plotted vs. phase amplitude at various switching slopes. (b) The 3D schematic for a three adjacent Gr-Si CCD pixels platform is shown with related circuitry to implement serial transfer and random-access modes due to  $V_{g1}$ ,  $V_{g2}$ , and  $V_{g3}$  clock phases. Photo charges will be held in the left well; after strong fringing field development by ramping up, the charge will be released by removing the central barrier, and graphene will read the enhanced charge density by recording  $I_{ds}$  in the avalanche or multiplication unit.

As transfer losses are unavoidable, controlled carrier multiplication can allow the lost carriers to boost  $\text{CTE} \geq 1$ . Reducing the inter-pixel distance will increase the fringing field. The minimum electrode separation attainable from photolithography is  $\sim 3 - 5 \mu\text{m}$  [1], while an undercut technique can reduce isolation up to  $\sim 0.1 \mu\text{m}$  [15], and electron beam lithography can further reduce the distance to 10 nm [38]. Moreover, factors like clock voltages integrated charges in the wells, and oxide thickness [17] also strongly influence the impact ionization probability.

To achieve carrier multiplication, electric fields larger than  $\sim 10^5 \text{ V/cm}$  are required [39–41]. In our dual-pixel Gr-Si CCD setup, the fringing field is enabled at  $t_1$ . The most probable moments for impact ionization are instantly after  $t_1$  and before  $t_2$ , where fringing fields are the strongest. At the same time, a larger inter-pixel distance reduces the strength of the fringing field to reach the avalanche threshold. The large pixel sizes and higher density of 2DHG can presumably affect the multiplication in our device.

### 3.4. Device Scheme for Efficient Carrier Multiplication

We would like to propose a device scheme that can overcome the above-observed limitations and improve carrier multiplication in Gr-Si CCD pixels. The impact ionization becomes highly probable when minority carriers (holes) get a chance to move through strong enough fringing fields. In addition, carrier density should be low to avoid self-



quenching, and multiplication can be significantly improved by providing sufficient acceleration to carriers before entering the fringing field.

The proposed device scheme uses three pixels as a single unit enabled by the serial charge transfer. The photo charges in these three adjacent MOS capacitors are temporarily held in the detector by a barrier until the avalanche unit is ramped to a strong fringing field. So, three clock phases are applied to three adjacent Gr-Si CCD pixels platforms ( $\sim 1 \mu\text{m}$  distance). This platform can boost CTE and transfer speed benefitting from the random access and serial transfer modes. In Figure 5b, the 3D schematic and related circuitry are shown. The direct readout is implemented for the avalanche unit connected with  $V_{g3}$ , while  $V_{g1}$  and  $V_{g2}$  are associated with the detector and transfer units.

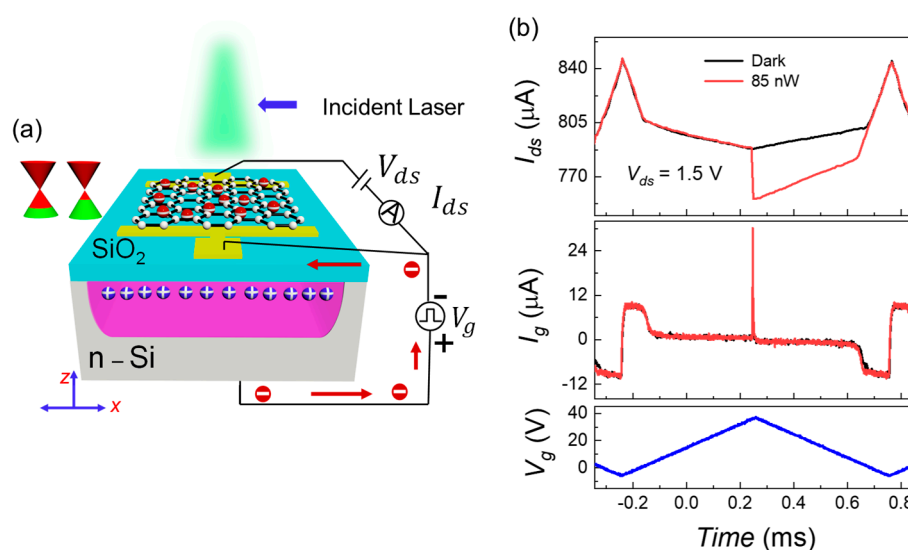
### 3.5. Out-of-Plane Avalanche Detection through Displacement and Channel Currents

The displacement current is not an appropriate readout probe for traditional CCDs having multiple rows and columns requiring multiple top-gating phases to transfer carriers from one pixel to the next until they reach the readout sense node. Contrary to that, the displacement current can be used for direct readout of an out-of-plane avalanche event (z-directed) from a single Gr-Si CCD pixel. Moreover, this out-of-plane carrier multiplication due to the electrostatic coupling of the Si/SiO<sub>2</sub> interface with the top tunable graphene channel can be in-situ readout through  $I_{ds}$ . The measurement scheme for recording the  $I_g$  and  $I_{ds}$  currents while silicon is dynamically biased is shown in Figure 6a. This measurement scheme is the same as the single-pixel characterization scheme shown in Figure 1a. The only difference is the application of a fast ramping biasing signal.

When a MOS capacitor is biased with a dynamic ramp  $V_g$ , the semiconductor experiences dynamically changing states, i.e., accumulation, depletion, and deep depletion [42,43]. The accumulation region through  $I_g = C_{ox} dV_g/dt$  depicts the collection of majority carriers at the Si/SiO<sub>2</sub> interface, where  $dV_g/dt$  is the voltage ramp rate. The formation of the potential well starts beyond flat band voltage; this marks the beginning of the depletion region. Then,  $I_g = C dV_g/dt$  as  $C_{ox}$  is replaced by the differential capacitance ( $C$ ), which is the series combination of  $C_{ox}$  and the semiconductor capacitance ( $C_{Si}$ ).

The  $I_g$  and  $I_{ds}$  currents are related to each other through  $\frac{\partial I_{ds}}{\partial t} = I_g \frac{\mu V_{ds}}{L^2}$ , where  $L$  is the pixel length. The correlation between these two currents in the dark and pulsed laser illuminations when silicon is ramped at fast pace (88 kV/s) is shown in Figure 6b. When the silicon absorber substrate is biased into accumulation (0 V to  $-6$  V and  $-6$  V to 0 V), the positive charge induced in the initially p-doped graphene is calculated by modeling the Gr-Si CCD heterostructure as an ideal parallel-plate capacitor.

During ramp-up (ramp-down), the quadratic decrease (increase) of  $I_{ds}$  is directly related to the linear decrease (increase) of majority carriers (electrons) concentration at the Si/SiO<sub>2</sub> interface where  $I_g = C_{ox} dV_g/dt$ . Whereas maximum  $I_{ds} = 847 \mu\text{A}$  at  $V_g = -6$  V corresponds to the sum of the graphene's maximum electrostatically doped and chemically doped holes, as shown in the top panel of Figure 6b. Then, this trend transitions in the depletion region (0.5 V to 5 V). Finally, space charge region donors in the deeply depleted well are reflected on graphene through electrostatically induced electrons;



**Figure 6.** Displacement current ( $I_g$ ) and channel current ( $I_{ds}$ ) are two alternate readout probes for a single Gr-Si CCD pixel (a) The 3D schematic and related circuitry for measurement of out-of-plane avalanche (vertical to the Si/SiO<sub>2</sub> interface in the silicon potential well) through  $I_g$  and  $I_{ds}$  due to fast ramping  $V_g$  is shown in Figure 5a. (b) Bottom panel: Fast ramping signal  $V_g$  is demonstrated, and the laser pulse is shined just before the maximum ramp voltage to exploit the strongest surface potential ( $\phi_{Si}$ ). Middle panel: The displacement current for light and dark conditions are shown. The rapid exponential increase corresponds to the photoionization event and subsequent avalanche. Top panel: The channel currents for light and dark conditions are shown. The quick reduction corresponds to the photoionization and following avalanche event.

The slow decreasing trend corresponds to a quadratically induced well where minimum  $I_{ds} = 791 \mu\text{A}$  at  $V_p = 38 \text{ V}$  corresponds to the maximum  $\phi_{Si}$ .

The pulsed laser (930 nm) is illuminated slightly before the ramp-up to ramp-down transition. Which benefits from the maximum  $\phi_{Si}$  of the strongly depleted space charge region to study post-photoionization and pre-integration avalanche events. The quick increase in  $I_g$  and decrease in  $I_{ds}$  belong to photoionization and successive multiplication for the pulsed laser-ON event. The sharp decrease in  $I_{ds}$  corresponds to a transient surge of hole integration at the interface. Then, by offering a negative feedback loop, the self-regulating phenomenon produces screening, forcing the change of  $\phi_{Si}$  to add with the voltage drop across oxide to maintain current continuity [44–47].

In our future work, we aim to systematically study a pre-transfer, out-of-plane avalanche in one pixel, which can help mitigate the transfer and defect trapping losses in the dual adjacent pixel platform along with the 3-phase measurement scheme shown in Figure 5b.

This work demonstrates the serial charge transfer in Gr-Si CCD for the first time. There is no previous work that we can directly compare. Since Gr-CCD is still at the initial prototype stage, it would not be appropriate to directly compare it with the functional parameters of commercial CCD devices. However, we would like to highlight the structural, fabrication, and operational advantages and limitations of the proposed device scheme with the traditional CCD structure in the below Table 1.

**Table 1.** The comparison between conventional silicon-based CCDs with novel Gr-Si CCD pixels is presented for different parameters, i.e., readout techniques, response time, cost of fabrication, and charge transfer efficiency.

Key Parameters	Gr-Si CCD	Silicon-Based CCD
Direct Readout	Yes	No
Broadband Response	Yes	No

Room Temperature Sensitivity	Higher ( $\sim 6 \times 10^4$ A/W)	Lower
Readout time	$\sim (1 - 1000)$ ps	$\sim 100 \mu\text{s}$ to $10$ s [48,49]
Cost of implementation	Low	High
Response time	$\sim (1 - 1000)$ ps	$\sim (1 - 1000)$ ps
CTE	92.4%	99.999% [50–52]
Readout & Integration	Independent & Non-destructive	Dependent

The small thermal carrier generation rate ( $G_{th}$ ) of  $312 \text{ e}/\mu\text{m}^2 \cdot \text{s}$  in silicon at room temperature has been reported, resulting in the inversion of the interface in  $\sim 200$  s [20]. Thus, the contribution of thermal charge for charging our Gr-Si CCD pixel is almost negligible compared to the levels of illuminating powers employed. The sophisticated and high-performance CCDs display a one-half decrease in the dark current for every 5 to 9 degrees Celsius when cooled below room temperature, called doubling temperature. The CCDs are only required to operate at very low temperatures when their core purpose is to sense the far infra-red (FIR) energy photons, i.e., the James Webb space telescope is designed to operate at the lowest temperature up to  $-266$  degrees Celsius, which enables it to record the past of a galaxy living at the far edge of the known universe. In our Gr-Si CCD photodetector, lowering the temperature will not help detect FIR wavelengths due to silicon's large intrinsic band gap (1.12 eV) absorption limit. Increasing the temperature will boost the dark current level, which is also an unwanted aspect.

The customized measurement setup for charge transport will likely induce frequent graphene burnouts, oxide leakage, and tunneling as the complementary gating phases  $V_{g1}$  and  $V_{g2}$  are directly connected to graphene channels, particularly when in-situ readout loops of both pixels are enabled. The existing measurement setup is not that sophisticated to measure the transferring of integrated holes through the  $I_{ds}$  of both pixels. The specific measurement setup offering multiple pulse modes and providing a good common ground is required. Moreover, it should be able to keep the alternating variation of gating phases from penetrating the  $I_{ds}$  loop, which is an intrinsically direct current (DC) and recorded by an oscilloscope that is electrically fed through an uninterruptible power source (UPS). The simultaneous measurement of the transferring events along the x-direction through both pixels is also enlisted in our future works.

#### 4. Conclusions

The random access and serial transfer modes are implemented to demonstrate the in-situ monitoring of the serial charge transfer process in a reciprocation platform composed of two adjacent Gr-Si CCD pixels. Due to excessive losses during reciprocating transfers, the maximum CTE is limited to 92.4%. The charge transfer efficiency intrinsically depends on factors like inter-pixel distance, phase clock amplitudes, switching slopes, oxide thickness, semiconductor doping density, and density of surface defects.

We also propose a scheme of three consecutive pixels for charge multiplication, as the fringing field can be enhanced by ramping up the avalanche unit before releasing the held carriers. The simultaneous application of two modes enables us to benefit from CCD and CMOS technologies altogether in one situation allowing flexible manipulation of charge packet. The out-of-plane multiplication is also demonstrated for a single Gr-Si CCD pixel, which can help overcome post-integration and pre-transfer losses.

**Author Contributions:** M.A., Y.D., J.L., H.G., S.C.B., B.Y. and Y.X. proposed the device concept and provided the overall guidance of the project. M.A., J.L., H.G., K.S. and Y.X. designed the device. M.A., Y.D., M.A.A., W.L. and F.T. fabricated and measured the device. M.A., Y.D., S.C.B. and Y.X. drafted the manuscript. All authors have read and agreed to the published version of the manuscript.

**Funding:** This research was funded by National Natural Science Foundation of China (NSFC), grant number 92164106, 61874094, and 62090034.

**Institutional Review Board Statement:** Not Applicable.

**Informed Consent Statement:** Not Applicable.

**Data Availability Statement:** The data related to this study is available from the corresponding authors upon reasonable request.

**Acknowledgments:** This work was supported by ZJU. Micro-Nano Fabrication Center.

**Conflicts of Interest:** The authors declare no conflict of interest.

## References

- Boyle, W.S.; Smith, G.E. Charge- Coupled Devices-a New Approach to Mis Device Structures. *IEEE Spectr.* **1971**, *8*, 18–27.
- Bigas, M.; Cabruja, E.; Forest, J.; Salvi, J. Review of CMOS Image Sensors. *Microelectron. J.* **2006**, *37*, 433–451.
- El Gamal, A.; Eltoukhy, H. CMOS Image Sensors. *IEEE Circuits Devices Mag.* **2005**, *21*, 6–20.
- Durini, D. *High Performance Silicon Imaging: Fundamentals and Applications of CMOS and CCD Sensors*; Woodhead Publishing: Cambridge, UK, 2019; ISBN 9780081024348.
- Shangguan, Q.; Chen, Z.; Yang, H.; Cheng, S.; Yang, W.; Yi, Z.; Wu, X.; Wang, S.; Yi, Y.; Wu, P. Design of Ultra-Narrow Band Graphene Refractive Index Sensor. *Sensors* **2022**, *22*, 6483.
- Cheng, Z.; Liao, J.; He, B.; Zhang, F.; Zhang, F.; Huang, X.; Zhou, L. One-Step Fabrication of Graphene Oxide Enhanced Magnetic Composite Gel for Highly Efficient Dye Adsorption and Catalysis. *ACS Sustain. Chem. Eng.* **2015**, *3*, 1677–1685.
- Chen, H.; Chen, Z.; Yang, H.; Wen, L.; Yi, Z.; Zhou, Z.; Dai, B.; Zhang, J.; Wu, X.; Wu, P. Multi-Mode Surface Plasmon Resonance Absorber Based on Dart-Type Single-Layer Graphene. *RSC Adv.* **2022**, *12*, 7821–7829.
- Zhang, Z.; Cai, R.; Long, F.; Wang, J. Development and Application of Tetrabromobisphenol A Imprinted Electrochemical Sensor Based on Graphene/Carbon Nanotubes Three-Dimensional Nanocomposites Modified Carbon Electrode. *Talanta* **2015**, *134*, 435–442.
- Anwar, M.A.; Ali, M.; Pu, D.; Bodepudi, S.C.; Lv, J.; Shehzad, K.; Wang, X.; Imran, A.; Zhao, Y.; Dong, S.; et al. Graphene—Silicon Diode for 2-D Heterostructure. *IEEE J. Electron Devices Soc.* **2022**, *10*, 970–975.
- Koppens, F.H.L.; Mueller, T.; Avouris, P.; Ferrari, A.C.; Vitiello, M.S.; Polini, M. Photodetectors Based on Graphene, Other Two-Dimensional Materials and Hybrid Systems. *Nat. Nanotechnol.* **2014**, *9*, 780–793.
- George, P.A.; Strait, J.; Dawlaty, J.; Shivaraman, S.; Chandrashekhara, M.; Rana, F.; Spencer, M.G. Ultrafast Optical-Pump Terahertz-Probe Spectroscopy of the Carrier Relaxation and Recombination Dynamics in Epitaxial Graphene. *Nano Lett.* **2008**, *8*, 4248–4251.
- Urich, A.; Unterrainer, K.; Mueller, T. Intrinsic Response Time of Graphene Photodetectors. *Nano Lett.* **2011**, *11*, 2804–2808.
- Zhang, Y.; Zhou, Z.; Wang, J.; Liu, S.; Zhang, Y. *Graphene Nanocomposites in Optoelectronics*; Springer International Publishing: Cham, Switzerland, 2015; ISBN 9783319138756.
- Banszerus, L.; Schmitz, M.; Engels, S.; Dauber, J.; Oellers, M.; Haupt, F.; Watanabe, K.; Taniguchi, T.; Beschoten, B.; Stampfer, C. Ultrahigh-Mobility Graphene Devices from Chemical Vapor Deposition on Reusable Copper. *Sci. Adv.* **2015**, *1*, e1500222.
- Guo, W.; Xu, S.; Wu, Z.; Wang, N.; Loy, M.M.T.; Du, S. Oxygen-Assisted Charge Transfer Between ZnO Quantum Dots and Graphene. *Small* **2013**, *9*, 3031–3036.
- Sun, Z.; Liu, Z.; Li, J.; Tai, G.A.; Lau, S.P.; Yan, F. Infrared Photodetectors Based on CVD-Grown Graphene and PbS Quantum Dots with Ultrahigh Responsivity. *Adv. Mater.* **2012**, *24*, 5878–5883.
- Konstantatos, G.; Badioli, M.; Gaudreau, L.; Osmond, J.; Bernechea, M.; De Arquer, F.P.G.; Gatti, F.; Koppens, F.H.L. Hybrid Graphene-Quantum Dot Phototransistors with Ultrahigh Gain. *Nat. Nanotechnol.* **2012**, *7*, 363–368.
- Nikitskiy, I.; Goossens, S.; Kufer, D.; Lasanta, T.; Navickaite, G.; Koppens, F.H.L.; Konstantatos, G. Integrating an Electrically Active Colloidal Quantum Dot Photodiode with a Graphene Phototransistor. *Nat. Commun.* **2016**, *7*, 11954.
- Howell, S.W.; Ruiz, I.; Davids, P.S.; Harrison, R.K.; Smith, S.W.; Goldflam, M.D.; Martin, J.B.; Martinez, N.J.; Beechem, T.E. Graphene-Insulator-Semiconductor Junction for Hybrid Photodetection Modalities. *Sci. Rep.* **2017**, *7*, 14651.
- Liu, W.; Lv, J.; Peng, L.; Guo, H.; Liu, C.; Liu, Y.; Li, W.; Li, L.; Liu, L.; Wang, P.; et al. Graphene Charge-Injection Photodetectors. *Nat. Electron.* **2022**, *5*, 281–288.
- Lv, J.; Dong, Y.; Cao, X.; Liu, X.; Li, L.; Liu, W.; Guo, H.; Wang, X.; Bodepudi, S.C.; Zhao, Y.; et al. Broadband Graphene Field-Effect Coupled Detectors: From Soft X-Ray to Near-Infrared. *IEEE Electron Device Lett.* **2022**, *43*, 902–905.
- Li, X.; Cai, W.; An, J.; Kim, S.; Nah, J.; Yang, D.; Colombo, L.; Ruoff, R.S. Large-Area Synthesis of High-Quality and Uniform Graphene Films on Copper Foils. *Science* **2009**, *323*, 1312–1315.
- Wan, X.; Xu, Y.; Guo, H.; Shehzad, K.; Ali, A.; Liu, Y.; Yang, J.; Dai, D.; Lin, C. Te; Liu, L.; et al. A Self-Powered High-Performance Graphene/Silicon Ultraviolet Photodetector with Ultra-Shallow Junction: Breaking the Limit of Silicon? *npj 2D Mater. Appl.* **2017**, *1*, 4.
- Lohmann, T.; Von Klitzing, K.; Smet, J.H. Four-Terminal Magneto-Transport in Graphene p-n Junctions Created by Spatially Selective Doping. *Nano Lett.* **2009**, *9*, 1973–1979.

25. Farmer, D.B.; Roksana, G.M.; Perebeinos, V.; Lin, Y.M.; Tuievski, G.S.; Tsang, J.C.; Avouris, P. Chemical Doping and Electron-Hole Conduction Asymmetry in Graphene Devices. *Nano Lett.* **2009**, *9*, 388–392.
26. Joshi, P.; Romero, H.E.; Neal, A.T.; Toutam, V.K.; Tadigadapa, S.A. Intrinsic Doping and Gate Hysteresis in Graphene Field Effect Devices Fabricated on SiO<sub>2</sub> Substrates. *J. Phys. Condens. Matter* **2010**, *22*, 334214.
27. Shin, Y.J.; Kwon, J.H.; Kalon, G.; Lam, K.T.; Bhatia, C.S.; Liang, G.; Yang, H. Ambipolar Bistable Switching Effect of Graphene. *Appl. Phys. Lett.* **2010**, *97*, 1–4.
28. Wang, H.; Wu, Y.; Cong, C.; Shang, J.; Yu, T. Hysteresis of Electronic Transport in Graphene Transistors. *ACS Nano* **2010**, *4*, 7221–7228.
29. Brant, J.C.; Leon, J.; Barbosa, T.C.; Araujo, E.N.D.; Archanjo, B.S.; Plentz, F.; Alves, E.S. Hysteresis in the Resistance of a Graphene Device Induced by Charge Modulation in the Substrate. *Appl. Phys. Lett.* **2010**, *97*, 042113.
30. Shi, Y.; Fang, W.; Zhang, K.; Zhang, W.; Li, L.-J. Photoelectrical Response in Single-Layer Graphene Transistors. *Small* **2009**, *5*, 2005–2011.
31. Jung, I.; Dikin, D.; Park, S.; Cai, W.; Mielke, S.L.; Ruoff, R.S. Effect of Water Vapor on Electrical Properties of Individual Reduced Graphene Oxide Sheets. *J. Phys. Chem. C* **2008**, *112*, 20264–20268.
32. Shi, Y.; Dong, X.; Chen, P.; Wang, J.; Li, L.J. Effective Doping of Single-Layer Graphene from Underlying SiO<sub>2</sub> Substrates. *Phys. Rev. B -Condens. Matter Mater. Phys.* **2009**, *79*, 1–4.
33. Liao, Z.M.; Han, B.H.; Zhou, Y.B.; Yu, D.P. Hysteresis Reversion in Graphene Field-Effect Transistors. *J. Chem. Phys.* **2010**, *133*, 44703.
34. Lee, Y.G.; Kang, C.G.; Jung, U.J.; Kim, J.J.; Hwang, H.J.; Chung, H.J.; Seo, S.; Choi, R.; Lee, B.H. Fast Transient Charging at the Graphene/ SiO<sub>2</sub> Interface Causing Hysteretic Device Characteristics. *Appl. Phys. Lett.* **2011**, *98*, 98–101.
35. Berglund, C.N.; Boll, H.J. Performance Limitations of the IGFET Bucket-Brigade Shift Register. *IEEE Trans. Electron Devices* **1972**, *19*, 852–860.
36. Berglund, C.N.; Strain, R.J. Fabrication and Performance Considerations of Charge-Transfer Dynamic Shift Registers. *Bell Syst. Tech. J.* **1972**, *51*, 655–703.
37. M.P.Singh, S.D.B. Influence of Clocking Waveform on Charge Transfer in Three Phase Charge Coupled Devices. *Solid. State. Electron.* **1976**, *19*, 279–287.
38. Vieu, C.; Carcenac, F.; Pépin, A.; Chen, Y.; Mejias, M.; Lebib, A.; Manin-Ferlazzo, L.; Couraud, L.; Launois, H. Electron Beam Lithography: Resolution Limits and Applications. *Appl. Surf. Sci.* **2000**, *164*, 111–117.
39. Madan, S.K.; Bhaumik, B.; Vasi, J.M. Experimental Observation of Avalanche Multiplication in Charge-Coupled Devices. *IEEE Trans. Electron Devices* **1983**, *30*, 694–699.
40. Sayle, W.E.; Lauritzen, P.O. Avalanche Ionization Rates Measured in Silicon and Germanium at Low Electric Fields. *IEEE Trans. Electron Devices* **1971**, *18*, 58–66.
41. Maes, W.; De Meyer, K.; Van Overstraeten, R. Impact Ionization in Silicon: A Review and Update. *Solid State Electron.* **1990**, *33*, 705–718.
42. Lou, L.F.; Tettermer, G.L. Characterization of Metal-Oxide-Semiconductor Capacitors with a Fast-Ramp Technique. *J. Appl. Phys.* **1988**, *63*, 5398–5405.
43. You, A.; Be, M.A.Y.; In, I. An Experimental Study of a Metal-Oxide- Semiconductor Photomultiplier. *J. Appl. Phys.* **1989**, *66*, 2678–2688.
44. Cova, S.; Ghioni, M.; Lacaita, A.; Samori, C.; Zappa, F. Avalanche Photodiodes and Quenching Circuits for Single-Photon Detection. *Appl. Opt.* **1996**, *35*, 1956.
45. Zappa, F.; Lotito, A.; Giudice, A.C.; Cova, S.; Ghioni, M. Monolithic Active-Quenching and Active-Reset Circuit for Single-Photon Avalanche Detectors. *IEEE J. Solid-State Circuits* **2003**, *38*, 1298–1301.
46. Hu, C.; Liu, M.; Zheng, X.; Campbell, J.C. Dynamic Range of Passive Quenching Active Reset Circuit for Single Photon Avalanche Diodes. *IEEE J. Quantum Electron.* **2010**, *46*, 35–39.
47. Liu, M.; Hu, C.; Campbell, J.C.; Pan, Z.; Tashima, M.M. Reduce Afterpulsing of Single Photon Avalanche Diodes Using Passive Quenching with Active Reset. *IEEE J. Quantum Electron.* **2008**, *44*, 430–434.
48. Awaki, H.; Hamaguchi, K.; Koyama, K.; Tomida, H.; Tsuru, T. Development of a Fast Readout System of an X-Ray CCD. *Nucl. Instrum. Methods Phys. Res. Sect. A Accel. Spectrometers Detect. Assoc. Equip.* **1999**, *436*, 170–173.
49. Alessandri, C.; Abusleme, A.; Guzman, D.; Passalacqua, I.; Alvarez-Fontecilla, E.; Guarini, M. Optimal CCD Readout by Digital Correlated Double Sampling. *Mon. Not. R. Astron. Soc. Lett.* **2020**, *455*, 1443–1450.
50. Touron, P.; Roy, F.; Magnan, P.; Marcelot, O.; Demiguel, S.; Virmondois, C. Capacitive Trench-Based Charge Transfer Device. *IEEE Electron Device Lett.* **2020**, *41*, 1388–1391.
51. Hardy, T.; Murowinski, R.; Deen, M.J. Charge Transfer Efficiency in Proton Damaged CCD's. *IEEE Trans. Nucl. Sci.* **1998**, *45*, 154–163.
52. Waczynski, A.; Polidan, E.J.; Marshall, P.W.; Reed, R.A.; Johnson, S.D.; Hill, R.J.; Delo, G.S.; Wassell, E.J.; Cheng, E.S. A Comparison of Charge Transfer Efficiency Measurement Techniques on Proton Damaged N-Channel CCDs for the Hubble Space Telescope Wide-Field Camera 3. *IEEE Trans. Nucl. Sci.* **2001**, *48*, 1807–1814.