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A Contemporary Design Process for Single-Phase Voltage Source Inverter Control Systems

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Abstract: This paper presents an overview of contemporary voltage source inverter control system design. Design begins with the theoretical considerations that lead to the creation of the system's differential control law. This stage does not include scaling coefficients for the output voltage, output current, and filter inductor current. Following this, the inverter is modelled in MATLAB's Simulink environment with an appropriate load and control system. If the resultant simulation provides satisfactory results, a hybrid system consisting of MATLAB's Simulink and dSpace libraries with the MicroLabBox device is used to interface the simulation with an experimental hardware model in real-time. This allows the hardware plant and measuring traces to be validated. ControlDesk is used to scale the relevant coefficients. During the final stage of the design process, a microprocessor is programmed to control the inverter according to the dSpace simulation results. This requires new scaling values. Throughout every stage of the design process, too high a value of the modulation index disables the reduction of output voltage distortions. This paper details the entire design process for both single-input and multi-input control systems, explaining the scaling process and the required software. Such a modern design process ensures the shortest time between conceptualization and the final product.

Keywords: voltage source inverter; coefficient diagram method; passivity based control; SISO control; MISO control; real-time interface

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1. Introduction

The design of a voltage source inverter (VSI) control system begins with a theoretical description of the differential control law that governs the system. The control system should then be verified via simulation (the standard approach is to use MATLAB's Simulink environment) before finally being implemented on the microprocessor or FPGA system of the experimental VSI. Continuous control laws require further discretization so better is to use the discrete control laws at the beginning. Following validation of the experimental VSI, the final product can be realized. Ideally, this approach is fast and effective. However, following theoretical calculations the output voltage, output current, and filter inductor current scaling factors remain undetermined. These factors all affect the coefficients within the control law. The scaling of voltages and currents in simulation is straightforward. The reference voltage amplitude is defined as unity, and all voltage and current measurements are divided by the input DC voltage. Contemporary design methodologies feature one additional step. Via a MicroLabBox-RTI1202 real-time interface hardware, the dSpace software (including libraries) can be used to drive the experimental VSI using the Simulink model. Throughout all stages of the design process, too high a value of the modulation index disables output voltage distortions from being reduced. The pulse-width modulation (PWM) modulator can become saturated during dynamic increases of the load [1]. However, a modulation index that is too low decreases the efficiency of the VSI. To strike a balance, the modulation index is set to 60% throughout this paper. The literature contains

many examples of the use of dSpace with different real-time interfaces in power electronic systems [2–4]. However, this paper demonstrates the entire process by which dSpace is used with a real-time hardware interface during the design process of a VSI. When using MicroLabBox the scaling process is similar to that of the final microprocessor controller, because the voltage and currents are amplified within the experimental VSI device and the hardware VSI plant is controlled. Furthermore, the reference sinusoidal waveform amplitude that corresponds to a modulation index of 100% depends on the PWM modulation scheme [5–7]. The reference waveform amplitude takes the value of unity for the Simulink modulator, and 0.5 for the dSpace modulator used for the first modulation scheme in this paper. When subject to microprocessor control, the amplitude depends on the quotient of the PWM unit comparator input frequency and the switching frequency (in the presented experiment it is 1640). The final step of the design process is the implementation of the controller on the microprocessor. Other than when using Simulink, this requires further scaling of the current versus voltage measurements. The scaling process requires dedicated software: dSpace requires ControlDesk; microprocessor control requires dedicated PC software that can support data exchange with the inverter via a USB port. An additional problem is the evaluation of a Bode plot of the measurement traces [8,9]. This is typically modelled within a frequency range lower than the resonant frequency of the output filter as a simple delay, with one switching period for the amplifiers and one switching period for the PWM modulator [10].

The objective of this paper is to provide a detailed account of the contemporary design of VSI control systems. This process will be demonstrated using two examples. The first example is a simple single input single output (SISO) control system that uses the discretized coefficient diagram method (CDM) [10–16], requiring only a single input variable: output voltage. The second example is a more complex multiple input single output (MISO) control system using passivity-based control (PBC) [10–12,17–20], with measurements of the output voltage, output current, and inductor current. Specifically, this paper uses improved PBC v2 (IPBC2) [10]. Figure 1 presents the entire VSI controller design process, from the theoretical description to the final product. This includes the use of MATLAB's Simulink environment, the combination of dSpace and ControlDesk via a MicroLabBox-RTI1202 real-time interface, Keil µVision C++, dedicated PC software written in C#, and the experimental model with a STM32F407VG microprocessor.

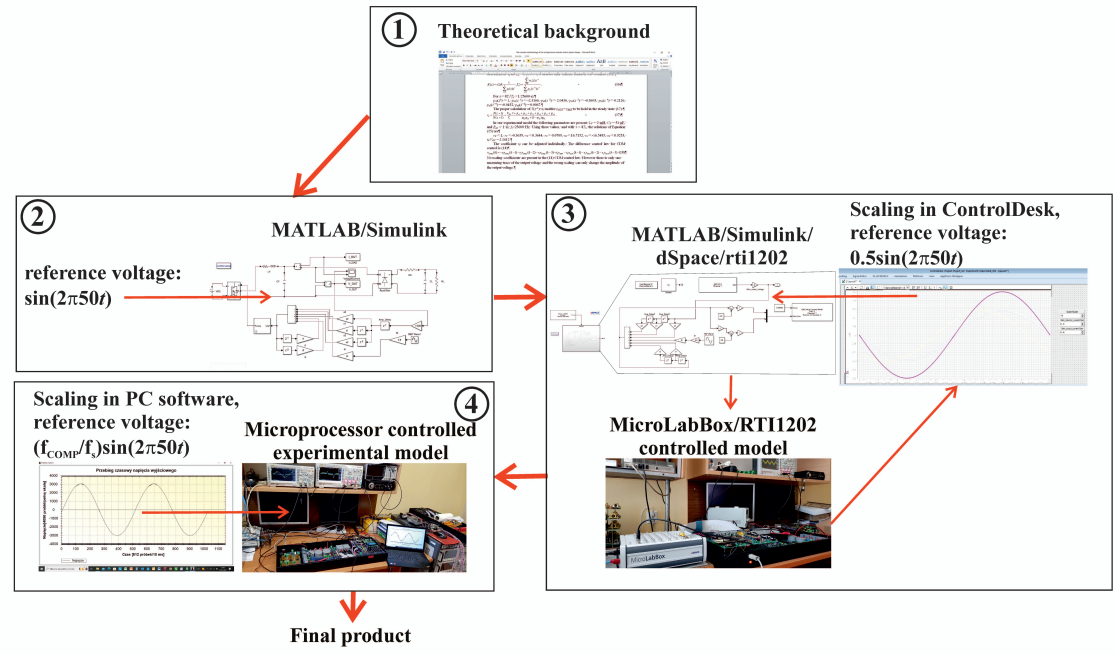


Figure 1. Flowchart of the modern VSI controller design process.

The novelty of the paper is:

1. Presentation of the full process of design–from a theoretical background, through the simulation, using real time interface (RTI) and dSpace libraries up to the final stage of the design process–programming the microprocessor that will control the VSI. Using real time interface creates design much more flexible.
2. Definition of requirements of the design process final success:
   (a) The control law should be realized in a similar way in all the stages of the design process. It means that in the simulation the input controller data and supply of the reference waveform was measured using a sample time equal to the switching period. The PWM modulator should have the sample time equal to the period of the waveform on the input of the microprocessor PWM unit comparator (the much higher frequency than the switching frequency).
   (b) The real time interface and the microprocessor should use the same software architecture based on interrupts (trigger events in case of the RTI) from the PWM modulator.
   (c) The scaling procedure is crucial because wrong scaling changes the control law coefficients. In none of the referred papers [2–4] concerning the RTI usage, the scaling procedure of voltages and currents is presented. In [3] where the RTI–MicroLabBox and dSpace software was used there is nothing about using ControlDesk–the software that enables scaling.

Scaling the microprocessor controller requires data transfer from the PC and using specialized software to visualize the measured values scaled in units of the analog-to-digital converter used in the microprocessor. The scaling procedure depends on the ratio of the PWM modulator comparator input frequency and the switching frequency. It is described in detail in the presented paper.

This paper will be useful for engineers and researchers who design VSIs, by presenting them the novel suite of design tools and techniques that are required, in addition to instructions on their application. Using RTI (MicroLabBox with dSpace) makes the design process more flexible and faster.

Sections 2–5 present the design process for SISO CDM control, and Sections 6–9 present the design process for MISO PBC control. The control results are presented and compared using the total harmonic distortion (THD) of the VSI output voltage for a nonlinear rectifier RC load with power factor $PF = 0.7$.

2. Theoretical Background of SISO CDM Control Materials

Figure 2 shows a VSI with a SISO controller. The output current is treated as an independent disturbance or the state variable, with the same result in both cases [11,16,20–24].

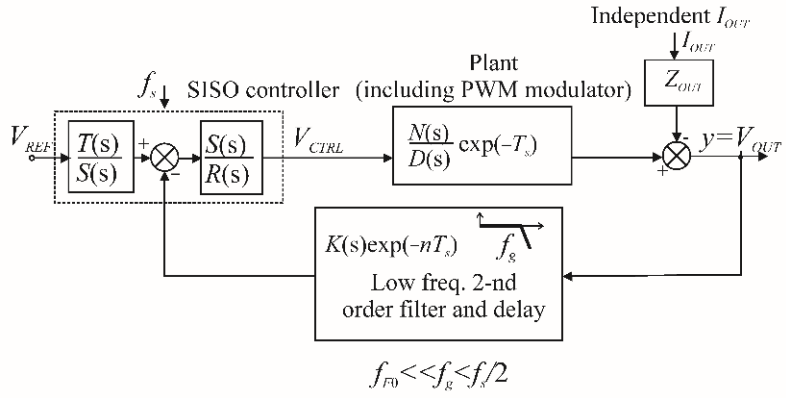


Figure 2. SISO control of a VSI.

One of the simplest control designs is Manabe's CDM controller [13,14,16], which uses *T*, *S*, and *R* polynomials. In its most basic form, the coefficients of the closed-loop characteristic equation are calculated from Manabe standard form. These coefficients provide the control for the time constant τ of the closed-loop system. The output voltage of a closed loop system with the output current treated as an independent disturbance is given by (1):

$$v_{OUT}(s) = \frac{T(s)N(s)}{R(s)D(s)+S(s)N(s)}v_{REF}(s) - \frac{Z_{OUT}R(s)D(s)}{R(s)D(s)+S(s)N(s)}I_{OUT}(s) \quad (1)$$

where *N(s)* contains all the loop delays. The characteristic equation of a closed-loop system is given by (2):

$$P(z^{-1}) = R(z^{-1})D(z^{-1}) + S(z^{-1})N(z^{-1}) = \sum_{i=0}^{n} p_{zi}z^{-i}. \quad (2)$$

To calculate the controller parameters, a model of the inverter plant is required [6]. For this paper, the inverter plant was modelled as an output L_FC_F filter described by the assigned state variables (3):

$$\mathbf{x} = [v_{OUT} \quad i_{LF} \quad i_{OUT}]^T, \quad (3)$$

and the state Equation (4):

$$\dot{\mathbf{x}} = \mathbf{A}\mathbf{x} + \mathbf{B}\mathbf{u}, \quad (4)$$

where matrix **A** and **B** are given by (5):

$$\mathbf{A} = \begin{bmatrix} 0 & \frac{1}{C_F} & -\frac{1}{C_F} \\ -\frac{1}{L_F} & -\frac{R_{LF}}{L_F} & 0 \\ 0 & 0 & 0 \end{bmatrix}, \mathbf{B} = \begin{bmatrix} 0 \\ \frac{1}{L_F} \\ 0 \end{bmatrix}. \quad (5)$$

The state Equation (4) are solved during a single *k*-th switching period T_s, for double edge three-level PWM, with a switching-on time period T_{ONk}. The solution of the state space equations depends on the type of modulation—double edge, three-level modulation was chosen as the most suitable for a four-transistor bridge. Some schemes of this type of modulation are presented in [5–7]. This paper uses the first presented scheme, as this is most appropriate for instantaneous control. An overview of the scheme is shown in Figure 3. The advantages of this controller include the possibility of controlling output voltage when crossing zero, and an output switching frequency double that of the transistor switching frequency.

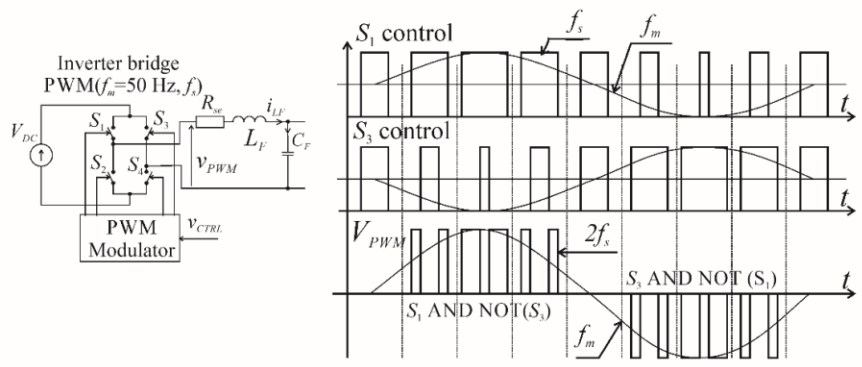


Figure 3. Overview of the first PWM modulation scheme.

Each transistor within the two legs of the H-bridge is switched with frequency f_s. However, the final switching frequency of the output waveform is $2f_s$, due to the current flowing through the pairs of switches connected in series: S_1 and S_4 or S_3 and S_2. This results in two output pulses during a single switching period. Within the modulation scheme the control of the switches can be described analytically as (6)–(9):

$$S_1 : T_{ON}(k)/T_s \;=\; 0.5M\sin(k\frac{2\pi}{f_s/f_m}) + 0.5M, \tag{6}$$

$$S_2 : NOT(S_1), \tag{7}$$

$$S_3 : T_{ON}(k)/T_s \;=\; 0.5M\sin((k\frac{2\pi}{f_s/f_m}) + \pi) + 0.5M, \tag{8}$$

$$S_4 : NOT(S_3), \tag{9}$$

where T_{ON} is the switching on time during a single switching period $T_s = 1/f_s$, and $k = 0 \ldots (f_s/f_m - 1)$ and f_s/f_m is an integer.

Solving the state space equations provides the exponential function $\mathbf{x}_{k+1}$ of T_{ONk}, which can then be linearized [6]. This gives the discrete linear state Equation (10):

$$\mathbf{x}_{k+1} \;=\; \mathbf{A}_D\mathbf{x}_k + \mathbf{G}_D T_{ONk}, \tag{10}$$

where the state matrix $\mathbf{A}_D$ and the state matrix $\mathbf{G}_D$ are given by (11), (12):

$$\mathbf{A}_D \;=\; e^{\mathbf{A}T_s} \;=\; \mathbf{\Phi}(T_s) \;=\; L^{-1}[(s\mathbf{I}-\mathbf{A})^{-1}]\Big|_{t\,=\,T_s},\; \mathbf{A}_D \;=\; \mathbf{\Phi}(T_s) \;=\; \begin{bmatrix} \phi_{11} & \phi_{12} & \phi_{13} \\ \phi_{21} & \phi_{22} & \phi_{23} \\ \phi_{31} & \phi_{32} & \phi_{33} \end{bmatrix}, \tag{11}$$

$$\mathbf{G}_D \;=\; e^{\mathbf{A}T_s/2}\mathbf{B}V_{DC} \;=\; \mathbf{\Phi}(T_s/2)\mathbf{B}V_{DC},\; \mathbf{G}_D \;=\; \begin{bmatrix} g_{11} \\ g_{21} \\ g_{31} \end{bmatrix}, \tag{12}$$

with coefficients ϕ_{ij} (13) and g_{i1} (14):

$$\begin{gathered} \xi_F \;=\; \tfrac{1}{2}R_{se}\sqrt{\tfrac{C_F}{L_F}},\; \omega_{F0} \;=\; \tfrac{1}{\sqrt{L_F L_F}}, \\ \phi_{11} \;=\; [\cos(\omega_{F0}T_s) + \xi_F\sin(\omega_{F0}T_s)]\exp(-\xi_F\omega_{F0}T_s), \\ \phi_{12} \;=\; \tfrac{1}{\omega_{F0}C_F}\sin(\omega_{F0}T_s)\exp(-\xi_F\omega_{F0}T_s), \\ \varphi_{13} \;=\; -\varphi_{12} + R_{LF}(\varphi_{11} - 1), \\ \phi_{21} \;=\; -\tfrac{C_F}{L_F}\varphi_{12}, \\ \phi_{22} \;=\; [\cos(\omega_{F0}T_s) - \xi_F\sin(\omega_{F0}T_s)]\exp(-\xi_F\omega_{F0}T_s), \\ \phi_{23} \;=\; 1 - \varphi_{11},\; \phi_{31} \;=\; 0,\; \phi_{32} \;=\; 0,\; \phi_{33} \;=\; 1. \end{gathered} \tag{13}$$

$$\begin{gathered} g_{11} \;=\; V_{DC}\omega_{F0}\sin(\omega_{F0}\tfrac{T_s}{2})\exp(-\xi_F\omega_{F0}\tfrac{T_s}{2}), \\ g_{21} \;=\; \tfrac{V_{DC}}{L_F}[\cos(\omega_{F0}\tfrac{T_s}{2}) - \xi_F\sin(\omega_{F0}\tfrac{T_s}{2})]\exp(-\xi_F\omega_{F0}\tfrac{T_s}{2}), \\ g_{31} \;=\; 0. \end{gathered} \tag{14}$$

For a double edge PWM and a digital modulator implementing all the required loop delays, the VSI gain is given by (15):

$$K_{VSI} \;=\; \frac{N(z^{-1})}{D(z^{-1})} \;=\; \frac{a_2z^{-2} + a_3z^{-3}}{1 + b_1z^{-1} + b_2z^{-2}}, \tag{15}$$

where (16):

$$a_2 = \frac{T_s}{V_{DC}} g_{11},\ a_3 = \frac{T_s}{V_{DC}} (\varphi_{12} g_{21} - \varphi_{22} g_{11}),\ b_1 = -(\varphi_{11} + \varphi_{22}),\ b_2 = \varphi_{11}\varphi_{22} - \varphi_{12}\varphi_{21}. \quad (16)$$

For a system that is subject to a disturbance, the degrees of R and S are greater than or equal to $n - 1$, where n is the degree of D. The second degree of S and the second degree of R are given by (17):

$$S(z^{-1}) = \sum_{i=0}^{2} s_i z^{-i},\ R(z^{-1}) = \sum_{i=0}^{2} r_i z^{-i},\ r_0 = 1. \quad (17)$$

The underlying objective of CDM control is to obtain the s_i and r_i coefficients are thereby solve the Diophantine Equation (18):

$$(1 + r_1 z^{-1} + r_2 z^{-2})(1 + b_1 z^{-1} + b_2 z^{-2}) + (s_0 + s_1 z^{-1} + s_2 z^{-2})(a_2 z^{-2} + a_3 z^{-3}) = 1 + \sum_{i=1}^{5} p_{zi} z^{-i}, \quad (18)$$

which can be written as (19):

$$\begin{bmatrix} 1 & 0 & 0 & 0 & 0 \\ b_1 & 1 & a_2 & 0 & 0 \\ b_2 & b_1 & a_3 & a_2 & 0 \\ 0 & b_2 & 0 & a_3 & a_2 \\ 0 & 0 & 0 & 0 & a_3 \end{bmatrix} \begin{bmatrix} r_1 \\ r_2 \\ s_0 \\ s_1 \\ s_2 \end{bmatrix} = \begin{bmatrix} p_{z1} - b_1 \\ p_{z2} - b_2 \\ p_{z3} \\ p_{z4} \\ p_{z5} \end{bmatrix}, \quad (19)$$

where the p_{zi} coefficients are assigned from the Manabe standard form, and it was assumed that $r_0 = p_0 = 1$. The coefficients p_i of the fifth degree of Manabe standard form for a continuous system are given by

$$p_0(s^0) = 1, p_1(s^1) = p_0\tau, p_2(s^2) = 0.4p_0\tau^2, p_3(s^3) = 0.08p_0\tau^3, p_4(s^4) = 0.008p_0\tau^4, p_5(s^5) = 0.0004p_0\tau^5,$$

where τ is the time constant of a closed-loop system. For f_s = 25,600 Hz, satisfactory experimental results were obtained with $\tau = 5.5T_s$. Lower values of τ lead to output voltage oscillations; higher values of τ lead to poorer control.

Via the zero-order hold method and a discretization cycle of T_s = 1/25,600 s, the MATLAB *c2d* function was used to obtain a discrete-time transfer function (20):

$$K(z) = c2d\left(\frac{1}{\sum_{i=0}^{5} p_i(s) s^i}, T_s\right) = \frac{\sum_{i=0}^{5} w_i(z) z^{-i}}{\sum_{i=0}^{5} p_{zi}(z^{-1}) z^{-i}}. \quad (20)$$

For $\tau = 5.5T_s$ (T_s = 1/25,600 s),

$$p_{z0}(z^0) = 1, p_{z1}(z^{-1}) = -1.9655, p_{z2}(z^{-2}) = 1.5925, p_{z3}(z^{-3}) = -0.7017, p_{z4}(z^{-4}) = 0.1886, p_{z5}(z^{-5}) = -0.0263.$$

The accurate calculation of $T(z^{-1}) = t_0$ enables $v_{OUT} = v_{REF}$ to be maintained in the steady state (21):

$$t_0 = \frac{P(z = 1)}{N(z = 1)} = \frac{V_{DC}}{T_s} \frac{1 + p_{z1} + p_{z2} + p_{z3} + p_{z4} + p_{z5}}{\varphi_{12} g_{21} + (1 - \varphi_{22}) g_{11}}. \quad (21)$$

The experimental model used the following parameters: L_F = 2 mH, C_F = 51 µF, R_{se} = 1 Ω, and f_s = 25,600 Hz. Using these values, and with $\tau = 5.5T_s$, the solutions of Equation (19) are

$$r_0 = 1, r_1 = -0.0299, r_2 = 0.3758, s_0 = 28.0795, s_1 = -20.2981, s_2 = -3.6181,$$
$$t_0/V_{DC} = 5.5090.$$

The coefficient t_0 can be adjusted individually and is multiplied by the modulation index M. This should always be less than unity to allow for the rapid increase of the voltage in the input of the output filter. The difference control law for CDM control is given by (22):

$$v_{CTRL}(k) = \begin{array}{c} -r_1 v_{CTRL}(k-1) - r_2 v_{CTRL}(k-2) + t_0 v_{REF} - \\ s_0 v_{OUT}(k-1) - s_1 v_{OUT}(k-2) - s_2 v_{OUT}(k-3) \end{array}, \quad (22)$$

which contains no scaling coefficient. The scaling coefficients will be further incorporated into Equation (22).

3. MATLAB's Simulink Simulation of SISO CDM Control

As shown in Figure 4, the controller was modelled in the Simulink environment of MATLAB R2021b. The Simulink model was tested with the calculated scaling coefficients. The simulation results are shown in Figure 5. The scaling coefficient is simply $1/V_{DC}$, because the reference sinusoidal waveform $\sin(2\pi 50t)$ has a unity amplitude. The PWM modulator unit has an input range of ±1. The output voltage measuring trace is modelled as a single switching period delay [10], with the PWM modulator contributing an additional delay of T_s. The most demanding test load is the nonlinear rectifier RC load (Figure 5c,d present it for R = 100 Ω, C = 430 µF, when PF = 0.7). This is defined by the EN 62040 standard [25] as the most common load for an uninterruptible power supply with an output power of less than 3 kW. Figure 5a,b show a less demanding nonlinear load with R = 100 Ω and C = 100 µF.

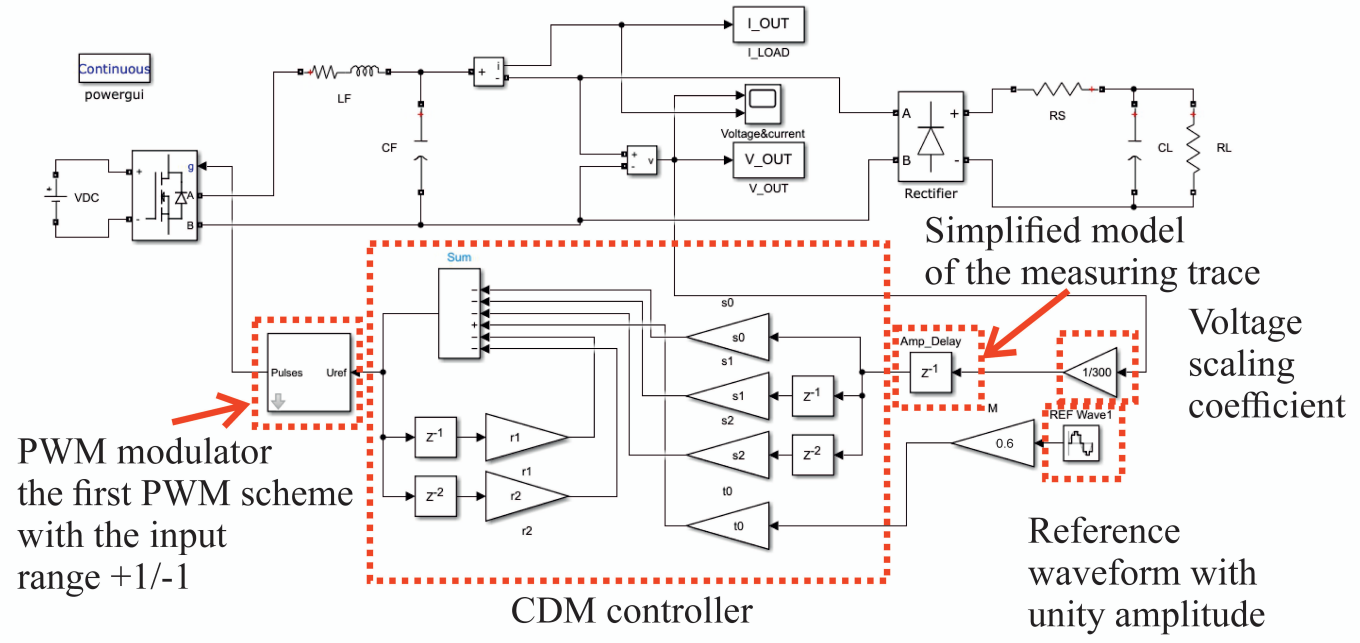


Figure 4. The MATLAB's Simulink model of the VSI with SISO-CDM control.

The performance of the control is estimated by the THD of the output voltage (Figure 5), with the operation of the VSI under CDM control (Figure 5b,d) being compared with its open loop operation (Figure 5a,c). The CDM controller was tested using a relatively low modulation index of $M = 0.6$ to prevent the saturation of the modulator that can occur for higher values of M. The same value will be used throughout this paper.

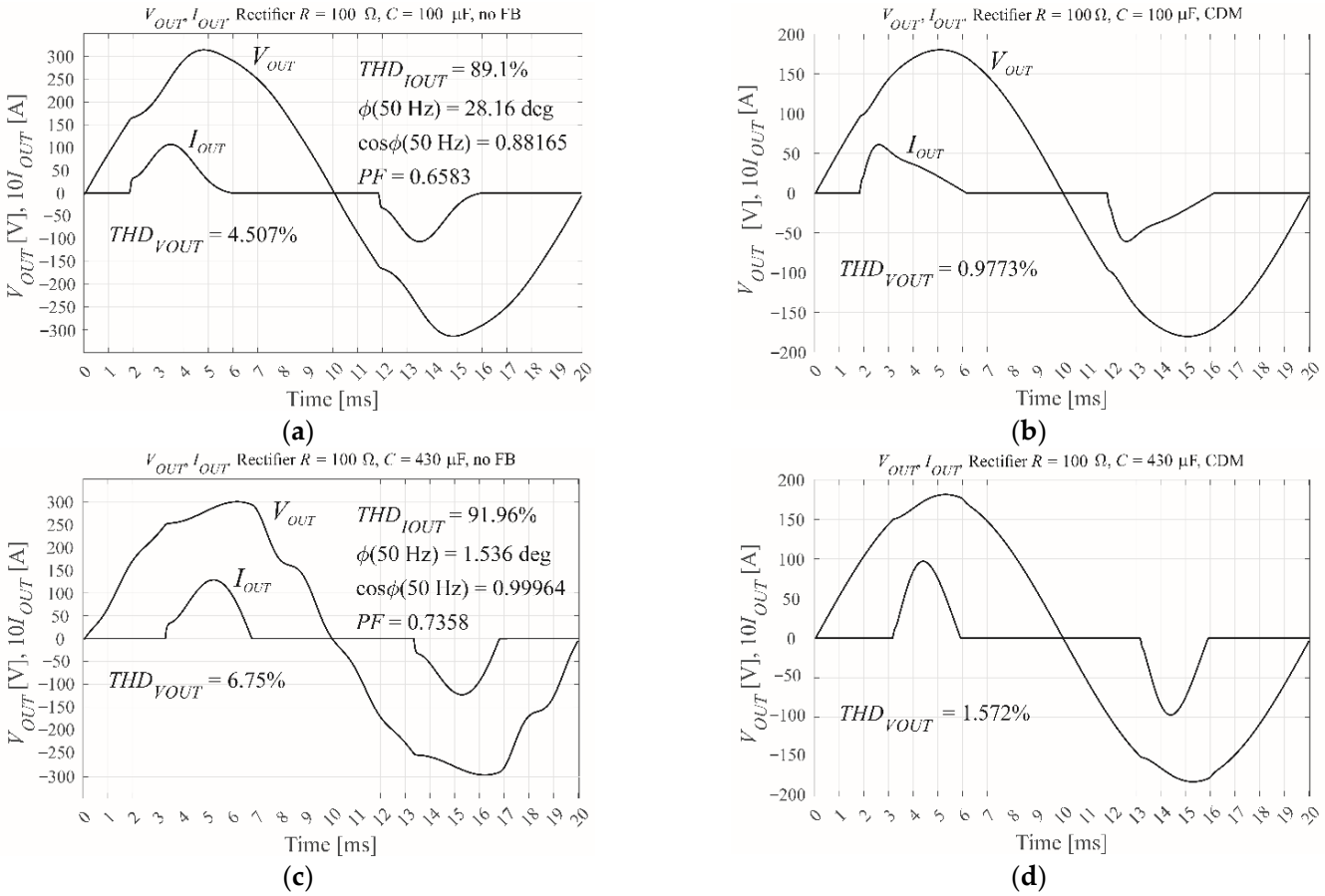


Figure 5. The simulated output voltage and current for the VSI when subject to a nonlinear rectifier RC load, showing (**a**) open loop with $R = 100\ \Omega$, $C = 100\ \mu F$, and $PF = 0.7$, (**b**) CDM control with $R = 100\ \Omega$, $C = 100\ \mu F$, and $M = 0.6$, (**c**) open loop with $R = 100\ \Omega$, $C = 430\ \mu F$, and $PF = 0.7$, and (**d**) CDM control with $R = 100\ \Omega$, $C = 430\ \mu F$, and $M = 0.6$.

4. Interfacing MATLAB's Simulink and dSpace Simulation of the SISO CDM Controller with the Experimental Model

Following initial simulations in Simulink, the MicroLabBox RTI1202 real-time interface was used to interface dSpace simulation blocks with the experimental model. To this end, the dSpace RTI1202 FPGA and dSpace RTI Electric Motor Control Blockset libraries were used. The compiled simulation was automatically loaded onto the MicroLabBox FPGA to provide high speed data conversion and computation with little time delay. The simulation should be designed to imitate the microprocessor procedure as closely as possible. The microprocessor control software used an infinite main loop (defined using while (1)), with the "watchdog" and all functions are handled by PWM interrupts which fetch the analogue-to-digital converter (ADC) values of the output voltage. In the dSpace simulation, the interrupts are represented by Trigger line 1 events from an EMC Multichannel PWM block, which are handled by an ADC Class 1 Hardware Interrupt block. This Hardware Interrupt (HWINT) block is connected to the input port of the Function-Call Subsystem, which contains all the components of the inverter control blocks, including the EMC Multichannel PWM block and the ADC Class 1 block. The sample time of each of these blocks is inherited

from the PWM block triggering event. In a similar manner to the microprocessor software, the switching frequency is the input of the PWM block.

Once loaded with the control software, MicroLabBox can drive the experimental inverter using four DIO Class 1 3.3 V digital outputs, operating on channels 1–4. MicroLabBox receives the measured output voltage via the ADC Class 1 channel 1, with a single conversion (−10–+10 V input range) following the trigger event from the PWM block. The PWM block is configured to drive a block of four transistors with inverting signals for the low transistors. A 500 ns dead time is implemented for the experimental inverter. For the case of inverted channels set as active, the block automatically reserves the same number of channels for inverted signals as specified for non-inverted signals. The first inverted channel is channel 3, corresponding to S_2 in Figure 3. The second inverted channel is channel 4, corresponding to S_4 in Figure 3. The PWM block inputs take values in the range 0–1. Hence, the input waveforms are sinusoidal with an amplitude of 0.5, shifted mutually 180 degrees in phase and both raised 0.5 with zero level. The generation of the two shifted strings for the PWM block inputs is presented in Figure 6. The measured output voltage waveforms are visualized via ControlDesk, which is part of the dSpace software package. The output voltage is scaled by using the Time Plotter feature of ControlDesk to compare two waveforms. For an open loop system and a nominal resistance load of 50 Ω, the measured output voltage should be given by the reference waveform $0.5\sin(2\pi 50t)$. Once these waveforms have been equalized, by changing the gain of the output voltage, the output voltage gain value is set as a scaling coefficient. The measuring trace can reverse the sign of the signal (in the experimental model), so the sign must be set correctly. With a modulation index of $M = 0.6$, it was found an output voltage scaling coefficient of −2.

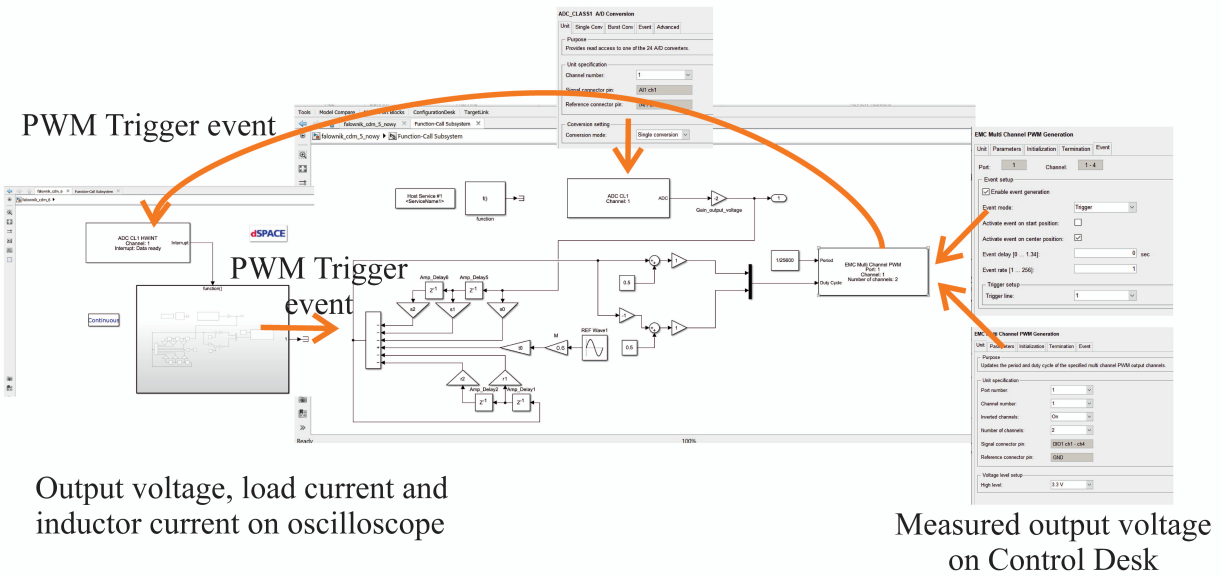


Figure 6. *Cont.*

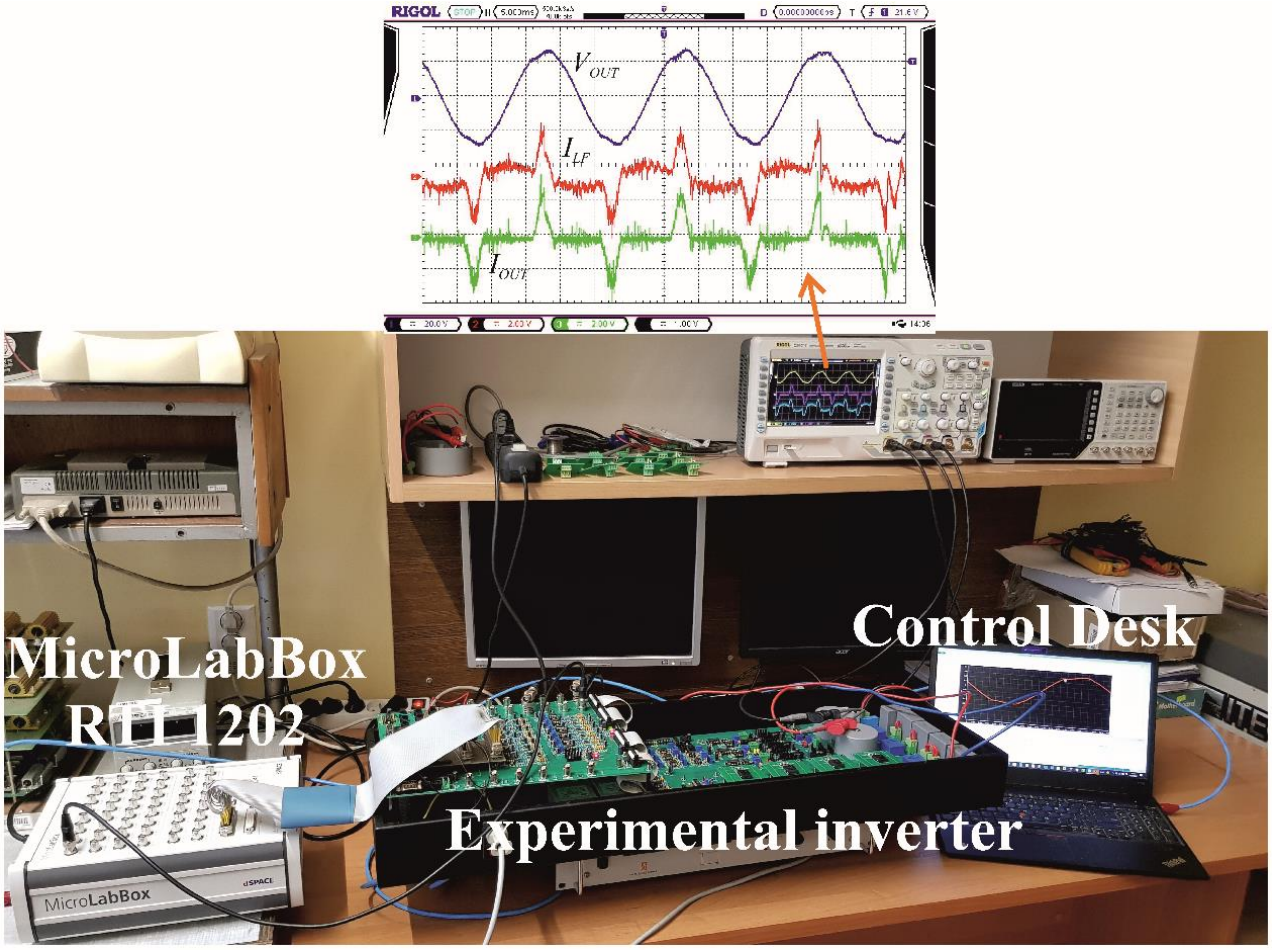
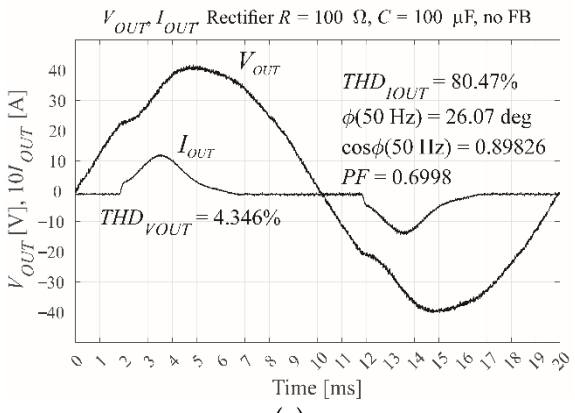
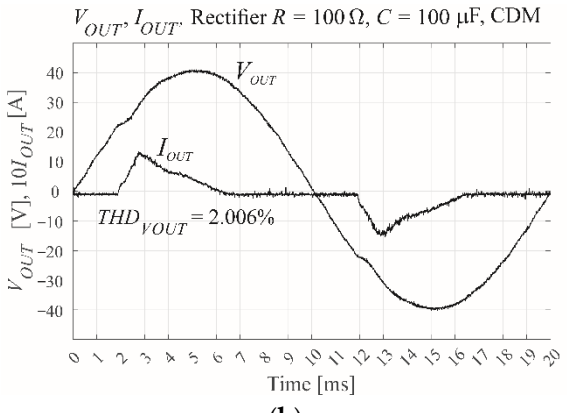


Figure 6. The real-time interface of the dSpace simulation blocks and the experimental inverter using MicroLabBox RTI1202.

Figure 7 shows the results of CDM control via the MicroLabBox, versus open loop control of the same system. Both approaches use a nonlinear rectifier *RC* load with100 µF or 430 µF, 100 Ω, and $PF \approx 0.7$. The results show a change in the shape of the load current, with the current loading forced to the load capacitor. A lower filter inductor value L_F would produce a smaller THD coefficient.

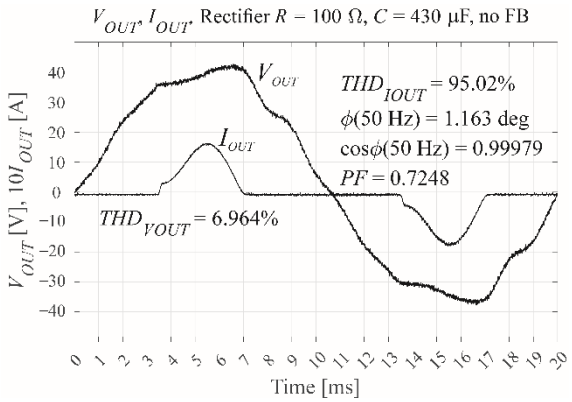


(**a**)

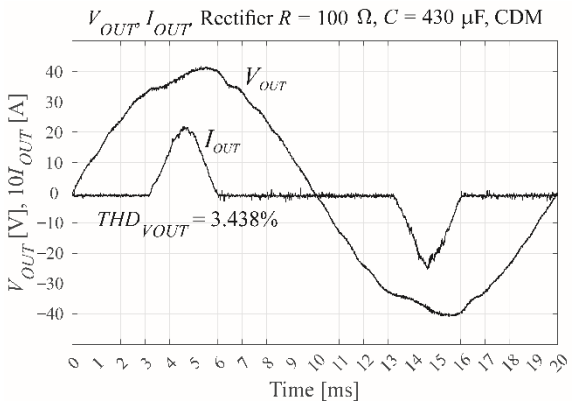


(**b**)

Figure 7. *Cont.*



(**c**)



(**d**)

Figure 7. The measured output voltage and current of the experimental VSI using MicroLabBox real time interface when subject to a nonlinear rectifier RC load, showing (**a**) open loop with R = 100 Ω, C = 100 μF, and PF = 0.7, (**b**) CDM control with R = 100 Ω, C = 100 μF, and M = 0.6, (**c**) open loop with R = 100 Ω, C = 430 μF, and PF = 0.7, and (**d**) CDM control with R = 100 Ω, C = 430 μF, and M = 0.6.

5. Implementation of the CDM Controller in the VSI Microprocessor

The final step of the design process was to implement the validated controller on the STM32F407VG microprocessor. The microprocessor code was written in Keil μVision 5 C++. As described in Section 4, the main function of the code consists of an infinite loop, with functions called by an event handler that waits for PWM unit interrupts. Hence, the control process is identical to that provided by MicroLabBox. However, the two approaches differ in terms of the scaling of the output voltage measuring trace. The dedicated PC application that handles data transmission, data visualization, and communication with the microprocessor-controlled inverter via USB port was written in C#. The purpose of this application is analogous to the role played by the ControlDesk software for the MicroLabBox controlled system. However, in the older solutions, it was possible to use the digital-to-analogue converter implemented in the microprocessor to visualize on the oscilloscope the internal waveforms from the microprocessor without the dedicated PC software. The reference voltage takes the form $0.5f_{COMPmax}/f_s\sin(2\pi 50t)$, where $f_{COMPmax}$ is the maximum frequency on the input of the PWM unit comparator and f_s is the switching frequency. Hence, the peak-to-peak amplitude of the reference voltage is given by $f_{COMPmax}/f_s$. For the experimental inverter, $f_{COMPmax}/f_s$ = 84 MHz/25,600 Hz ≈ 3281. Therefore, the maximum amplitude of the reference waveform was 1640. The 13-bit (12 bits plus the sign) ADC controller allowed measurement in the range −4095–4095. Using the visualization provided by the PC application, the hardware gain of the voltage measurement trace was adjusted to a nominal output voltage amplitude of 3000 units—Greater than the reference amplitude of 1640 units. This provided more accurate measurement across the entire ADC range. Finally, the voltage gain scaling coefficient g_v should be 1640/3000. Again, a modulation index of M = 0.6 was used. Figure 8 shows the output current and voltage and inductor current waveforms when using microprocessor control, in addition to an image of the experimental setup.

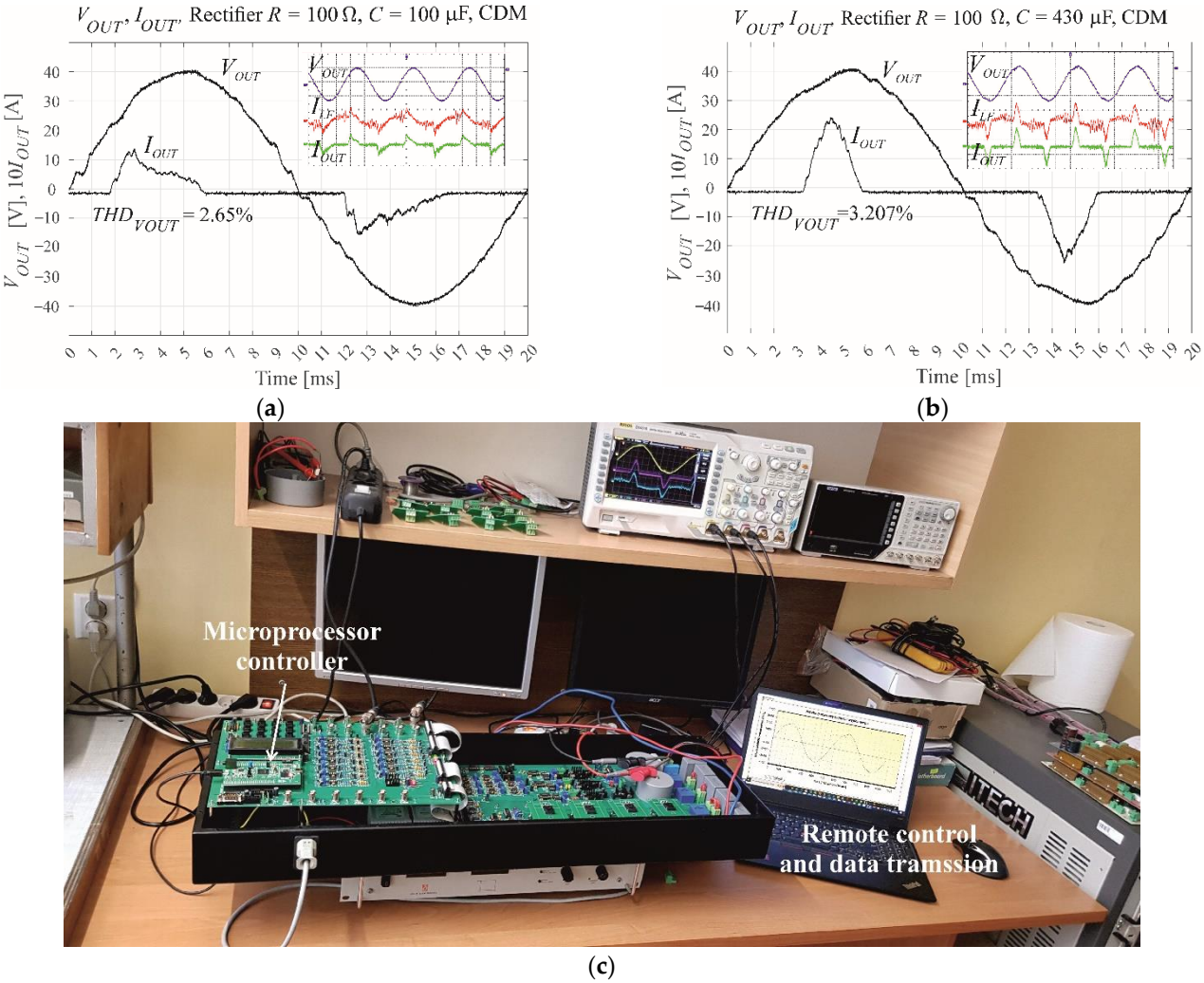


Figure 8. Waveforms of the output voltage, output current, inductor current and measurement of the output voltage THD for CDM and (**a**) a nonlinear rectifier RC load with R =100 Ω, C = 100 µF, and M = 0.6, and (**b**) a nonlinear rectifier RC load with R =100 Ω, C = 430 µF, and M = 0.6, in addition to (**c**) an image of the experimental environment showing the VSI and the microprocessor controller.

6. Theoretical Background of MISO PCB Control

Without direct measurement of the output current (an independent disturbance), SISO control is unable to precisely control the output voltage in the case of large, rapid changes in the output current for a standard [25] nonlinear rectifier RC load. This functionality is provided by MISO PCB control. For IPBC2, the output voltage, output current, and inductor current are input variables of the controller.

Figure 9 models the control of a VSI by MISO. It was shown in [10] that each of the experimental model's measurement traces can be approximately modelled as a single switching period delay. For the described system, this delay had a value of 39 µs. The additional delay is implemented by the PWM modulator, with the data stored in its registers during the kth period controlling the width of the pulses during the k+1th period. Two different MISO PBC controllers were tested: one that did not account for the double switching period delay, and one that made a simplified prediction of the state variables in subsequent periods using the discrete model of a VSI [12]. There was no noticeable difference between the two controllers in terms of the quality of the VSI output voltage at a relatively high switching frequency of f_s = 25,600 Hz, and with C_F = 50 µF. The simplified approach is sufficient for the presentation of the VSI control design methodology. The

load current i_{OUT} is treated as the independent disturbance and is modelled as the current source.

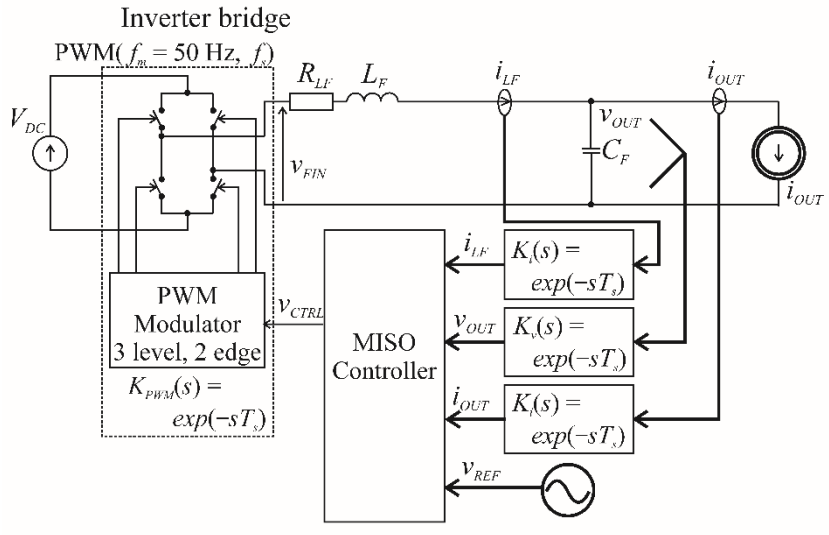


Figure 9. MISO control of a VSI.

The central principle of PBC is that the system is stable if it is passive. The system is passive if the energy supplied to it exceeds the stored energy. Energy is stored within two non-dissipative components—The filter coil and the filter capacitor. The energy stored within a system is described by the Hamiltonian function $H(x)$ (also known as the Lyapunov function [18]). The Hamiltonian function of the error vector **e** is (23):

$$H(\mathbf{e}) = \frac{1}{2}(L_F(i_{LF} - i_{LFref})^2 + C_F(v_{OUT} - v_{OUTref})^2) = \frac{1}{2}\mathbf{e}^T\mathbf{P}^{-1}\mathbf{e}, \quad (23)$$

where

$$\mathbf{e} = \begin{bmatrix} L_F(i_{LF} - i_{LFref}) \\ C_F(v_{OUT} - v_{OUTref}) \end{bmatrix}, \ \mathbf{P}^{-1} = \begin{bmatrix} 1/L_F & 0 \\ 0 & 1/C_F \end{bmatrix}. \quad (24)$$

The equilibrium of a closed-loop system is asymptotically stable [19] if $H(\mathbf{e})$ has a minimum at $\mathbf{x} = \mathbf{x}_{\text{ref}}$ (25):

$$\left.\frac{\partial H(\mathbf{e})}{\partial \mathbf{x}}\right|_{\mathbf{x}=\mathbf{x}_{ref}} = 0, \ \left.\frac{\partial^2 H(\mathbf{e})}{\partial \mathbf{x}^2}\right|_{\mathbf{x}=\mathbf{x}_{ref}} > 0, \text{ where } \mathbf{x} = \begin{bmatrix} L_F i_{LF} & C_F v_{OUT} \end{bmatrix}^T. \quad (25)$$

The system is passive if the time derivative of $H(\mathbf{e})$ is negative (26):

$$\frac{\mathrm{d}H(\mathbf{e})}{\mathrm{d}t} < 0. \quad (26)$$

The control law of IPBC2 for single-phase inverters is based on the control law for interconnection and damping assignment PBC (IDAPBC) [17,19,20]. The equation for a closed loop PBC system is given by (27):

$$\dot{\mathbf{e}} = [\mathbf{J} - (\mathbf{R} + \mathbf{R}_a)]\mathbf{P}^{-1}\mathbf{e}. \quad (27)$$

The equation for an open loop system is given by (28):

$$\dot{\mathbf{x}} = [\mathbf{J} - \mathbf{R}]\mathbf{P}^{-1}\mathbf{x} + \begin{bmatrix} V_{DC} \\ 0 \end{bmatrix} m + \begin{bmatrix} 0 \\ -1 \end{bmatrix} i_{OUT}. \quad (28)$$

The IPBC2 control law is given by the difference between the closed loop and open loop Equation (29):

$$\dot{\mathbf{e}} - \dot{\mathbf{x}} = [\mathbf{J} - \mathbf{R}]\mathbf{P}^{-1}(\mathbf{e} - \mathbf{x}) - \mathbf{R}_a\mathbf{P}^{-1}\mathbf{e} - \begin{bmatrix} V_{DC} \\ 0 \end{bmatrix} m - \begin{bmatrix} 0 \\ -1 \end{bmatrix} i_{OUT}. \quad (29)$$

The interconnection matrix **J**, the damping matrix **R**, and the PBC controller matrix $\mathbf{R}_a$, are defined as (30):

$$\mathbf{J} = \begin{bmatrix} 0 & -1 \\ 1 & 0 \end{bmatrix}, \mathbf{R} = \begin{bmatrix} R_{LFe} & 0 \\ 0 & 0 \end{bmatrix}, \mathbf{R}_a = \begin{bmatrix} R_i & 0 \\ 0 & K_v \end{bmatrix}, \quad (30)$$

where R_i is the current error gain, K_v is the voltage error conductive gain, and R_{LFe} is the serial equivalent resistance of the inverter.

The final form of the IPBC2 control law is then given by (31) and (32):

$$v_{CTRL}(t) = L_F di_{LFref}/dt + (R_{LFe} + R_i)i_{LFref} + v_{OUTref} - R_i i_{LF}, \quad (31)$$

$$i_{LFref} = C_F dv_{OUTref}/dt - K_v(v_{OUT} - v_{OUTref}) + i_{OUT}. \quad (32)$$

Now consider a difference control law for a single-phase VSI with a PBC that is easy to implement using microprocessor control (33) and (34):

$$v_{CTRL}(k) = -R_i i_{LF}(k) + (R_i + R_{LFe})i_{LFref}(k) + L_F \frac{i_{LFref}(k) - i_{LFref}(k-1)}{T_c} + v_{OUTref}(k), \quad (33)$$

$$i_{LFref}(k) = K_v[v_{OUTref}(k) - v_{OUT}(k)] + C_F \frac{v_{OUTref}(k) - v_{OUTref}(k-1)}{T_c} + i_{OUT}(k). \quad (34)$$

This difference control law (Equations (33) and (34)) is used throughout the development of the MISO PCB controller, including MATLAB's Simulink simulations, the MicroLabBox interfaced dSpace simulations, and the microprocessor control of the VSI.

The values $R_{LFe} + R_i$ and K_v should be positive. This allows the closed loop IPBC system [10,11] to have roots $\lambda_{1,2}$ with negative real components (35):

$$\lambda_{1,2} = \frac{\left\{-[(R_{LFe}+R_i)C_F + L_F K_V] \pm \sqrt{[(R_{LFe}+R_i)C_F + L_F K_v]^2 - 4L_F C_F[1 + (R_{LFe}+R_i)K_v]}\right\}}{2L_F C_F} \quad (35)$$

The real components of these roots are always negative for positive values $R_{LFe} + R_i$ and K_v. As such, this condition does not provide any upper bounds for current and voltage gains. The higher the gains, the greater the convergence of the error tracking. However, excessively high IPBC2 gain values can cause oscillations of the VSI output voltage. Such oscillations occur when the control voltage increases more quickly than the width of the PWM pulses can change. This creates a saturation-like effect within the control loop. The higher the switching frequency, the higher the speed of the PWM modulator, and hence the maximum acceptable gains [11]. The fastest change in modulation during a single switching period T_s is V_{DC} (V_{DC}/T_s). At all times, the delay of the modulator is omitted. During a single sampling period, the approximation $d(v_{OUTref})/dt \approx 0$ can be made. Therefore, from Equation (34) it was obtained (36), (37) and (39):

$$i_{LFref}(kT_s) \approx K_v[v_{OUTref}(kT_s) - v_{OUT}(kT_s)] + i_{OUT}(kT_s), \quad (36)$$

$$i_{LFref}(kT_s) \approx (\frac{1}{R_{LOAD}} - K_v)v_{OUT}(kT_s) + v_{OUTref}(kT_s), \quad (37)$$

$$\frac{di_{LFREF}(kT_s)}{dt} \approx (\frac{1}{R_{LOAD}} - K_v)\frac{dv_{OUT}(kT_s)}{dt}. \quad (38)$$

Correspondingly, from Equation (33) it obtained (39) and (40):

$$\frac{dv_{CTRL}(kT_s)}{dt} \approx L_F \frac{d^2 i_{LFref}(kT_s)}{dt^2} + (R_{LFe} + R_i)\frac{di_{LFref}(kT_s)}{dt} - R_i \frac{di_{LF}(kT_s)}{dt}, \quad (39)$$

$$\begin{aligned} \frac{dv_{CTRL}(kT_s)}{dt} &\approx L_F\left(\frac{1}{R_{LOAD}} - K_v\right)\frac{d^2 v_{OUT}(kT_s)}{dt^2} + \\ (R_{LFe} + R_i)\left(\frac{1}{R_{LOAD}} - K_v\right)&\frac{dv_{OUT}(kT_s)}{dt} - R_i \frac{di_{LF}(kT_s)}{dt} \end{aligned} \quad (40)$$

During a single switching cycle, for $R_{LOAD} >> 1/(2\pi f_s C_F)$, the following approximations (41), (42) can be made:

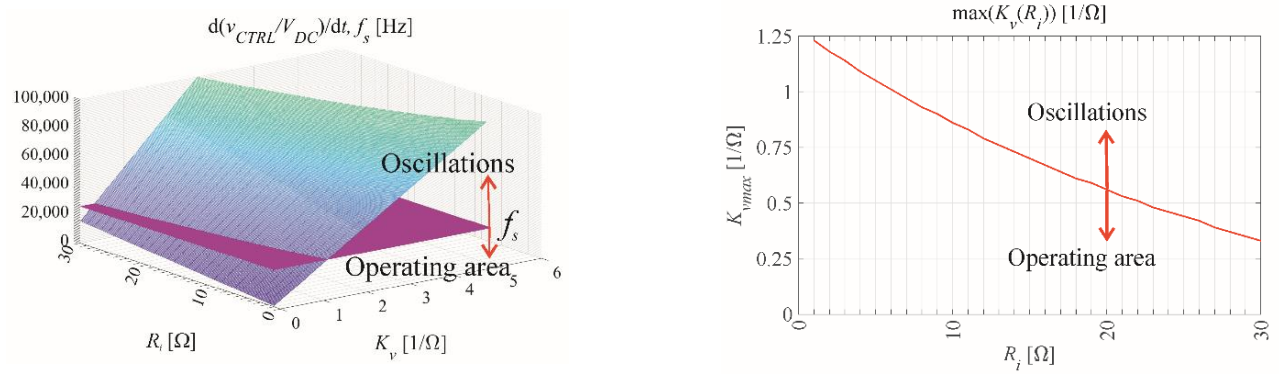
$$\begin{aligned} \left.\frac{di_{LF}(kT_s)}{dt}\right|_{\max,\min} &\approx \pm\frac{V_{DC}}{L_F}, \\ \left.\frac{dv_{OUT}(kT_s)}{dt}\right|_{\max} \approx \frac{i_{LF}}{C_F},\ \left.\frac{d^2 v_{OUT}(kT_s)}{dt^2}\right|_{\max} &\approx \left.\frac{d}{dt}\left(\frac{i_{LF}}{C_F}\right)\right|_{\max} \approx \pm\frac{V_{DC}}{L_F C_F} \end{aligned} \quad (41)$$

$$\left.\frac{dv_{CTRL}(kT_s)}{dt}\right|_{\max} \approx K_v[L_F + (R_i + R_{LFe})T_s]\frac{V_{DC}}{L_F C_F} + R_i\frac{V_{DC}}{L_F} \quad (42)$$

From Equation (43) it was obtained the upper boundary conditions on the gains R_i and K_v (43):

$$K_v[1 + (R_i + R_{LFe})\frac{T_s}{L_F}]\frac{1}{C_F} + R_i\frac{1}{L_F} < f_s. \quad (43)$$

Equation (43) demonstrates the influence of switching frequency $f_s = 1/T_s$ on the maximum values of the gains R_i and K_v. Figure 10 demonstrates the mutual relationship between the two gain values. In accordance with Figure 10b, throughout this paper safe gain values of R_i = 15 Ω and K_v = 0.3 1/Ω are used.



(**a**) (**b**)

Figure 10. The relationship between maximum voltage gain K_v and current gain R_i for the assigned VSI parameters f_s = 25,600 Hz, L_F = 2 mH, C_F = 51 µF, and R_{LFe} = 1 Ω in (**a**) 3-D and (**b**) 2-D.

7. MATLAB's Simulink Simulation of MISO PBC Control

Figure 11 presents the Simulink simulation model. The THD is very low, with the MISO-PBC controller (33), and (34) perfectly damping disturbances in the output voltage. The modulation coefficient is less than unity to allow the control voltage to increase. The results of the simulation are ideal; the quantity of THD present is almost negligible. This is a result of using the currents as controller inputs. The scaling coefficient for each of the output voltage, output current, and inductor current is simply $1/V_{DC}$. The modulation index is M = 0.6.

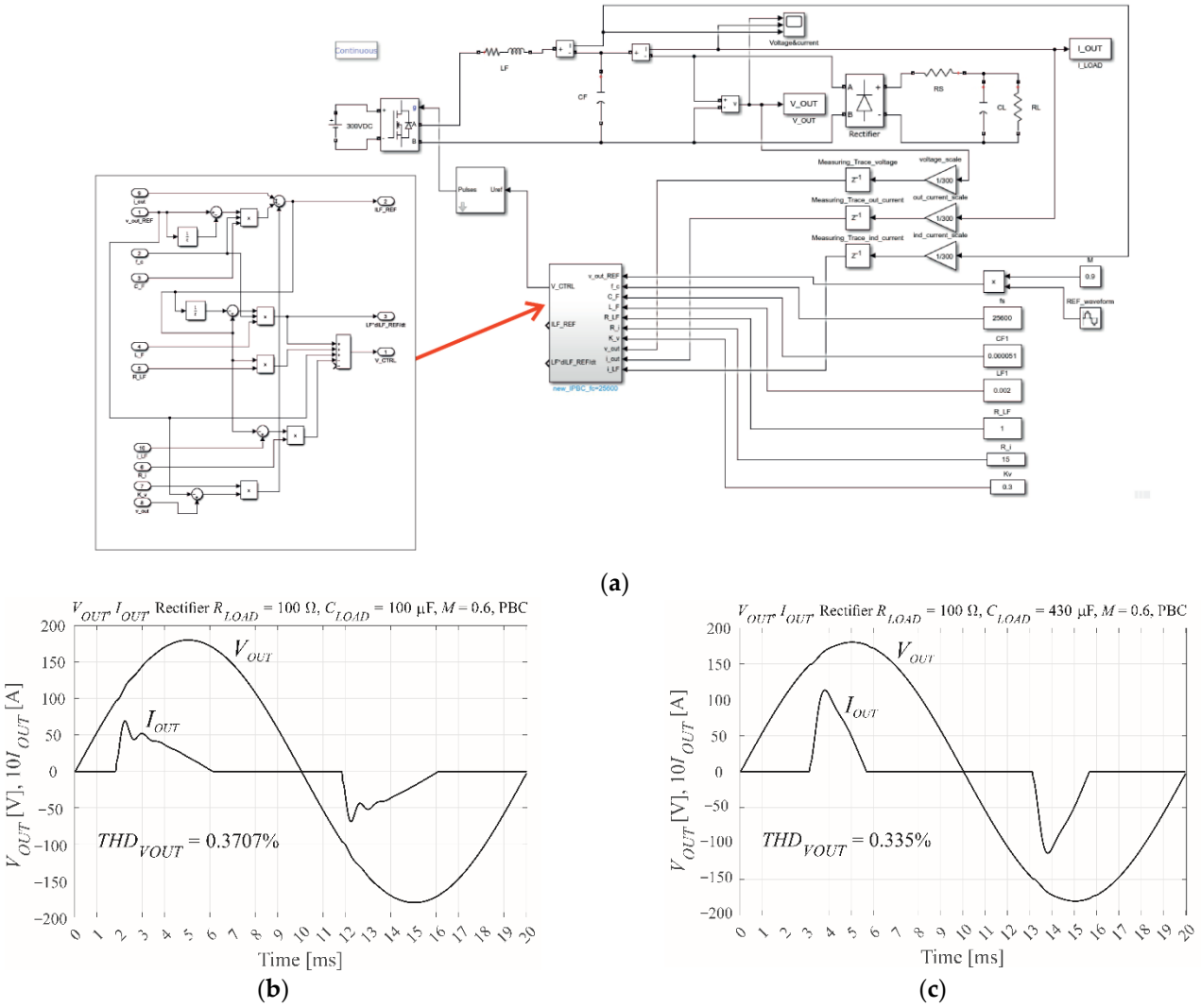
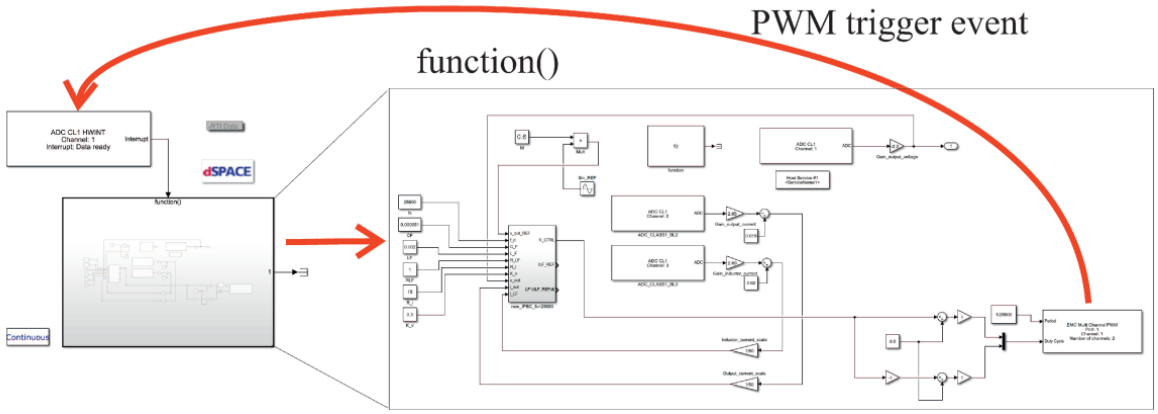


Figure 11. Overview of PBC control, showing (**a**) the MATLAB's Simulink simulation model of the IPBC2 controller and the simulation model of the inverter with the nonlinear rectifier RC load, (**b**) the simulated output voltage and current with R = 100 Ω, C = 100 μF, and M = 0.6, and (**c**) the simulated output voltage and current with R = 100 Ω, C = 430 μF, and M = 0.6.

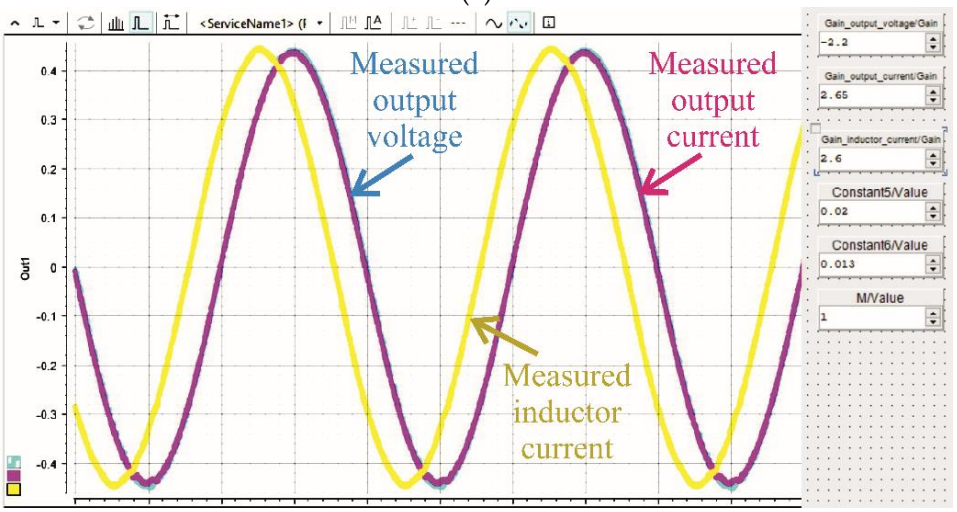
8. Interfacing MATLAB's Simulink and dSpace Simulation of the MISO PBC Controller with the Experimental Model

Figure 12a shows the combined Simulink and dSpace models. Shown in Figure 12c, three independent ADCs are used for the output voltage, the output current, and the inductor current. Each ADC is triggered by PWM events. The gain values of R_i = 15 Ω and K_v = 0.3 1/Ω are the same as the Simulink model (Figure 11). The modulation index is M = 0.6. However, new scaling of the three measured signals is required. For open loop control with a load of nominal resistance 50 Ω and minimum output capacitance of C_F = 1 μF, which ensures that currents I_{OUT} and I_{LF} are approximately equal at the 50 Hz harmonic, the voltage and current traces should have sufficient amplification that they are equal to the reference voltage. The amplification includes the gain of the experimental model measuring traces. The reference voltage is given by 0.5sin(2π50t), as shown in Figure 12b. Note that although the figure shows an amplitude of 0.45, the maximum amplitude is 0.5. Finally, the current values are divided by the value of R_{NOM}: 50 Ω in the presented case. Experimental model measurements [10] show that the delay of the measuring traces and the PWM modulator at f_s = 25,600 Hz can be omitted when designing the controller. ControlDesk software (Figure 12b) was used to tune the scaling coefficients

of the measuring traces. The final gain values were −2 for output voltage, 2.65/50 for output current, and 2.60/50 for inductor current.



(**a**)



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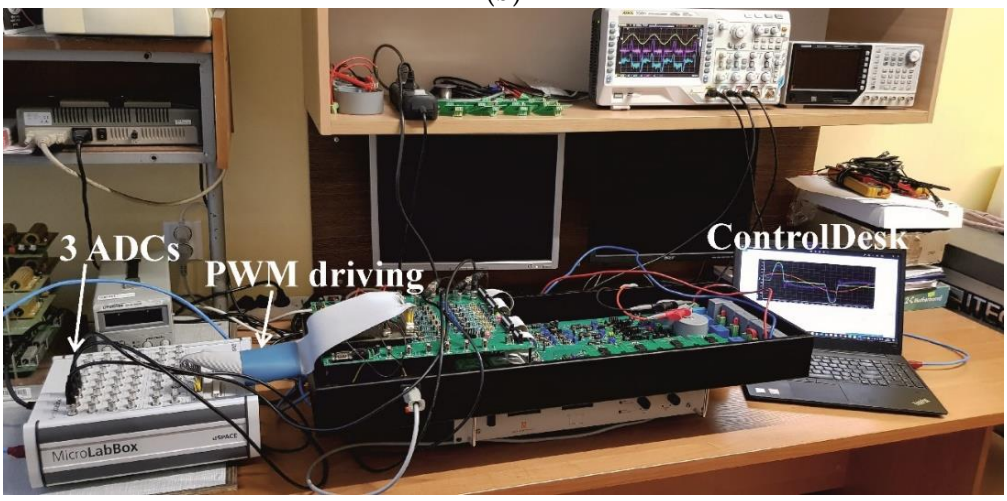


(**c**)

Figure 12. The MicroLabBox real-time interface between the dSpace simulation and the experimental VSI, showing (**a**) the combined Simulink and dSpace simulation model for MicroLabBox (RTI1202) operation, (**b**) scaling of the measuring traces using ControlDesk, and (**c**) an image of the experimental setup showing the three ADCs, the PWM driver, and ControlDesk running on a laptop.

Figure 13 shows the distortions in the output voltage of the VSI when controlled by MicroLabBox. Unlike for SISO-CDM control (Figure 7), the current waveforms are shaped accurately. This is due to MISO control of the output and inductor currents.

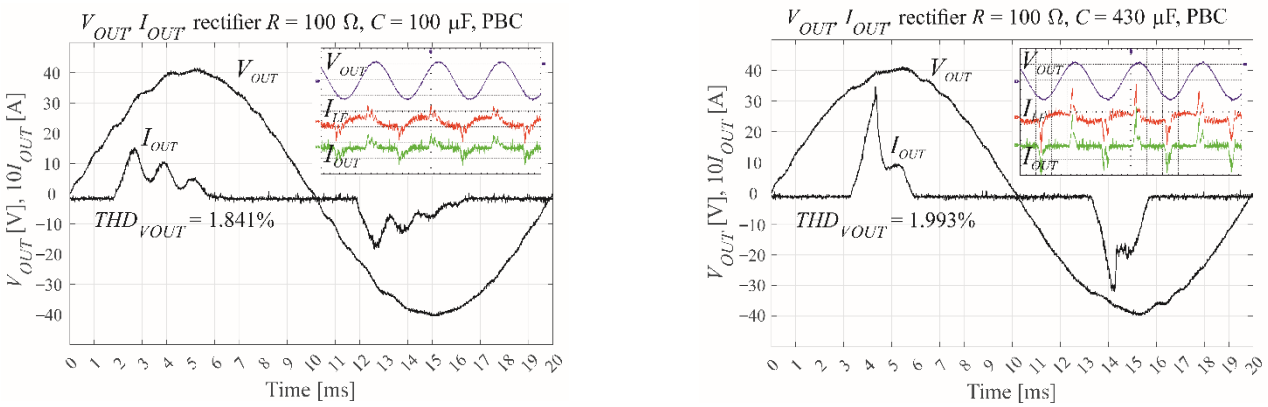
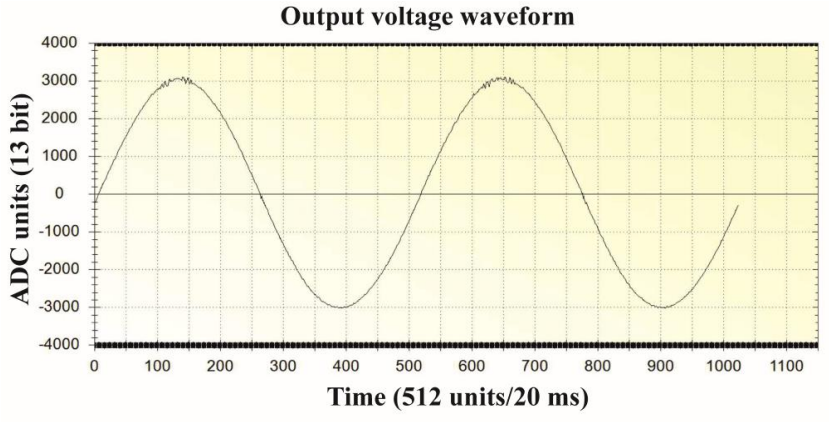


Figure 13. The PBC-controlled VSI output voltage and current as measured in-system using MicroLabBox for a nonlinear rectifier RC load with (**a**) R = 100 Ω, C = 100 μF, and M = 0.6, and (**b**) R = 100 Ω, C = 430 μF, and M = 0.6.

9. Implementation of the MISO PBC Controller in the VSI Microprocessor

The STM32F407VG microprocessor was chosen due to its fast clock speed of 168 MHz, in addition to its 84 MHz maximum PWM comparator input frequency. The microprocessor is capable of floating point hardware operation and has three independent ADCs that can be simultaneously used to measure the output voltage, output current, and inductor current. The amplitude of the reference voltage is $0.5f_{COMPmax}/f_s = 0.5 \times 84$ MHz$/25600 \approx 1640$. The ADCs obtain measurements in the range −4095–4095. During scaling the system should function under open loop control, with a small output capacitance of C_F = 1 μF and a nominal resistive load of 50 Ω. When using the dedicated PC application to transmit data from the VSI the output voltage is hardware adjusted to 3000 units. Hence, the voltage scaling coefficient is 1640/3000 = 0.547. The current values vary, and as such, they are tuned to a lower value of 2000, from within the −4095–4095 range. With a resistive load of 50 Ω, the current scaling coefficient is (1640/2000)/50 = 0.0164. The modulation index is M = 0.6. Figure 14 shows the scaling of voltage measurements, in addition to the measured output voltage and current of the VSI. Control of the current substantially affects the shape of the current waveforms, and reduces distortion of the output voltage.



(**a**)

Figure 14. *Cont.*

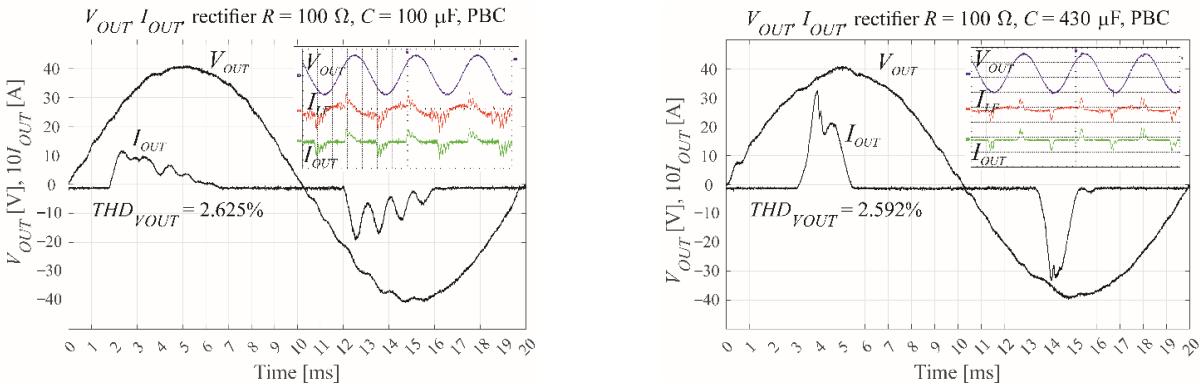


Figure 14. Overview of the VSI as controlled by IPBC2 via the STM32F407VG microprocessor, showing (**a**) scaling of the output voltage measurement, (**b**) measured output voltage and current with R = 100 Ω, C = 100 μF, and M = 0.6, and (**c**) measured output voltage and current with R = 100 Ω, C = 430 μF, and M = 0.6.

10. Results

The hardware model presented above used the MATLAB's Simulink 2021b and dSpace Release 2021b along with ControlDesk v.7.5 for MicroLabBox real-time interface 1202, or Keil μVision 5 for STM32F407VG microprocessor control, and a dedicated PC application for USB data exchange that was developed in-house using Microsoft Visual Studio C++ 2019. This hardware model, together with a MicroLabBox RTI1202 real-time interface, were used in the design process of two different VSI controllers: one SISO control system and one MISO control system. The results of using these controllers were evaluated by measuring the THD of the output voltage of the simulated or experimental VSI, when subject to a standard (EN62040) nonlinear rectifier RC load with R = 100 Ω, C = 100 μF, or C = 430 μF, and PF = 0.7. The modulation index was reduced to M = 0.6 to prevent the modulator from being saturated by rapid increases in the load current. The control procedures of both the real-time interface and the microprocessor were called by PWM block interrupts. For both control systems, the fully simulated system provided better results (lower THD) than the systems that utilized the experimental VSI. One reason for this could be an inaccurate discrete model of the inverter plant within the control design. The CDM control was based upon this model, with linearized functions of the output voltage, output current, inductor current, and duty ratio. Another possible reason could be the approximation of the measuring traces using only the delay values.

Despite lower performance than the simulated system, the results of the experimental system were satisfactory, and exceeded the requirements of EN 62040-3. Measuring both the output and inductor current allows the MISO controller to accurately shape the output current waveform. This study demonstrates the importance of the precise scaling of voltages and currents. The scaling values differed across each stage of the design procedure and required different procedures at each stage to tune them accurately. This included the use of dedicated software when working with the experimental model controlled by a microprocessor. The relatively low modulation index is important to avoid saturation and enable a faster increase of the inductor current in case of a rapid increase in the load current increase. To this end, the product of the modulation index and the filter inductor inductance should be limited. Table 1 summarizes the findings for each system. The results of the MicroLabBox and microprocessor control procedures are very similar, with a difference in THD of less than 1%.

Table 1. Summary of the degree of THD for the Simulink model, real-time MicroLabBox control, and STM32F407VG microprocessor control.

Control Type; Nonlinear Rectifier Load RC Parameters Modulation Index M	Simulation	MicroLabBox and Experimental Model	Microprocessor and Experimental Model
Open loop, R = 100 Ω, C = 100 μF	4.51%	4.35%	-
Open loop, R = 100 Ω, C = 430 μF	6.75%	6.96%	-
CDM, R = 100 Ω, C = 100 μF, M = 0.6	0.98%	2.01%	2.65%
CDM, R = 100 Ω, C = 430 μF, M = 0.6	1.57%	3.44%	3.21%
PBC, R = 100 Ω, C = 100 μF, M = 0.6	0.37%	1.84%	2.63%
PBC, R = 100 Ω, C = 430 μF, M = 0.6	0.34%	1.99%	2.59%

11. Conclusions

This paper detailed the four stages of VSI control system design (Figure 1): development of the theoretical background, modelling, and simulation of the system using MATLAB's Simulink, control of the experimental VSI using dSpace via a MicroLabBox real-time interface, and implementation of the control system on a STM32F407VG microprocessor for direct control of the experimental VSI. Two control systems were used to demonstrate this process: SISO CDM and MISO PBC. The motivation behind the described design process is the assumption that the differential control laws are consistent throughout each stage of development. Control of the MicroLabBox and the microprocessor is based on PWM block interrupts, with the control procedures called once during each switching period. This approach is feasible as the differential control law obtained from the theory is the same for both simulation and hardware implementation. The primary differences between each stage of the design process are the values of the voltage and current scaling coefficients. These values should be precisely tuned for each stage as the coefficients of the control law would be changed by wrongly scaling. ControlDesk was used to tune the MicroLabBox scaling. Scaling of the microprocessor-based system required dedicated software that enabled data transfer from the hardware. This data transfer to PCB was achieved via USB, with the dedicated software working as a digital oscilloscope scaled in the microprocessor ADC units (Figure 14a). The value of the modulation index is very important during each stage of the design process; an excessively large value can cause saturation of the modulator in the case of rapid increases in load current. Lower values of the product of the modulation index and the filter inductor inductance provide faster changes in the inductor current.

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