

Article

Universal Filter Based on Compact CMOS Structure of VDDDA

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Abstract: This paper proposes the simulated and experimental results of a universal filter using the voltage differencing differential difference amplifier (VDDDA). Unlike the previous complementary metal oxide semiconductor (CMOS) structures of VDDDA that is present in the literature, the present one is compact and simple, owing to the employment of the multiple-input metal oxide semiconductor (MOS) transistor technique. The presented filter employs two VDDDAs, one resistor and two grounded capacitors, and it offers low-pass: LP, band-pass: BP, band-reject: BR, high-pass: HP and all-pass: AP responses with a unity passband voltage gain. The proposed universal voltage mode filter has high input impedances and low output impedance. The natural frequency and bandwidth are orthogonally controlled by using separated transconductance without affecting the passband voltage gain. For a BP filter, the root mean square (RMS) of the equivalent output noise is 46 μ V, and the third intermodulation distortion (IMD3) is -49.5 dB for an input signal with a peak-to-peak of 600 mV, which results in a dynamic range (DR) of 73.2 dB. The filter was designed and simulated in the Cadence environment using a 0.18- μ m CMOS process from Taiwan semiconductor manufacturing company (TSMC). In addition, the experimental results were obtained by using the available commercial components LM13700 and AD830. The simulation results are in agreement with the experimental one that confirmed the advantages of the filter.

Keywords: VDDDA; biquad filter; operational transconductance amplifier; multiple-input technique

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1. Introduction

Analog filters are very useful in an analog signal processing system [1–4]. They are used to pass the desired frequency band from the input section to the output section. Therefore, the frequency filter is an essential element of any signal processing system that will be indispensable. Especially, in sensor applications, a filter is very important to detect the wanted signal, for example, in the phase sensitive detection [5], electrocardiographic (ECG) system [6], biosensors [7], etc. The biquad active filter has been a very popular research topic for last three decades. The main reason for the popularity of the biquad filter design is that it can be modified to obtain five filtering functions, which are the low-pass: LP, band-pass: BP, band-reject: BR, high-pass: HP and all-pass: AP functions. Compared to the first-order configuration, this filter can give only three LP, HP and BP functions, as

well as the higher order filter, which mostly gives only one filtering response. The versatile biquad filter that gives multiple filtering functions within the same configuration is well-known as the universal or multifunction filter. In the open literature, this type of active filter has been proposed continuously [8–12].

The voltage differencing differential difference amplifier (VDDDA) [13] is a very useful and versatile building block for the voltage-mode active biquad filtering design. With the operational transconductance amplifier (OTA) at the input stage of the VDDDA, the filtering characteristics (for example, the passband voltage gain, bandwidth, quality factor, the cut-off frequency or phase response of the VDDDA-based filter) can be controlled via the transconductance (g_m). Moreover, with the unity gain voltage differential difference amplifier (DDA) at the output stage of the VDDDA, it is very useful for the voltage-mode filter design without the use of additional or external voltage summing or a voltage differencing circuit, especially in the two-integrator loop filter design. Additionally, some VDDDA-based voltage-mode filters can cascade without the requirement of additional buffer devices. In this point of view, several active biquad filters using the VDDDA have been reported [13–24]. The voltage mode biquad filters using the voltage differential difference device (called the differential difference current conveyor transconductance amplifier (DDCCTA)) have been also proposed in references [25–27]. These biquad filters can be classified into two categories based on their design techniques, which are based on two integrator loops [13–15,17,19–22,25,27] and based on a passive resistor-inductor-capacitor (RLC) circuit [16,18,23,24,26]. The RLC based biquad filters proposed in [16,18,23,24] have very simple circuitry with a single VDDDA. However, these biquad filter realized from the RLC circuit have the following disadvantages: they consist of a floating capacitor [16,18,24,26], the natural frequency (f_0) and quality factor (Q) are not orthogonally controlled by changing the transconductance of the VDDDA [16,18,23,24], high impedance nodes at the input stage and a low impedance node at the output stage are not obtained [16,18,23,24,26] and additional circuits such as the unity gain inverting voltage amplifier or double-gain voltage amplifier are required for obtaining many filtering functions [16,18,24,26]. Two-integrator loop-based biquad filters with high input impedance were obtained in references [13–15,17,19–22,27]. Additionally, a low output impedance property for all output nodes was obtained in references [19,21,22]. In [13,14,20–22], the f_0 and Q were orthogonally controlled by the separated transconductance. However, the biquad filter proposed in references [13,14,20–22] requires three VDDDAs. Additionally, the passband voltage gain of three VDDDA-based filters in references [13,14,22] is not constant during tuning the f_0 and Q for some filtering responses. The two-integrator loop filter in references [15,17] cannot provide five filter responses. Additionally, two VDDDA-based biquad filters in references [15,17,19] and the biquad filter using DDCCTA in references [25,27] cannot achieve the orthogonal control of the f_0 and Q by separated transconductance. As reviewed above, it was found that the two VDDDA-based universal biquad filters with the feature of orthogonal control of the f_0 and Q by the separated transconductance were been available in the open literature.

The multiple-input MOS transistor (MI-MOST) is an effective technique that may reduce the count of the transistors needed to build some active blocks and simplify their CMOS topologies. This technique was, for the first time, presented and experimentally confirmed by Khateb et al. [28–30]. Recently, several active functional blocks, such as the differential difference amplifier (DDA) [28], differential difference current conveyors (DDCC) [30–32], fully differential difference amplifier (FDDA) [33] and multiple-input OTA [6,34–36], were designed based on this technique. It was shown that applications based on the MI-MOST technique can be realized with less numbers of active blocks, smaller chip areas and reduced power consumptions compared to conventional designs [6,28–36].

In the past, a multiple-input OTA was used to reduce the number of components, silicon area, and power dissipation in the OTA-C filter design where a third-order elliptic low-pass filter was built by five double-input OTAs instead of seven single-input OTAs

[37]. Another example is the use of a two-input-stage OTA instead of a conventional OTA to build a leapfrog realization of a seventh-order elliptic filter in order to facilitate the signal addition required in the feedback paths of the leapfrog realization [38]. In both the aforementioned examples, additional active transistors were used to realize the multiple-input terminals. Another way to obtain multiple-input MOST is the utilizing of a multiple-input floating-gate transistor (MIFG) [39]. However, this technique is based on charge conservation; hence, it cannot be used in CMOS technologies with gate leakage [40].

Figure 1 shows an example of multiple-input gate-driven MOST with two inputs. Each input (V_1 and V_2) is connected to the gate (G) of the MOST (M) by a parallel connection of an input capacitor (C_1 and C_2) and high resistance (R_{MOS1} and R_{MOS2}) created by two MOST (M_R) operating as a diode in the cut-off region. Due to using the transistor M_R , the chip area is saved. Note that the multiple-input technique could be applied to the gate terminal [6,36], bulk terminal [28], bulk-gate terminal [34] or bulk-quasi-floating-gate terminal of the MOST [29]. However, unlike the aforementioned multiple-input techniques, the multiple-input gate-driven MOST offers the advantage of that regardless of the CMOS technology used; both transistor types (N-MOS and PMOS) could be created with a multiple-input signal.

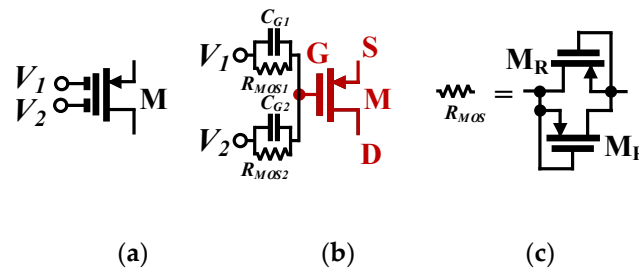


Figure 1. The multiple-input metal oxide semiconductor transistor (MOST): (a) symbol, (b) realization and (c) realization of R_{MOS} [28].

This paper presents a universal filter based on the compact CMOS structure of the multiple-input gate-driven VDDDA. The paper is organized as follows: Section 2 presents the CMOS structure of the VDDDA and the proposed universal filter. Sections 3 and 4 present the simulation and experimental results, respectively. The comparison of the proposed biquad filter with other filters using VDDDA is discussed and explained in Section 5, and finally, Section 6 concludes the paper.

2. Proposed Universal Filter

2.1. Basic Concept of the VDDDA

The VDDDA is a connection of OTA and a unity gain DDA. The basic version of the VDDDA with circuit symbols, as in Figure 2a, is an analog functional block with five terminals. The high-impedance input voltage terminals are v_+ , v_- , z , n and p . The low-impedance output voltage terminal is w . Note that the z terminal is also the output current terminal. An ideal corresponding equivalent circuit of the VDDDA is illustrated in Figure 2b. The circuit performance is described by the matrix Equation (1):

$$I_+ = I_- = I_n = I_p = 0; I_z = g_m (V_+ - V_-); V_w = V_z - V_n + V_p, \quad (1)$$

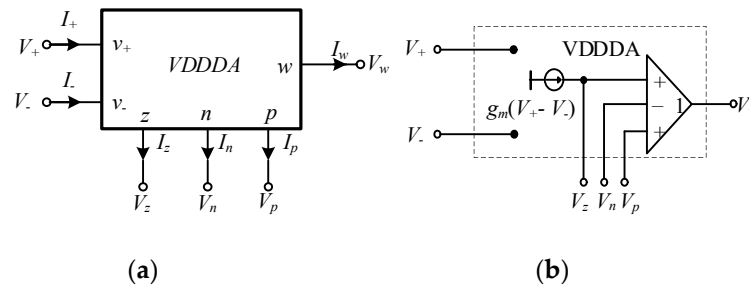


Figure 2. Voltage differencing differential difference amplifier (VDDDA): (a) electrical symbol and (b) equivalent circuit [13].

2.2. The CMOS Structure of the VDDDA

The VDDDA consists of a transconductance stage (g_m) followed by a differential difference amplifier (DDA), as shown in Figure 3. The transconductance stage is formed by a differential stage (M_1, M_2, M_5, M_{10} and M_{11}) and a doubled output stage (M_6, M_{12}, M_7 and M_{13}). Thanks to the negative feedback between the output (drain of M_6) and the input terminals of M_1 , the linearity of the transconductance is increased. The capacitor C_{1a} and the MOS resistor R_{MOS1} are used to obtain a class AB output stage. The capacitor C_{c1} creates the compensation network of the transconductor. The resistor R_{set} is used to set the transconductance value in such a way that $g_{m,set} \approx 1/R_{set}$ for $R_{set} \gg 1/g_m$, where g_m is the internal transconductance of this stage [41]. Note that the tuning mechanism is very simple; the difference of the input voltages ($V_+ - V_-$) will appear across R_{set} due to the negative unity feedback. The resistor current I_{Rset} will be controlled by the value of R_{set} . The output current I_z is a copy of I_{Rset} . The DDA is created in similar manner as the transconductance stage. The bias current I_b and the transistor M_{17} create the bias current and voltage needed for the circuit. It is worth noting that the minimum voltage supply of the proposed VDDDA structure is given by one gate-source and one drain-source voltage, i.e., $V_{DDmin} = V_{GSM5} + V_{DSM10}$. Hence, the structure is suitable for low-voltage supply applications.

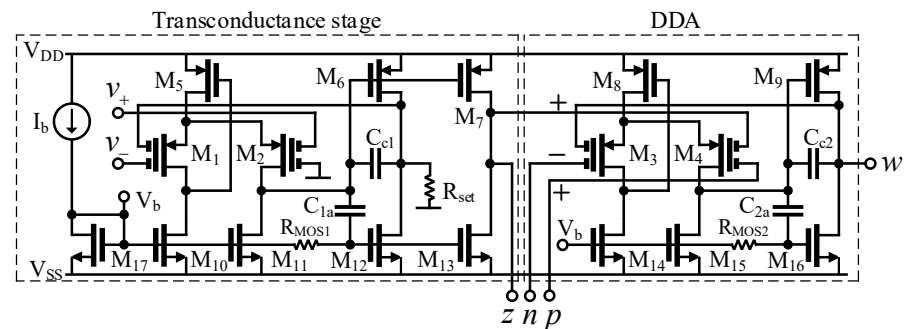


Figure 3. The CMOS structure of the VDDDA.

2.3. The Universal Biquad Filter based on VDDDAs

Most of the published papers on universal biquad filters have not shown the method to design the topology. Therefore, new researchers or designers do not understand how to get the completed circuits. In this paper, a simple method to design the biquad filter is also presented to achieve the important goal of this design, which is to use only two VDDDAs to get the orthogonal tune of the quality factor and the natural frequency by using separated transconductance. The proposed biquad universal filter is designed from the parallel RLC circuit connecting with the voltage differencing circuit, as shown in Figure 4. There are three input voltages applied to the circuit: v_{i2} is applied through the inductor, v_{i3} is applied to the resistor and v_{i4} is applied at the inverting input of the voltage differencing circuit. For a conventional design, other input voltages can be applied

through the capacitor. However, using a grounded capacitor is required for this design to ensure the reduction in fabrication space and the compensation of parasitic effects.

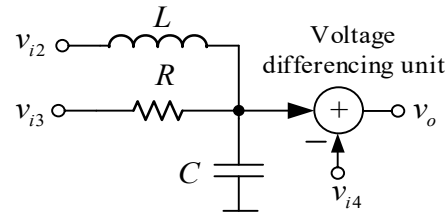


Figure 4. Method to design the proposed biquad filter.

Considering the circuit shown in Figure 4, the following output voltage, v_o , is obtained:

$$v_o = \frac{\frac{1}{LC} v_{i2} + s \frac{1}{CR} v_{i3} - \left(s^2 + s \frac{1}{CR} + \frac{1}{LC} \right) v_{i4}}{s^2 + s \frac{1}{CR} + \frac{1}{LC}}, \quad (2)$$

Based on Equation (2), several filter responses can be obtained from the same topology by appropriately applying the input signal to the input voltage nodes v_{i2} , v_{i3} and v_{i4} of the filter, and this detail will be described later. The natural frequency, bandwidth (BW) and quality factor for Equation (2) are obtained by

$$\omega_0 = \sqrt{\frac{1}{LC}}, \quad (3)$$

$$BW = \frac{1}{RC}, \quad (4)$$

and

$$Q = R \sqrt{\frac{C}{L}}, \quad (5)$$

Equations (3) and (4) indicate that the ω_0 and BW (or the Q) are orthogonally controlled. It is vital to note that the Q is controlled through the resistor R without affecting the natural frequency. To get the required natural frequency and bandwidth for the practical design, the natural frequency must be first designed by setting the inductance (L) and capacitance (C) values. Then, the required bandwidth or quality factor can be achieved by independently setting the resistance value without disturbing the natural frequency.

Considering the method to design the filter in Figure 4, there are four sub-circuits, which are the inductor, resistor, grounded capacitor and the voltage summing circuit. These passive inductor and resistors can be replaced by active simulators using the VDDDA. The active inductor used in this design is modified from the floating lossless inductance simulator using two VDDDA's proposed in reference [42]. Only one VDDDA is required for the active inductor in our work. Additionally, the active resistor and voltage differencing circuit can be realized from one VDDDA. Based on this principle, the proposed universal biquad filter is illustrated in Figure 5. The proposed filter comprises two VDDDA's, two grounded capacitors and one resistor, where the VDDDA₁, C_1 and R_1 operate as the active inductors. The active resistor and voltage differencing circuit is constructed from VDDDA₂, and the grounded capacitor C_2 acts as C in Figure 4. There are four input voltage nodes: v_{i1} , v_{i2} , v_{i3} and v_{i4} , which is slightly different from the principle in Figure 4. The input voltage nodes v_{i2} , v_{i3} and v_{i4} are the same as the principle in Figure 4. The additional v_{i1} node is added to get the all-pass response, which will be given more

detail later. It is found that all input voltage nodes of the proposed universal biquad filter are high impedance, while the output voltage (v_o) node is low impedance. The proposed universal biquad filter can cascade without the requirement of any voltage buffers at the input and output stages. Moreover, it consists of all the grounded capacitors, which ensures a reduction in the fabrication space and compensation of the parasitic effects.

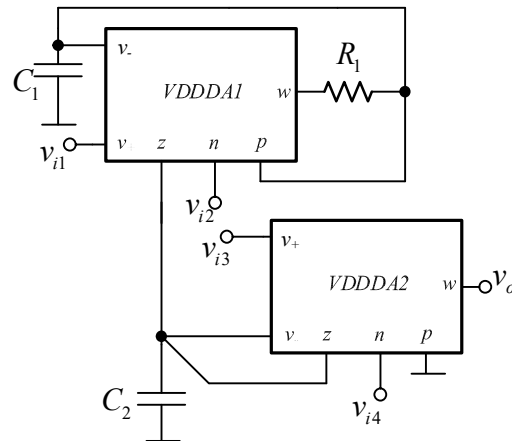


Figure 5. The universal filter based on the VDDDA.

Considering the circuit shown in Figure 5, the following output voltage, v_o , is obtained.

$$v_o = \frac{s \frac{g_{m1}}{C_2} v_{i1} + \frac{g_{m1}}{C_1 C_2 R_1} v_{i2} + s \frac{g_{m2}}{C_2} v_{i3} - \left(s^2 + s \frac{g_{m2}}{C_2} + \frac{g_{m1}}{C_1 C_2 R_1} \right) v_{i4}}{s^2 + s \frac{g_{m2}}{C_2} + \frac{g_{m1}}{C_1 C_2 R_1}}, \quad (6)$$

Based on Equation (6), several filter responses can be given from the same filtering topology in Figure 5 by applying the appropriate input voltage signal to the input nodes of the filter as follows:

- Noninverting low-pass filter with unity voltage gain is given at the output voltage node v_o of the proposed filter by applying the input signal into the input voltage node v_{i2} while the other input voltage nodes are grounded.
- Noninverting band-pass filter with unity voltage gain is given at the output voltage node v_o of the proposed filter by applying the input signal into the input voltage node v_{i3} while the other input voltage nodes are grounded.
- Inverted high-pass filter with unity voltage gain is given at the output voltage node v_o of the proposed filter by applying the input signal into the input voltage nodes v_{i2} , v_{i3} and v_{i4} while the input voltage node v_{i1} is grounded.
- Inverted band-stop filter with unity voltage gain is given at the output voltage node v_o of the proposed filter by applying the input signal into the input voltage nodes v_{i3} and v_{i4} while other nodes are grounded.
- Inverted all-pass filter with unity voltage gain is given at the output voltage node v_o of the proposed filter by setting $g_{m1} = g_{m2}$ and applying the input signal into the input voltage nodes v_{i1} , v_{i3} and v_{i4} while the input voltage node v_{i2} is grounded. Although it requires the matching conditions of g_{m1} and g_{m2} , this is the active matching condition that is easier to control than the passive matching one.
- Inverted all-pass filter without the matching condition is given at the output voltage node v_o of the proposed filter by connecting the z terminal to the p terminal of the VDDDA₂, then applying the input signal into the input voltage nodes v_{i3} and v_{i4} while the other input voltage nodes are grounded.

From the above statement, it is found that the selection of filter responses does not require additional circuits—for example, inverting or double-gain amplifiers. The natural frequency, bandwidth and quality factor for Equation (6) are obtained by

$$\omega_0 = \sqrt{\frac{g_{m1}}{C_1 C_2 R_1}}, \quad (7)$$

$$BW = \frac{g_{m2}}{C_2}, \quad (8)$$

and

$$Q = \frac{1}{g_{m2}} \sqrt{\frac{g_{m1} C_2}{C_1 R_1}}, \quad (9)$$

Equations (7) and (8) indicate that the ω_0 and BW (or the Q in Equation (9)) are orthogonally controlled. In a practical design to get the required natural frequency and bandwidth, the natural frequency must be first designed by setting the g_{m1} , R_1 , C_1 and C_2 . Then, the required bandwidth or quality factor can be achieved by independently setting the g_{m2} without disturbing the natural frequency.

2.4. Effects of Nonideal VDDDA Characteristics

The nonideal properties of the VDDDA will affect the performances of the proposed universal biquad filter. Therefore, these nonideal cases will be considered and studied in this section. There are two nonideal characteristics, which are the voltage tracking errors and parasitic impedances, at the VDDDA terminals. Firstly, the voltage tracking error in the voltage differencing stage of the VDDDA will be considered. The VDDDA property with the voltage tracking errors is given by

$$\begin{pmatrix} I_+ \\ I_- \\ I_z \\ I_n \\ I_p \\ V_w \end{pmatrix} = \begin{pmatrix} 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ g_m & g_m & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & \beta_z & -\beta_n & \beta_p & 0 \end{pmatrix} \begin{pmatrix} V_{v+} \\ V_{v-} \\ V_z \\ V_n \\ V_p \\ I_w \end{pmatrix}, \quad (10)$$

Here, $\beta_z = 1 - \varepsilon_z$ and ε_z ($|\varepsilon_z| \ll 1$) denotes the voltage tracking error from the z to w terminal, $\beta_n = 1 - \varepsilon_n$ and ε_n ($|\varepsilon_n| \ll 1$) denotes the voltage tracking error from the n to w terminal and $\beta_p = 1 - \varepsilon_p$ and ε_p ($|\varepsilon_p| \ll 1$) denotes the voltage tracking error from the p to w terminal. Considering these errors, the output voltage of the proposed universal filter can be expressed as follows:

$$v_o = \frac{\left[\begin{aligned} &(1 - \varepsilon_{z2}) \left(s \frac{g_{m1}}{C_2} + \frac{\varepsilon_{p1} g_{m1}}{C_1 C_2 R_1} \right) v_{i1} + (1 - \varepsilon_{n1}) (1 - \varepsilon_{z2}) \frac{g_{m1}}{C_1 C_2 R_1} v_{in2} + \\ &(1 - \varepsilon_{z2}) \left(s \frac{g_{m2}}{C_2} + \frac{\varepsilon_{p1} g_{m2}}{C_1 C_2 R_1} \right) v_{i3} - (1 - \varepsilon_{n2}) D^*(s) v_{i4} \end{aligned} \right]}{D^*(s)}, \quad (11)$$

where

$$D^*(s) = s^2 + s \left[\frac{\varepsilon_{p1}}{C_1 R_1} + \frac{1}{C_2} g_{m2} \right] + \frac{\varepsilon_{p1} g_{m2} + (1 - \varepsilon_{z1}) g_{m1}}{C_1 C_2 R_1}, \quad (12)$$

Therefore, the ω_0 , BW and Q with nonideal gains are, respectively, given as

$$\omega_0^* = \sqrt{\frac{\varepsilon_{p1} g_{m2} + (1 - \varepsilon_{z1}) g_{m1}}{C_1 C_2 R_1}}, \quad (13)$$

$$BW^* = \frac{\varepsilon_{p1}}{C_1 R_1} + \frac{1}{C_2} g_{m2}, \quad (14)$$

and

$$Q^* = \frac{C_1 C_2 R_1}{\varepsilon_{p1} C_2 + C_1 R_1 g_{m2}} \sqrt{\frac{\varepsilon_{p1} g_{m2} + (1 - \varepsilon_{z1}) g_{m1}}{C_1 C_2 R_1}}. \quad (15)$$

It is noticeable that the voltage gain, natural frequency, bandwidth and the quality factor are affected by the voltage tracking errors. Additionally, it is found in Equation (14) that the transconductance, g_{m2} will slightly affect the natural frequency due to the ε_{p1} . However, these voltage tracking errors are much less than one; their effects can be neglected at low-frequency operations.

The effects of parasitic impedances at the input and output terminals of the VDDDA are considered next. These parasitic impedances are the parallel C_+ and R_+ at the v_+ terminal, the parallel C_- and R_- at the v_- terminal, the parallel C_z and R_z at the z terminal, the parallel C_n and R_n at the n terminal, the parallel C_p and R_p at the p terminal and the R_w (series at the w terminal) at the low output impedance w terminal, as shown in Figure 6.

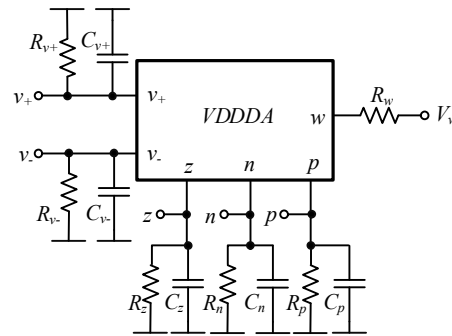


Figure 6. The parasitic effects on the VDDDA.

Considering these parasitic impedances, the output voltage under the parasitic effect is given by

$$v_o = \frac{\left(s \frac{g_{m1}}{C_2^* R_1^*} + \frac{G_1^* g_{m1}}{C_1^* C_2^* R_1^*} \right) v_{i1} + g_{m1} v_{in2} + \left(s \frac{g_{m2}}{C_2^* R_1^*} + \frac{G_1^* g_{m2}}{C_1^* C_2^* R_1^*} \right) v_{i3} - D^{**}(s) v_{n2}}{D^{**}(s)}, \quad (16)$$

where

$$D^{**}(s) = s^2 + s \left(\frac{G_1^*}{C_1^*} + \frac{G_2^*}{C_2^*} + \frac{g_{m2}}{C_2^*} \right) + \frac{G_1^* g_{m2} R_1 + G_1^* G_2^* R_1^* + g_{m1}}{C_1^* C_2^* R_1^*}, \quad (17)$$

and $C_1^* = C_1 + C_{-1} + C_{p1}$, $C_2^* = C_2 + C_{z1} + C_{-2} + C_{z2}$, $G_1^* = G_{-1} + G_{p1}$, $G_2^* = G_{z1} + G_{-2} + G_{z2}$, $R_1^* = R_1 + R_{w1}$, $G_{-1} = 1/R_{-1}$, $G_{p1} = 1/R_{p1}$, $G_{z1} = 1/R_{z1}$, $G_{-2} = 1/R_{-2}$ and $G_{z2} = 1/R_{z2}$. The ω_0 , BW and Q with parasitic effects are respectively given as

$$\omega_0^{**} = \sqrt{\frac{G_1^* g_{m2} R_1 + G_1^* G_2^* R_1^* + g_{m1}}{C_1^* C_2^* R_1^*}}, \quad (18)$$

$$BW^{**} = \frac{G_1^*}{C_1^*} + \frac{G_2^*}{C_2^*} + \frac{g_{m2}}{C_2^*}, \quad (19)$$

and

$$Q^{**} = \frac{C_1^* C_2^* R_1^*}{C_2^* G_1^* R_1 + C_1^* G_2^* R_1^* + C_1^* g_{m2} R_1^*} \sqrt{\frac{G_1^* g_{m2} R_1 + G_1^* G_2^* R_1^* + g_{m1}}{C_1^* C_2^* R_1^*}}. \quad (20)$$

It is noticeable that the voltage gain, natural frequency, bandwidth, the quality factor and operational frequency range of the proposed filter are affected by the parasitic impedances in the VDDDA. Additionally, it is found from Equation (20) that the transconductance, g_{m2} , will slightly affect the natural frequency due to the parasitic impedance, G_1^* . However, the effect of the parasitic capacitances can be minimized by setting the value of $C_1 \gg C_{-1}$ and C_{p1} and $C_2 \gg C_{z1}$, C_{-2} and C_{z2} , while the parasitic resistance R_{w1} can be minimized by setting the value of $R_1 \gg R_{w1}$. As mentioned above, using grounded capacitors is advantageous for the compensation of parasitic effects.

3. Simulation Results

The CMOS circuit of the VDDDA and the filter application were designed and simulated in the Cadence environment using a 0.18- μm CMOS process from TSMC. The voltage supply is $V_{DD} = -V_{SS} = 0.9\text{ V}$, the bias current is $I_b = 50\text{ }\mu\text{A}$ and the total power consumption is 0.99 mW. The transistors aspect ratio of the VDDDA shown in Figure 3 are $M_1 - M_4 = 90\text{ }\mu\text{m}/3\text{ }\mu\text{m}$; $M_5 - M_9 = 2 \times 90\text{ }\mu\text{m}/3\text{ }\mu\text{m}$; M_{10} , M_{11} , M_{14} , M_{15} and $M_{17} = 30\text{ }\mu\text{m}/3\text{ }\mu\text{m}$; M_{12} , M_{13} and $M_{16} = 2 \times 30\text{ }\mu\text{m}/3\text{ }\mu\text{m}$ and $M_R = 4\text{ }\mu\text{m}/5\text{ }\mu\text{m}$. The values of the passive components are C_{c1} , C_{c2} , C_{1a} and $C_{2a} = 2.6\text{ pF}$ and $C_G = 0.5\text{ pF}$.

Figure 7 shows the frequency responses of V_w/V_n and V_w/V_z (V_w/V_p), where the gain at low frequency is -7 dB and 5 dB and the -3 dB bandwidth is 6.3 MHz and 6.1 MHz, respectively. Figure 8 shows the relation of the simulated and ideal transconductance versus the R_{set} . Note that the curves match for the lower value of R_{set} .

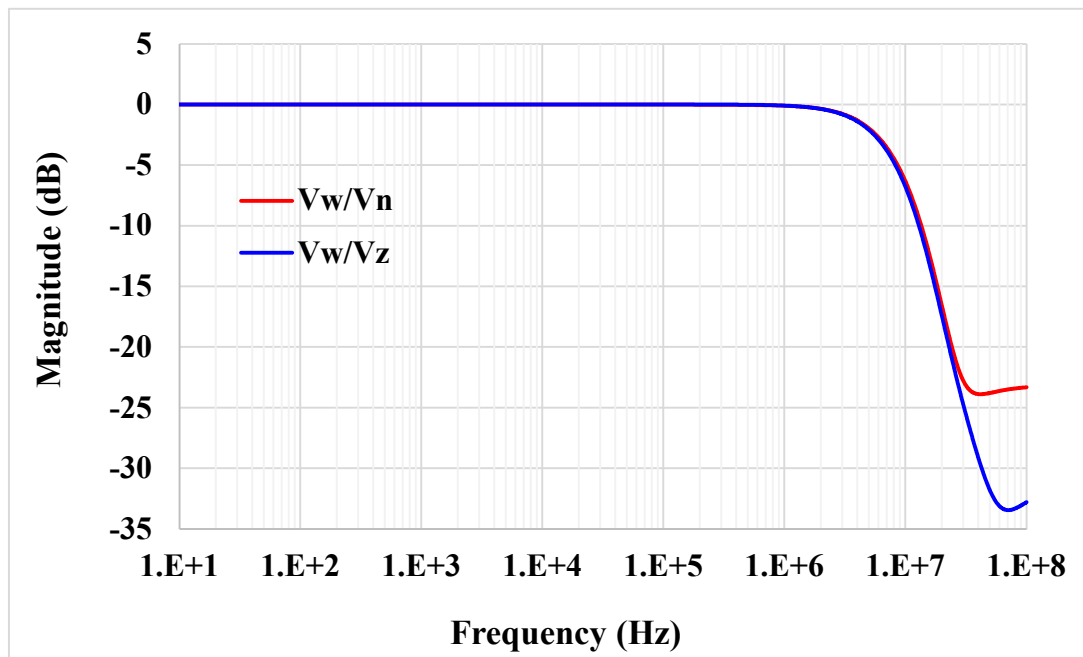


Figure 7. The frequency responses of $|V_w/V_n|$ and $|V_w/V_z|$.

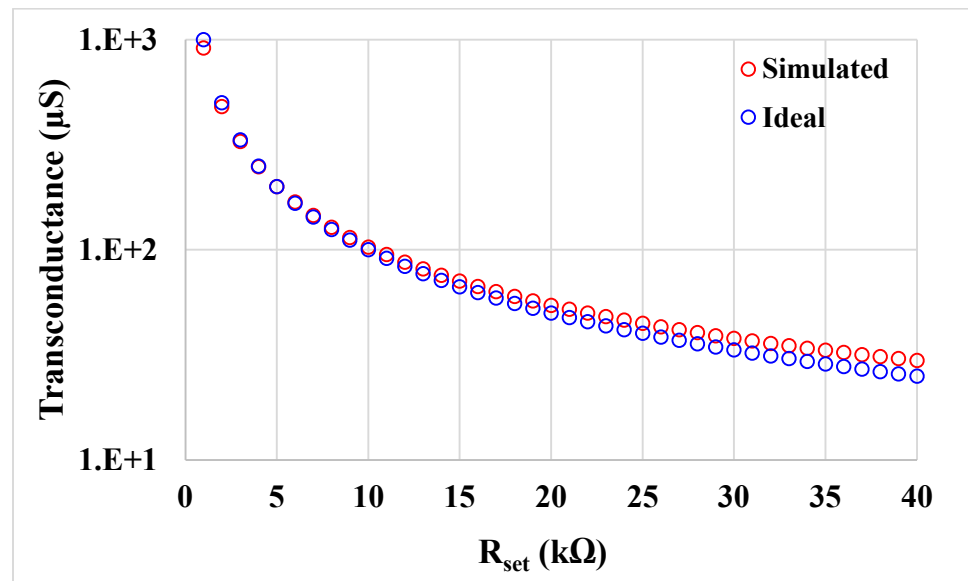


Figure 8. The transconductance value of the simulated and ideal transconductor versus R_{set} .

For the proposed filter in Figure 5, the values of the passive components were selected as $C_1 = C_2 = 335$ pF, $R_1 = 10$ kΩ, and the value of the resistor of the transconductors was $R_{set1} = R_{set2} = 9$ kΩ. Figure 9 shows the frequency characteristics of the LP, HP, BP, BR and AP filters, while the phase response of the AP filter is shown in Figure 10. However, for the BR response, the attenuation was obtained around -26 dB due to nonideal characteristics of the VDDDA, as explained in Section 2.4. The simulated natural frequency was $f_0 = 50$ kHz. Figure 11 shows the tunability of the BP filter for $R_{set2} = 6$ kΩ, 9 kΩ and 12 kΩ, while $R_{set1} = 9$ kΩ. Figure 12 shows the tunability of the BP filter for $R_{set1} = 6$ kΩ, 9 kΩ, 12 kΩ, 15 kΩ and 18 kΩ, while $R_{set2} = 9$ kΩ. The frequency f_0 was 60.9 kHz, 50.1 kHz, 44.1 kHz, 39.3 kHz and 36.3 kHz, respectively. The Monte Carlo analysis (including transistors and passive device mismatches) of the BP filter with 200 runs is shown in Figure 13. The curves are overlapped and confirm the stability of the circuit. Figure 14 shows the histogram of the bandwidth (BW) of the BP filter with 200 runs of the Monte Carlo analysis. While the mean value is 57.8 kHz, the standard deviation is only 47.3 Hz.

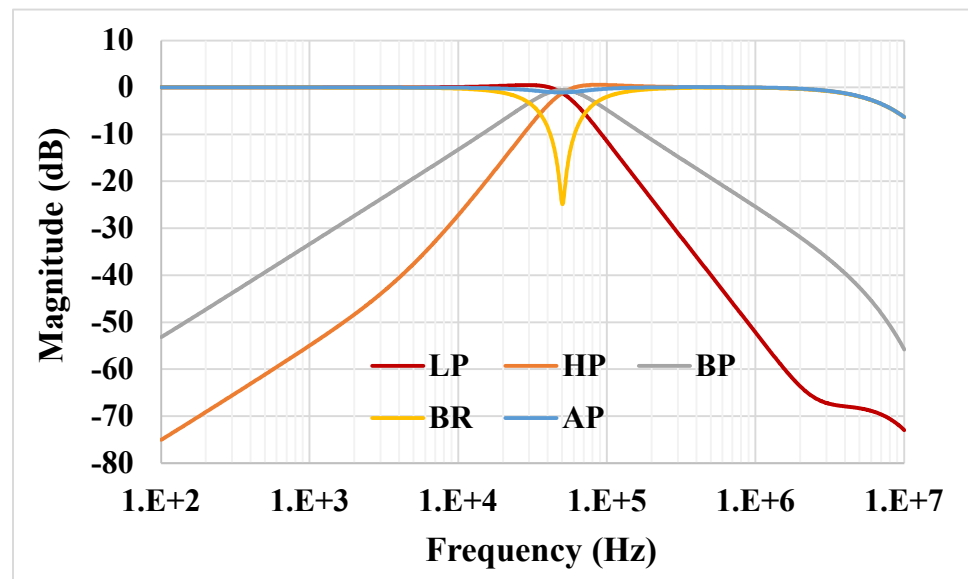


Figure 9. Frequency characteristics of the proposed universal filter.

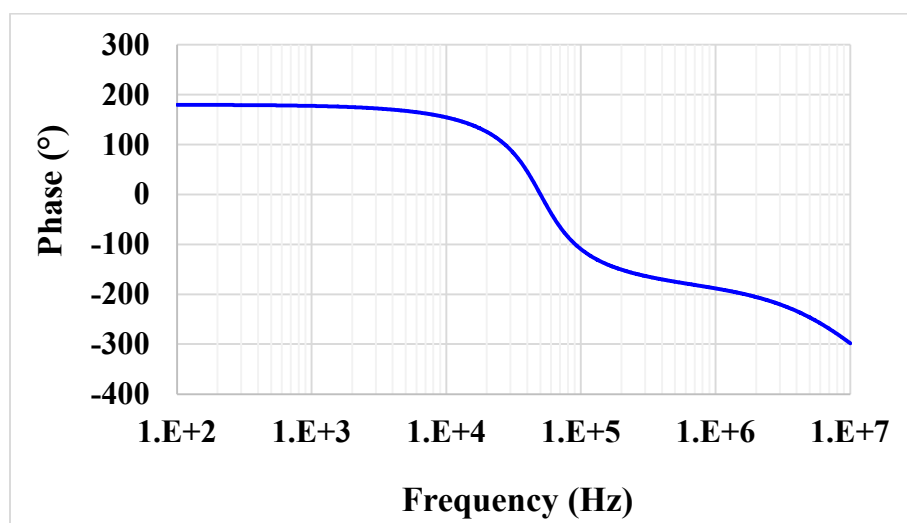


Figure 10. Phase characteristics of the all-pass (AP) filter.

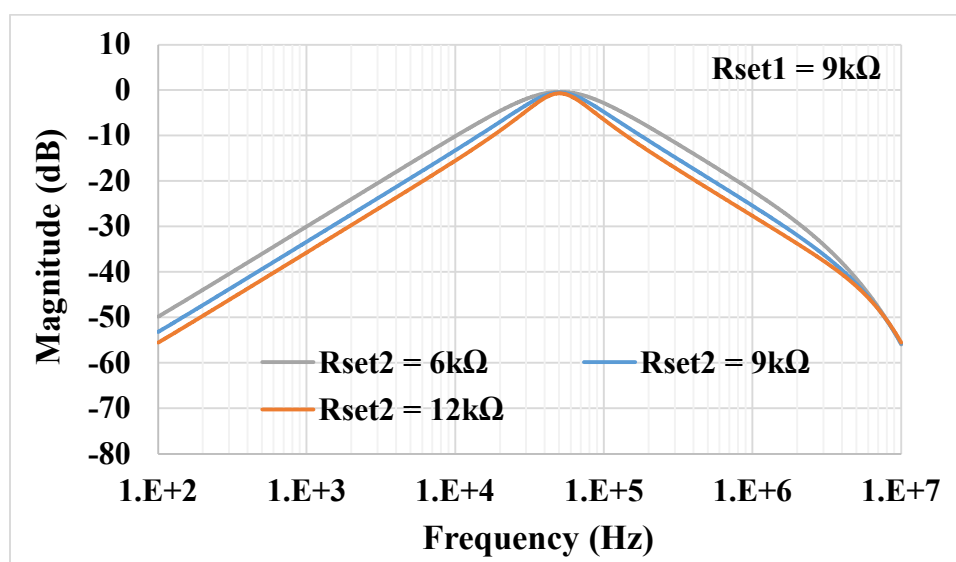


Figure 11. Tunability of the band-pass (BP) filter for different R_{set2} and the constant R_{set1} .

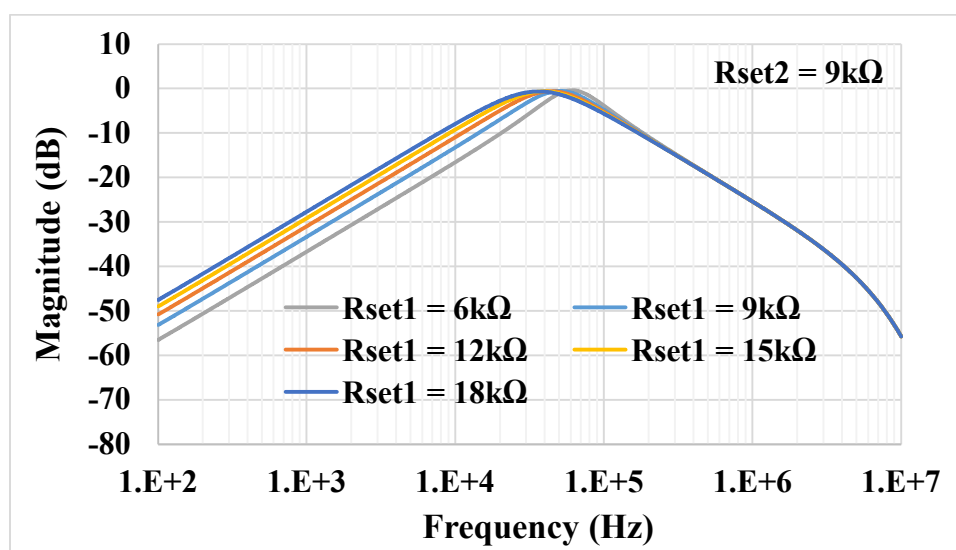


Figure 12. Tunability of the BP filter for different R_{set1} and the constant R_{set2} .

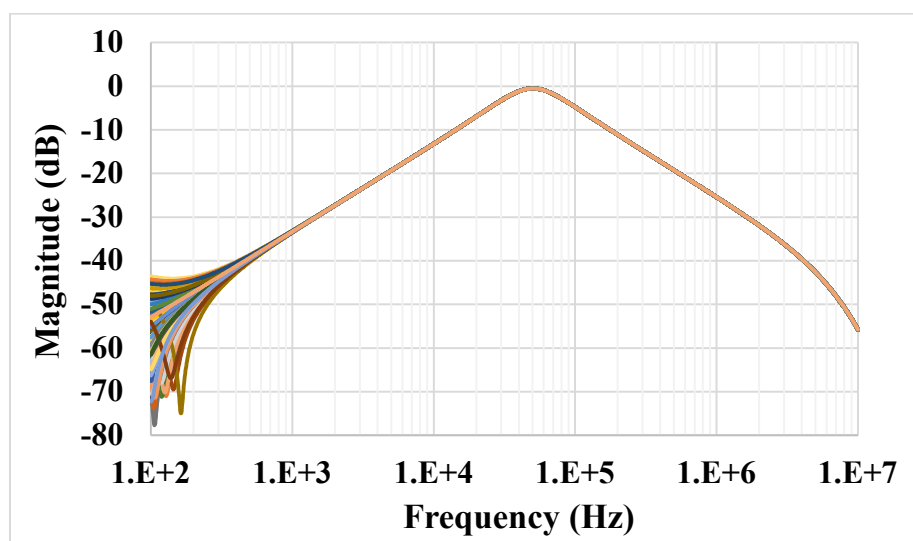


Figure 13. Monte Carlo analysis of the frequency characteristics of the BP filter with 200 runs.

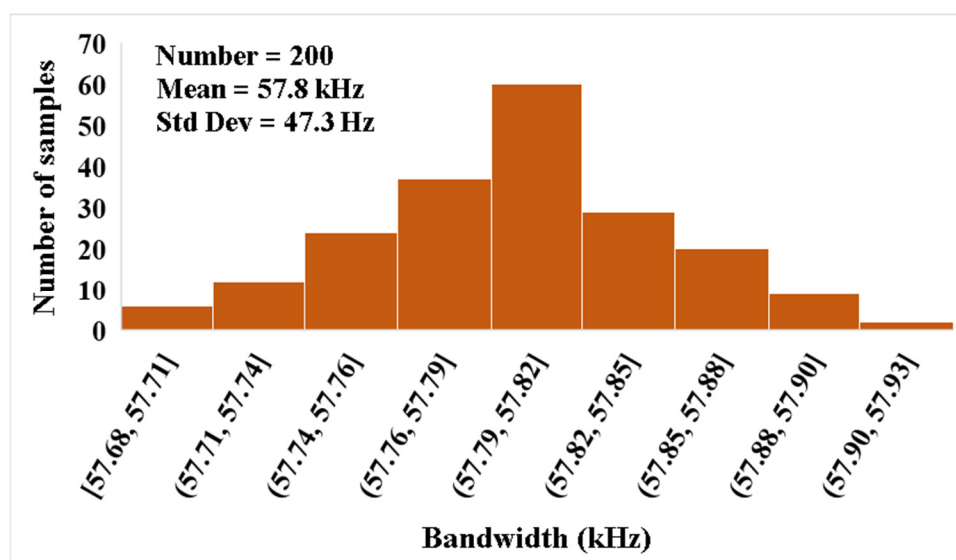


Figure 14. The histogram of the bandwidth of the BP filter with 200 runs of the Monte Carlo analysis.

The results of the process, voltage and temperature (PVT) corner analysis of the BP filter are shown in Figure 15. The process corners for the MOST were fast-fast, fast-slow, slow-fast and slow-slow, for capacitor and resistor corners were fast and slow, the voltage supply corners $V_{DD} = -V_{SS}$ were 890 mV and 910 mV and, finally, the temperature corners were -20 and 80 °C. While the nominal value of the BW is 57.8 kHz, the minimum BW is 57.17 kHz, and the maximum BW is 58.55 kHz under all corner variations. To test the third intermodulation distortion of the BP filter, two closely spaced tones were applied to the input of the BP filter. The first tone was a sine wave signal with 100-mVpp @ 49 kHz and the second tone with 100-mVpp @ 51 kHz. The spectrum of the output signal is shown in Figure 16. The third intermodulation distortion (IMD3) was -65.148 dB. Figure 17 shows the IMD3 of the BP filter versus the peak-to-peak value of the input signal. It is clear that the filter offers IMD3 of -34 dB for the 600-mVpp input signal. As shown in Figure 18, the RMS value of the output noise integrated in the pass band of the filter (29.11 kHz–86.9 kHz) is $46 \mu\text{V}_{\text{rms}}$, and the RMS value of the input signal for 2% IMD3 is 0.2121 V; hence, the dynamic range of the BP filter is 73.27 dB.

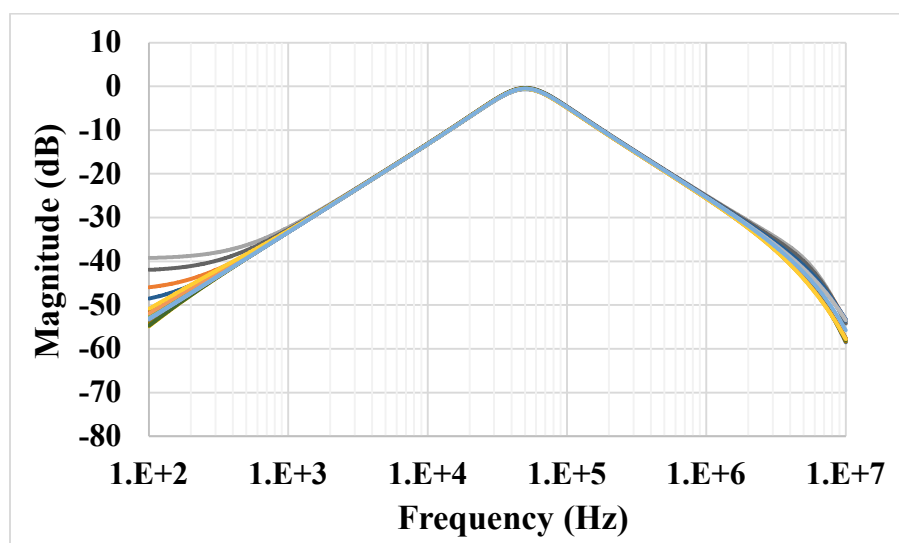


Figure 15. The process, voltage and temperature (PVT) corner analysis of the BP filter.

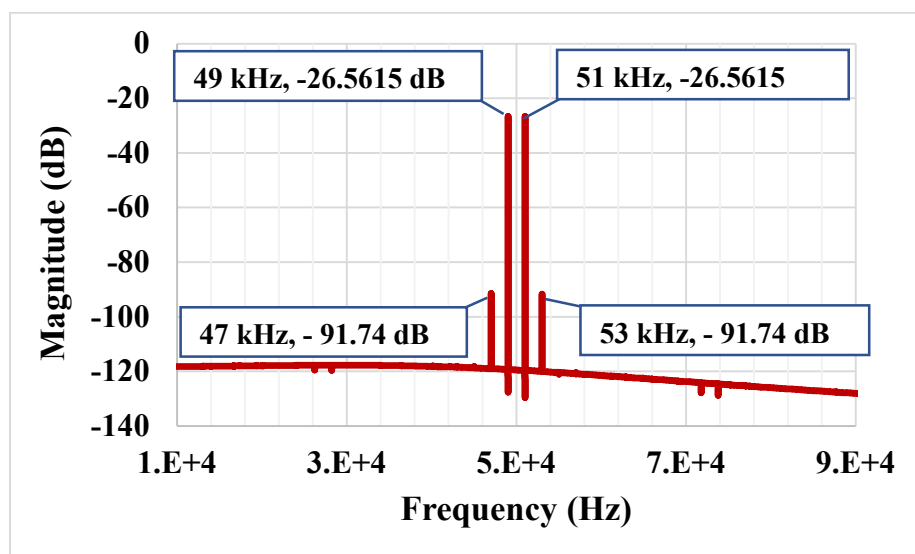


Figure 16. The spectrum of the output signal of the BP filter.

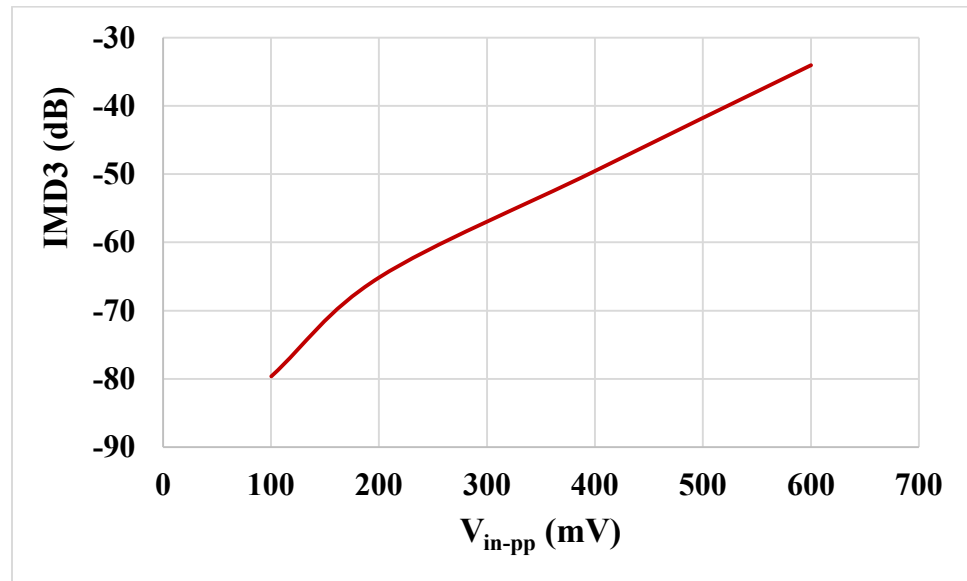


Figure 17. The third intermodulation distortion (IMD3) of the BP filter versus the peak-to-peak value of the input signal.

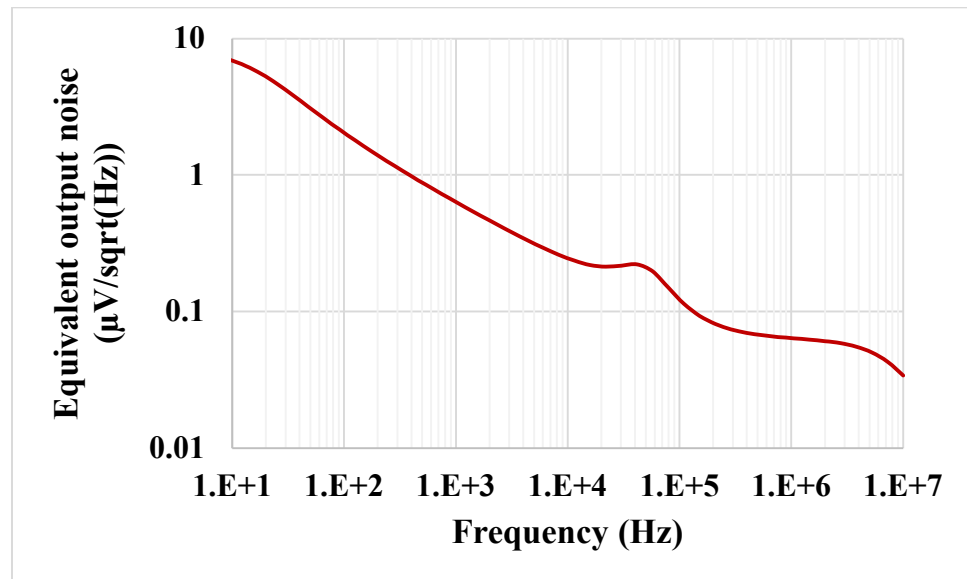


Figure 18. The equivalent output noise of the BP filter.

4. Experimental Results

Theoretically described behaviors of the proposed universal filter were also verified experimentally by implementing the VDDDA from LM13700 (transconductance stage) and AD830 (differential difference amplifier stage), as shown in Figure 19. The transconductance (g_m) of LM13700 is electronically controlled with $g_m = I_B/2V_T$, where I_B is the bias current, and V_T is the thermal voltage. The bias currents and supply voltages were chosen as $I_{B1} = 115 \mu A$, $I_{B2} = 90 \mu A$ and $V_{CC} = -V_{EE} = 5 V$, respectively. The values of the grounded capacitors and resistor were chosen as $C_1 = C_2 = 5.5 nF$ and $R_1 = 1 k\Omega$, respectively. The calculated natural frequency and quality factor were $f_0 = 50 kHz$ and $Q = 1$, respectively. Figure 20 shows the frequency characteristics of the LP, HP, BP and BR filters. The experimental natural frequency was $f_0 = 49 kHz$. However, for the experimental BR response, the attenuation was obtained around $-35 dB$ due to nonideal characteristics of the VDDDA, as explained in Section 2.4. Figure 21 shows the gain response of the band-pass filter at different I_{B2} values ($42 \mu A$, $90 \mu A$ and $165 \mu A$). It is observed that the natural

frequency is electronically tuned by the bias current I_{B2} without disturbing the bandwidth or quality factor. The electronic adjustability of the natural frequency via the bias current I_{B1} is shown in Figure 22. The experimental result shows that the natural frequency $f_0 = 26$ kHz, 38 kHz and 49 kHz was obtained. The measured input and output waveforms of the BP filtering function are, respectively, shown in Figure 23, where a sine wave signal with a peak-to-peak value of 40 mVpp @ 5 kHz, 50 kHz and 500 kHz was applied to the input of the filter.

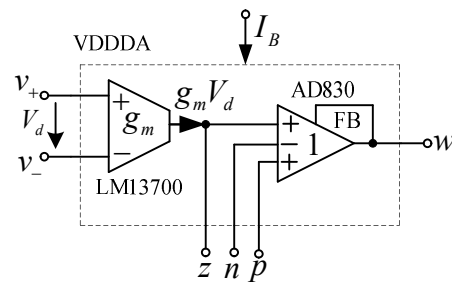


Figure 19. VDDDA based on the commercial components.

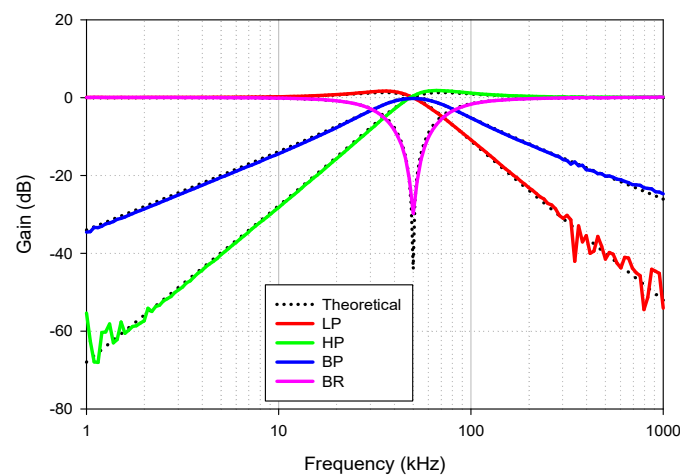


Figure 20. Experimental frequency characteristics of the proposed universal filter.

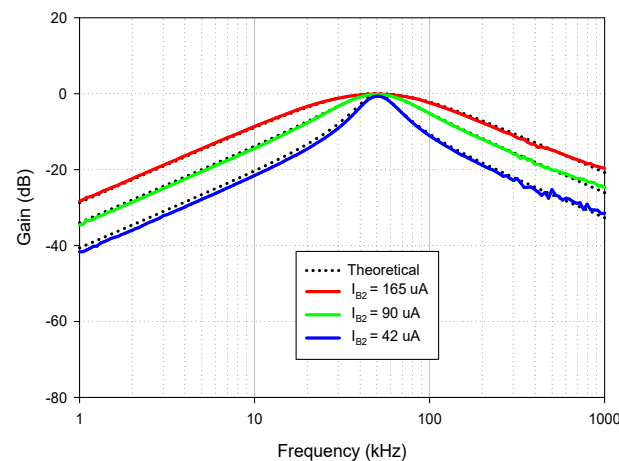


Figure 21. Experimental BP response for different bias current (I_{B2}) values ($I_{B1} = 155 \mu\text{A}$, $R_1 = 1 \text{ k}\Omega$ and $C_1 = C_2 = 5.5 \text{ nF}$).

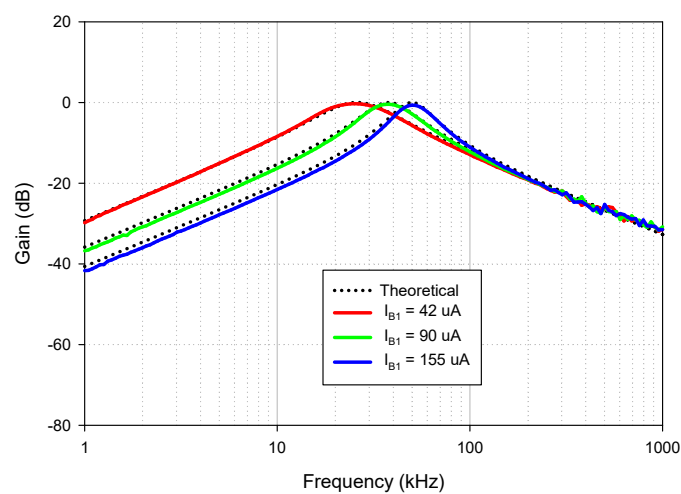
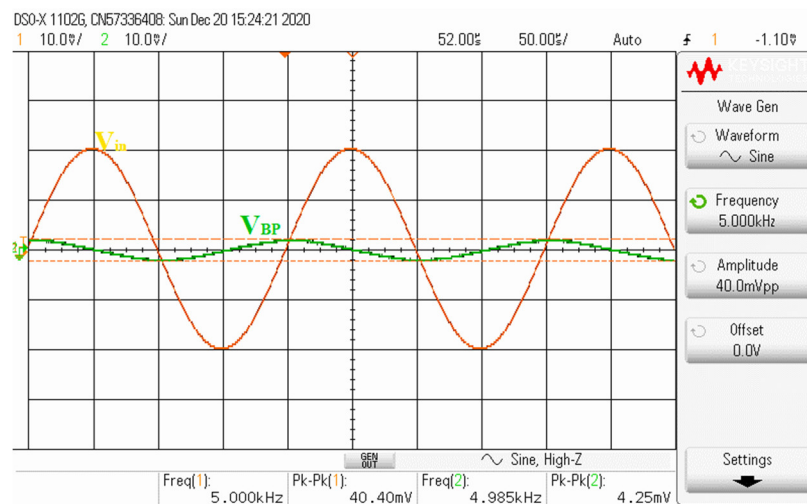
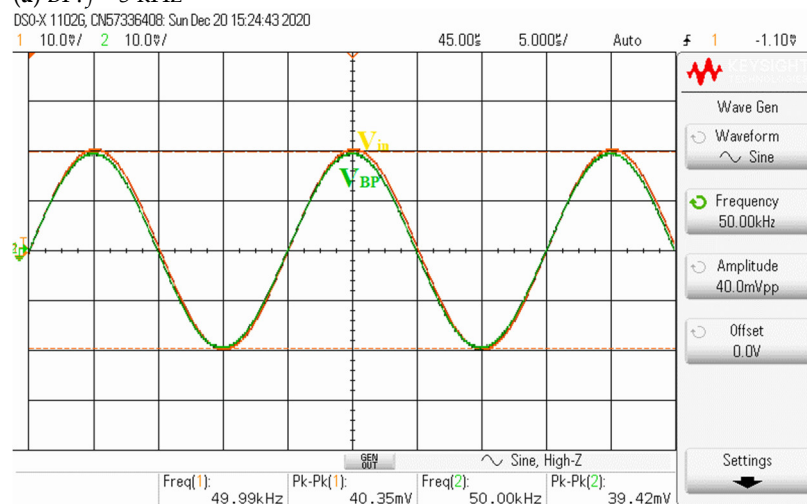


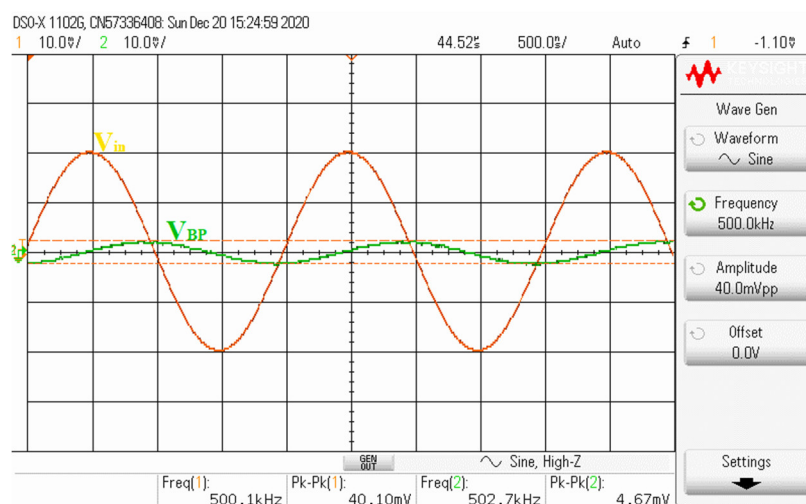
Figure 22. Experimental BP responses for different I_{B1} values ($I_{B2} = 195 \mu\text{A}$, $R_I = 1 \text{ k}\Omega$ and $C_1 = C_2 = 5.5 \text{ nF}$).



(a) BP: $f = 5 \text{ kHz}$



(b) BP: $f = 50 \text{ kHz}$

(c) BP: $f = 500$ kHz**Figure 23.** Measured BP filtering transient response.

Next, the inverting all-pass biquad filter with unity voltage gain was tested by setting the transconductances $g_{m1} = g_{m2}$ ($I_{B1} = I_{B2} = 200 \mu\text{A}$) and applying the input voltage signal to the input voltage nodes, v_{i1} , v_{i3} and v_{i4} , while the input voltage node v_{i2} was grounded. Although it requires the matching conditions of I_{B1} and I_{B2} , this is the active matching condition that is easier to control than the passive matching condition. The passive elements were still chosen as the resistor $R_1 = 1 \text{ k}$ and the capacitors $C_1 = C_2 = 5.5 \text{ nF}$. Figure 24 shows the experimental phase and magnitude response of the proposed voltage-mode universal biquad filter. The graph shows that the output phase response of the AP filter is shifted from -180 to 180 degrees. However, at the frequency close to the natural frequency, the experimental voltage gain is slightly different from the ideal due to nonideal characteristics of the VDDDA, as explained in Section 2.4. The measured input and output waveforms of the AP filtering function are, respectively, shown in Figure 25a–c, where a sine wave signal with a peak-to-peak value of 40 mVpp @ 5 kHz , 100 kHz and 500 kHz was applied to the input of the filter. It appeared that the proposed filter can be used as the phase shifter circuit with constant output amplitude.

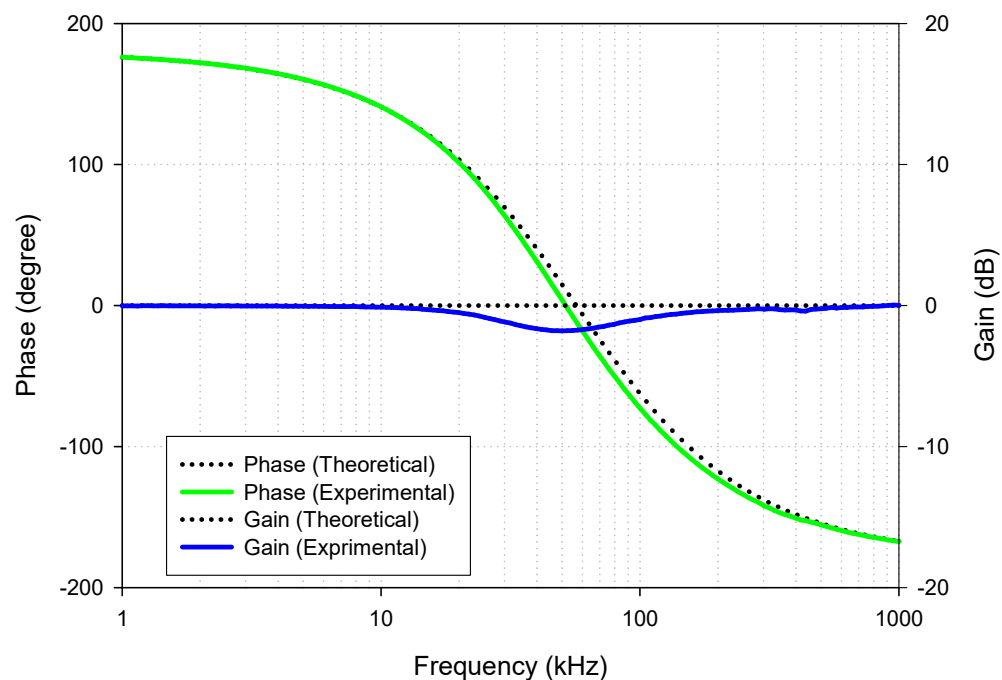
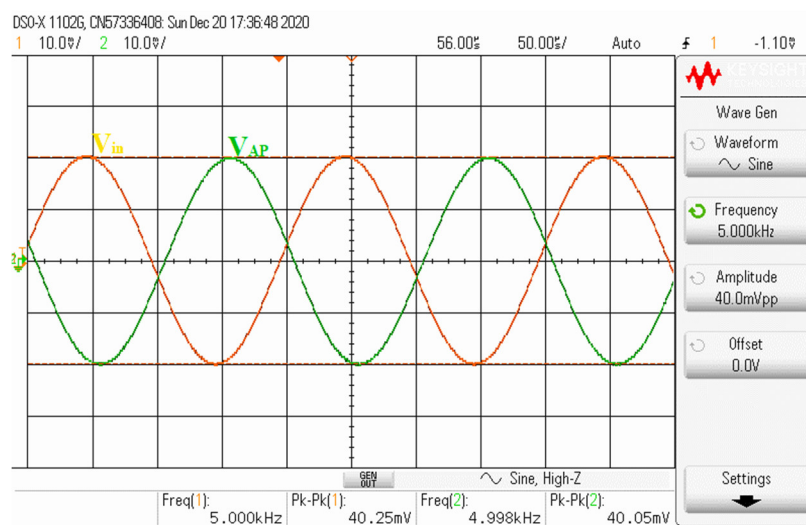


Figure 24. Experimental gain and phase response of the AP filter ($I_{B1} = I_{B2} = 200\mu\text{A}$, $R_1 = 1\text{ k}$ and $C_1 = C_2 = 5.5\text{ nF}$).



(a) AP: $f = 5\text{ kHz}$

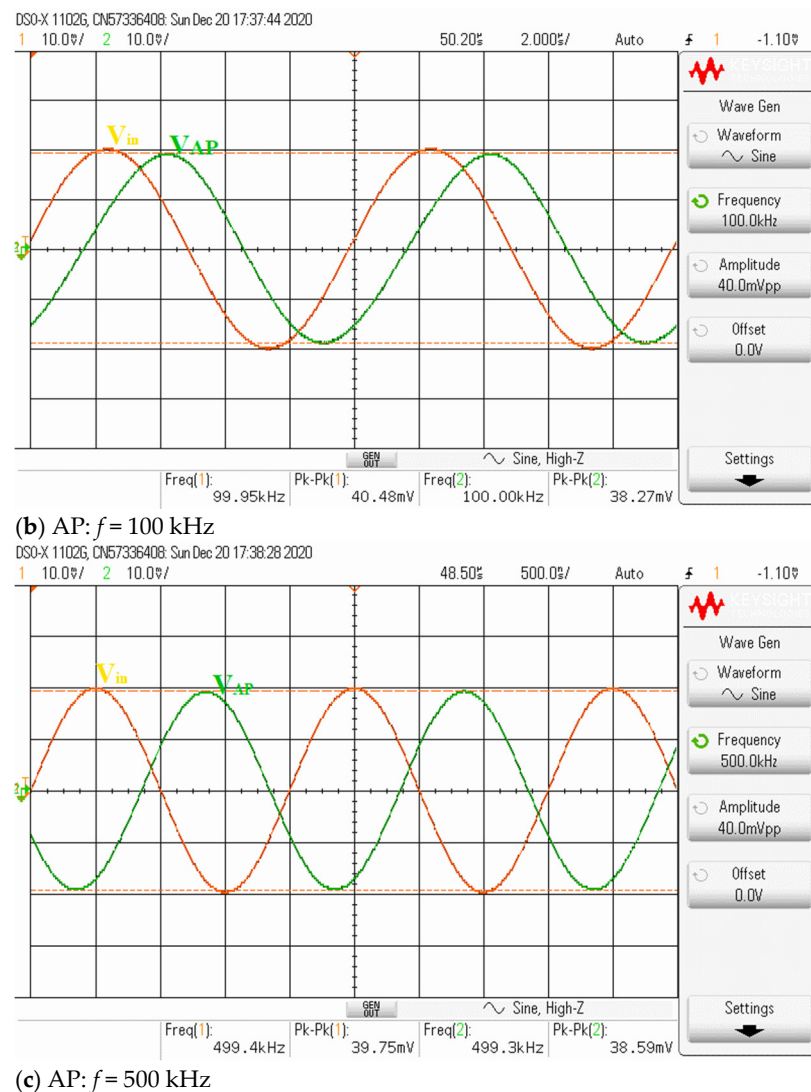


Figure 25. Measured AP filtering transient response.

5. Comparison

Table 1 compares the proposed universal biquad filter with previous biquad filters using the VDDDA [13–24]. These biquad filters are the multiple input multiple output (MIMO) [13,14,23], multiple input single output (MISO) [16,18,19,21,24] and single input multiple output (SIMO) [14,17,20,22] configurations. The design technique used in [13–15,17,19–22] were based on two integrator loops, while the filters in [16,18,23,24] were based on a passive RLC circuit. The proposed filter was designed from the parallel RLC circuit connecting with the voltage differencing circuit, and the VDDDA is very useful for this design. The RLC-based biquad filters proposed in references [16,18,23,24] were very simple circuitry with a single VDDDA as the active building block. Additionally, in [18,24], the f_0 and Q were orthogonally controlled via the passive resistor. However, these biquad filters realized from the RLC circuit had the following disadvantages: for example, they consisted of a floating capacitor [16,18,24], the f_0 and Q were not orthogonally controlled by changing the separated transconductance of the VDDDA [16,18,23,24], none of the high-impedance nodes and low-impedance nodes were given in references [16,18,23,24] and the unity gain inverting voltage amplifier or double-gain voltage amplifier was required for obtaining several filtering functions [16,18,24]. These limitations of the RLC-based filters have been improved in this work. The two-integrator loop-based biquad filters with high input impedance were obtained from references [13–15,17,22–25], and the low output impedance property for all output nodes was obtained from references

[14,22,25]. In [13,14,20–22], the f_0 and Q were orthogonally controlled by the separated transconductance. Additionally, the two VDDDA-based filters in reference [15] achieved orthogonal control of the f_0 and Q via the passive resistor. Additionally, the f_0 and Q of the proposed filters in references [13,14,20–22] could be linearly and independently controlled by simultaneously setting the transconductances in the integrator circuits. However, the biquad filter proposed in references [13,14,20–22] required three VDDDA-s. Additionally, the passband voltage gain of the three VDDDA-based filters in references [13,14,22] were not constant during tuning the f_0 and Q for some filtering responses. The two-integrator loop filter in references [15,17] could not provide five filter responses. Additionally, two VDDDA-based biquad filters in references [15,17,22] could not achieve orthogonal control of the f_0 and Q by separated transconductance. The performances of the universal filters in references [13–18,23,24] were proved via simulation only, while both simulation and experiment were verified in this work.

Table 1. Comparison of the proposed biquad filter and other filters using VDDDA.

Ref	Filtering Category	No. of VDDDA	No. of R + C	Use of all Grounded Capacitors	High Impedance of all Input Nodes	Low output Impedance for all Output Node	Electronic Tune of Q without Affecting ω_0	Filtering Functions	Constant Pass-band Gain during Tuning ω_0 and Q for all Responses	Technology	Additional Circuit	Results	Power supply Voltages & Power Consumption*	Dynamic Range & Noise
[13]	MIMO	3	1 + 2	Yes	Yes	No	Yes	LP, BP, HP, BR, AP	No	0.18 μ m TSMC CMOS	No	Simulation	± 0.9 V & N/A	N/A
[14]	MIMO	3	1 + 2	Yes	Yes	No	Yes	LP, BP, HP, BR, AP	No	0.18 μ m TSMC CMOS	No	Simulation	± 0.9 V & N/A	N/A
[15]	SIMO	2	2 + 2	Yes	Yes	No	No	LP, BP, HP	Yes	0.18 μ m TSMC CMOS	No	Simulation	± 0.9 V & N/A	N/A
[16]	MISO	1	1 + 2	No	No	No	No	LP, BP, HP, BR, AP	Yes	0.25 μ m TSMC CMOS	Inverting Amp. & double gain Amp.	Simulation	± 1.25 V & 1.58 mW	N/A
[17]	SIMO	2	0 + 2	Yes	Yes	No	No	LP, BP, HP, BR	Yes	0.18 μ m TSMC CMOS	No	Simulation	± 0.9 V & 0.21 mW	N/A
[18]	MISO	1	2 + 2	No	No	No	No	LP, BP, HP, BR, AP	Yes	0.25 μ m TSMC CMOS	Inverting Amp.	Simulation	± 1.25 V & N/A	N/A
[19]	MISO	2	0 + 2	Yes	Yes	Yes	No	LP, BP, HP, BR, AP	Yes	Commercial ICs	No	Simulation & Experiment	± 5 V	N/A
[20]	SIMO	3	1 + 2	Yes	Yes	No	Yes	LP, BP, HP, BR, AP	Yes	0.18 μ m TSMC CMOS & Commercial ICs	No	Simulation & Experiment	± 0.9 V & 0.34 mW	N/A
[21]	MISO	3	1 + 2	Yes	Yes	Yes	Yes	LP, BP, HP, BR, AP	Yes	Commercial ICs	No	Simulation & Experiment	± 5 V & N/A	N/A
[22]	SIMO	3	1 + 2	Yes	Yes	No	Yes	LP, BP, HP, BR, AP	No	0.18 μ m TSMC CMOS & Commercial ICs	No	Simulation & Experiment	± 0.9 V & N/A	N/A
[23]	MIMO	1	1 + 2	Yes	Yes	No	No	LP, BP	Yes	0.18 μ m TSMC CMOS	No	Simulation	± 0.9 V & 0.73 mW	N/A

Ref	Filtering Category	No. of VDDDA	No. of R + C	Use of all Grounded Capacitors	High Impedance of all Input Nodes	Low output Impedance for all Output Node	Electronic Tune of Q without Affecting ω_0	Filtering Functions	Constant Pass-band Gain during Tuning ω_0 and Q for all Responses	Technology	Additional Circuit	Results	Power supply Voltages & Power Consumption*	Dynamic Range & Noise
[24]	MISO	1	2 + 2	No	No	No	No	LP, BP, HP, BR, AP	Yes	Commercial ICs	Inverting Amp.	Simulation	± 5 V & N/A	N/A
Proposed Filter	MISO	2	1 + 2	Yes	Yes	Yes	Yes	LP, BP, HP, BR, AP	Yes	0.18 μ m TSMC CMOS & Commercial ICs	No	Simulation & Experiment	± 0.9 V & 0.99 mW	73.27 dB & 46 μ Vrms

* The power consumption, dynamic range and noise are taken from the simulation. N/A: information not available/shown.

6. Conclusions

In this work, a new universal biquad filter using VDDAs was proposed. The design technique used in this work was based on the parallel RLC circuit connecting with a voltage differencing circuit. The proposed filter is composed of two VDDAs, one resistor and two grounded capacitors, which ensure reduction in a fabrication space and the compensation of parasitic effects. Five filtering responses with unity passband voltage gain are obtained. The AP response is achieved without matching by connecting the z terminal to the p terminal of VDDA₂. The f_0 and Q are orthogonally controlled from separated transconductance (f_0 is tuned by g_{m1} , and Q is tuned by g_{m2}). This feature can be electronically controlled by implementing the VDDA from the commercially available ICs. The performance and functionality of the proposed universal biquad filter were demonstrated with a simulation and experimental results, confirming the theory.

Author Contributions: Conceptualization, W.J. and F.K.; Methodology, W.J., F.K.; and T.K.; Validation, W.J., F.K. and T.K.; Formal Analysis, W.J., F.K. and K.P.; Investigation, W.J., F.K. and K.P.; Writing—Original Draft Preparation, W.J. and F.K.; Writing—Review and Editing, W.J., F.K.; T.K. and K.P. All authors have read and agreed to the published version of the manuscript.

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