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A Quick Start Method for MEMS Disk Resonant Gyroscope

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Abstract: High-precision disk resonator gyroscope has a high quality factor in order to improve the performance of the gyroscope, as the high quality factor can lead to a long starting time. In this paper, a control system of the driving loop of the disk MEMS resonant gyroscope with the quick start is designed. The control system has functions of quick frequency locking and fast step response. Coarse-precision mode transition system is designed for quick frequency locking. A large-small mode transition system is designed for fast step response. The correctness of the design is verified by circuit test. The test results show that the start-up time is reduced by over 80% compared with the traditional control loop.

Keywords: disk resonator gyroscope; quick start; phase locked loop (PLL)

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1. Introduction

Navigation includes astronomical navigation, satellite navigation, inertial navigation, radio navigation, etc., among which only inertial navigation is autonomous. Inertial navigation is difficult to disturb as it does not rely on external signals. Gyroscope and accelerometer are the core devices in the inertial navigation system. With the progress of micromachining technology, MEMS gyroscope has been widely used in fields like automotive, consumer electronics, industry, aerospace and other fields because of its small volume, low power consumption and low cost [1–6].

Disk resonant gyroscope (DRG) is a high-performance MEMS gyroscope which has attracted much attention in recent years [7–9]. It has the advantages of mode matching, high quantity factor, high impact resistance and being insensitive to environmental vibration [2,10]. With the increase of quality factor of the gyroscope, the start-up time also increases. Therefore, it is necessary to change the control system of driving mode to realize fast start of driving mode.

The start-up time of gyro driving mode mainly includes frequency locking time [11] and step response time. At present, most gyro driving mode control systems are using PLL (phase locked loop) to maintain stable operation [2,12–14]. In the digital phase-locked loop, the direct digital frequency synthesizer is used to generate sinusoidal signal to activate the gyro. There is deviation between the initial frequency of DDS (Direct digital frequency synthesizer) module and the resonant frequency of driving mode. Therefore, a phase-locked loop is needed to make the frequency of the output signal of DDS equal to the resonance of gyro driving mode. However, the amplitude of the output signal of the driving mode is very small at start-up, resulting in a long frequency locking time. In addition, the increase of the high quality factor of the gyro increases the step response time of driving mode [15].

Typical driving circuits use PLL to maintain the gyroscope vibrating at its resonant frequency. A quick frequency locking system with coarse-precision mode transition was

proposed in paper [11]. The coarse resonance control loop is implemented using non-ideal differentiator, amplifiers and limiter for delaying the pickoff signal and a PLL is used for the precision loop. The control system is implemented by using analog electronics. A fully integrated excitation electronics for bulk micro machined gyroscopes was proposed in paper [16], which enables quick start-up or powerful continuous stage drive of a resonating sensor. The charge pump circuit converts the low voltage signal at the resonant frequency to a 20 V differential square wave to obtain large excitation force. Large excitation force can realize the quick start of gyroscope. A novel closed-loop drive circuit for the micro machined gyroscope has been presented in paper [17]. A comparator is used instead of the AGC (Automatic gain control) circuit in this closed loop circuit to control the amplitude of the output signal, which overcomes the disadvantages of limited linear operational range and limited output signal amplitude. This method increases the excitation force and reduces the starting time. The method is simple and easily achieved. However, this control method cannot suppress the phase noise.

It can be seen that the method of quick start is mainly realized by increasing the excitation force. The control system is mainly implemented by using analog electronics. This paper introduces a method to realize the rapid start-up of dish vibratory gyroscope by adjusting the parameters of phase-locked loop in different stages. The control system realizes quick frequency locking and fast step response. A coarse precision mode conversion system is designed in this paper to shorten the frequency locking time. A large-small mode conversion system is designed to shorten the step response time of mechanical structure. This method enables the gyro to start faster. Compared with method in [11], the method in this paper uses less resources and is more suitable for digital circuit implementation.

In the second section, the working principle, frequency locking characteristics and step response characteristics of MEMS disk resonator gyro are introduced. In the third section, the design of quick frequency locking control system, fast response system and amplitude control system are introduced. In Section 4, the test results are introduced. The conclusion is presented in Section 5.

2. Architecture and Motion Model of Disk Gyroscope

2.1. Basic Structure of Mems Disk Resonator Gyroscope

The structure of MEMS disk resonant gyroscope is shown in Figure 1. The gyroscope is composed of concentric nested rings with spokes connected by spokes, and the resonator is supported by a central anchor. There are 16 electrodes around the disk resonator. There are also internal electrodes for electrostatic tuning [18–20].

Figure 1. Structure of disk gyroscope.

The dynamic equations of driving mode and sensing mode are shown in Equation (1) [21–23]:

$$\begin{cases} \ddot{x} + \frac{2}{\tau_x} \dot{x} + k_{12}y + (c_{12} - 2A_g\Omega)\dot{y} + \omega_x^2x = f_x \\ \ddot{y} + \frac{2}{\tau_y} \dot{y} + k_{21}x + (c_{21} + 2A_g\Omega)\dot{x} + \omega_y^2y = f_y \end{cases} \quad (1)$$

where Ω is the input angular rate; ω and k are the resonant frequency and stiffness of each axis, respectively; A_g is the angular gain; $\tau = 2Q/\omega$, Q is the quality factor.

The displacement of the driving mode can be written as:

$$x = A \sin \omega_d t \quad (2)$$

The start-up time of driving mode mainly includes two parts: frequency locking time and step response time. In the control system using PLL, the frequency locking time is the time when the frequency of the oscillator (DDS is generally used in digital control system) reaches the resonant frequency of the gyro driving mode from the starting frequency; when the frequency is locked, the gyro is in resonant state. The amplitude of the output signal of the driving mode begins to increase. This stage can be approximated as a step response. In Figure 2, the start-up time of MEMS disk resonator gyroscope is illustrated. The quality factor of gyro is more than 420,000.

Figure 2. The start-up time of MEMS disk resonator gyroscope.

As shown in the Figure 2, curve N1 represents the change of frequency and curve N2 represents the change of amplitude. T1 is the time of frequency locking and T2 is the time of step response. The difference between the initial frequency and resonant frequency of DDS module is 2 Hz. Therefore, at the initial time, the driving mode is in forced vibration. The amplitude of vibration is very low. As the output frequency of DDS module gradually approaches the resonant frequency, the driving mode is transiting to the resonant state. As shown in Figure 2, the output voltage of the driving mode gradually increases. It can be concluded that if the start-up time is required to reduce, the frequency locking time and the step response time of the driving mode are required to reduce respectively. The characteristics of frequency locking and step response of driving mode are analyzed below.

2.2. Analysis of Frequency Locking Characteristics

Frequency locking is mainly realized by phase-locked control loop. The phase control loop is a servo system, which mainly realizes the locking and tracking control of frequency and phase. In order to analyze the characteristics of the phase control loop, the phase control loop of the gyro needs to be simplified. If the analog front stage, ADC (Analog to digital converter), DAC (Digital to analog converter) and amplitude control loop are ignored, a simplified phase control loop structure can be obtained, as shown in Figure 3.

Figure 3. Principle of phase control loop.

As shown in Figure 3 the phase difference between the driving mode output signal and the excitation signal is obtained by demodulation. The phase difference is input into the loop filter to obtain FTW (frequency tuning word). DDS is used to generate sinusoidal signal required for excitation. The structure is further equivalent to a control system as shown in Figure 4.

Figure 4. Principle of phase locked loop.

Where K_d is the gain of the phase detector, K_u/s is the frequency domain model of DDS, and K_u is the gain of DDS. K_d can be written as Equation (3)

$$K_d = \frac{K_{d1}K_{d2}}{2} \quad (3)$$

where K_{d1} is the amplitude of the input signal and K_{d2} is the amplitude of the reference signal. The loop gain can be written as:

$$G(s) = \frac{K_d K_u}{s} \frac{1 + s\tau_2}{\tau_1 s} \quad (4)$$

The loop gain of phase control loop is related to the amplitude K_{d1} of the input signal and the gain K_u of the DDS module. It can be represented as shown in Figure 5.

Figure 5. Frequency characteristics of phase control loop of driving mode.

The DC gain of the loop is:

$$\omega_5^2 = \omega_3 \omega_4 = \frac{K_d K_v}{\tau_1} \quad (5)$$

The ratio of ω_4 to ω_3 determines the loop damping. When the ratio is 2, the damping is about 0.7. The bandwidth of PLL is:

$$\omega_4 = \sqrt{\frac{2K_d K_v}{\tau_1}} \quad (6)$$

By bringing Equation (3) into Equation (6), it can be derived:

$$\omega_4 = \sqrt{\frac{K_{d1} K_{d2} K_v}{\tau_1}} \quad (7)$$

The bandwidth of the loop is related to the amplitude of the input signal of the PLL. At startup, when the driving mode does not reach the resonant state, the amplitude of driving mode output signal K_{d1} is small. At this time, the frequency locking range is small. Due to the small loop gain, the frequency locking time is also long.

2.3. Analysis of Step Response Characteristics

When the frequency reaches or approaches the resonant frequency of the driving mode, the change of driving mode amplitude can be regarded as step response. It can be seen from Equation (1) that the driving mode can be approximated as a two-stage underdamped system. For an underdamped second-order system, the peak time, that is, the time required for the unit step response to reach the first peak, can be written as:

$$t_p = \frac{\pi}{\omega_d} = \frac{\pi}{\omega_n \sqrt{1 - \xi^2}} \quad (8)$$

where ω_n is the undamped oscillation frequency and ω_d is the damped oscillation frequency. The peak time is related to the gyro damping ratio. With the increasing quality factor of high-precision gyroscope, the start-up time of gyroscope will inevitably increase. As shown in Figure 6, the step response time of MEMS disk resonator gyroscope used in this paper is shown.

Figure 6. The time of step response.

In Figure 6, M1, M2 and M3 are the voltage values of the output of the gyro driving mode under different driving forces. M1 has amplitude fluctuation near 5V due to output saturation caused by excessive driving force. And the amplitude is stabilized at 5V earlier because of output saturation. Under different driving forces, the time for the output to reach the stable value is approximately equal. The time in the three curves exceeds 80s, which is obviously unacceptable for the requirement of fast start. Therefore, the time of driving mode step response must be reduced.

3. Design of Control System for Quick Start of Driving Mode

The characteristics of frequency locking time and step response time can be obtained through the analysis in Section 2. This section introduces the design of a quick start control system.

3.1. Design of Quick Frequency Locking Control System

According to the analysis in Section 2.2, the reason for the long frequency locking time is that the output voltage of the driving mode is low at the initial stage of startup, which reduces the loop gain of the PLL. This will result in longer frequency locking time and cause the frequency locking range to become smaller or even unable to lock. Therefore,

to solve this problem, the coarse-precision mode transition system shown in Figure 7 is introduced in this paper.

Figure 7. Phase control loop with quick frequency locking.

The difference from the traditional phase-locked loop is that the input of the phase detector in the phase-locked control loop is variable. In the initial stage of startup, the output signal of the gyro driving mode $x_1(t)$ is transformed into a square wave signal as shown in Figure 8. The square wave is used as the input of the phase detector to realize the quick locking of the phase control loop. After the frequency is approximately locked, the output signal of the gyro driving mode $x_1(t)$ is used as the input of the phase detector to achieve more accurate locking and tracking.

Figure 8. Square wave signal.

The square wave signal $f(t)$ converted by $x_1(t)$ is shown in Figure 8. The square wave can be written as Equation (9)

$$f(t) = \begin{cases} E & x_1(t) \geq 0 \\ -E & x_1(t) < 0 \end{cases} \quad (9)$$

where E is the amplitude of the square wave signal, and it can be obtained by Fourier expansion of the square wave signal.

$$f(t) = \frac{4E}{\pi} \left[\sin 2\pi ft + \frac{1}{3} \sin 6\pi ft + \frac{1}{5} \sin 10\pi ft + \dots + \frac{1}{n} \sin 2n\pi ft + \dots \right] \quad (10)$$

Since the subsequent digital signal processing contains a digital filter, the high-frequency term can be filtered after demodulation, so $f(t)$ can be approximately written as:

$$f(t) \approx \frac{4E}{\pi} \sin 2\pi ft \quad (11)$$

The demodulation is realized by multiplier. In this design, due to the use of sigma delta ADC, there is a down sampling process. The ADC data output rate is much lower

than the sampling rate, so the multiplier can be realized by serial structure, which is simple in structure and occupies less resource. The demodulation result is shown in Equation (12).

$$\begin{aligned} f_d(t) &= \frac{4E}{\pi} \sin 2\pi f t \times K_{d2} \cos(2\pi f + \varphi_0) \\ &= \frac{2E}{\pi} K_{d2} \sin(4\pi f t + \varphi_0) + \frac{2E}{\pi} K_{d2} \sin(\varphi_0) \end{aligned} \quad (12)$$

Since the subsequent digital signal processing contains a digital filter, the high-frequency term can be filtered after demodulation. The gain of the phase discriminator can be written as

$$K_{d2} \approx \frac{2EK_{d2}}{\pi} \quad (13)$$

At this time, the loop gain of the PLL can be written as:

$$G(s) = \frac{2EK_{d2}K_v}{\pi s} \frac{1 + s\tau_2}{\tau_1 s} \quad (14)$$

The bandwidth of PLL is:

$$\omega_4 = \sqrt{\frac{2EK_{d2}K_v}{\pi\tau_1}} \quad (15)$$

The loop gain of PLL is no longer affected by the amplitude of input signal. The locking time of the loop can be changed by changing the value of E . When the frequency is approximately locked, the loop is converted to accurate locking. At this time, the input of the PLL is no longer the converted square wave signal, but the signal before conversion. The amplitude of the amplitude control loop is used as the switching signal. It will be converted when the amplitude of the driving mode is greater than the set value. The amplitude control loop is introduced in Section 3.3.

3.2. Design of Quick Step Response Control System

The MEMS disk resonator gyroscope uses capacitive excitation, and its equivalent structure is shown in Figure 9. The capacitance formed by the resonator and the excitation electrode can be regarded as a flat plate capacitance. The capacitance can be written as:

$$C_1 = \frac{A\epsilon_0\epsilon_r}{x_0 + x} \quad (16)$$

where x_0 is the initial plate spacing and x is the moving distance. As shown in Figures 1 and 9, for the vibration mode $n = 2$, capacitors with an angle difference of 90° have opposite displacements to each other. The capacitance can be written as:

$$C_2 = \frac{A\epsilon_0\epsilon_r}{x_0 - x} \quad (17)$$

Figure 9. Model of excitation capacitance.

In signal processing, the difference between the two changes can be obtained to increase the signal amplitude. When $x \ll x_0$, the variation of capacitance can be obtained as Equation (18).

$$\Delta C = C_1 - C_2 = \frac{A\epsilon_0\epsilon_r}{x_0 - x} - \frac{A\epsilon_0\epsilon_r}{x_0 + x} \approx \frac{2A\epsilon_0\epsilon_r}{x_0^2}x \quad (18)$$

A voltage of V_1 is applied to the excitation electrode and a voltage of V_p is applied to the mass block, so that the voltage difference between the electrode and the mass block is:

$$V = V_p - V_1 \quad (19)$$

Therefore, the energy stored in the capacitor is:

$$E = \frac{1}{2}CV^2 = \frac{A\epsilon_0\epsilon_r V^2}{2(x_0 + x)} \quad (20)$$

Electrostatic force can be written as:

$$F = -\frac{\partial E}{\partial x} = -\frac{A\epsilon_0\epsilon_r V^2}{2(x_0 + x)^2} \quad (21)$$

The differential excitation voltages $V_{dc} + V_{ac}\sin\omega_d t$ and $V_{dc} - V_{ac}\sin\omega_d t$ are applied to the electrodes respectively, and the resulting driving force is:

$$\begin{aligned} F_{tot} &= \frac{A\epsilon_0\epsilon_r}{2(x_0 - x)^2} (V_{dc} + V_{ac}\sin\omega_d t)^2 - \frac{A\epsilon_0\epsilon_r}{2(x_0 + x)^2} (V_{dc} - V_{ac}\sin\omega_d t)^2 \\ &\approx \frac{2A\epsilon_0\epsilon_r V_{dc} V_{ac}}{x_0^2} \sin\omega_d t \end{aligned} \quad (22)$$

According to Equation (8), the step response time of driving mode is fixed under fixed driving force. Therefore, the time of step response can be reduced by converting the driving force. Equation (23) gives the expression of the driving force, which can be simplified to obtain:

$$F_{tot} \propto V_{dc} V_{ac} \sin\omega_d t \quad (23)$$

The driving force is proportional to DC voltage V_{dc} and AC amplitude V_{ac} . V_{dc} is mainly used for amplitude adjustment. The increase or decrease of the value is limited. As the digital control circuit is used in this paper, sinusoidal digital signal is mainly generated by DDS module, and then it converts to corresponding analog signal through DAC. Therefore, it can easily realize the multiplication change of V_{ac} by shift operation. As shown in Figure 10, quick step response is realized by changing the value of V_{ac} .

As shown in Figure 10, M1, M2 and M3 are the original step response curves, and M4 and M5 are the output curves corresponding to the quick step response. Taking M5 as an example, in the initial stage, the V_{ac} in M5 is the same as that in M1, so it has the same upward slope in the initial stage. After reaching the predetermined value, the value of V_{ac} is reduced to make it stable quickly.

Figure 10. The time of quick step response.

It should be noted that whether it is quick frequency locking or quick step response, the control loop is always a servo system, so the stability of the system must be considered. In Section 3.1, the loop gain of the quick frequency locking loop is conducted, which is simplified as follows:

$$G(s) \propto 2EK_{d2} \quad (24)$$

The loop gain is proportional to E and K_{d2} . In the design of quick step response, V_{ac} is increased at the initial stage of start-up, which will inevitably lead to the increase of K_{d2} in the same proportion, resulting in the increase of loop gain $G(s)$. There will be a certain margin in the design of phase loop. The increase of V_{ac} leads to insufficient margin. This will result in the instability of phase control loop. Therefore, at the initial stage of step response, the relative invariance of $G(s)$ must be guaranteed while increasing V_{ac} . Therefore, it is necessary to reduce the value of E at this stage. After switching to a smaller V_{ac} , E can be restored to its original size. Therefore, the quick locking circuit in Section 3.1 is improved and the structure diagram is shown in Figure 11. Figure 11 is the final version of the quick start method in this paper. It can realize fast frequency locking and fast step response. Compared with Section 3.1, the control of the amplitude of the signal input to the DAC is increased, and the E value is changed synchronously. The test results of this circuit will be given in Section 4.

Figure 11. Control system of quick start driving loop.

3.3. Control System of Amplitude Stable Loop

Gyro control system needs amplitude control loop to avoid change of amplitude caused by noise. In addition, the quick frequency locking circuit and fast step response circuit need to judge whether to convert the mode by monitoring the amplitude of the driving mode signal. The structure of amplitude control circuit is shown in Figure 12. The excitation voltages $V_{dc} + V_{ac}\sin\omega t$ and $V_{dc} - V_{ac}\sin\omega t$ are applied to the electrodes of the gyro driving mode. The amplitude of gyro output signal is controlled by PI controller.

Figure 12. Amplitude control loop.

4. Circuit Realization and Test

According to the above analysis, the whole gyro system is implemented at PCB level. The assembled PCB is shown in Figure 13. The charge amplifier, ADC, DAC and other modules are built by discrete devices, and the digital signal processing is implemented by FPGA.

Figure 13. Gyro control circuit.

The test platform is shown in Figure 14. The value of the register in FPGA can be output to PC through serial port. The frequency tuning word of DDS module, that is, the vibration frequency of driving mode, can be output in this way. The amplitude detected by the amplitude control loop can also be output in this way.

Figure 14. Test platform.

Firstly, the quick locking control system is tested, and the frequency tuning word of DDS is output to PC. Convert the output value to the corresponding frequency.

In Figure 15, the difference between the initial frequency and the resonant frequency of the driving mode is 2 Hz. At the beginning, the PLL is in the coarse locking state, and the frequency can be locked quickly. At this time, the frequency has large jitter. When the amplitude of the driving mode increases to the set value, the loop turns to precise locking. At this time, the accuracy of the phase-locked loop becomes higher.

Figure 15. Vibration frequency of driving mode.

As shown in Figures 16 and 17, the phase-locked loop using quick frequency locking control system is compared with the loop using only precise locking control system. In Figure 16, when the initial frequency difference is 2 Hz, the frequency locking time of quick frequency locking control system is less than 8 s and the time of one-step locking control system is 25 s. Using quick frequency locking control system can achieve frequency locking in a faster time. Compared with the single step locking mode, the locking time using quick frequency locking control system is reduced by 68%. Moreover, after conversion to precise locking, the two modes have the same frequency accuracy.

Figure 16. Comparison of two control modes when the initial frequency deviation is 1Hz.

Figure 17. Comparison of two control modes when the initial frequency deviation is 10Hz.

From Figure 17, when the initial frequency difference is 10 Hz, the frequency locking time of quick frequency locking control system is 15 s. The frequency locking time of one-step locking is 90 s.

From the previous analysis, the time required for the coarse resonance control mode can be changed by changing the value of E in Equation (14). As shown in Figure 18, the initial frequency difference is 10 Hz. When E takes different values, the time required for quick frequency locking control system is different. In Figure 18, $E1:E2:E3 = 16:8:1$. With the increase of E , the initial frequency jitter is greater and the loop locking time is shorter.

Figure 18. Vibration frequencies of driving modes under different parameters.

From Figure 19, the change of vibration frequency of driving mode under different initial frequencies can be obtained. When E does not change and the initial frequency offset is 1 Hz, 5 Hz and 10 Hz, respectively, the slope of frequency change in the three startup stages is the same, and the startup time increases with the increase of initial frequency offset.

Figure 19. Variation of vibration frequency of driving mode under different initial frequencies.

The test of fast step response has been given in the Figure 10. The Figure 20 shows the change of the amplitude of the output signal of the driving mode when the initial frequency deviation is 2 Hz.

Figure 20. Changes in frequency and amplitude at start-up.

As shown in Figure 20, the frequency and amplitude variation diagram of driving mode tested by quick frequency locking and fast step response method when the initial frequency deviation is 2 Hz. It can be seen from the Figure 20 that when the frequency difference is 2 Hz, the amplitude of the output signal of the driving mode is very small. When the frequency is approximately locked, the amplitude of the signal begins to increase rapidly. After increasing to the set value, the output signal is quickly stabilized at a small amplitude value by switching V_{ac} . The switching of V_{ac} also brings frequency jitter. At 9 s, the frequency and phase stability have been realized. Figure 6 has shown the variation of amplitude when using the traditional method. It can be seen that when using the traditional method, the start-up time is greater than 80 s. Comparing Figures 6 and 20, the fast start-up method in this paper reduces the start-up time by more than 80%. The time domain waveform observed by the oscilloscope is shown in Figure 21, where T3 is the time of frequency locking and T4 is the time of step response.

Figure 21. Amplitude change during start-up.

5. Conclusions

A quick frequency locking circuit and a fast step response circuit are proposed in this paper in order to realize quick start of gyro driving mode. When the frequency is not locked, the coarse-precision mode transition system is used to realize quick frequency locking. In the initial stage of frequency locking, the coarse locking method is adopted to increase the frequency locking range of the gyro and reduce the frequency locking time. After the frequency becomes stable, the control mode is switched to precise frequency locking control. After frequency locking, the circuit of large-small driving force conversion

is used to achieve fast step response. At the initial stage of step response, a large driving force is used to realize rapid increase of the amplitude of the signal output by the driving mode. After reaching the preset value, it turns to small driving force to achieve amplitude stability. The test results show that when the difference between the starting frequency and the resonant frequency is 2 Hz, the quick frequency locking time is reduced by 68% compared with the traditional method. Through the control method of fast step response, the step response time is less than 4 s. When the difference between the starting frequency and the resonant frequency is 2 Hz, the total startup time for the driving mode amplitude to reach stability is less than 9 s. The total start-up time is reduced by more than 80%. The quick start-up of high quality disk resonant MEMS gyroscope is realized.

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