

A 0.8 V, 5.3–5.9 GHz Sub-Sampling PLL with 196.5 fs_{rms} Integrated Jitter and −251.6 dB FoM

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Abstract: This paper proposes a hybrid dual path sub-sampling phase-locked loop (SSPLL), including a proportional path (P-path) and an integral path (I-path), with 0.8 V supply voltage. A differential master–slave sampling filter (MSSF), replacing the sub-sampling charge pump (SSCP), composed the P-path to avoid the degraded feature caused by the decreasing of the supply voltage. The I-path is built by a rail-to-rail SSCP to suppress the phase noise of the voltage-controlled oscillator (VCO) and avoid the trouble of locking at the non-zero phase offset (as in type-I PLL). The proposed design is implemented in a 40-nm CMOS process. The measured output frequency range is from 5.3 to 5.9 GHz with 196.5 fs root mean square (RMS) integrated jitter and −251.6 dB FoM.

Keywords: SSPLL; hybrid dual path loop; low jitter; low power consumption



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1. Introduction

Since 1969, the LC-based phase-locked loops (PLLs) have been developed for over fifty years [1]. Several designs of LC-based PLLs are reported recently to save power consumption [2–8] as urgent demands of low power requirements for integrated circuits (ICs) appear. Decreasing supply voltage is an effective way to achieve low power. However, low voltage always limits the performance of circuits. Therefore, improving the noise feature with lower supply voltage is very attractive.

In a classical charge pump PLL (CPPLL) system [9–15], phase noise is mainly generated from two parts: out-of-band noise which is dominated by the voltage-controlled oscillator (VCO) (noise of low pass filter is neglected); and in-band noise which is dominated by the phase detector, charge pump and divider. Several efforts have been addressed to study the phase noise of VCOs [16–18] and designs with ultra-low power consumption have been published [19–21]. Hence, this paper concentrates on the improvement of in-band noise at low supply voltage.

From the literature review, compared with widely used CPPLLs, sub-sampling PLL (SSPLL) and type-I PLL can suppress in-band noise effectively. In an SSPLL system, the multiplication factor N of the noise of charge pump is rejected and the noise of divider is removed [22–24]. However, the sub-sampling charge pump (SSCP) is not suitable for low voltage application, since it suffers from deteriorated current noise. In a type-I PLL, although the exclusive-OR gate and the master–slave sampling filter (MSSF) can work well with low voltage [25], the suppression of out-band noise is limited. Furthermore, locking at non-zero phase offset which causes spur noise is a serious trouble for type-I PLL. Therefore, the architectures of SSPLL and type-I PLL cannot be utilized for low voltage application directly.

Some previous published low-voltage PLL designs [2–5] demonstrate that transferring the PLL loop into a dual path loop which includes a proportional path (P-path) and an integral path (I-path) is a beneficial method to mitigate the limitation of circuits performances at the architectural level. Therefore, the dual path system might provide a chance

for designers to take full advantage of the SSPLL and type-I PLL and, meanwhile, avoid the drawbacks of these two structures.

Based on the problems and the possible idea of the solution, we present a hybrid dual path type-II SSPLL which can work at 0.8 V supply voltage with 196.5 fs_{rms} integrated and -251.6 dB FoM (figure of merit as expressed in Equation (1) [26]).

$$FoM_{PLL} = 20 \log \left(\frac{Jitter_{rms}}{1 \text{ s}} \right) + 10 \log \left(\frac{Power}{1 \text{ mW}} \right) \quad (1)$$

2. Architecture of Proposed SSPLL

2.1. Conceptual Block Diagram

The main objective of this study is to design a dual path type-II SSPLL to reduce the in-band noise with low supply voltage. As mentioned above, the MSSF, in the type-I PLL, can operate well at low voltage without feature limitation. Hence, the MSSF can take charge of the P-path directly. The SSCP is kept to compose the I-path, in order to suppress the noise of the VCO by the type-II structure. Although the performance of the charge pump is degraded, the gain of the I-path is much smaller than the gain of the P-path, therefore, the noise contribution in the PLL system is much smaller than that of the P-path (the theoretical verification will be implemented in the following sections). Moreover, the sub-sampling-based PLL has the probability to lock at an unwanted frequency, so a frequency-locked loop (FLL) is necessary to be added to avoid this frequency uncertainty. We design an all-digital FLL (ADFLL) which consists of a digital divider and an adaptive frequency calibration (AFC) [27]. The all-digital circuit is beneficial for the power saving as it can be fully powered off, after the calibration is done. The overall conceptual block diagram for the proposed system is presented in Figure 1.

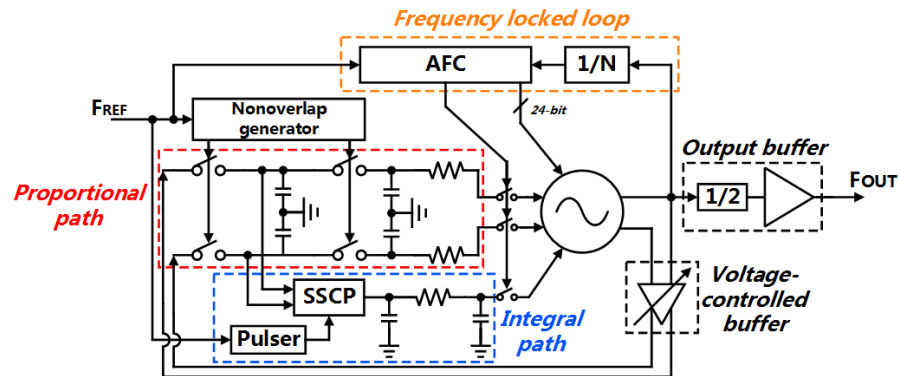


Figure 1. Conceptual architecture of proposed hybrid dual path SSPLL.

As indicated in [25], the traditional exclusive-OR based type-I PLL always faces the spur noise trouble, because of locking at the non-zero phase offset. Although the ideal MSSF can remove the voltage ripple on the control line of the VCO, current leakage from varactors and clock feedthroughs from the MSSF would introduce large ripples. To mitigate this phenomenon, we propose a differential MSSF to transfer the single path ripples into common-mode ripples.

Furthermore, we add a voltage-controlled buffer (VCBUF) at the output of the VCO to isolate the signal of the VCO away from the changeable load from the MSSF during the sampling.

2.2. Loop Analysis

A linear phase-domain model of the proposed SSPLL system is shown in Figure 2. We can treat this model as a time-continuous system if the bandwidth (BW) of the PLL f_{BW} is an order of magnitude smaller than that of the reference clock frequency f_{REF} [28] (called “Gardner’s Limit”).

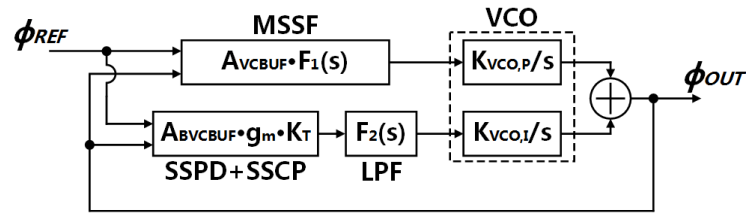


Figure 2. Linear model of the proposed SSPLL.

Unlike the traditional SSPLL, the proposed system has two paths as mentioned above. The relationship of these two paths determines the stability of the loop and phase noise performance of the system. Hence, we need to analyze the transfer function first.

In the P-path, to simplify the calculation, a single-end structure of the MSSF is analyzed in Figure 3, where C_{VAR} is the capacitance of the varactor in the VCO.

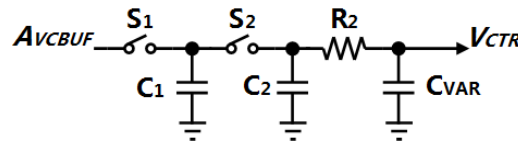


Figure 3. Single-end structure MSSF.

As a continuous-time approximation, since the Gardner's Limit is assumed to be satisfied, the switched capacitor C_1 can act as a series-equivalent resistor R_1 :

$$R_1 = \frac{1}{f_{REF} \cdot C_1} \quad (2)$$

where f_{REF} is the reference clock frequency. The gain of the MSSF in s-domain is given as Equation (3).

$$F_1(s) = \frac{sR_2C_{VAR} + 1}{s^3R_1R_2^2C_2C_{VAR}^2 + s^2R_2C_{VAR}(2R_1C_2 + R_1C_{VAR} + R_2C_{VAR}) + s(R_1C_2 + R_1C_{VAR} + 2R_2C_{VAR}) + 1} \quad (3)$$

where we choose $C_1 = 64$ fF, $C_2 = 16$ fF, $C_{VAR} = 10$ fF and $R_2 = 21$ k Ω to push the poles and zeros far away from f_{BW} and the gain of the MSSF can be approximated as 1. Thus, the open-loop gain of the P-path is obtained as follows:

$$G_{PP}(s) \approx A_{VCBUF} \cdot 1 \cdot \frac{K_{VCO,P}}{s} \quad (4)$$

where A_{VCBUF} is donated as the amplitude of the output signal from the voltage-controlled buffer.

Then, in the I-path, we can get the gain of the SSCP directly from the introduced modeling in the traditional SSPLL [22]:

$$\beta_{SSCP} = A_{VCBUF} \cdot g_m \cdot \frac{\tau_{PUL}}{T_{REF}} = A_{VCBUF} \cdot g_m \cdot K_T \quad (5)$$

where g_m is the transconductance of the input transistor of the SSCP, τ_{PUL} is the pulse width of the pulser, T_{REF} is the period of the reference clock. Moreover, the transfer function of the I-path low pass filter (LPF) can be easily acquired:

$$F_2(s) = \frac{sR_{int}C_{int2} + 1}{s^3R_{int}^2C_{int1}C_{int2}^2 + s^2R_{int}C_{int2}(2C_{int1} + C_{int2}) + s(C_{int1} + C_{int2})} \quad (6)$$

where C_{int1} is the integral capacitor, and R_{int} and C_{int2} are the low pass resistor and capacitor, respectively. We choose $C_{int1} \gg C_{int2}$ and $1/2\pi R_{int}C_{int2} \gg f_{BW}$ to get $F_2(s) \approx 1/sC_{int1}$. Hence, the open-loop gain of the I-path is given as:

$$G_{IP}(s) \approx A_{VCBUF} \cdot g_m \cdot K_T \cdot \frac{K_{VCO,I}}{s^2 C_{int1}}. \quad (7)$$

If we set $K_{VCO,P} = K_{VCO,I} = K_{VCO}$, the system open-loop gain is:

$$G_{SSPLL}(s) = G_{PP}(s) + G_{IP}(s) = \frac{A_{VCBUF} \cdot K_{VCO}}{s} \cdot \left(1 + \frac{g_m K_T}{s C_{int}}\right) \quad (8)$$

where a zero appears at $f_z = g_m K_T / 2\pi C_{int1}$.

In order to ensure the stability of the SSPLL, the zero needs to be smaller than f_{BW} . In other words, $g_m K_T$ should be much smaller than $s C_{int1}$ around the angular frequency of the reference ω_{BW} , which means that $G_{PP}(s) \gg G_{IP}(s)$. Hence, f_{BW} is determined by the P-path.

3. Circuit Implementation

3.1. Class-C VCO with Start-Up Circuit

Due to high power efficiency, a complementary cross-coupled Class-C VCO based on the design in [29] is chosen to be implemented. As shown in Figure 4, the NMOS cross-coupling pair M_1/M_2 operates in the Class-C scheme. The current mirror including M_1/M_2 and M_{B1}/M_{B2} work as a start-up circuit. When circuits are powered up, the bias voltage V_B is set high enough to ensure the pair M_1/M_2 (operating in Class-B) has a enough negative resistance to start to oscillate. Then, currents flowing through M_1/M_2 increase, as the oscillating amplitude increases. Thus, currents in M_{B1}/M_{B2} increase due to the current mirror scheme. The excess current, flowing in the tail resistor R_{tail} , results in lower voltage at V_B , then forcing the pair M_1/M_2 to work in the Class-C domain.

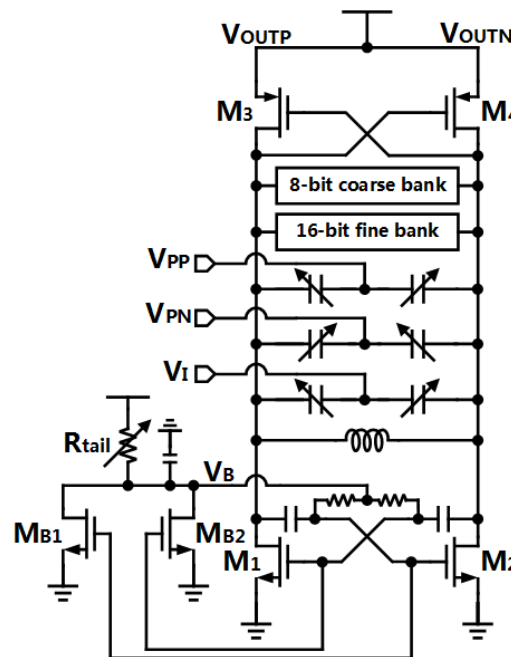


Figure 4. Structure of the proposed complementary cross-coupled Class-C VCO.

Different from [29], the current source is replaced by a tail resistor in the proposed VCO to eliminate the flicker noise generating from the tail transistor. Moreover, the voltage biasing scheme of the PMOS pairs M_3/M_4 is removed, since the DC gain of a operational amplifier (op-amp) could be limited seriously with low supply voltage. The removal of

this function would not have much influence on the Class-C operation, since the currents are reused in the pair M_1/M_2 and M_3/M_4 , and Class-C shaping of the current can flow in both M_1/M_2 and M_3/M_4 as well. To verify that, the current shapings are shown in Figure 5 with transient simulation.

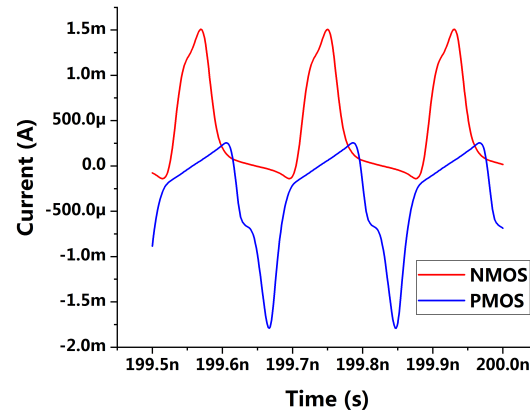


Figure 5. Current-shaping in the Class-C region.

Moreover, the sub-sampling loop of the PLL can lock at an arbitrary integer-N ratio of the reference frequency f_{REF} without an FLL [22], thus, the smallest tuning step of capacitor banks should be smaller than f_{REF} to allow ADPLL to select proper digital-control bits for the VCO. In order to ensure the desired large frequency tuning range (about 10%) as well, a 16-bit fine cap bank and an 8-bit coarse cap bank are proposed (Figure 4). Figure 6 captures the both tuning curves of the coarse bank and the fine bank.

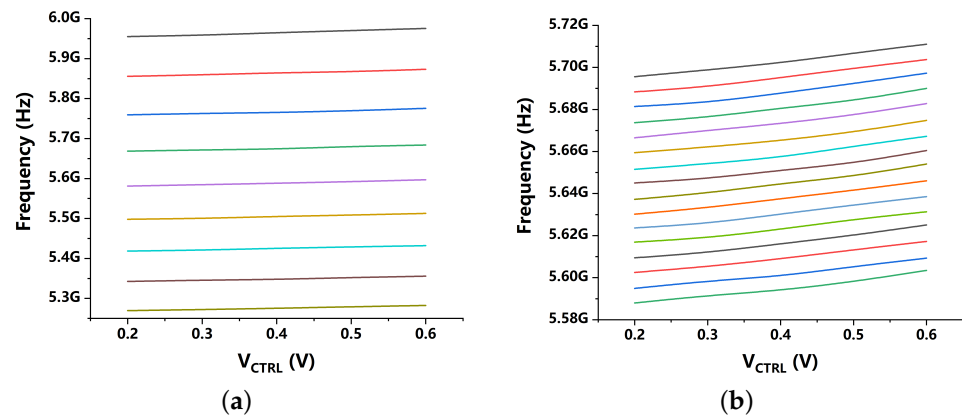


Figure 6. Tuning curves of the proposed VCO. (a) coarse-tuning curves, (b) fine-tuning curves.

3.2. Voltage-Controlled Buffer

A VCO buffer is necessary to isolate the VCO and the MSSF, because the sampling capacitor changes the load of the VCO during a complete sampling period if the MSSF is directly connected with outputs of the VCO, which causes considerable spur noise.

As in Equation (8), f_{BW} of the proposed SSPLL is determined by the P-path, thus, the bandwidth of the system cannot be adjusted by the pulser as in the conventional SSPLL. The only parameter left to play with in Equation (8) is the amplitude of the VCO buffer. The proposed structure is shown in Figure 7. The input voltage V_{CBUF} controls the current source M_5 and M_6 to change the drive capability of the self-biased inverters so as to adjust the output amplitude.

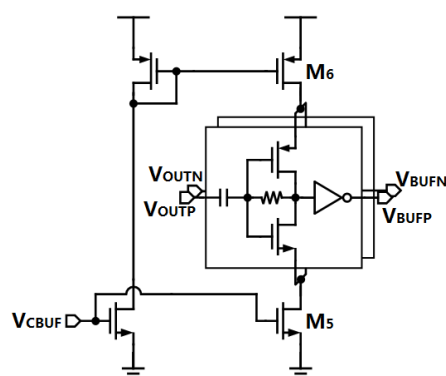


Figure 7. Structure of the proposed VCO buffer.

A series of transient simulations are carried out. Results capture the curve indicating the varying amplitudes as V_{CBUF} increases, as shown in Figure 8a. A Monte-Carlo simulation is carried out in Figure 8b to show the variation of the output common-mode voltages as the process changes.

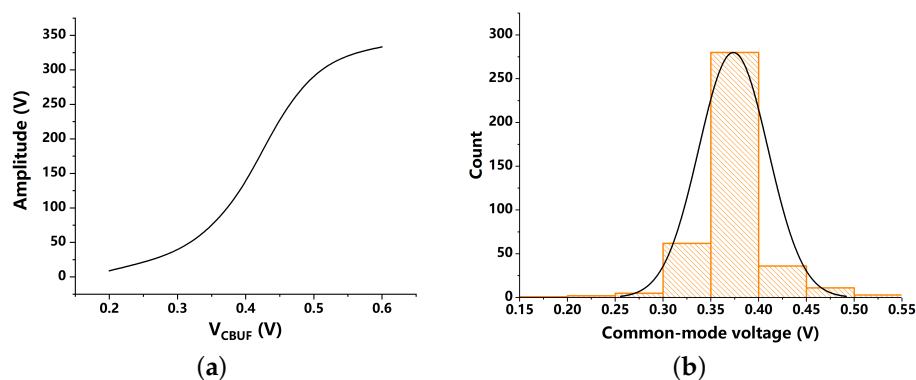


Figure 8. Transient simulation results of the proposed VCO buffer. (a) output amplitude variation, (b) output common-mode voltage variation.

3.3. Rail-to-Rail Sub-Sampling Charge Pump

According to the Monte-Carlo simulation results of the VCO buffer, it is noticed that the common-mode voltages have a large range changing from 0.15 V to 0.55 V which may let the input transistors of the traditional SSCP be switched off. In order to mitigate this serious problem, we propose a rail-to-rail SSCP as shown in Figure 9.

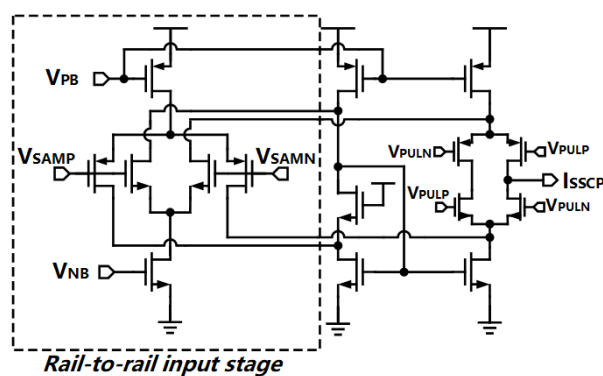


Figure 9. Structure of the proposed rail-to-rail SSCP.

The rail-to-rail input stage is adopted by the folded structure and the headrooms of the current mirror transistors are relieved, which is suitable for the low voltage design.

The transconductor g_m is simulated as the input common-mode voltage varies as shown in Figure 10. The complementary inputs of the SSCP ensure that at least one pair of transistors (NMOS or PMOS) are always be turned on. The value of g_m shows 635 μS and 800 μS as the output common-mode voltage of the VCO buffer appears at the worst cases of the variation. Although the variation of g_m is 38.5%, the noise contribution of the proposed SSCP is quite small, thus, this variation can be neglected (we will discuss this in the following section).

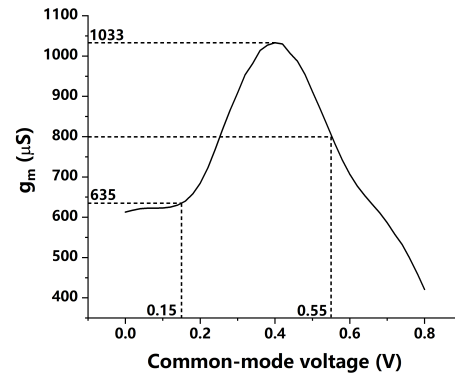


Figure 10. Variation of transconductor of the SSCP as input common-mode voltage changes.

4. Phase Noise Analysis

An s-domain phase noise model is shown in Figure 11. The noise contribution of the LPF is neglected.

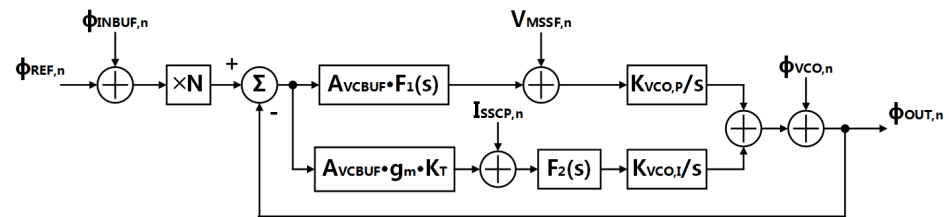


Figure 11. Phase noise linear model of the proposed SSPLL.

According to transfer function of each part, the whole system phase noise is given as:

$$\begin{aligned} \phi_{OUT,n}^2 = & \left(\phi_{REF,n}^2 + \phi_{INBUF,n}^2 \right) \cdot \left| \frac{N \cdot G_{SSPLL}(s)}{1 + G_{SSPLL}(s)} \right|^2 + V_{MSSF,n}^2 \cdot \left| \frac{1}{1 + G_{SSPLL}(s)} \cdot \frac{K_{VCO}}{s} \right|^2 \\ & + I_{SSCP,n}^2 \cdot \left| \frac{1}{1 + G_{SSPLL}(s)} \cdot \frac{K_{VCO}}{s^2 C_{int1}} \right|^2 + \phi_{VCO,n}^2 \cdot \left| \frac{1}{1 + G_{SSPLL}(s)} \right|^2 \end{aligned} \quad (9)$$

where $\phi_{REF,n}$, $\phi_{INBUF,n}$ and $\phi_{VCO,n}$ are the phase noise contribution from the reference clock, the input buffer and the VCO, respectively, $V_{MSSF,n}$ is the voltage noise from the MSSF, $I_{SSCP,n}$ is the current noise from the SSCP. Combining with the simulated noise from each part, the fitted phase noise at the output of the SSPLL system is shown in Figure 12. We find that the noise contribution from the SSCP (I-path) is much smaller than the noise from the MSSF (P-path), since the I-path gain $G_{IP}(s)$ is much smaller than the P-path gain $G_{PP}(s)$. Thus, compared with traditional SSPLL, the degraded noise feature of the SSCP cannot have much influence on the noise performance of the proposed dual path SSPLL. The calculated integrated RMS jitter in Figure 12 is 180 fs.

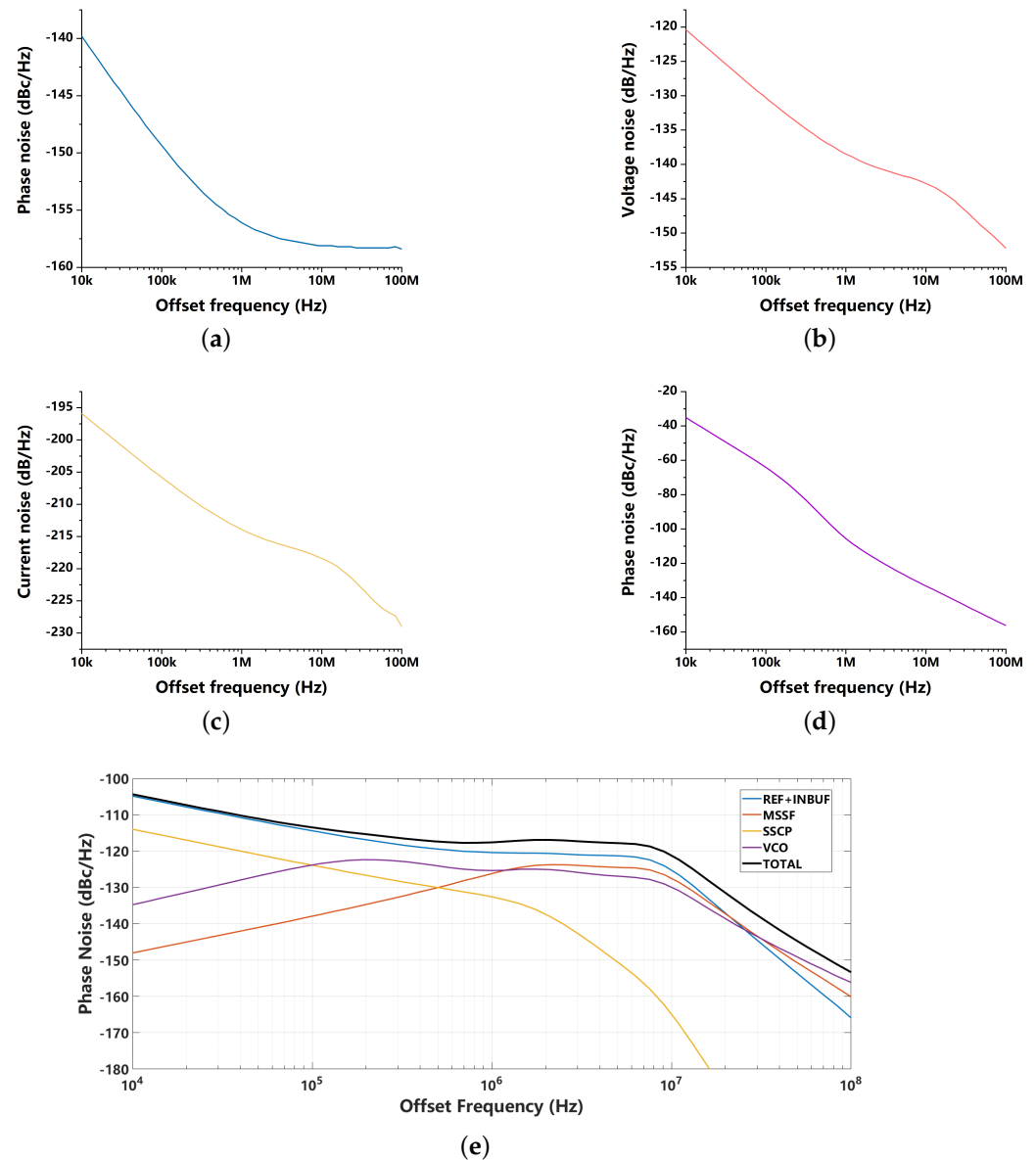


Figure 12. Fitted phase noise: (a) phase noise of the reference clock and the input buffer; (b) voltage noise of the MSSF; (c) current noise of the SSCP; (d) phase noise of the VCO; (e) phase noise of the SSPLL.

5. Measurement Results

The proposed low-voltage hybrid dual-path SSPLL is fabricated in 40-nm CMOS technology. The chip micrograph is shown in Figure 13 and the active core area is $450 \times 400 \mu\text{m}^2$. The power dissipation breakdown is also captured in Figure 13.

A Rohde & Schwarz FSWP50 phase noise analyzer and a Rohde & Schwarz FSW50 spectrum analyzer are used to test the phase noise and spur noise of the proposed SSPLL, respectively. The measured output frequency range is 5.3 to 5.9 GHz, thus, the central output frequency is 5.6 GHz. Figure 14 shows the phase noise and spur at the central frequency (divided by 2, at 2.8 GHz). The tested RMS integrated phase noise is 207.9 fs. The in-band phase noise at 1 MHz offset frequency is -125.9 dBc/Hz which is -119.9 dBc/Hz when the output frequency is referred at 5.6 GHz. Moreover, the tested spur is -51.8 dBc at central frequency as shown in Figure 14b.

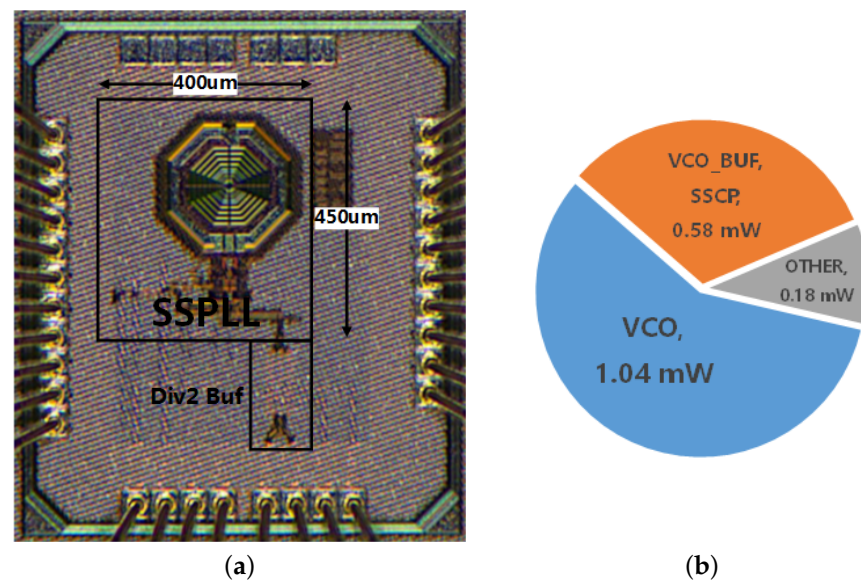


Figure 13. (a) chip micro-photo and (b) power dissipation breakdown.

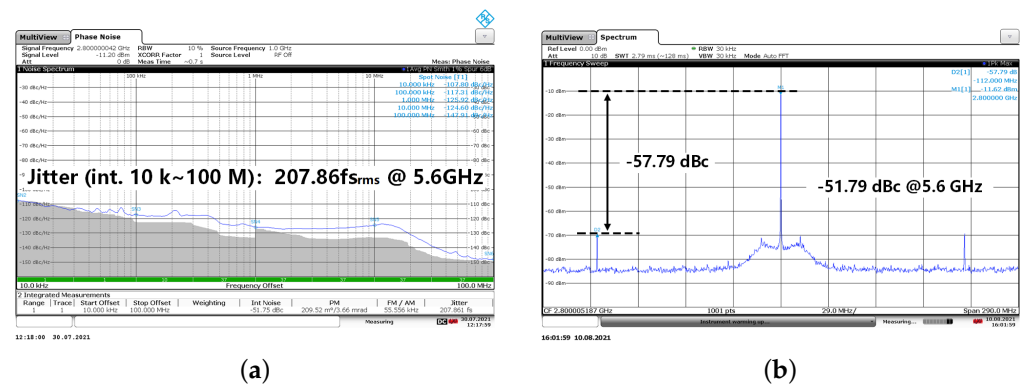


Figure 14. (a) phase noise and (b) spur noise at central output frequency (divided by 2).

Figure 15 shows the curves of tested phase noise covering the output frequency range from 5.3 GHz to 5.9 GHz. The largest integrated jitter appears at 5.5 GHz and the smallest integrated jitter shows at 5.7 GHz. Combining with the power consumption, the worst and the best FoM (from Equation (1)) of the proposed circuit are -249.8 dB and -251.6 dB, respectively.

Table 1 shows the results of this study compared with the results of prior art PLLs. The proposed SSPLL achieves good phase noise performance while achieving low power dissipation.

Table 1. Performance comparison.

	Tech. (nm)	Supply (V)	Out Freq. (GHz)	Ref. Freq. (MHz)	Ref. Spur (dBc)	RMS Jitter (fs)	Power (mW)	FoM (dB)
This work	40	0.8	5.6	112	-51.8	196.5 (10 k–100 M)	1.8	-251.6
[6]	65	0.9	6.8	106.25	-40	190 (10 k–100 M)	2.25	-251
[8]	65	0.45	2.4	10	-50.1	2800 (1 k–100 M)	0.265	-236.8
[15]	28	-	7.77	80	-66.4	82 (10 k–10 M)	14.7	-250
[23]	16	0.9/1.8	18	450	-	164 (1 k–10 M)	29.2	-241
[24]	65	1.2	5	50	-77	357 (10 k–10 M)	3.9	-243

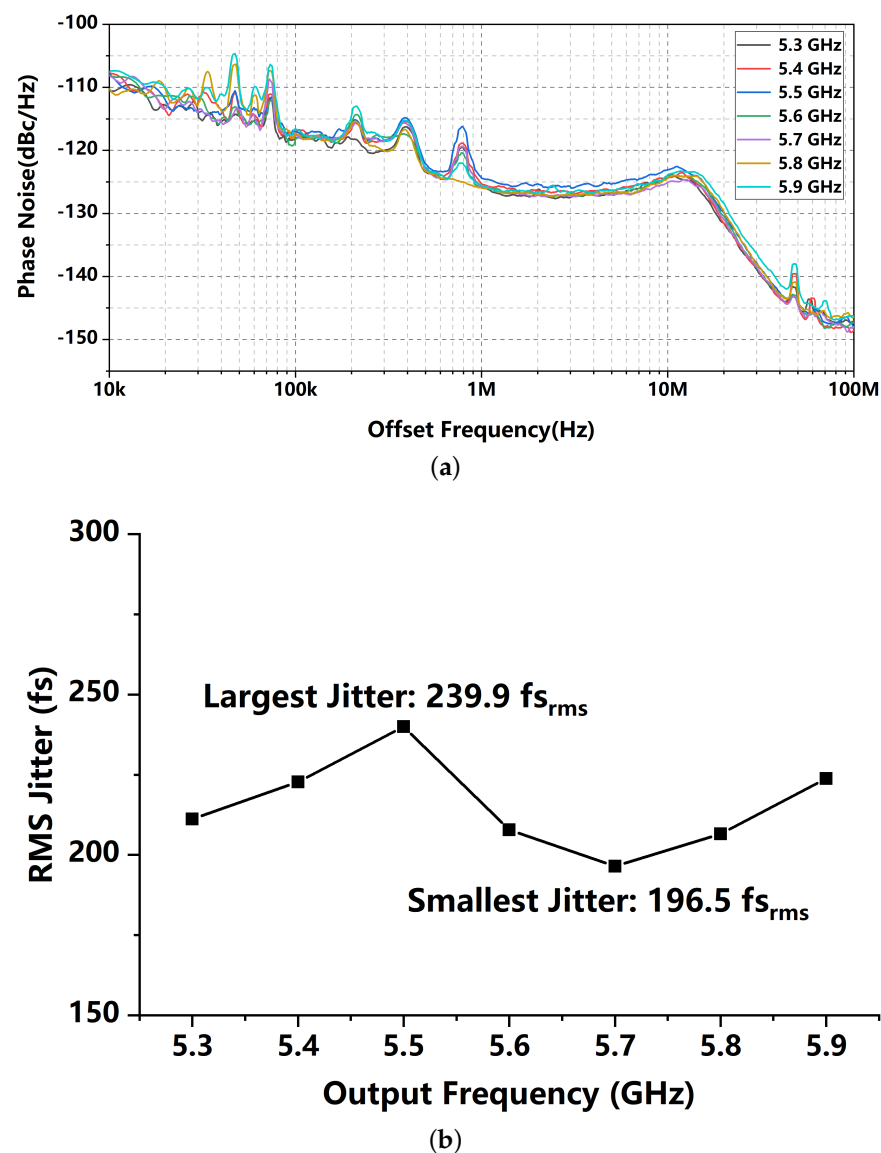


Figure 15. (a) phase noise curves and (b) integrated jitters covering the frequency range from 5.3 GHz to 5.9 GHz.

6. Conclusions

This paper proposes a hybrid dual path SSPLL, including a P-path and an I-path, with 0.8 V supply voltage which is fabricated in the 40-nm CMOS technology. A differential MSSF, replacing the SSCP, composed the P-path to avoid the degraded feature caused by the decreasing of the supply voltage. The I-path is built by a rail-to-rail SSCP to suppress the phase noise of the VCO and avoid the trouble of locking at the non-zero phase offset (as in type-I PLL). The measurement results indicate that the SSPLL can operate at the 5.3 to 5.9 GHz frequency range, 196.5 fs RMS integrated jitter and 1.8 mW power dissipation with -251.6 dB FoM. Compared with prior art PLLs, this SSPLL reaches a good phase noise performance with low power dissipation.

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