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A 0.6-μW Chopper Amplifier Using a Noise-Efficient DC Servo Loop and Squeezed-Inverter Stage for Power-Efficient Biopotential Sensing

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Abstract: To realize an ultra-low-power and low-noise instrumentation amplifier (IA) for neural and biopotential signal sensing, we investigate two design techniques. The first technique uses a noise-efficient DC servo loop (DSL), which has been shown to be a high noise contributor. The proposed approach offers several advantages: (i) both the electrode offset and the input offset are rejected, (ii) a large capacitor is not needed in the DSL, (iii) by removing the charge dividing effect, the input-referred noise (IRN) is reduced, (iv) the noise from the DSL is further reduced by the gain of the first stage and by the transconductance ratio, and (v) the proposed DSL allows interfacing with a squeezed-inverter (SQI) stage. The proposed technique reduces the noise from the DSL to 12.5% of the overall noise. The second technique is to optimize noise performance using an SQI stage. Because the SQI stage is biased at a saturation limit of $2V_{DSAT}$, the bias current can be increased to reduce noise while maintaining low power consumption. The challenge of handling the mismatch in the SQI stage is addressed using a shared common-mode feedback (CMFB) loop, which achieves a common-mode rejection ratio (CMRR) of 105 dB. Using the proposed technique, a capacitively-coupled chopper instrumentation amplifier (CCIA) was fabricated using a 0.18-μm CMOS process. The measured result of the CCIA shows a relatively low noise density of 88 nV/rtHz and an integrated noise of 1.5 μV_{rms}. These results correspond to a favorable noise efficiency factor (NEF) of 5.9 and a power efficiency factor (PEF) of 11.4.

Keywords: ultra-low power; instrumentation amplifier; body control; electrode offset; dc servo loop; input-referred noise

1. Introduction

Recently, there is a growing interest in wearable, portable, and personal health monitoring. By detecting abnormal health conditions during daily monitoring, this approach provides a new method of preventive healthcare. Monitoring human biopotential and neural signals is also important for early diagnosis and medical treatment [1]. Concerning the biopotential monitoring applications, sensors and their interfaces providing high-quality signals are of great importance. Besides, these sensor devices demand both long operating time and a compact form factor. A battery is widely used, however, it requires frequent battery recharging or replacement, and there is a limit in its size for some applications such as implantable sensors. To achieve a compact form factor by reducing the volume of the battery, low power consumption is in great demand for wearable and portable sensor devices.

Signals from humans have an amplitude of around 1 mV for an electrocardiogram (ECG) and from 10 to 100 μV for an electroencephalogram (EEG) over a frequency band from 0.5 to 150 Hz [2]. The local

field potential (LFP) has a typical amplitude of 1 mV over 1 to 200 Hz. These low-frequency signals must first be amplified before any signal processing can be applied. One issue with amplification is the overlap of these signals with 1/*f* noise. To mitigate the effect of 1/*f* noise, a chopping technique can be applied for instrumentation amplifiers (IAs) [3–12]. Another issue is the electrode offset voltage V_{EOS} generated at the tissue-electrode interface by electrochemical effects. To reject V_{EOS}, a DC servo loop (DSL) has been used in a capacitively-coupled chopper instrumentation amplifier (CCIA) [3]. This approach has the advantage of removing bulky external capacitors. However, the DSL achieves the V_{EOS} rejection by increased input-referred noise (IRN). The IRN $\overline{V_{n,in}^2}$ of a CCIA can be expressed as [3]

$$\overline{V_{n,in}^2} = \left(\frac{C_{in} + C_{fb} + C_{hp} + C_P}{C_{in}}\right)^2 \overline{V_{n,in,Gm}^2} \quad (1)$$

where $\overline{V_{n,in,Gm}^2}$ represents the input-referred noise of a transconductor. The C_{in}, C_{fb}, and C_P are the input, feedback, and parasitic capacitors that are connected to the input of the CCIA, respectively. The C_{hp} is the capacitor in the DSL which is used to create a high-pass corner to reject V_{EOS}. When a large C_{hp} is used, the result (1) shows that it increases the IRN by charge dividing, causing the DSL to be a high noise contributor; previous studies often neglected this important issue. For example, the IRN increases from 0.7 to 6.7 μV_{rms} [4] and from 2.8 to 4.7 μV_{rms} [6] when the DSL is enabled. Thus, in these cases, the DSL contributes 89.5% [4] and 40.4% [6] of the overall noise. The increased noise significantly degrades both the noise efficiency factor (NEF) [7] and the power efficiency factor (PEF) [10].

Several methods have been proposed to improve the DSL. In [5], a digitally-assisted foreground calibration is used to allow the DSL to handle residual offset. In [7], a dual DSL which consists of coarse and fine DSLs reduces the value of C_{hp} from 670 to 100 fF. In [8], the output of a DSL is connected to the cascode branch of a transconductor to mitigate the charge dividing effect. Nevertheless, these CCIAs consume 3.48 µW [7] and 2.13 µW [8], which results in relatively high PEFs of 18.3 and 10.5 (over a 10-kHz bandwidth), respectively. The results indicate that previous work suffers from high noise contribution from the DSL and achieves a relatively low noise-power efficiency.

In this paper, we investigate two design techniques to realize a 0.6-µW chopper amplifier with a PEF of 11.4 over a 200-Hz bandwidth. The first technique optimizes noise performance using a squeezed-inverter (SQI) stage. Because the SQI stage allows for the reduction of the supply voltage to a saturation limit of $2V_{DSAT}$, its bias current can be increased to reduce noise. The second technique is to reduce the relatively high noise from the DSL. Unlike conventional DSLs, which are connected to the input of the CCIA through C_{hp}, we apply the output of the DSL to the body of a transconductor. The proposed approach not only removes the charge dividing effect but also reduces the noise by the transconductance ratio and the open-loop gain. Furthermore, this approach solves the problem of interfacing the DSL to the SQI stage, which has a different supply voltage. Using this approach, the noise contribution of the DSL is reduced to 12.5%. The fabricated CCIA achieves a relatively low noise density of 88 nV/rtHz with an integrated noise of 1.5 μV_{rms}. The result corresponds to a favorable NEF of 5.9 and a PEF of 11.4 by consuming only 0.68 µW, demonstrating a power-efficient low-noise amplifier.

2. Design

Figure 1 shows the schematic of the proposed CCIA. The input transconductor G_{m1} is realized using an SQI stage biased at $V_{DD,L}$ = 0.2 V. The transconductors G_{m2}, G_{m3}, and G_{m4} are folded-cascode, two-stage opamp, and common source stages biased at $V_{DD,H}$ = 0.8 V, respectively. Transconductor G_{m3} is used as the integrator in the DSL. We consider the input offset voltages V_{OSi} (i = 1 to 3) for G_{mi}. The input V_{in} is up-modulated to chopping frequency f_{CH} by the chopper CH_{in}, then down-modulated to baseband by CH_{out}. The common-mode (CM) voltage $V_{CM2} = V_{DD,H}/2$, which bypasses the chopper CH_{out}, is used to bias G_{m2} through pseudo-resistors $R_{b1,2}$. A Miller capacitor

$C_{m1,2}$ is used for stability. The mid-band gain of the CCIA is defined by input capacitor $C_{in1,2}$ and feedback capacitor $C_{fb1,2}$. The current consumptions of G_{m1}, G_{m2}, G_{m3}, and G_{m4} are 1.61 µA, 60 nA, 210 nA, and 80 nA, respectively.

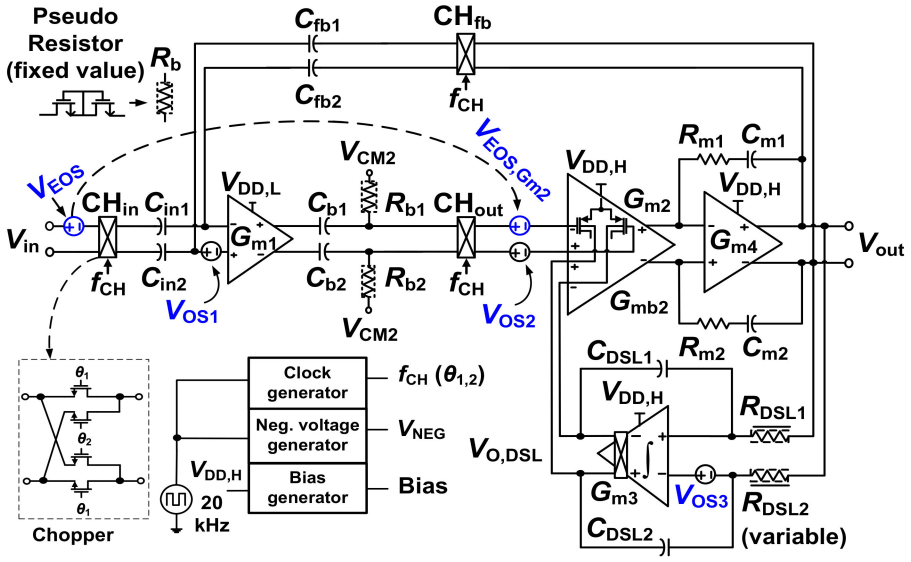


Figure 1. Schematic of the proposed capacitively-coupled chopper instrumentation amplifier (CCIA) using body-controlled DC servo loop (DSL). $C_{in1,2}$ = 4 pF, $C_{fb1,2}$ = 40 fF, $C_{b1,2}$ = 3 pF, $C_{m1,2}$ = 4 pF, $R_{m1,2}$ = 4 MΩ, and $C_{DSL1,2}$ = 5 pF.

Although the SQI stage provides low noise operation, interfacing it with the DSL poses a challenge. This is because the input range of the SQI stage is limited by $V_{DD,L}$ = 0.2 V, while the DSL senses the output V_{out} with a wide swing. We believe that this is one reason why previous studies do not implement a DSL [10]. To solve this problem, we modify the conventional DSL by connecting the output $V_{O,DSL}$ of the DSL to G_{m2} using the body terminal. We note that this approach is different from the previous approach wherein the output of the DSL is connected to the virtual ground node of the input transconductor through C_{hp} [3,4,6]. The proposed approach offers several advantages: (1) because the proposed DSL uses G_{m2} instead of C_{hp}, the charge dividing effect is removed and noise from the DSL is reduced, (2) the noise from DSL is further reduced by the open-loop voltage gain A_{V1} of G_{m1} as well as by the square of the transconductance ratio, and (3) by rejecting both V_{EOS} and V_{OS2}, output offset is suppressed.

Figure 2 shows the simplified model of the proposed CCIA. Offset voltage V_{OS1} creates an output ripple due to finite amplifier bandwidth. The amplitude of the output ripple can be expressed as $V_{out,ripple} = (V_{OS1}A_{V1}G_{m2})/(2C_{m1,2}f_{CH})$ [4]. To suppress this ripple, we use capacitors $C_{b1,2}$ in front of CH_{out}. Because V_{OS1} is blocked by $C_{b1,2}$, the residual ripple appearing at f_{CH} can be neglected. Both V_{OS2} and V_{EOS} create output offset $V_{out,OS}$ at the output. The rejection of V_{EOS} and V_{OS2} is explained as follows: When V_{EOS} is up-modulated to f_{CH}, it is partially suppressed by $C_{fb1,2}$ at the virtual input node of G_{m1}. The residual offset $V_{EOS,\omega}$ existing at f_{CH} can be expressed as $V_{EOS,\omega} = V_{EOS}\, C_{in1,2}/(A_V C_{fb1.2})$, where A_V is the overall open-loop voltage gain of the amplifier. This residual offset is amplified by A_{V1}. Simulation results show that A_{V1} is 29 dB with a low-pass corner of 954 kHz. Additionally, a high-pass corner frequency of 1 Hz is created by $C_{in1,2}$ and bias resistor $R_{1,2}$ inside G_{m1} (See Figure 3). Then, $V_{EOS,\omega}$ is down-converted by CH_{out} to create an offset voltage $V_{EOS,Gm2} = A_{V1}V_{EOS,\omega}$ at the input of G_{m2}. We observe the sum of offset voltages, $V_{OS2,tot} = V_{OS2} + V_{EOS,Gm2}$, at the input of G_{m2}. Transconductors G_{m2} and G_{m4} have a low-pass characteristic with a 3-dB frequency of about 10 Hz, and $V_{OS2,tot}$ generates offset current $I_{O,Gm2}$ at the output of G_{m2}. The offset current is integrated by G_{m4}, which creates the output offset $V_{out,OS}$. This is sensed by the DSL, then $V_{O,DSL}$ is applied to the body of the differential pair of G_{m2}. The generated current $I_{O,DSL} = G_{mb2}V_{O,DSL}$

compensates $I_{O,Gm2}$. The DSL continues integrating, and $V_{out,OS}$ is suppressed by the amount $1/LG(s)$, where the loop gain LG can be expressed as $LG(s) = g_{mb1,2}/(s^2 C_{m1,2} R_{DSL1,2} C_{DSL1,2})$.

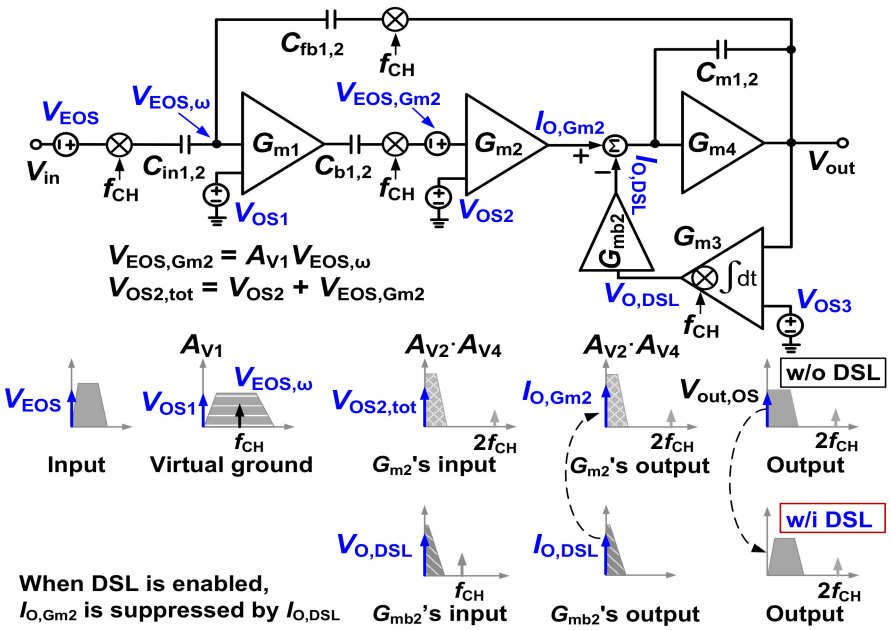


Figure 2. A simplified model of the proposed CCIA.

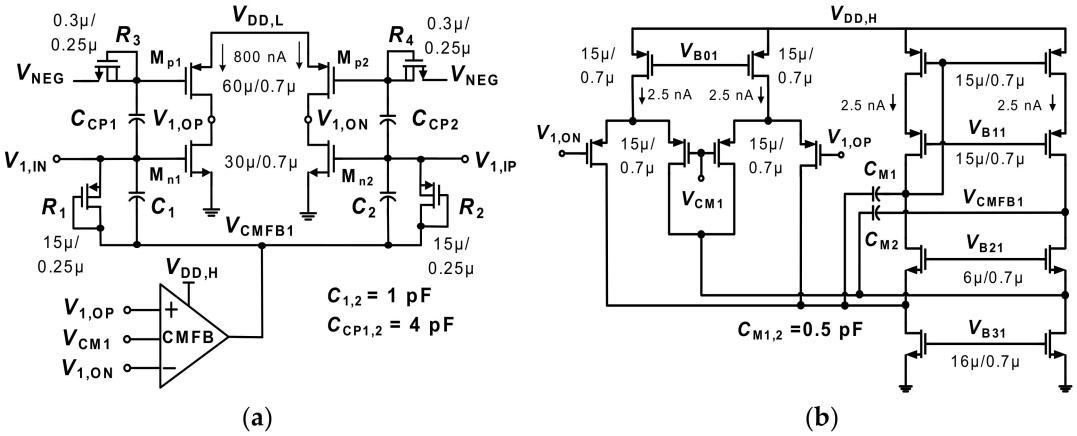


Figure 3. (**a**) Schematic of the squeezed-inverter stage using the shared common-mode feedback (CMFB). V_{CM1} = 0.1 V, V_{NEG} = −0.18 V, and V_{CMFB1} = 0.098 V (nominal value). (**b**) Schematic of the proposed CMFB circuit. V_{B01} = 0.57 V, V_{B11} = 0.28 V, V_{B21} = 0.49 V, and V_{B31} = 0.23 V.

The selection of f_{CH} involves considering the various tradeoff between input impedance, output ripple, and residual offset. $V_{out,ripple}$ can be reduced by increasing f_{CH}. One drawback of increasing f_{CH} is that it reduces the input impedance Z_{in}. Besides, there is greater charge injection and clock feed-through during the switching of the chopper [13]. To determine suitable f_{CH}, we perform periodic steady-state (PSS) and periodic noise analysis (PNOISE) simulations. Considering the tradeoff and the amplifier bandwidth, we select f_{CH} = 10 kHz.

3. Circuit Implementation

Figure 3a shows a schematic of the G_{m1} implemented using an SQI stage [10] modified to improve the common-mode rejection ratio (CMRR). The transistors in the SQI stage are biased in the subthreshold region using $V_{DD,L}$ = 0.2 V. The IRN of the G_{m1} can be expressed as

$$\overline{V^2_{n,in,Gm1}} = \frac{8kT}{g_{m,n} + g_{m,p}} \cong \frac{4kTnU_{th}}{I_{DC}} \quad (2)$$

where I_{DC} = 800 nA is the bias current, $g_{m,n}$ and $g_{m,p}$ are the transconductance of M_{n1} and M_{p1}, respectively, U_{th} = 26 mV is the thermal voltage, and n = 1.5 is the subthreshold factor [9]. The SQI stage reduces the noise by increasing I_{DC}. Because the supply voltage is reduced to a saturation limit of $2V_{DSAT}$~0.2 V, both low noise and low power operation can be achieved.

To generate I_{DC}, bias voltages beyond supply rails are used for M_{n1} and M_{p1}. The bias voltage for M_{n1} is pushed above the supply rail by using a common-mode feedback (CMFB) loop. The bias voltage V_{NEG} for M_{p1} is pushed below the ground by using a negative voltage generator, which is applied to the gate of M_{p1} through a pseudo-resistor $R_{3,4}$. Because the transistors work in the subthreshold region without a tail current source, balancing the bias current for the input pair is challenging. To address this, we use a shared CMFB loop. Figure 3b shows the schematic of the CMFB circuit for the SQI stage. It monitors the CM voltage of outputs $V_{1,ON}$ and $V_{1,OP}$. Then, the output V_{CMFB1} of the CMFB circuit is applied to the gate of $M_{n1,,2}$ through pseudo-resistors $R_{1,2}$. Because any change in V_{CMFB1} affects the input pair by the same amount, this approach provides balanced bias currents for the SQI stage.

Figure 4a shows the schematic of the negative voltage generator. It consists of a 1/10-scaled current replica, two switched-capacitor (SC) paths, a level shifter, and a folded-cascode (FC) amplifier. The SC network consists of the main path and a low noise replica. The FC amplifier and the main SC path generate the bias voltage V_G for M_{1B} by regulating V_D to $V_{DD,L}/2$. The replica path is responsible for copying V_G to generate V_{NEG}. The current mirror defines an 80 nA through M_{1B}, which is the 1/10-scaled current of $M_{p1,2}$. The negative voltage generator draws 18 nA from $V_{DD,H}$ and 80 nA from $V_{DD,L}$. Figure 4b shows the statistical distribution of V_{NEG} obtained from Monte Carlo simulations. The result shows an average value of −177.3 mV with a standard deviation of 12.4 mV.

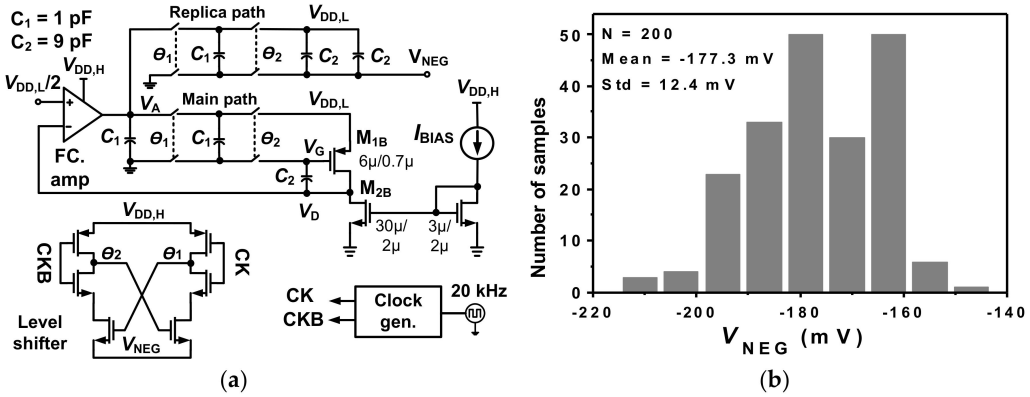
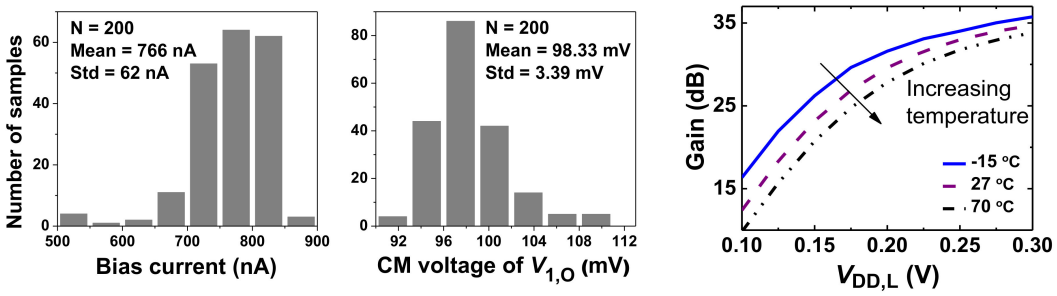


Figure 4. (**a**) Schematic of the negative voltage generator, (**b**) statistical distribution of V_{NEG}.

Figure 5a,b shows the statistical distributions of the bias current and the output CM voltage obtained from 200 Monte Carlo simulations. Both random mismatch and process variations are considered. The result shows an average bias current of 766 nA with a standard deviation of 62 nA. The output CM voltage shows an average value of 98.3 mV with a standard deviation of 3.4 mV. Compared to previous work which uses two separate CMFB loops [10], the proposed approach increases the CMRR from 85 to 105 dB. This indicates that the proposed shared CMFB loop is effective in improving CMRR. Figure 5c shows the gain of the SQI stage depending on temperatures as a function

of $V_{DD,L}$. Because the transistors are biased in the subthreshold region, the increased threshold voltage with temperature reduces the gain [10]. We note that the SQI stage still provides a gain >20 dB when $V_{DD,L}$ is reduced to 0.15 V at 70 °C. At room temperature, the SQI stage achieves a gain of 29 dB with $V_{DD,L}$ = 0.2 V.



(**a**) (**b**) (**c**)

Figure 5. Monte Carlo simulation results for the (**a**) bias current, (**b**) output common-mode (CM) voltage of the squeezed-inverter (SQI) stage. (**c**) simulated gain of the SQI stage depending on $V_{DD,L}$ and temperature.

Figure 6 shows a schematic of G_{m2} with the body-controlled DSL. The bias current of G_{m2} is 40 nA. The CMFB circuit (not shown) generates the output V_{CMFB2} using a 20 nA bias current (See Table 1 for the power consumed by the CMFB circuits). The overall current of G_{m2} is only 60 nA. Figure 7a shows a schematic of the DSL. The $R_{DSL1,2}$ and $C_{DSL1,2}$ are the resistors and capacitors in the DSL, respectively. $R_{DSL1,2}$ is a variable pseudo-resistor controlled by V_{PR}, which is realized by cascading floating PMOS transistors. The input of G_{m3} is associated with offset V_{OS3}. Voltage V_{OS3} can disturb V_{out} of the CCIA similarly to other offsets (V_{OS1}, V_{OS2}, $V_{EOS,Gm2}$). To reduce the effect of V_{OS3}, two choppers, CH_{D1} and CH_{D2}, are added to the integrator. Because the bandwidth of the integrator is relatively narrow (~30 mHz), V_{OS3} is up-modulated to the outside of the integrator's bandwidth by CH_{D2}. Figure 7b shows a schematic of the two-stage opamp for G_{m3}. The first stage is biased using 5 nA. The second stage is biased at 200 nA for enhanced swing. The CMFB circuit generates V_{CMFB3} using a 5 nA bias current. The overall current is 210 nA.

Table 1. Power breakdown.

Block	Components	Current (nA)	Voltage (V)
G_{m1} (SQI stage)	Input pair	1600	0.2
	CMFB	10	0.8
G_{m2} (Folded-cascode)	Input pair	20	0.8
	Cascode branch + CMFB	40	0.8
G_{m3} (Two-stage opamp)	Input pair	5	0.8
	Common source + CMFB	205	0.8
G_{m4} (Common-source)	Input pair	80	0.8
Bias circuits	Current mirror	80	0.2
	Bias generators	65.5	0.8
Total power		676.4 nW	

The transfer function of the DSL has a low-pass characteristic for V_{out}. It can be expressed as $-g_{mb1,2}/(sR_{DSL1,2}C_{DSL1,2})$, where $g_{mb1,2}$ is the body transconductance integrated into G_{m2}. Within the

feedback loop, the DSL creates a high-pass corner to reject V_{EOS}. Using the condition $C_{fb1,2} << C_{in1,2}$, the transfer function of the CCIA can be expressed as

$$H(s) \cong -\frac{A_{V1}g_{m1,2}}{C_{m1,2}} \frac{s}{\left(s+\eta\omega_{ugb}/\beta A_{V1}\right)\left(s+\beta A_{V1}g_{m1,2}/C_{m1,2}\right)} \quad (3)$$

where $g_{m1,2}$ is the transconductance of the input pair of the G_{m2}, $\eta = (g_{mb1,2}/g_{m1,2}) \approx 0.25$, $\omega_{ugb} = 2\pi f_{ugb} = 1/(R_{DSL1,2}C_{DSL1,2})$ is the unity-gain frequency of the integrator, and $\beta = C_{fb1,2}/C_{in1,2}$ is the feedback factor. Using (2), we obtain a high-pass corner frequency $f_{hp} = (\eta/\beta A_{V1})\, f_{ugb}$.

Because f_{hp} created by the DSL depends on the value of pseudo-resistor, we investigate the variability of $R_{DSL1,2}$. Figure 8a shows the value of the $R_{DSL1,2}$ as a function of temperature for various V_{PR}. The resistance increases with V_{PR} while it decreases with temperature. Figure 8b shows the statistical distribution of the resistance obtained from Monte Carlo simulations at 27 °C and V_{PR} = 0.4 V. The result shows that the average value of $R_{DSL1,2}$ is 34.1 GΩ with a standard deviation of 1.6 GΩ. Figure 9 shows a schematic of the bias generator. It consists of a constant-g_m current reference and six branches to generate the bias voltages for the amplifier. Overall current consumption is 47.5 nA.

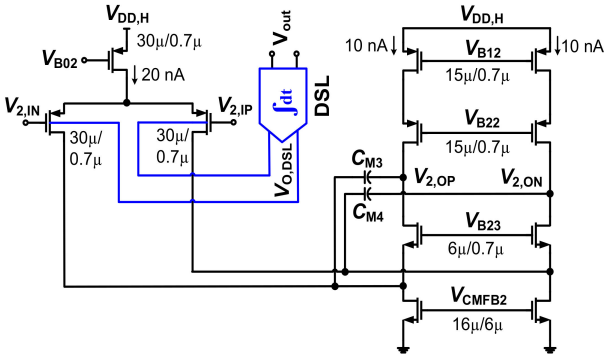


Figure 6. Schematic of transconductor G_{m2} with body-controlled DSL. $C_{M3,4}$ = 0.5 pF. $V_{B02} = V_{B12}$ = 0.52 V, V_{B22} = 0.18 V, V_{B23} = 0.6 V, and V_{CMFB2} = 0.28 V (nominal value).

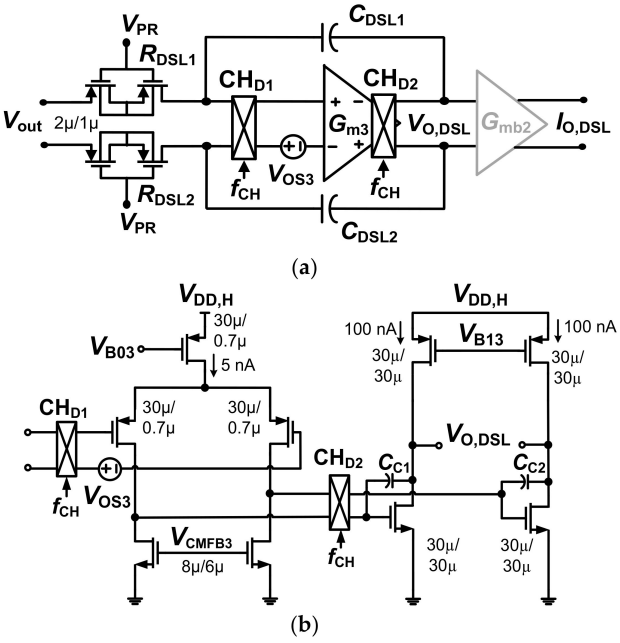


Figure 7. (**a**) schematic of the DSL and (**b**) schematic of the two-stage opamp G_{m3}. $C_{DSL1,2}$ = 5 pF, $C_{C1,2}$ = 0.5 pF. V_{B03} = 0.57 V, V_{B13} = 0.34 V, and V_{CMFB3} = 0.29 V (nominal value).

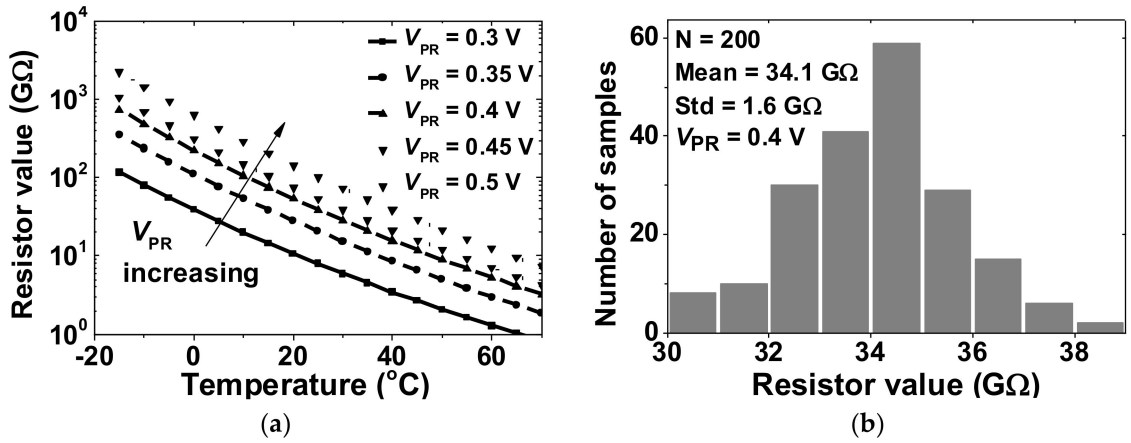


Figure 8. (**a**) simulated value of the pseudo-resistor as a function of temperature for various V_{PR} and (**b**) Monte Carlo simulation result of the pseudo resistor value at V_{PR} = 0.4 V.

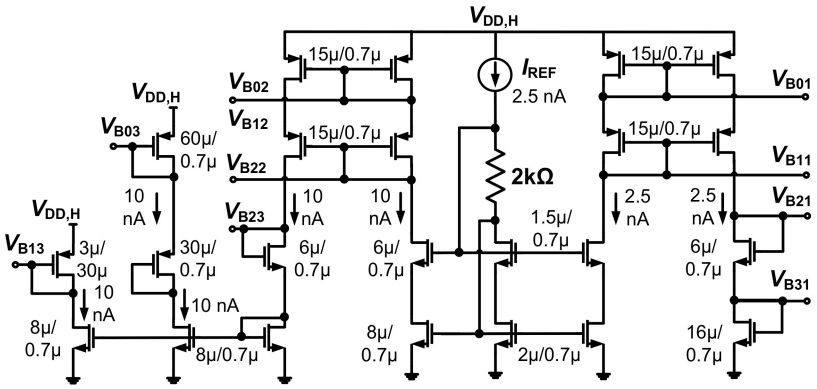


Figure 9. Schematic of the bias generator.

The proposed CCIA uses a narrow margin for the stacked transistors in the SQI stage. Therefore, we investigate the effect of supply and temperature on the performance of the amplifier. Figure 10 shows the effect of $V_{DD,L}$ on the bias current (SQI stage only), noise, and bandwidth. When $V_{DD,L}$ is increased, it is tracked by V_D and V_G in the negative generator, which increases V_{NEG} to keep the bias current. When $V_{DD,L}$ is reduced below 0.15 V, the two stacked transistors are driven in the deep subthreshold region, which reduces the current and the gain. We note that the CCIA still operates with an integrated noise < 1.5 μV_{rms} when $V_{DD,L}$ is reduced to 0.15 V. The amplifier bandwidth gradually increases with $V_{DD,L}$, which agrees with the previous result [10].

Because $V_{DD,L}$ is relatively low, an external electromagnetic interference can affect the sensor interface. In the proposed CCIA, the differential input signal V_{IN} is up-modulated to f_{CH} while the CM signal is not chopped. Therefore, chopping provides some means of rejection of external interference. In the case when the external interference exists at around f_{CH}, it can affect the CCIA, however, this is well beyond the amplifier bandwidth (1–200 Hz). When the CCIA is used for the sensor readout, a theoretical input range calculated using a gain of 40 dB and the maximum output swing of 0.8 V_{pp} is 8 mV_{pp}, which agrees with the measured value of 6 mV. Because the input is capacitively-coupled, it provides a relatively high DC blocking allowed by the voltage rating of $C_{in1,2}$.

Figure 11 shows the effect of temperature on the amplifier. The bias current increases with the temperature as expected from the constant-g_m current reference, which increases V_{NEG}. The two temperature-dependent parameters of the subthreshold current are mobility and the threshold voltage [14]. The increased threshold voltage with temperature reduces the gain A_v. The bandwidth can be expressed as $BW = \omega_p(1+\beta A_v)$, where ω_p is the 3-dB frequency and β is the feedback factor.

Furthermore, the increased temperature reduces the bandwidth [15,16]. The amplifier achieves an integrated noise of less than 2 μV_{rms} over the temperature range from −5 °C to 45 °C.

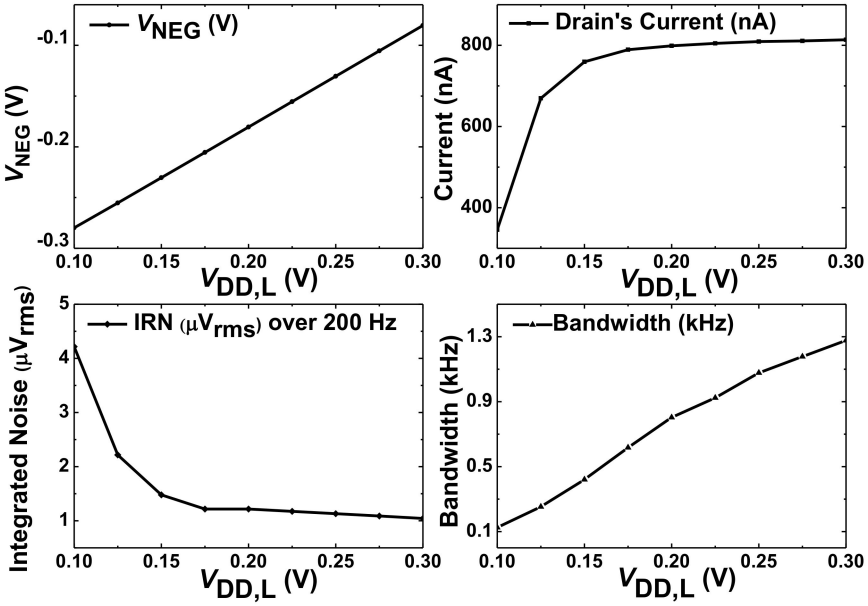


Figure 10. Simulated results showing the effect of $V_{DD,L}$ on the noise and bandwidth of the proposed CCIA.

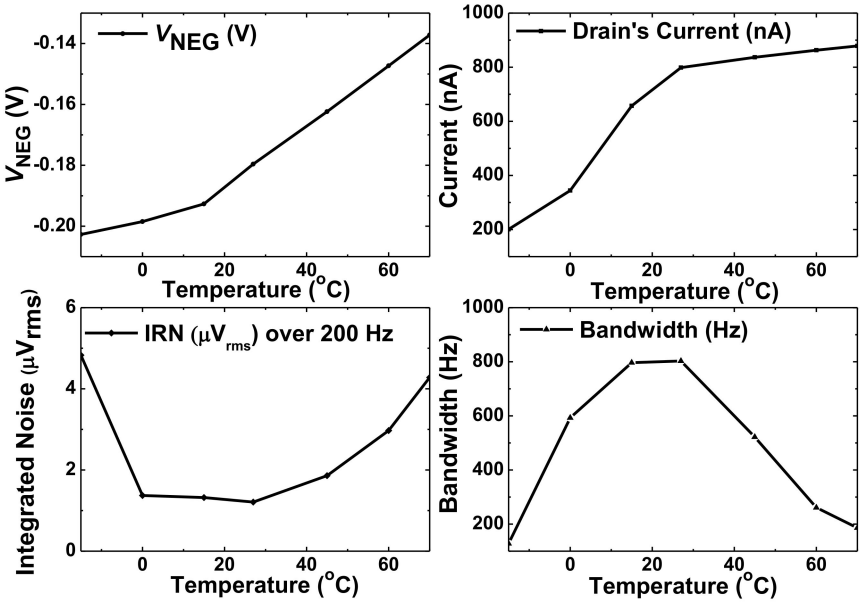


Figure 11. Simulated bias current, noise, and bandwidth depending on temperature.

The IRN of the CCIA, $\overline{V_{n,in}^2}$, can be expressed as

$$\begin{aligned}\overline{V_{n,in}^2} &= \left(\frac{C_{tot}}{C_{in1,2}}\right)^2\left[\overline{V_{n,in,Gm1}^2} + \frac{1}{A_{V1}}\left\{\overline{V_{n,in,Gm2}^2} + \overline{V_{n,out,DSL}^2}\left(\frac{g_{mb1,2}}{g_{m1,2}}\right)^2\right\}\right] \\ &= \left(\frac{C_{tot}}{C_{in1,2}}\right)^2\left[\frac{4kTnU_{th}}{I_{DC}} + \frac{8kTn}{A_{V1}g_{m1,2}}\left(1+\frac{g_{m3,4}+g_{m9,10}}{g_{m1,2}}\right) + \frac{2}{A_{V1}}\left(\frac{g_{mb1,2}}{g_{m1,2}}\right)^2\left\{\left(8kTnR_{DSL1,2} + \overline{V_{n,in,OTA}^2}\right)\left(\frac{1}{sR_{DSL1,2}C_{DSL1,2}}\right)^2\right\}\right]\end{aligned} \quad (4)$$

where $C_{tot} = C_{in1,2} + C_{fb1,2} + C_p$, $\overline{V^2_{n,in,Gm1}}$ and $\overline{V^2_{n,in,Gm2}}$ are the input-referred noise of G_{m1} and G_{m2}, respectively, $\overline{V^2_{n,out,DSL}}$ is the output-referred noise of the DSL, and g_{mi} represents the transconductance of the transistors in G_{m2}. The noise from the DSL includes the thermal noise of $R_{DSL1,2}$ and the noise $\overline{V^2_{n,in,OTA}}$ = 1.8 nV/√Hz of the two-stage opamp. We note that $\overline{V^2_{n,out,DSL}}$ is not only multiplied by $(g_{mb1,2}/g_{m1,2})^2 << 1$, but is also reduced by A_{V1} = 29 dB. Using the values $g_{m1,2}$ = 0.7 µS, $g_{m3,4}$ = 0.35 µS, $g_{m9,10}$ = 0.7 µS, $C_{in1,2}$ = 4 pF, $C_{fb1,2}$ = 40 fF, and C_p = 66.5 fF, we obtain $\overline{V^2_{n,in}}$ = 84.2 nV/√Hz. Using the shot noise model [10], we obtain a similar value for $\overline{V^2_{n,in}}$. Over the signal bandwidth of 200 Hz, the integrated noise contributions from G_{m1}, G_{m2}, DSL, and the other blocks are 44.9%, 39.1%, 12.5%, and 3.5%, respectively.

4. Measured Results

Figure 12 shows a microphotograph of the CCIA fabricated using a 180-nm CMOS process. The core area is 0.19 mm^2. The supply voltages $V_{DD,L}$ and $V_{DD,H}$ are generated using external power supplies. Figure 13 shows the measured frequency response of the CCIA. The result shows a mid-band gain of 40 dB with a 3-dB bandwidth of 800 Hz. The high-pass corner f_{hp} was successfully created using the proposed DSL and varies from 0.36 to 2.4 Hz when V_{PR} is changed from 0.68 to 0.35 V. Figure 14 shows that the measured low-frequency CMRR > 105 dB. The power supply rejection ratios (PSRRs) measured at $V_{DD,L}$ and $V_{DD,H}$ show that low-frequency $PSRR_L$ > 80 dB and $PSRR_H$ > 75 dB, respectively.

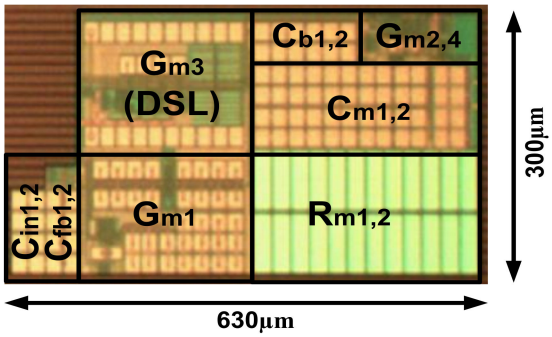


Figure 12. Chip microphotograph of the proposed CCIA.

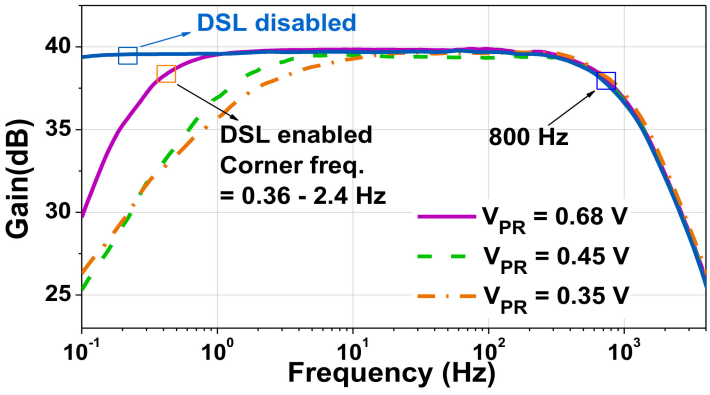


Figure 13. The measured frequency response.

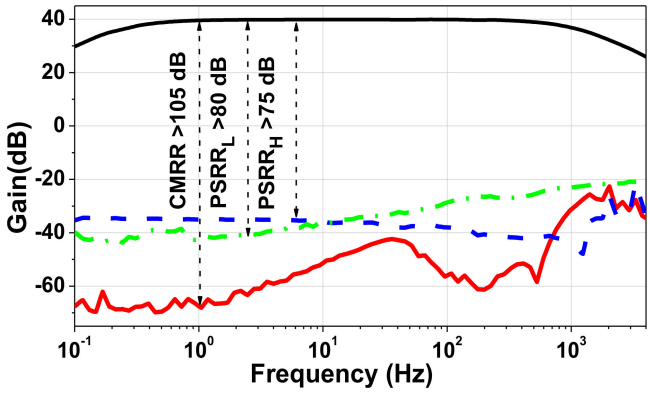


Figure 14. Measured CMRR and power supply rejection ratio (PSRR) as a function of frequency.

Figure 15 shows the measured noise spectral density. The input-referred noise density is 88 nV/rtHz, which is slightly higher than the calculated value of 84.2 nV/rtHz. When the DSL is enabled, the noise integrated from 1 to 200 Hz increases from 1.3 to 1.5 μV_{rms}. We note that the noise contribution from the DSL is just 12.5%, which is much lower than the previous results of 89.5% [4] and 40.4% [6]. Figure 16 shows the measured output of the CCIA for prerecorded human EEG (~100 µV) and ECG (~1 mV) input signals [17]. Table 1 shows the power breakdown of the proposed CCIA.

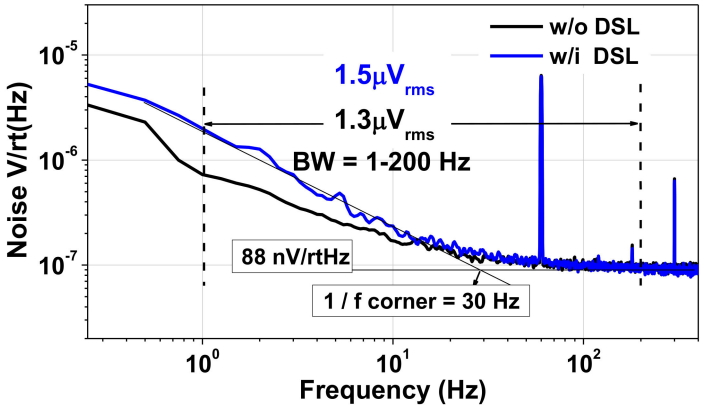


Figure 15. Measured input-referred noise voltage spectral density.

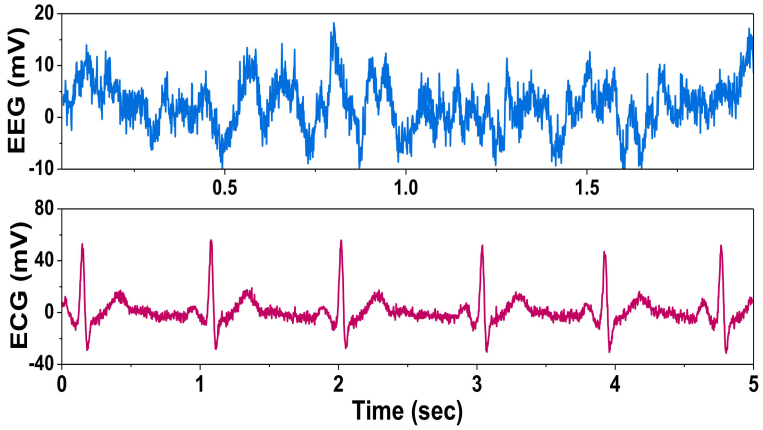


Figure 16. Measured output of the CCIA.

Table 2 shows a performance comparison with the state of the art. The tradeoff between the noise and power can be evaluated using PEF as

$$\mathrm{PEF} = V_{\mathrm{ni,\,rms}}^2 \frac{2P_{\mathrm{DC}}}{\pi U_{\mathrm{th}} 4kT \cdot BW} = \mathrm{NEF}^2 \cdot V_{\mathrm{DD}} \tag{5}$$

where $V_{\mathrm{ni,rms}}$ is the input-referred root-mean-square (rms) noise voltage, P_{DC} is the power consumption, and BW is the amplifier bandwidth. The previous approaches [4,7,12] use relatively-high currents to reduce noise. Because a high supply voltage $V_{\mathrm{DD}} > 1$ V is used except for in [6], the large power consumption >1.8 µW leads to a relatively high PEF. By using the SQI stage with an ultra-low voltage, the proposed CCIA achieves a competitive noise performance of 1.5 μV_{rms} at a relatively low power of 0.61 µW (0.68 µW including bias generators). Our work achieves a good PEF of 10.2 (11.4 with bias generators) which is the lowest of the work shown in Table 2. Besides, the proposed CCIA has the lowest noise contribution of 12.5% from the DSL. The work in [10] achieves a good NEF/PEF = 2.1/1.6, however, their design does not include a DSL. Therefore, direct comparison is difficult. Although the dual power approach requires additional buck converter, a high-efficiency (>80%) converter consuming sub-nW can be used for voltage step-down [18,19].

Table 2. Performance summary and comparison.

	[3]	[4]	[6]	[7]	[12]	**This Work**
Power (µW)	2.0	1.8	0.6	3.48	2.8	0.61/0.68 †
Supply (V)	1.8	1.0	0.5	1.2	1.2	0.2/0.8
Current (µA)	1.1	1.8	1.2	2.9	2.3	1.6/0.36 1.68 †/0.43 †
Input cap. (pF)	15	12	12	20	1.0	4
Gain (dB)	41	40	40	40	25.7	40
CMRR (dB)	100	134	106	85	78	105
Noise (μV_{rms})	1.0	6.7	4.7	N/A	1.8	1.5
Noise floor (nV/rtHz) Bandwidth (Hz)	100 100	60 100	140 250	47 N/A	80 200	88 200
DSL noise contribution (%)	N/A	89.5	40.4	26	N/A	12.5
NEF */PEF *	5.4/52.5	37.4/1398	7.5/27.9	3.9/18.3	7.4/66.4	5.7/10.2 5.9 †/11.4 †
Tech. (nm)	800	65	180	130	40	180
Area (mm^2)	1.7	0.3	1.0	0.3	0.07	0.19

* Including DSL, † Including bias circuits. When the additional power (84 nW) of an 80% efficient buck converter is included, NEF/PEF increases to 6.5/12.6.

5. Conclusions

In this paper, we investigated a sub-µW chopper amplifier using a noise-efficient DSL and power-efficient SQI stage. The proposed DSL not only removes the charge dividing effect but also reduces noise caused by both the transconductance ratio and the open-loop gain. Using the proposed approach, the noise contribution from the DSL is reduced to below 12.5%, which is much lower than the value seen in previous work. For power efficiency, we use an SQI stage biased by a supply voltage reduced to the $2V_{\mathrm{DSAT}}$ saturation limit. The challenge of biasing the SQI stage and interfacing with a DSL having a different supply domain is addressed. Measurement of the fabricated CCIA shows an IRN of 1.5 μV_{rms} with the DSL enabled. The noise density is 88 nV/rtHz at a 40 dB gain when consuming 0.6 µW. The PEF is 11.4, which compares favorably with the state of the art.

Author Contributions: X.T.P. designed the circuit, performed the experimental work, and wrote the manuscript. N.T.N. performed noise analysis and revised the manuscript. V.T.N. performed circuit simulations and revised the manuscript. J.-W.L. conceived the project, organized the paper content, and edited the manuscript. All authors have read and agreed to the published version of the manuscript.

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