



Letter

# 0.5 V Fifth-Order Butterworth Low-Pass Filter Using Multiple-Input OTA for ECG Applications

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**Abstract:** This paper presents a 0.5 V fifth-order Butterworth low-pass filter based on multiple-input operational transconductance amplifiers (OTA). The filter is designed for electrocardiogram (ECG) acquisition systems and operates in the subthreshold region with nano-watt power consumption. The used multiple-input technique simplifies the overall structure of the OTA and reduces the number of active elements needed to realize the filter. The filter was designed and simulated in the Cadence environment using a 0.18  $\mu\text{m}$  Complementary Metal Oxide Semiconductor (CMOS) process from Taiwan Semiconductor Manufacturing Company (TSMC). Simulation results show that the filter has a bandwidth of 250 Hz, a power consumption of 34.65 nW, a dynamic range of 63.24 dB, attaining a figure-of-merit of 0.0191 pJ. The corner (process, voltage, temperature: PVT) and Monte Carlo (MC) analyses are included to prove the robustness of the filter.

**Keywords:** fifth-order low-pass filter; operational transconductance amplifier; multiple-input bulk-driven technique; subthreshold region; nanopower

## 1. Introduction

Continuous-time filters are widely used in biomedical systems devoted to applications in electroencephalographic (EEG), electromyographic (EMG), and electrocardiographic (ECG) systems. The biological signals processed in these systems typically occupy the frequency range of 0.05–250 Hz, with an amplitude of 15  $\mu\text{V}$ –5 mV [1]. In more detail, the frequency/amplitude ranges for EEG, EMG, and ECG signals are 0.05–60 Hz/15–100  $\mu\text{V}$ , 10–200 Hz/0.1–5 mV, and 0.05–250 Hz/100  $\mu\text{V}$ –5 mV, respectively. Figure 1 shows a typical data acquisition system for ECG signal processing. The pre-amplifier stage amplifies a low-amplitude ECG signal, then the low-pass filter selects the frequency range and eliminates out-of-band noise. The filtered analog signal is converted into digital form by an analog-to-digital converter (ADC) and then it is further processed by a digital signal processing (DSP) block. This work focused on the design of a low-pass filter with the cutoff frequency of 250 Hz. The analog low-pass filters for ECG acquisition systems should be designed to meet specific requirements, such as high dynamic range, low-power consumption, and small chip area. There are many low-pass filters for ECG acquisition systems described in the literature [2–10]. The Butterworth approximation is usually used because it provides a better linear phase and flat response within each

bandwidth. Considering the analog filters in [2–10], one can distinguish two main techniques that have been used to realize the low-pass Butterworth filters: the cascade approach [2–6] and the ladder simulation approach [7–10]. The cascade structure can be obtained by cascading several biquad filters, which leads to a simple and easy-to-tune realization.

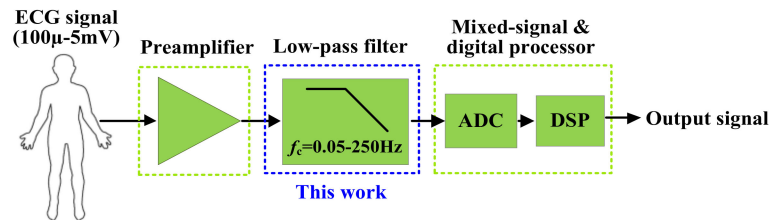


Figure 1. Electrocardiogram acquisition system.

The present work focused on the second approach, i.e., the ladder simulation of a prototype filter. In particular, we designed a fifth-order low-pass Butterworth filter based on the RLC prototype shown in Figure 2. As it is widely known, the high-order filters based on the RLC prototypes have lower pass-band sensitivity to the variation of passive elements, compared with that of the cascade approach.

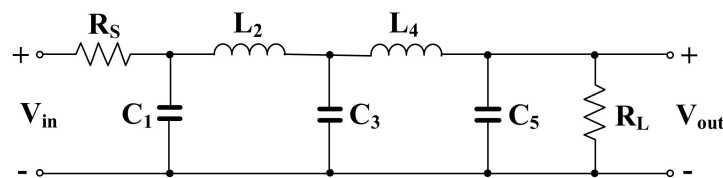
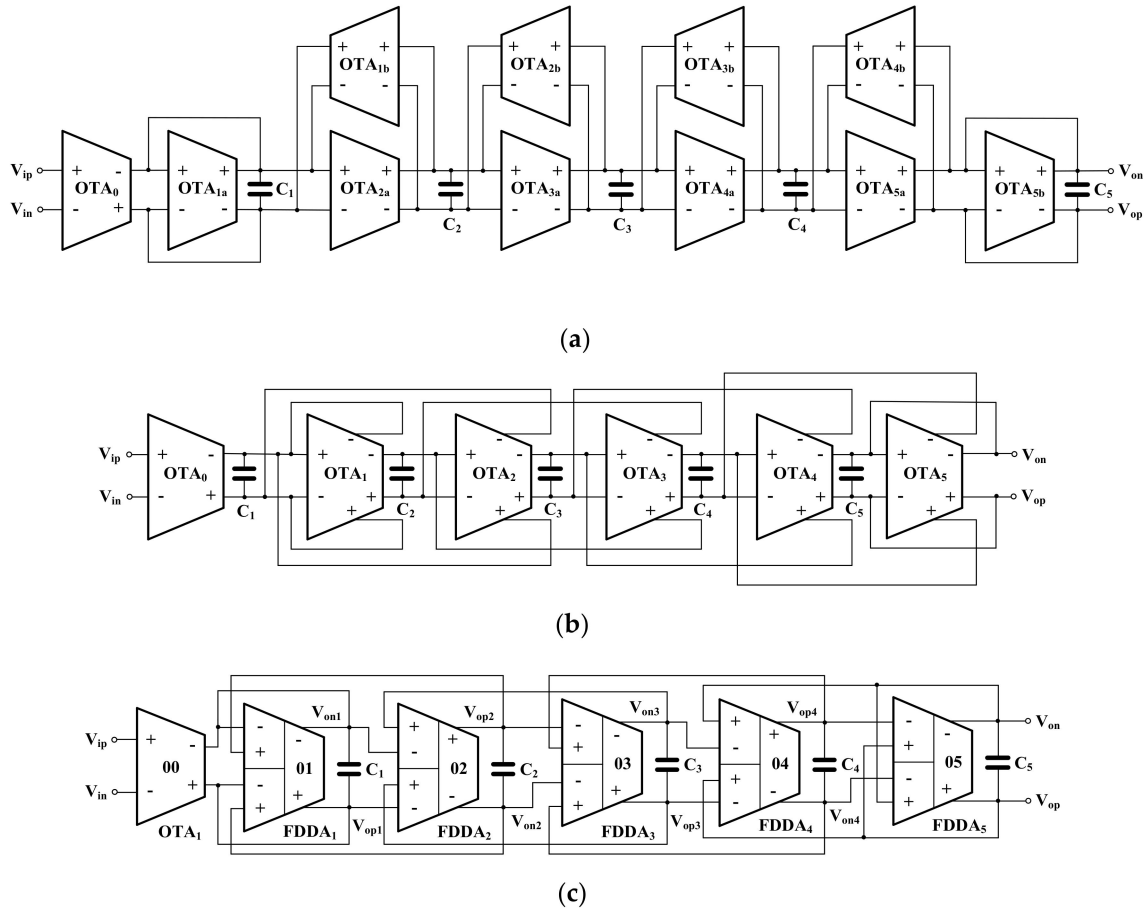


Figure 2. Prototype of a fifth-order low-pass filter.

The fifth-order low-pass Butterworth filters derived from the LC ladder-type filter were reported in [7–10]. The fifth-order Butterworth low-pass filter using fully differential operational transconductance amplifiers (FD-OTAs) is shown in Figure 3a [7]. The floating inductors  $L_2$  and  $L_4$  are simulated using OTA-based gyrators. The resistors  $R_S$  and  $R_L$  are simulated using OTAs as well. It should be noted that the filter in [7] employs eleven FD-OTAs and consumes 453 nW of power. The number of active devices that are used to realize this fifth-order Butterworth filter can be reduced by using multiple-output fully differential OTA (MOFD-OTA) as shown in Figure 3b [8,9], or fully differential-difference transconductance (FDDA) (a multiple-input active device) as shown in Figure 3c [10]. The structures in [8,9] employ six MOFD-OTA while the structure in [10] employs five FDDAs and one OTA. The filter in [8] consumes 350 nW of power and offers a 49.9 dB dynamic range while the filter in [9] consumes 41 nW of power and offers a 61.2 dB dynamic range. The filter in [10] consumes 453 nW of power and offers a 50 dB dynamic range.

This paper proposes a fifth-order Butterworth low-pass filter based on multiple-input operational transconductance amplifiers. It is clearly shown that the number of active devices needed to realize the fifth-order low-pass filter can be reduced by using the multiple-input OTA and results in reducing the power consumption and the active chip area. A novel technique with a multiple-input gate-driven (MIGD) transistor is used to realize multiple-input OTA with an internal CMOS structure as simple as a conventional OTA, hence, no additional current branches or cascade connections of multiple OTAs is needed. Unlike the floating-gate technique, the multiple-input technique does not require any additional processing steps to eliminate the trapped charge effect on the isolated gate nor any auxiliary circuit. Another advantage is that the multiple-input gate-driven P- or N-MOS transistors can be realized with any CMOS process. It is worth noting that the results presented in this work are based on pre-layout simulation and this work does not include the physical realization of the filter, nor the experimental testing in the context of ECG applications. However, the principle of multiple-input transistors, as multiple-input bulk-driven and multiple-input

bulk-driven quasi-floating-gates, have been confirmed experimentally by Khateb et al. in previous works [11–13]. The paper is organized as follows: Section 2 shows the principle of multiple-input gate-driven OTA and the filter design based on it, Section 3 the simulation results, and finally Section 4 the conclusion.



**Figure 3.** Fifth-order Butterworth low-pass filters, (a) FD-OTA-C filter [7], (b) MOFD-OTA-C filter [8,9], (c) FDDA-based filter [10].

## 2. Fifth-Order Butterworth Low Pass Filter

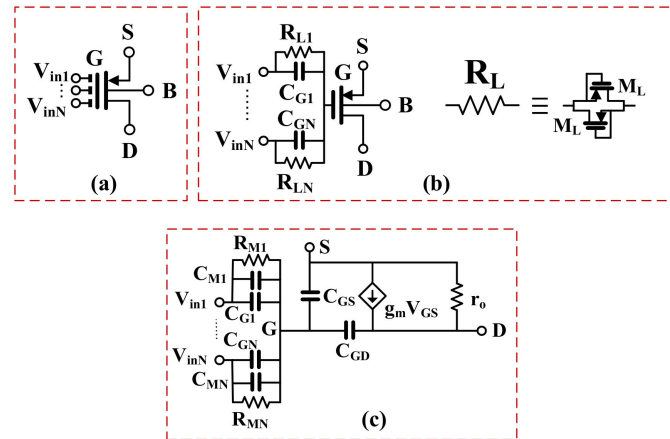
### 2.1. Multiple-Input Gate-Driven OTA

The active filter proposed in this work exploits multiple-input OTAs, which allows for simplifying its overall structure [14]. The multiple-input OTA is realized using a concept of a multiple-input MOS transistor. The symbol and CMOS realization of this element are shown in Figure 4a,b, respectively. As it is seen in Figure 4b, the multiple-input MOS can be seen as a connection of an “internal” MOS transistor and a voltage divider/analog summing circuit, composed of capacitances  $C_{Gi}$  ( $i = 1 \dots N$ ). The capacitors  $C_{Gi}$  are shunted by the large resistances  $R_{Li}$ , which ensures proper biasing of the gate terminal of the internal MOS for DC. The large resistances can be realized using an anti-parallel connection of two minimum-size MOS transistors operating in a cutoff region, as shown in Figure 4b. The small-signal equivalent circuit of the resulting multiple-input MOS is shown in Figure 4c. Assuming  $1/\omega C_{Gi} \ll R_{Li}$ , the gate potential  $V_G$  is given by

$$V_G = \sum_{i=1}^N \frac{C_{Gi}}{C_\Sigma} V_{ini} \quad (1)$$

where  $C_\Sigma$  is the sum of the capacitances  $C_{Gi}$  and the input capacitance of an internal MOS seen from its gate terminal  $C_{in}$ :

$$C_\Sigma = C_{in} + \sum_{i=1}^N C_{Gi} \quad (2)$$



**Figure 4.** MIGD MOS transistor, (a) symbol, (b) realization, (c) small-signal model.

Since the AC signal at the gate of the internal MOS transistor is attenuated by the capacitive divider, the transconductance of the multiple-input device seen from its  $i$ -th input, and operating in the subthreshold region, can be expressed as:

$$g_{mi} = \frac{I_D}{n_p U_T} \cdot \frac{C_{Gi}}{C_\Sigma} \quad (3)$$

where  $I_D$  is the DC drain current,  $n_p$  is the subthreshold slope, and  $U_T$  is the thermal potential. As it is seen from (3), the transconductance seen from the  $i$ -th input is equal to the transconductance of the internal MOS, multiplied by the voltage gain of the capacitive voltage divider.

The lower input transconductance  $g_{mi}$  entails a lower intrinsic voltage gain of the multiple-input MOS, as well as an increased input-referred noise. Both parameters are degraded by the factor of  $C_\Sigma/C_{Gi}$ . However, it is worth noting that the linear range for such a device is also increased by the factor of  $C_\Sigma/C_{Gi}$ , therefore, its dynamic range (DR) remains the same as that of the internal MOS.

The multiple-input MOS transistors were used to design a multiple-input OTA. The symbol and CMOS realization of the circuit are shown in Figures 5 and 6, respectively. The multiple-input MOS transistors  $M_1$  and  $M_2$  were used to create a multiple-input differential pair, biased by the self-cascode current sources  $M_{7,7c}$  and  $M_{8,8c}$ . The drain currents of the input differential pair are transferred to the outputs ( $I_{o+}$  and  $I_{o-}$ ) through the current mirrors composed of the self-cascode transistors  $M_{3/3c}$ - $M_{4/4c}$  and  $M_{5,5c}$ - $M_{6,6c}$ . The current mirrors are loaded with the self-cascode current sources  $M_{10,10c}$  and  $M_{9,9c}$ . Note that the tail node that supplies the differential pair in Figure 6 is drawn with two branches for esthetic reasons. The application of self-cascode connections in this design allows for an increase in the output resistance of the OTA, which entails increasing the DC voltage gain of this circuit. The transistors  $M_{9c}$ - $M_{11c}$  form a simple common-mode feedback circuit (CMFB) circuit, which forces the output common-mode level to be equal to the reference potential  $V_{CM}$ . All the transistors operate in a subthreshold triode region. If the common-mode level is increasing/decreasing, the channel resistances of  $M_{10c1,c2}$  are increasing/decreasing as well, thus lowering the currents flowing through  $M_{10}$  and  $M_9$ , and consequently, decreasing/increasing the common-mode level to the desired value. The transistors  $M_{9c}$  and  $M_{10c}$  are divided into two devices, which makes the circuit insensitive to the output differential signals of the OTA, at least for small amplitudes of the signal. For larger amplitudes of the output

signals, one can observe nonlinear components of the drain currents  $I_{D9}$  and  $I_{D10}$ , caused by the differential output voltage of the OTA. However, this nonlinear effect is not apparent at the differential output of OTA, since variation of  $I_{D9}$  and  $I_{D10}$  are identical. This effect, however, causes variation of the output common-mode level. Figure 7 illustrates the large signal transfer characteristics and the common-mode level variation for unloaded OTA in Figure 6 controlled with differential signals. Note, moderate nonlinear effects are caused by the nonlinear output conductance of the OTA rather than that of the CMFB. Variations of the common-mode output voltage are maintained at an acceptable level.

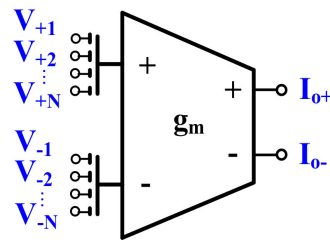


Figure 5. Symbol of a multiple-input operational transconductance amplifier (OTA).

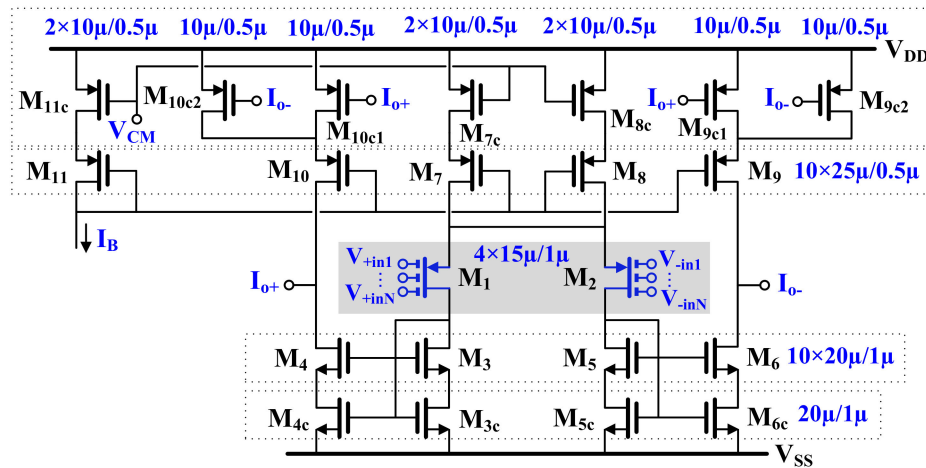


Figure 6. CMOS implementation for an MIGD OTA.

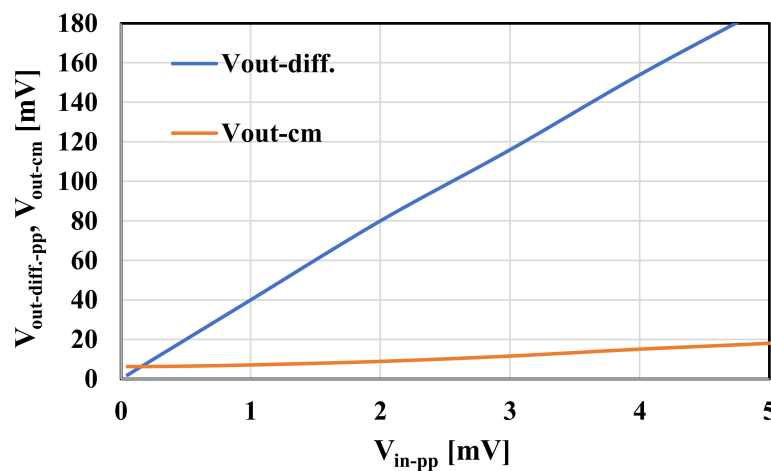


Figure 7. Output differential voltage and common-mode level versus input differential voltage for unloaded OTA in Figure 6.

One can say that the applied CMFB has a simple structure and does not consume additional power from supply rails. On the other hand, it slightly limits the maximum output voltage swing due

to nonzero voltage drops across transistors  $M_{9c}$ – $M_{11c}$  and variations of the output common-mode level caused by differential signals. However, the negative effects can be maintained at an acceptable level.

Assuming  $1/\omega C_{Gi} \ll R_{Li}$ , the differential output current of the OTA can be expressed as:

$$I_{o+} - I_{o-} = I_B \tanh \left( \sum_{i=1}^N \frac{V_{+ini} - V_{-ini}}{n_p U_T} \cdot \frac{C_{Gi}}{C_\Sigma} \right) \quad (4)$$

where  $I_B$  is the biasing current (it was assumed that  $I_{D7} = I_{D8} = I_{D11}$ ). From (4), the small-signal transconductance from  $i$ -th input is given by:

$$g_{mi} = \frac{I_D}{n_p U_T} \cdot \frac{C_{Gi}}{C_\Sigma} \quad (5)$$

The DC voltage gain of the OTA from the  $i$ -th input can be expressed as:

$$A_{vd} = g_{mi} r_{out} \quad (6)$$

where  $r_{out}$  is the output resistance of the OTA, given by:

$$r_{out} \cong g_{m4,6} r_{ds4,6} r_{ds4c,6c} \parallel g_{m9,10} r_{ds9,10} (r_{ds9,10c} / 2) \quad (7)$$

Thanks to the self cascode connections, the voltage gain of the OTA can be at an acceptable level, despite the lower transconductance of the input differential pair.

From (4), the third order harmonic distortion of the OTA for a sinusoidal signal applied to one pair of input terminals, while the other pairs are shorted to ground the AC signals, can be expressed as:

$$HD_3 = \frac{1}{48} \left( \frac{V_{+i} - V_{-i}}{n_p U_T} \cdot \frac{C_{Gi}}{C_\Sigma} \right)^2 \quad (8)$$

Thus, as it is seen from (8), the input linear range is increased by the factor of  $C_\Sigma / C_{Gi}$ , i.e., the voltage attenuation factor introduced by the input capacitive divider.

The input referred noise of the OTA, including both thermal and flicker noise components, can be expressed as:

$$\overline{v_{nti}^2} = 2 \left( \frac{U_T}{I_B} \right)^2 \left( \frac{C_\Sigma}{C_{Gi}} \right)^2 \left[ \overline{i_{1,2}^2} + 2 \overline{i_{3-6}^2} + 2 \overline{i_{9,10}^2} \right] \quad (9)$$

where:

$$\overline{i_{1,2}^2} = 2qI_B + \frac{K_{Fp} \left( \frac{I_B}{U_T} \right)^2}{f C_{OX} (WL)_{1,2}} \quad (10)$$

$$\overline{i_{3-6}^2} = 4kT g_{ds3-6c} \left( 1 + \frac{2}{3} \frac{g_{ds3-6c}}{g_{m3-6}} \right) \frac{(g_{m3-6} r_{ds3-6c})^2}{(1 + g_{m3-6} r_{ds3-6c})^2} + \frac{1}{4} \cdot \frac{K_{Fn} \left( \frac{I_B}{U_T} \right)^2}{f C_{OX} [(WL)_{3-6eff}]} \quad (11)$$

$$\overline{i_{10-14}^2} = 4kT g_{ds9-10c} \left( 1 + \frac{2}{3} \frac{g_{ds9-10c}}{g_{m9-10}} \right) \frac{(g_{m9-10} r_{ds9-10c})^2}{(1 + g_{m9-10} r_{ds9-10c})^2} + \frac{1}{4} \cdot \frac{K_{Fp} \left( \frac{I_B}{U_T} \right)^2}{f C_{OX} [(WL)_{9,10eff}]} \quad (12)$$

where  $g_{ds9-10c} = g_{ds9-10c1} / g_{ds9-10c1}$ ,  $WL_{ieff} = (WL_i \cdot WL_{ic}) / (WL_i + WL_{ic})$ ,  $i = 3 \dots 10$ ,  $WL_{9,10c} = WL_{9,10c1} + WL_{9-10c2}$ ,  $K_{Fn}$  and  $K_{Fp}$  are the flicker noise constants for n- and p-channel transistors, respectively, and  $C_{OX}$  is the oxide capacitance per unit area.

As it is easy to note from (9), the input referred noise is increased by the factor of  $C_\Sigma / C_{Gi}$ , as compared with the input noise of a single-input OTA biased with the same current. However, if the multiple input OTA is realized with  $N$  identical OTAs, each biased with the current of  $I_B / N$ ,

then the input transconductance from each input and the input referred noise would be the same as that for the proposed realization (see the Appendix A). Since the linear range in the proposed design is increased  $C_\Sigma / C_{Gi}$  times, then the DR of the proposed solution is also increased in the same proportion. The improved DR can be considered as the most important advantage of the proposed approach. Note that a similar capacitive attenuation approach that increase the dynamic range of OTAs has been presented before [15].

## 2.2. Proposed Filter

The proposed fifth-order Butterworth low-pass filter is shown in Figure 8a. It was developed from the LC-ladder filter based on the OTA-C topology. Its signal flow graph is shown in Figure 8b, where  $\tau_1 = C_1 / g_{m1}$ ,  $\tau_2 = C_2 / g_{m2}$ ,  $\tau_3 = C_3 / g_{m3}$ ,  $\tau_4 = C_4 / g_{m4}$ , and  $\tau_5 = C_5 / g_{m5}$ . The filter comprises five MIGD OTAs and five capacitors. The number of active devices is reduced from 6 to 5, as compared with [8–10], which allows for the reduction of the active area and power.

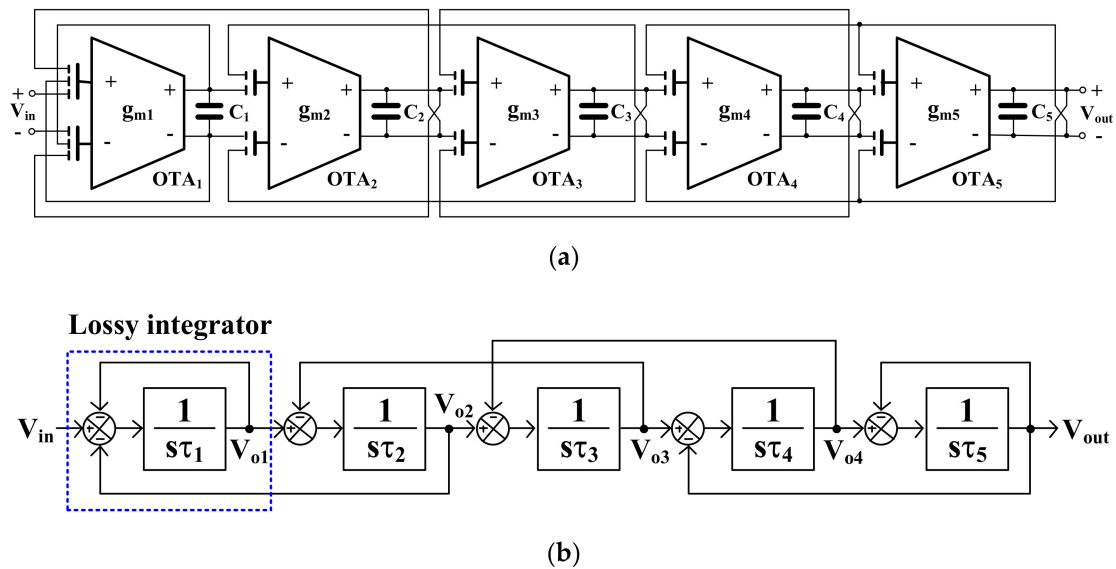


Figure 8. (a) Proposed fifth-order Butterworth low-pass filter, (b) signal flow graph.

Considering OTA<sub>0</sub>, OTA<sub>1</sub> in Figure 3b and OTA<sub>0</sub>, FDFA<sub>1</sub> in Figure 3c, it can be noted that these devices are used to realize a floating resistor [9]. In this work these components together with the capacitor C<sub>1</sub> create a lossy integrator as shown in Figure 9a [8], Figure 9b [10]. The ideal transfer function of these circuits can be expressed as:

$$\frac{V_{op1} - V_{on1}}{V_{ip} - V_{in}} = \frac{g_{mo} / g_{m1}}{(sC_1 / g_{m1}) + 1} \quad (13)$$

It is evident that the circuits work as lossy integrators, where the voltage gain can be controlled by  $g_{mo}$ . Usually, all transconductances are set to be equal for easy tuning. Figure 9c shows the lossy integrator based on the three-input OTA that is proposed in this paper. The ideal transfer function of the circuit in Figure 9c can be expressed as:

$$\frac{V_{op1} - V_{on1}}{V_{ip} - V_{in}} = \frac{1}{(sC_1 / g_{m1}) + 1} \quad (14)$$

Thus, the circuit works as a lossy integrator with unity gain. Assuming that  $g_{mo} = g_{m1}$ , Equations (13) and (14) will be identical. Thus, it can be concluded that the OTA<sub>0</sub> in Figure 3b,c can be removed by using multiple-input OTA. This application can only be realized using multiple-input OTA



and it is not possible by using conventional OTA. It should be noted that only the parts mentioned above in Figure 9a of [8], Figure 9b of [10] are modified, the other parts (OTA<sub>2-5</sub> or FDDA<sub>2-5</sub>) are not changed and the feedback connection is still similar to the filters in [8,10].

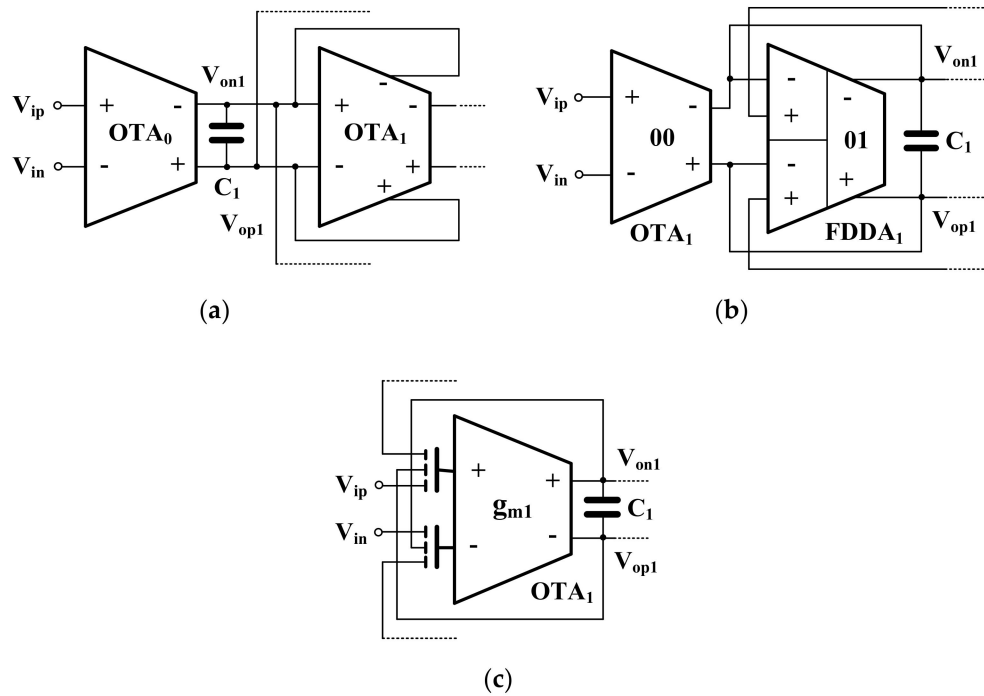


Figure 9. Lossy integrator, (a) circuit in [8], (b) circuit in [10], (c) proposed circuit.

### 3. Results and Discussion

The circuit was designed in the Cadence environment using a TSMC 0.18  $\mu\text{m}$  CMOS process with a metal-insulator-metal (MIM) capacitor. The OTA with bias current  $I_B = 3.3 \text{ nA}$  consumes 8.25 nW under a 0.5 V supply voltage. The isolation between OTA inputs is assured by the large value resistance of the MOS transistor operating in a cutoff region. The input currents are well below 100 pA for input range rail-to-rail.

The RLC filter in Figure 2 was designed for the cut-off frequency of 250 Hz. The prototype element values were chosen as follows:  $R_S = R_L = 1 \Omega$ ,  $C_1 = C_5 = 393.4 \mu\text{F}$ ,  $C_3 = 1.27 \text{ mF}$ , and  $L_2 = L_4 = 1.03 \text{ mH}$ . For the OTA-C filter  $C_1 = C_5 = 5.43 \text{ pF}$ ,  $C_2 = C_4 = 14.2 \text{ pF}$ ,  $C_3 = 17.57 \text{ pF}$ , and the bias current for each OTA was  $I_B = 3.3 \text{ nA}$ . Note that the bias current circuit serves to bias all OTAs hence the maximum power consumption of the filter is 34.65 nW. Figure 10 shows the frequency responses of the RLC and the proposed filter. The gain magnitude at low frequency was  $-6 \text{ dB}$  and  $-6.4 \text{ dB}$  and the cut-off frequency ( $f_c$ ) was 250.2 Hz and 250.4 for the RLC and OTA filters, respectively. Both curves are in good agreement up to  $-70 \text{ dB}$ . Figure 11 shows the frequency response of the filter with different bias currents ranging from 0.1 nA to 3.3 nA while the  $f_c$  was in the range of 17.11 Hz to 250.4 Hz. The tuning capability and the linear relation between  $f_c$  and  $I_B$  are demonstrated in Figure 12. The transient response of the filter for the input sine wave of  $V_{inpp} = 100 \text{ mV}$  and 10-Hz frequency are illustrated in Figure 13. The total harmonic distortion (THD) was 1%.

To check the influence of the process, voltage, and temperature (PVT) variations on the filter performance, the corner analysis was performed. The MOS transistor corners (ss, sf, fs, ff), MIM capacitor corners (ss, ff), voltage supply corners (490 mV, 510 mV), and temperature corners ( $0^\circ\text{C}$ ,  $60^\circ\text{C}$ ) were used. The variation of the gain was in the range of  $-7.2 \text{ dB}$  to  $-6.13 \text{ dB}$  while the variation of the cut-off frequency was in the range of 100.6 Hz to 326.7 Hz, as shown in Figure 14. Note that the temperature corner has the most effect of the variation of the frequency response since the circuit operates in a subthreshold region. However, since the circuit is proposed for biomedical applications it is expected



that the temperature variation will be less than the chosen temperature corners. Although the variation of the cut-off frequency is large, the needed value can be simply re-adjusted by the bias current. Note that the amplitudes of the bumps at low bias currents in Figure 11 and at higher frequencies in Figure 14 do not exceed 1.6 dB and do not affect stability of the circuit in a significant manner.

The Monte Carlo analysis with 200 runs was performed for the filter gain and cut-off frequency as shown in Figures 15 and 16, respectively. The mean value of the gain was  $-6.23$  dB with standard deviation of  $0.14$  dB, while the mean value of the cut-off frequency was  $251.7$  Hz with standard deviation of  $4.9$  Hz. Figure 17 shows the output referred noise density of the filter. The integrated in-band noise between  $0.1$  Hz to  $250$  Hz shows that the output referred noise is  $77 \mu\text{V}_{\text{rms}}$ . Figure 18 shows the performance of the proposed filter in processing the ECG signal where (a) depicts the ECG signal with a distortion signal ( $5 \text{ mV}/500 \text{ Hz}$ ) that was applied at the input of the filter and (b) depicts the filtered output signal.

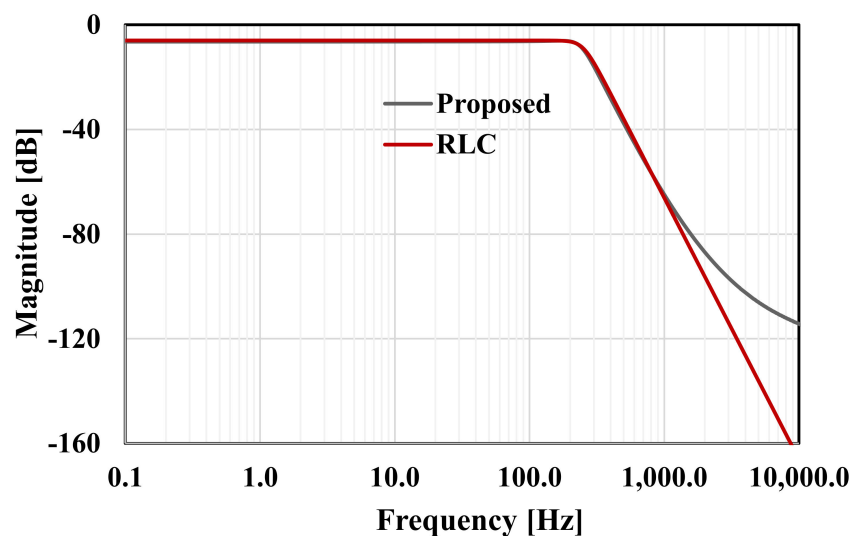


Figure 10. The frequency response of the RLC and the proposed filter.

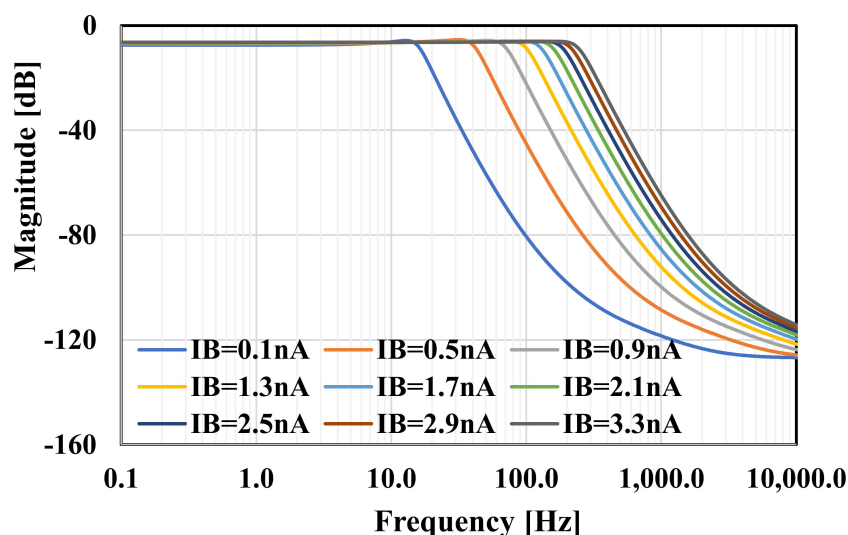


Figure 11. The frequency response of the proposed filter with different bias currents.

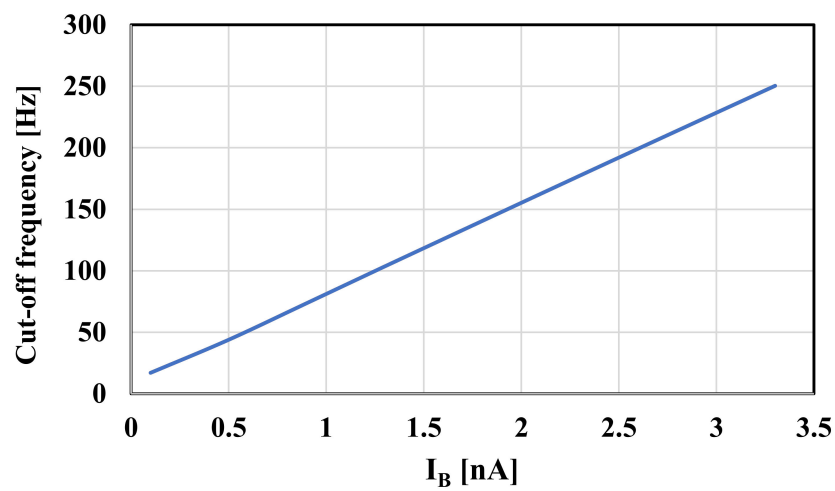


Figure 12. The cut-off frequency versus the bias current.

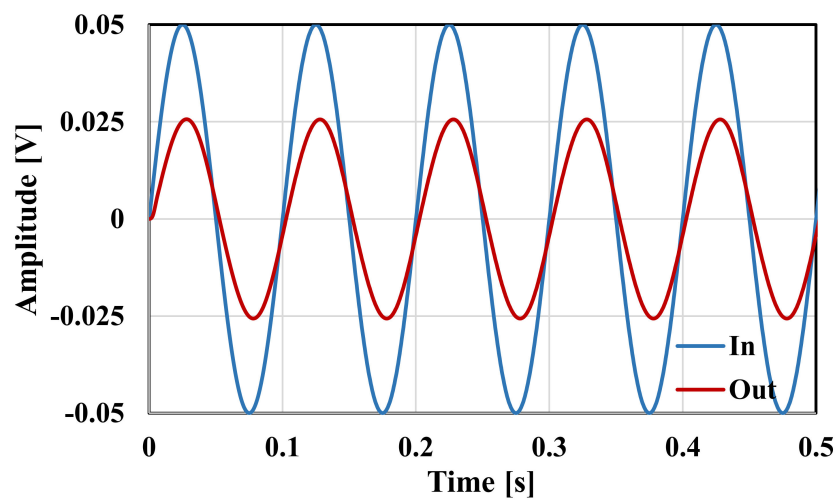


Figure 13. The transient response of the filter for input sine wave with  $V_{inpp} = 100$  mV and 10 Hz.

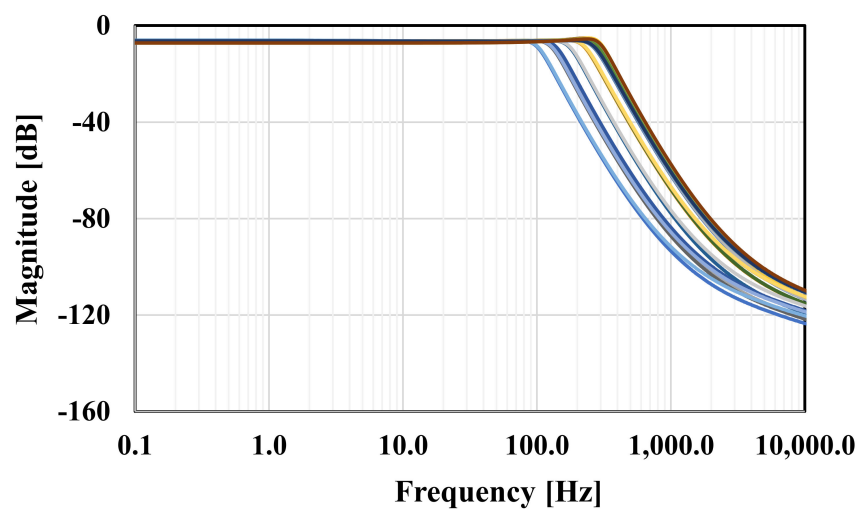


Figure 14. The frequency response of the proposed filter under process, voltage and temperature (PVT) corners.

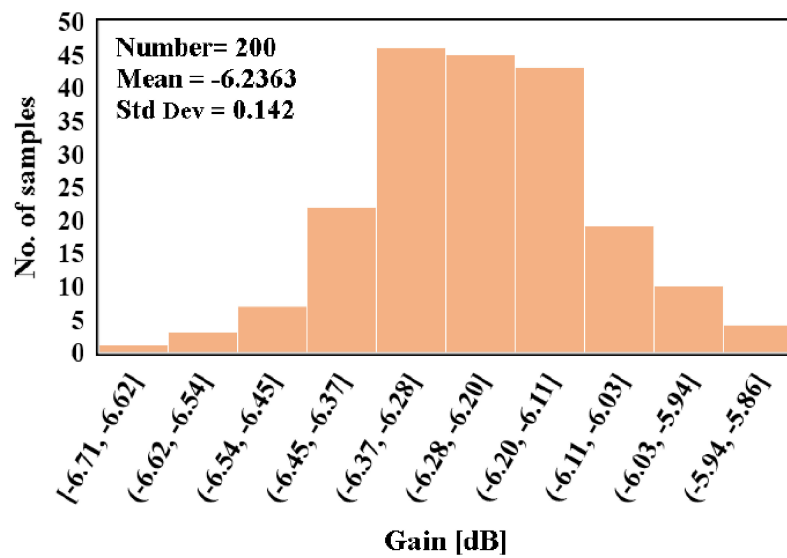


Figure 15. Monte Carlo simulation of the voltage gain.

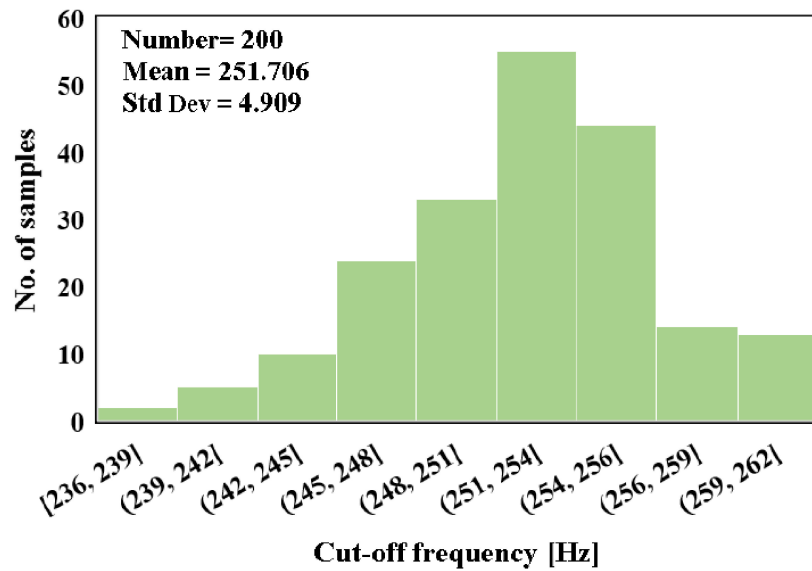


Figure 16. Monte Carlo simulation of the cut-off frequency.

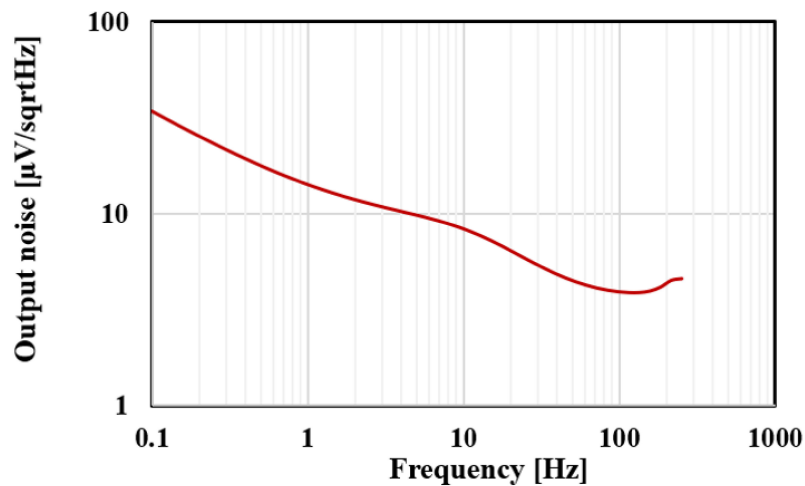
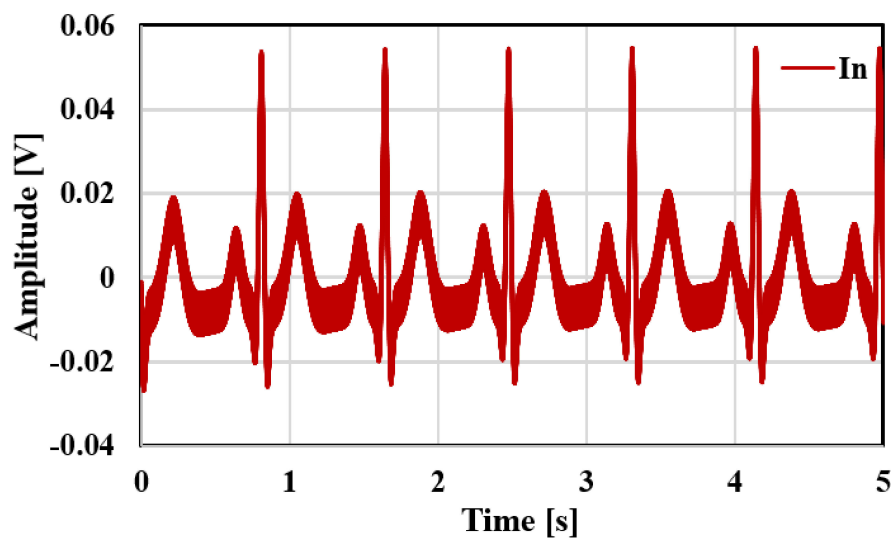
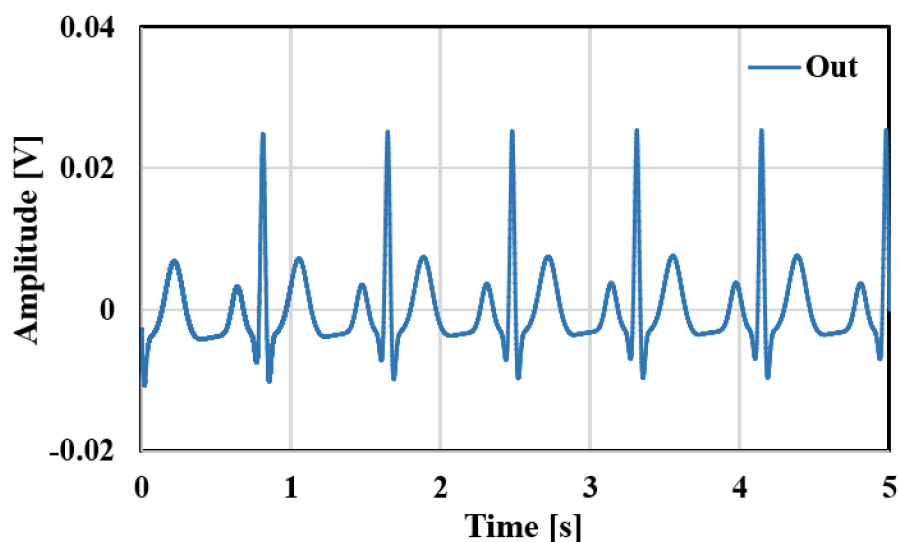


Figure 17. The output referred noise density of the proposed filter.



(a)



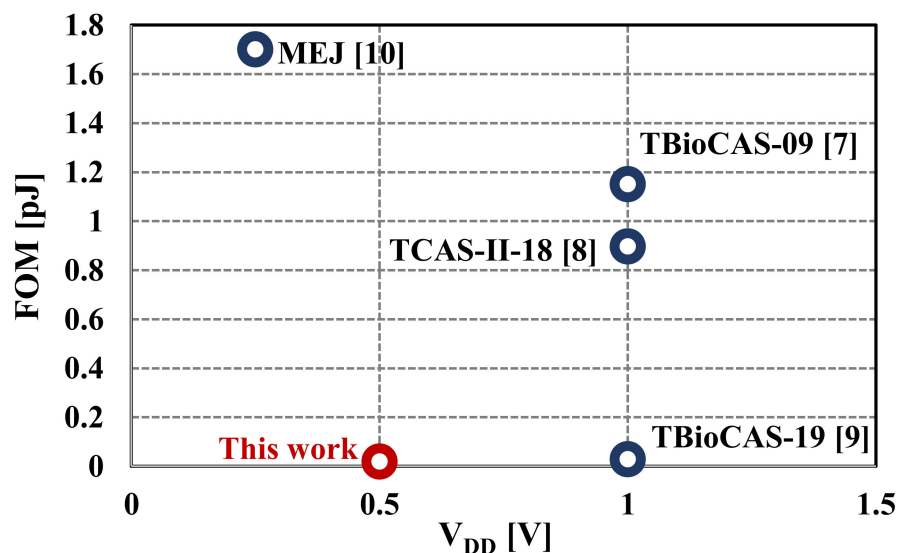
(b)

**Figure 18.** Transient response of the filter for ECG signal: (a) input; (b) output.

The summary and comparison between the proposed filter and some previous works are shown in Table 1. Only the fifth-order Butterworth low-pass filters simulated by the LC-ladder type filter and suitable for ECG signal acquisition [7–10] have been selected for comparison. From Table 1, it is clear that the proposed filter has a lower number of active devices, power consumption, and figure-of-merit (FOM). Finally, the FOM versus  $V_{DD}$  of fifth-order low-pass filters are shown in Figure 19. Compared with the works in [7,8,10], the proposed filter offers clearly better FOM. The FOM is even slightly lower than the one in [9] with half the value of  $V_{DD}$ . It is worth noting that the estimated chip area of 2-inputs and 3-inputs OTA based on the MIGD technique is increased by approximately 5% and 8%, respectively, compared to that of a single-input conventional OTA with the same transistor dimensions. This confirms the advantage of this technique of saving chip area. Note, a similar conclusion of this advantage based on experimental results is stated in [11]. The small chip area of the proposed filter is evident in Table 1 compared with that of [10] that used off-chip capacitors for filter realization.

**Table 1.** Performance comparison between the proposed filter and other fifth-order low-pass filters for ECG signal acquisition.

Symbol	This Work	MEJ (2019) [10]	IEEE TBioCAS (2019) [9]	IEEE TCAS-II (2018) [8]	IEEE TBioCAS (2009) [7]
$V_{DD}$ [V]	0.5	0.25	1	1	1
Tech [ $\mu\text{m}$ ]	0.18	0.13	0.18	0.18	0.18
$V_{TH}$ [V]	0.5	0.44	0.5	0.5	0.5
Order (N)	5	5	5	5	5
No. of active device	5 MIGD-OTAs	6 FDDTAs	6 OTAs	6 OTAs	11 OTAs
Structure	$G_m$ -C fully-diff.	$G_m$ -C fully-diff.	$G_m$ -C fully-diff.	$G_m$ -C fully-diff.	$G_m$ -C fully-diff.
BW [Hz]	250	100	250	250	250
IRN [ $\mu\text{V}_{rms}$ ]	167	4.7	134	100	300
DR [dB]	63.24	57.00	61.2	49.9	50
Power (P) [nW]	34.65	603	41	350	453
FOM = $P/(N * BW * DR)$ [pJ]	0.0191	1.7	0.0286	0.896	1.15
LV capability = $V_{TH}/V_{DD} * 100$ [%]	100	176	50	50	50
Area [ $\text{mm}^2$ ]	0.08 (estim.) (off-chip cap.)	0.67 (off-chip cap.)	0.24	0.12	0.13
Obtained results	Simulation	Measured	Measured	Measured	Measured

**Figure 19.** Figure-of-merit (FOM) against  $V_{DD}$  of the fifth-order low-pass filters.

#### 4. Conclusions

In this paper, a fifth-order Butterworth low-pass filter using multiple-input OTA was proposed. The design proves that the number of OTAs for realizing the fifth-order low-pass filter architecture can be reduced using multiple-input OTAs. This entails the reduction of both the power consumption and the active area. Comparison with other designs in the literature shows that the proposed structure is the most beneficial, regarding the number of active devices and power consumption. The proposed filter was simulated with a 0.18  $\mu\text{m}$  CMOS process and supplied with 0.5 V, which entailed operation in a subthreshold region. Simulation results including PVT corner and Monte Carlo (MC) analyses confirmed the robustness of the design.

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## Appendix A

Let us compare noise properties of a fully-differential OTA in Figure A1a, biased with current  $I_B$ , and a multiple-input OTA composed of  $n$  identical OTAs of the same structure, but biased with currents of  $I_B/n$  (Figure A1b). For simplicity, let us consider only the thermal noise.

The mean-square value of the output noise current of the OTA in Figure A1a, operating in a weak-inversion region can be expressed as:

$$\overline{i_n^2} = 2qI_B A \quad (A1)$$

where  $q$  is the electron charge and  $A$  is a constant depending on the particular structure of the OTA. Consequently, the input referred noise is given by:

$$\overline{v_n^2} = \frac{2qI_B A}{g_m^2} \quad (A2)$$

The output noise current of each OTA in Figure A1b is:

$$\overline{i_n^2} = 2q \frac{I_B}{N} A \quad (A3)$$

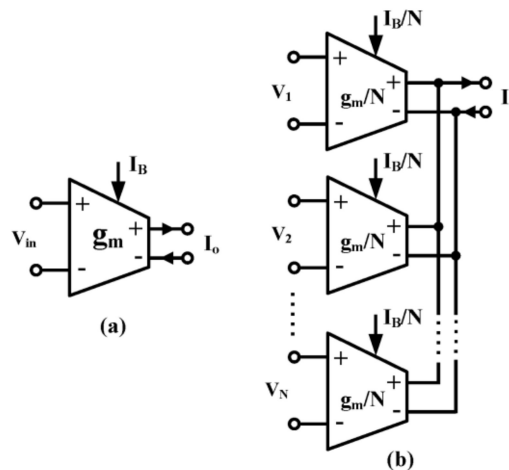
However, the total output noise current, equal to the sum of  $N$  output currents, is the same as that for the reference OTA in Figure A1a. If the total output noise is referred to one input, we obtain:

$$\overline{v_{ni}^2} = \frac{\overline{i_n^2}}{\left(\frac{g_m}{N}\right)^2} = \frac{2qI_B A}{g_m^2} N^2 \quad (A4)$$

Thus, the rms value of the input noise is given by:

$$\sqrt{\overline{v_{ni}^2}} = N \sqrt{\frac{2qI_B A}{g_m^2}} \quad (A5)$$

If a noiseless passive voltage divider, with  $N$  inputs, and a voltage gain of  $1/N$  from each input is added at the input of the OTA in Figure A1a, then the rms value of the  $i$ -th input referred noise voltage is given by the same equation, namely, the  $i$ -th input-referred noise is the same as that for the OTA in Figure A1b.



**Figure A1.** Single-input fully-differential OTA (a) and multiple-input fully-differential OTA (b).

If we define the dynamic range as the ratio of the maximum input rms voltage, limited by an assumed level of nonlinear distortion ( $V_{inmax}$ ) to the  $i$ -th input referred noise, then for the multiple-input OTA in Figure A1b we have:

$$DR_{mi} = \frac{V_{inmax}}{\sqrt{v_{ni}^2}} \quad (A6)$$

Since in the subthreshold region the linear range of a differential pair does not depend on the biasing current, then for the OTA in Figure A1a, with an additional passive voltage divider, the linear range will be extended  $N$  times, and the DR will be:

$$DR_{pd} = N \cdot \frac{V_{inmax}}{\sqrt{v_{ni}^2}} = N \cdot DR_{mi} \quad (A7)$$

Hence, the dynamic range of the OTA with a passive, noiseless voltage divider at the input is  $N$  times as large as that for the OTA composed of  $N$  identical OTAs, biased with  $N$ -times lower current. Similar proof could be concluded for flicker noise, however, in such a case not only the total biasing current, but also the total areas of transistor channels should be equal for the two compared circuits, i.e., the transistor channel areas of each OTA in Figure A1b should be  $N$  times smaller than for that of the OTA in Figure A1a.

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