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A VCO-Based CMOS Readout Circuit for Capacitive MEMS Microphones

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Abstract: Microelectromechanical systems (MEMS) microphone sensors have significantly improved in the past years, while the readout electronic is mainly implemented using switched-capacitor technology. The development of new battery powered “always-on” applications increasingly requires a low power consumption. In this paper, we show a new readout circuit approach which is based on a mostly digital Sigma Delta ($\Sigma\Delta$) analog-to-digital converter (ADC). The operating principle of the readout circuit consists of coupling the MEMS sensor to an impedance converter that modulates the frequency of a stacked-ring oscillator—a new voltage-controlled oscillator (VCO) circuit featuring a good trade-off between phase noise and power consumption. The frequency coded signal is then sampled and converted into a noise-shaped digital sequence by a time-to-digital converter (TDC). A time-efficient design methodology has been used to optimize the sensitivity of the oscillator combined with the phase noise induced by $1/f$ and thermal noise. The circuit has been prototyped in a 130 nm CMOS process and directly bonded to a standard MEMS microphone. The proposed VCO-based analog-to-digital converter (VCO-ADC) has been characterized electrically and acoustically. The peak signal-to-noise and distortion ratio (SNDR) obtained from measurements is 77.9 dB-A and the dynamic range (DR) is 100 dB-A. The current consumption is 750 μ A at 1.8 V and the effective area is 0.12 mm². This new readout circuit may represent an enabling advance for low-cost digital MEMS microphones.

Keywords: MEMS microphone; oscillator-based sensor; sigma-delta modulation; time-domain circuit; VCO-ADC

1. Introduction

The fast growth of the Internet of Things (IoT) and the upward trend of the mobile market are increasing the use of voice communication and speech recognition applications [1–3]. In some cases, an always-listening function is required to interact with the user voice commands, consequently, a low power consumption should be a key feature of such systems. In addition, low cost, small size, and easy integration are often the main imposed requirements for a microphone design. In recent years, to meet these basic needs, conventional Electret Condenser Microphones (ECM) have been replaced by Microelectromechanical systems (MEMS) sensors [4–7]. The MEMS high signal-to-noise ratio (SNR), good sensitivity, and the possibility to place a large number of these sensors in the same device make this technology well suited for current audio applications [8,9].

The low bandwidth of the audio signals enables the design of interfaces for MEMS acoustic sensors, usually employing oversampled Sigma Delta ($\Sigma\Delta$) data converters [10,11]. $\Sigma\Delta$ modulators

based on a switched-capacitor (SC) technology have a larger power consumption in comparison with continuous-time (CT) $\Sigma\Delta$ s, but with a more robust behavior against circuit impairments like modulator clock jitter [12]. Current deep submicron CMOS technologies have led to working with reduced power supply voltages, what makes this challenging is the analog design of either SC- $\Sigma\Delta$ s or CT- $\Sigma\Delta$ s. However, this technology scaling impacts the performance of digital circuits in a positive way, especially in terms of area and power consumption.

Recently, time-to-digital conversion is becoming a good solution to overcome the challenges that low supply voltages pose to conventional analog circuit designs [13–15]. An alternative option to replace $\Sigma\Delta$ modulators are the oscillator-based analog-to-digital converters (ADCs). They are noise-shaped architectures wherein the information is encoded into the frequency of a digital signal; in contrast with the classical voltage encoding, therefore, the dynamic range (DR) is not limited by the power supply. In addition, they can be mostly implemented with digital circuits, taking advantage of the technology integration benefits and lower power consumption.

As shown in Figure 1a, readout circuits for capacitive MEMS sensors can be done by directly connecting the sensing element as the load of an oscillator [16,17]. This way, the reactance change in the sensor modulates the oscillation frequency. By using some digital circuitry, this frequency-modulated signal can be converted into a noise-shaped bit stream. Alternatively, in Figure 1b, the sensor can be connected via an analog interface, generating a voltage signal proportional to the MEMS acoustic stimuli, which can be converted to the digital domain by a combination of a voltage-controlled oscillator (VCO) and digital circuitry. Both approaches behave like a CT- $\Sigma\Delta$ modulator, showing the first-order noise-shaping property at its output spectrum.

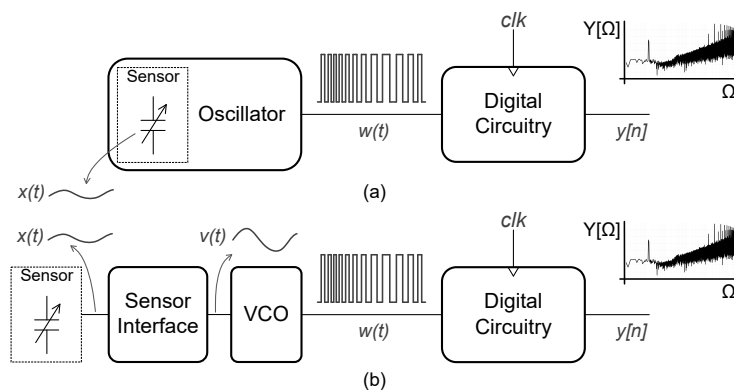


Figure 1. Oscillator-based analog-to-digital converter (ADC) for capacitive Microelectromechanical systems (MEMS) sensors: (a) Sensor connected as the load of an oscillator; (b) sensor connected via an analog interface.

Typically, VCO-based analog-to-digital converters (VCO-ADCs) are implemented with ring oscillators (ROs) [18–22]. As in a conventional ADC, the VCO-ADC performance is limited by flicker and thermal noise. This circuit noise appears as phase noise in the RO, which is demodulated at the output, after sampling, as a low frequency noise affecting the overall system SNR. Another factor that limits the DR in VCO-ADC open-loop configuration is the distortion resulting from the nonlinear relationship between the input voltage and the RO oscillation frequency for large input signals. Due to these limitations, a careful design of the RO present in the ADC is required.

This paper introduces a pseudo-differential architecture for a MEMS microphone readout circuit based on a mostly digital $\Sigma\Delta$ ADC. The MEMS sensor is coupled to an impedance converter that modulates the frequency of a RO. The time-encoded output data of the RO is sampled with a time-to-digital converter (TDC). Finally, a thermometer-to-binary (T2B) encoder and a binary adder generate a multibit noise-shaped digital signal, which can be easily transformed into any standard audio interface by means of digital signal processing, without requiring a data-weighted averaging (DWA) technique or feedback digital-to-analog converter (DAC) linearity calibration, compared to a

multibit SC- $\Sigma\Delta$. Since the proposed VCO-ADC is mainly implemented with digital circuitry, it is a scalable solution in terms of area and power consumption, in contrast to SC- $\Sigma\Delta$ -based readout circuits for MEMS microphones. Furthermore, the SNR performance of this VCO-ADC implemented in a 130 nm CMOS process can compete with the SC- $\Sigma\Delta$ or the CT- $\Sigma\Delta$ performance [11,23].

The paper is organized as follows. Section 2 presents the system level architecture. Section 3 describes the circuit implementation at transistor level. Section 4 shows electrical and acoustical measurements obtained from the prototyped CMOS ASIC. Finally, Section 5 concludes the paper.

2. System Level Architecture

Figure 2 shows the main blocks at the system level of the proposed VCO-ADC. It is composed of two single-ended channels which, combined in a pseudo-differential architecture, present full integration with dual-backplate (DBP) MEMS microphones. This kind of transducer is built by adding a second backplate to the conventional single-backplate (SBP) MEMS microphone, resulting in a differential capacitive sensor with even-order harmonics cancellation [8]. In the presented architecture, both the positive (P) and the negative (N) channels are identical. As a requirement of the target audio application, the output of the ADC is a multibit sequence. Nevertheless, if a single-bit signal is preferred instead, the multibit output can be processed with a noise-shaper coder.

The output of the capacitive MEMS sensor $x(t)$ is coupled into the ADC input via an impedance converter, generating the signal $v(t)$, which sets the frequency of the VCO. The oscillator output, after a level shifter, is divided by a factor of four in order to adjust the oscillation frequency and make it compatible with the implemented demodulation circuit. The frequency-modulated signal $w(t)$ obtained at the output of the divider is passed through a 31-stage delay line, producing a delayed copy of $w(t)$ for each tap. The output signals of the delay chain $w1(t)$ – $w31(t)$ are sampled and demodulated, applying the first-order difference $(1 - z^{-1})$. By using a T2B converter, the demodulated signals $s1[n]$ – $s31[n]$ form the multibit signal $y[n]$. The digital output of the converter $z[n]$ is given by the two's-complement subtraction of both single-ended branches.

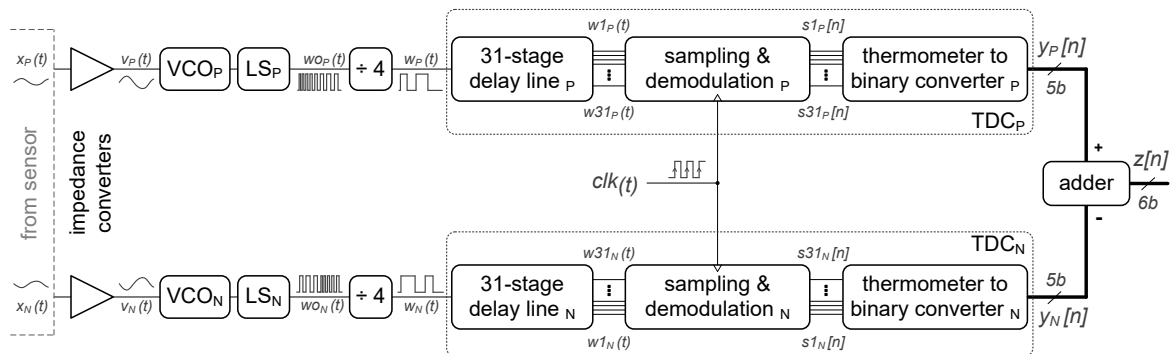


Figure 2. Architecture of the proposed pseudo-differential voltage-controlled oscillator (VCO)-based analog-to-digital converter (VCO-ADC).

The signal level applied to the microphone is expressed in a logarithmic scale, assuming 0 dB_{SPL} as a reference for the human hearing threshold of 20 μ Pa of sound pressure level (SPL). The sensitivity of the DBP MEMS to be used in the proposed ADC is 12 mV_{rms}/Pa (94 dB_{SPL}).

As mentioned above, the voltage signal $v(t)$ controls the frequency of $w(t)$, being the frequency variation in the VCO proportional to the magnitude sensed by the transducer connected to the ADC. Due to power consumption and noise reasons, it would be advisable that the target frequency of signal $w(t)$ in Figure 1 is $f_0 = 4$ MHz and the oscillator gain should be $k_{VCO} = 12$ MHz/V, with a relative frequency deviation $k_d = k_{VCO} / f_0 = 3$ V⁻¹. Given that the instantaneous oscillation frequency is

$$f(t) = f_0 \cdot (1 + k_d \cdot v(t)), \quad (1)$$

these VCO design parameters set a limit for the single-ended peak amplitude of $v(t)$ close to ± 333 mV (≈ 126 dB_{SPL}), but this is only an ideal assumption. Actually, certain factors like the distortion components can be seen as a frequency variation caused by the input signal.

Currently use of low order modulators is due to the development of new audio interfaces like MIPI SoundWire[®]. It includes support for multiple data rates in the order of tens of megahertz, which is higher than the standard sampling rates of $\Sigma\Delta$ ADCs, reducing the need for high-order modulators. In this design, the sampling frequency (f_s) is 20 MHz. However, depending on the VCO quantization architecture, this sampling rate might not be enough to achieve the resolution required for audio applications.

For example, using a single reset counter that counts the edges of $w(t)$ in a sampling clock period, the theoretical signal-to-quantization-noise ratio (SQNR) that could be achieved in Figure 1 is

$$SQNR = 6.02 \cdot \log_2 \left(\frac{2AK_{VCO}}{f_s} \right) - 3.41 + 30 \cdot \log_{10} OSR + 20 \cdot \log_{10} \left(\text{sinc} \left(\frac{1}{2OSR} \right) \right), \quad (2)$$

where A is the amplitude of the input signal and OSR is the oversampling ratio equals $f_s/(2BW)$ [19]. Applying Equation (2) and assuming a differential input signal with $A = 16.97$ mV, which corresponds to 1 Pa (94 dB_{SPL}) of sound pressure in the target MEMS microphone, with the VCO parameters depicted before, the estimated SQNR of this configuration will be limited to 47.74 dB over the audio bandwidth ($BW = 20$ kHz). Instead, a valid alternative is the use of a TDC for the quantization of the time-encoded signal $w(t)$, which emulates a much higher sampling rate than the actual sampling clock frequency. By using this solution, we can get a multibit sequence presenting an enhanced SQNR without increasing the system clock frequency and with an excellent trade-off between the VCO oscillation frequency, the number of VCO phases, and the number of stages in the TDC.

In this paper, we propose a different approach based on a high-rate sampler that interpolates samples between two clock edges and implements an analog finite-impulse-response (FIR) decimator. This system can be better explained using the pulse frequency modulation (PFM) approach introduced in [24,25]. In Figure 3a, signal $v(t)$ is passed through a PFM modulator composed of a VCO, an edge detector block, and a pulse-shaping filter $h(t)$. According to [25], the PFM modulator behaves like a signal coder, whose output spectrum reproduces the input signal together with some modulation components $M(s)$ (Figure 3c). For band-limited signals, $M(s)$ lie at frequencies much higher than the input signal.

As a virtue of the pulse shaping filter $h(t)$, the spectrum of signal $w(t)$ also has nulls at the multiples of f_s (Figure 3c). These nulls provide a first-order spectral shaping after sampling of components $M(s)$ and their aliases (Figure 3d). To further improve the SQNR, we add a low pass FIR filter implemented with continuous time delays, as shown in Figure 3b. The FIR filter reduces the level of modulation components $M(s)$ prior to sampling. As a consequence, the signal at the output of the PFM modulator can be converted into a multibit signal. As an intuitive explanation of the FIR filter operation, the power of the input signal is now multiplied by the number of stages of the delay line, while the modulation components are filtered by this extra low-pass FIR filter, as evidenced in Figure 3b. This results in an ADC resolution enhancement.

The first component of the TDC is the 31-stage delay line, shown in Figure 4a. The ideal delay time of the entire chain corresponds to the sampling period of the system, denoted by $T_s = 1/f_s$. Ideally, the time delay of every single element is T_d and equals $T_s/31$. By implementing this number of basic delay units, the resolution achieved in the proposed first-order VCO-ADC will be enough for an audio application, as will be shown afterwards from behavioral simulations. Also, the required value of T_d in every delay unit can be implemented with the selected CMOS process employing basic digital buffers.

The output taps of the delay line $w_1(t)$ – $w_{31}(t)$ are registered with the system clock and the first-order difference is applied, as shown in Figure 4b. Then, using the T2B encoder, the demodulated single-bit sequences $s_1[n]$ – $s_{31}[n]$ are combined into a 5-bit signal $y[n]$. This is the output of the single-ended channel, and it shows a first-order noise-shaping property at its power spectrum.

The pseudo-differential output of the VCO-ADC is the 6-bit sequence $z[n]$ which, unlike the single-ended configuration, cancels the even harmonic distortion components.

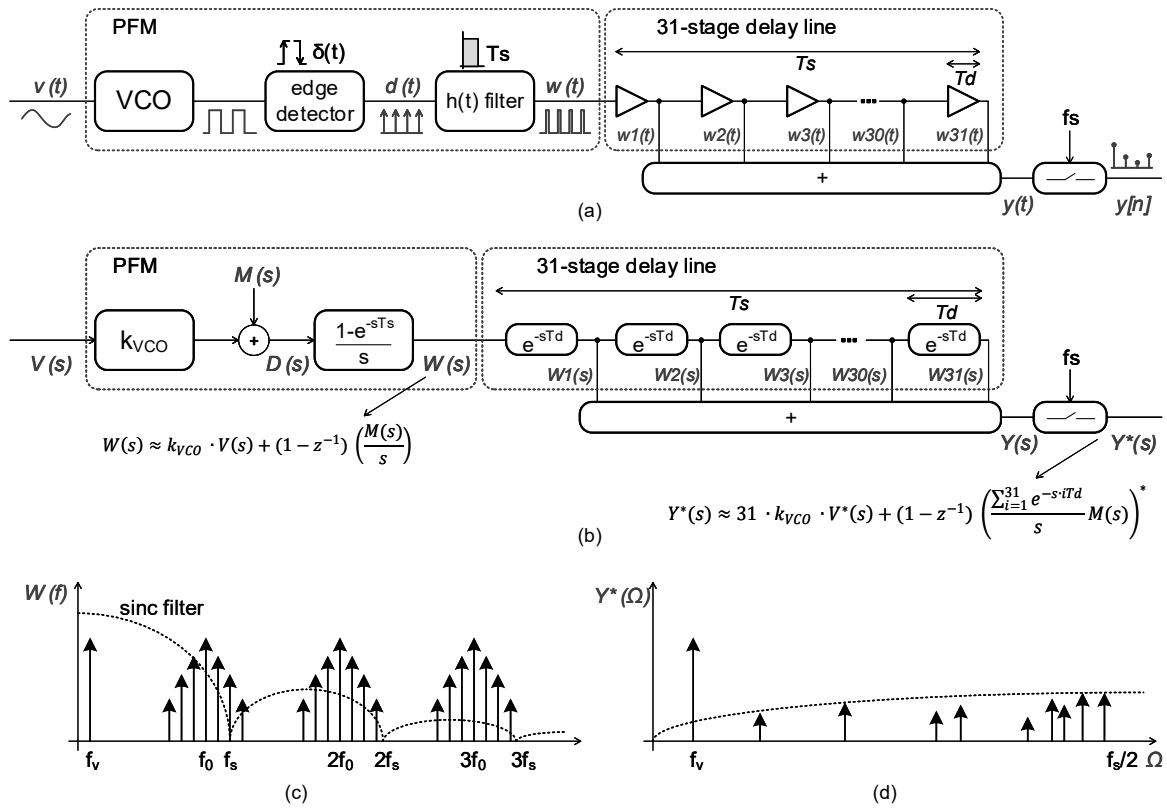


Figure 3. Pulse frequency modulation VCO-ADC: (a) Time model; (b) Laplace model; (c) filtered signal $w(t)$; (d) sampled output $y[n]$.

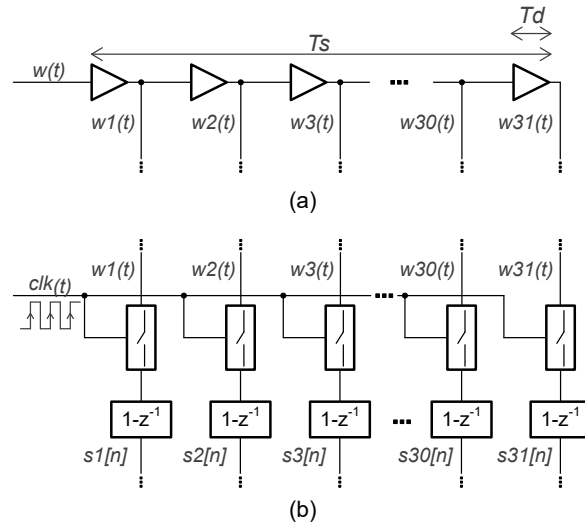


Figure 4. Time-to-digital converter: (a) 31-stage delay line; (b) sampling and demodulation schema.

Figure 5 depicts the behavior of the quantization method applied in both the single-ended channels. The signal $w(t)$ is delayed by a time T_d in each of the delay elements of the TDC, $w31(t)$ being the last delayed component with a delay time equivalent to T_s . The states of the signals $w1(t)$ – $w31(t)$ are sampled at the rising edges of the clk signal. The first difference of these sampled data is computed, generating the discrete sequences $s1[n]$ – $s31[n]$. Finally, the multibit signal $y[n]$ is given by the sum of the values of these discrete sequences at every sampling period.

Figure 6 shows the result of a behavioral simulation of the VCO-ADC architecture presented in Figure 2 without the impedance converters. The input-referred spectra have been calculated using an input tone corresponding to 94 dB_{SPL} at 1 kHz. The SQNR obtained in the audio bandwidth under these conditions is 80.9 dB and 86.1 dB-A if an A-Weighting filter is applied (Figure 6b). Note that the simulated spectra show first-order noise shaping. The A-Weighting curve is commonly used in audio measurements to mimic the sound pressure detected by the human ear, which is less sensitive to low audio frequencies.

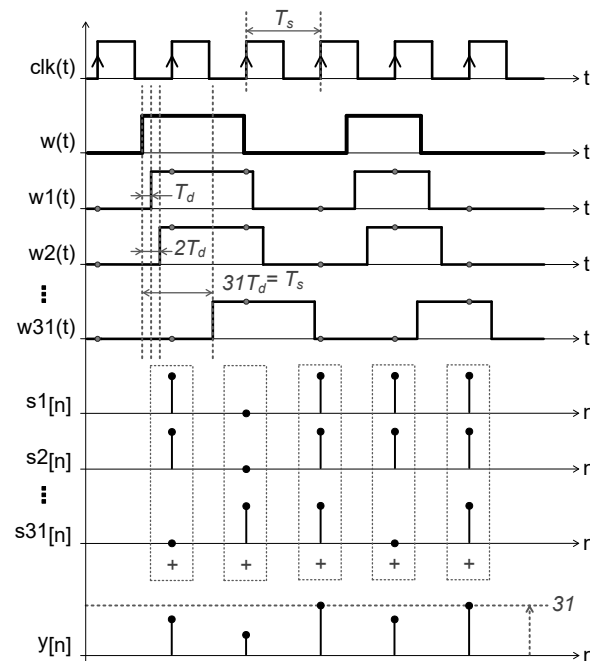


Figure 5. Chronogram of digital signals in the single-ended channel configuration.

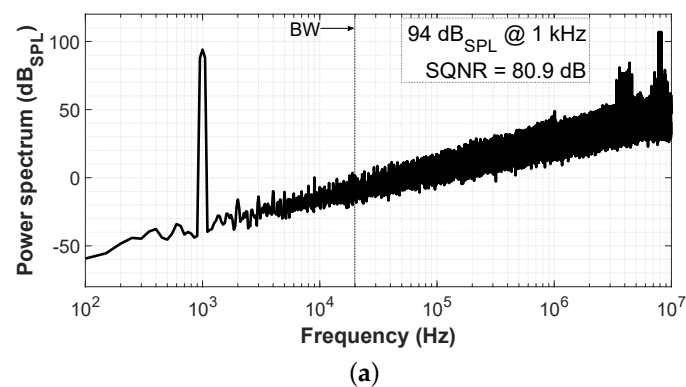


Figure 6. Cont.

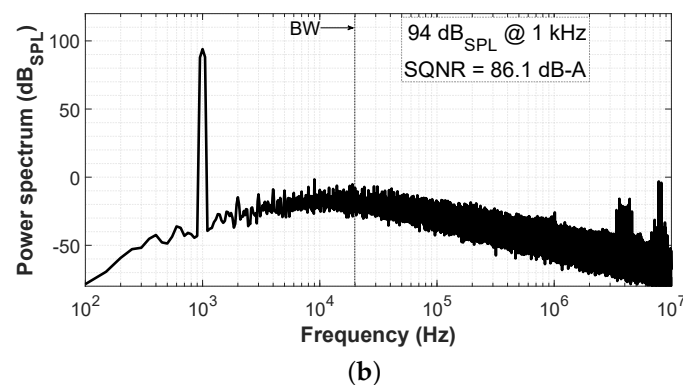


Figure 6. Simulated spectrum for an input signal of 94 dB_{SPL} at 1 kHz: (a) Non-A-Weighted; (b) A-Weighted.

Analysis of Nonidealities

As mentioned in Section 1, phase noise and distortion may affect the performance of the VCO implementation. The effect of phase noise in oscillators has been extensively studied in [26–28], concluding that phase noise is influenced by certain factors such as the topology of the oscillator, the oscillation frequency, the size of the transistors, and the power consumption. In this ADC, the VCO is optimized in terms of phase noise and distortion by applying the method described in [29]. Furthermore, the distortion is mitigated by the pseudo-differential configuration.

However, jitter present in the sampling clock may have a negative impact on the performance of the proposed VCO-ADC. Jitter can be seen as a deviation of the sampling period from the ideal value and, in real implementations, its presence may be unavoidable [30]. Some approaches for the jitter sensitivity reduction in CT-ΣΔs have been published, for example in [31,32]. Figure 7a shows the simulated SQNR for the proposed system assuming different values of clock jitter. The SQNR remains without important changes up to 1% of period jitter rms value ($T_s = 50$ ns). The performance of the system will be significantly degraded if a sampling clock with a jitter σ above 1% is applied.

Another possible nonideality that may adversely impact the performance of the system is the mismatch of the digital delay line. In a CMOS prototype implementation, due to Process-Voltage-Temperature (PVT) variations, the real delay time (T_d) of the delay elements could be different from the nominal case. Figure 7b shows the simulated SQNR for different values of delay mismatch, represented as a percent of T_d . A loss of 2 dB in the SQNR can be observed within a margin of $\pm 5\%$ of mismatch in every element of the delay line, which is a permissible variation according to the specifications posed by the target audio application.

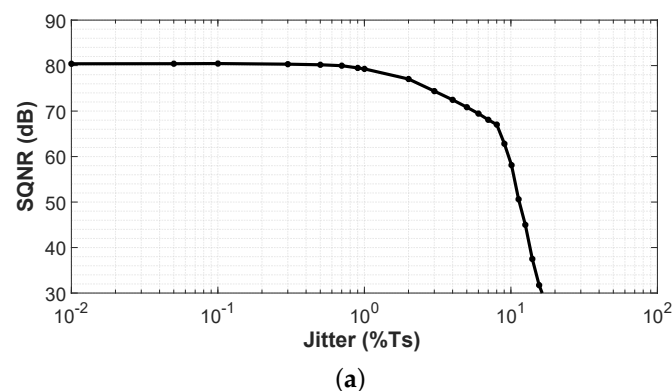


Figure 7. Cont.

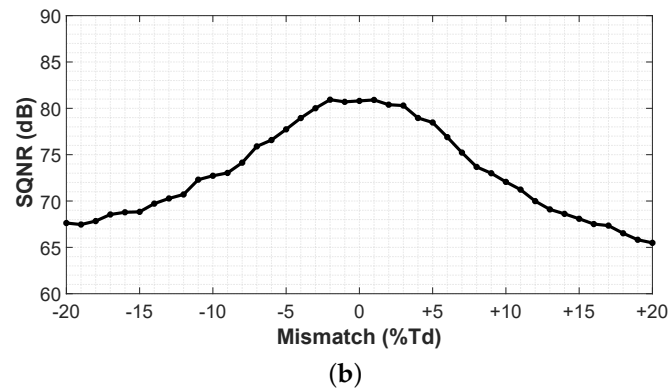


Figure 7. Simulated signal-to-quantization-noise ratio (SQNR) for an input signal of 94 dB_{SPL} at 1 kHz with (a) clock jitter variation and (b) digital delay line mismatch.

3. Circuit Design

Figure 8 shows the simplified schematic of the analog core for the single-ended channel configuration in the proposed VCO-ADC. The MEMS sensor is biased by a high-ohmic biasing circuit [8] and a NMOS (M0) transistor in the common-drain amplifier configuration. M0 acts as a voltage buffer stage that adapts the high-impedance input signal $x(t)$ into the low-impedance output signal $v(t)$. The DC operating point of the buffer is established by the gigaohms order bias resistor, denoted as R_{HO} , which is implemented by two asymmetric branches of stacked PMOS diodes. The dimensions of M0 have been estimated in order to minimize its noise contribution to the overall ADC SNR and also to keep its gain close to unity.

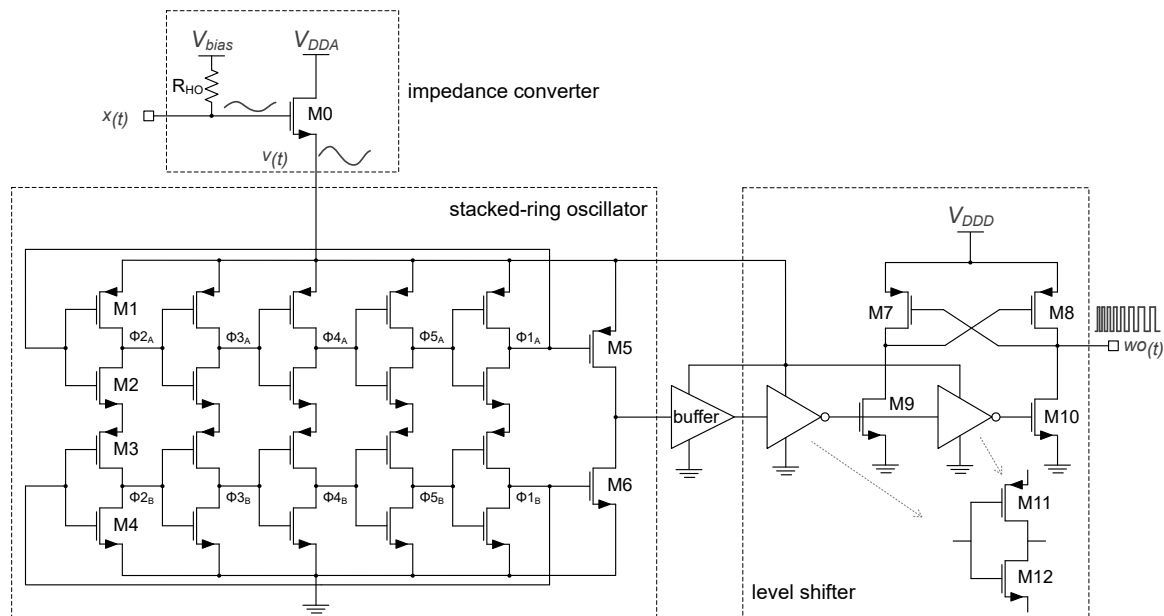


Figure 8. Single-ended analog core of the proposed VCO-ADC: Impedance converter, 5-stage stacked-RO, and differential cascode voltage switch level shifter.

The low phase noise, the ease of implementation, and the good sensitivity make the ROs excellent candidates to be used in VCO-ADCs [18–22]. In addition, one of the most important advantages of ROs is the possibility to use their multiphase output. This allows a multibit quantization approach presenting an enhanced SQNR, but at the cost of involving more complex digital circuits. In this VCO-ADC a single RO output phase has been connected to the 31-stage delay line in order to minimize the area and complexity of the digital circuitry. However, by using the implemented TDC solution,

a sufficient SQNR is achieved in the 20 kHz audio bandwidth, as has already been proven by behavioral simulations in the previous Section.

The oscillator implemented in this converter is a 5-stage inverter-based RO built with two stacked rings, which shows a better phase noise compared to the conventional single-ring architecture [33]. In Figure 8, both stacked rings, connected through the NMOS devices of the upper chain of inverters to the PMOS transistors of the lower side, oscillate like a conventional RO having the same f_0 , but with a difference in phase of 180° . Given that only one RO output phase has to be connected to the TDC, the stacked signals at ϕ_{1B} and ϕ_{1A} with amplitude $V_{SS}-v(t)/2$ and $v(t)/2-v(t)$, respectively, are combined into a single signal of amplitude $V_{SS}-v(t)$ by means of M5 and M6. A buffer is employed to square the RO output oscillation. The signal amplitude after the buffer is still variable and depends on the level of $v(t)$. Therefore, the level shifter of Figure 8 is needed to keep constant logic levels at the input of the digital circuitry, regardless of the VCO-ADC input signal. This way, the level of the time-encoded signal $wo(t)$ is always compatible with the digital supply voltage, which is $V_{DDD} = 1.8$ V in this case. The PMOS transistors of the level shifter (M7–M8) are $W/L = 1 \mu\text{m}/400 \text{ nm}$ and the NMOS (M9–M10) are $W/L = 4 \mu\text{m}/400 \text{ nm}$, whereas the transistors of the inverters (M11 and M12) are $W/L = 1.1 \mu\text{m}/400 \text{ nm}$ and $W/L = 740 \text{ nm}/400 \text{ nm}$, respectively.

The RO design process involved the methodology proposed in [29] to find an optimized oscillator in terms of phase noise, sensitivity, and distortion that benefits from a reduced simulation time. This methodology is based on periodic steady-state (PSS) sweep simulations to estimate the f_0 , the gain, and the distortion of the RO. Additionally, the periodic noise (*pnoise*) analysis is used to compute the phase noise, which can be referred to the ADC input to predict the SNR. As shown in [29], such analyses achieve very good accuracy with an important speed up in the simulation time, which allows an interactive optimization of the RO design instead of using conventional slow transient simulations.

After applying this optimization process, the selected RO have $W/L = 288 \mu\text{m}/900 \text{ nm}$ for M1–M3 and $W/L = 288 \mu\text{m}/1.9 \mu\text{m}$ for M2–M4 devices. This RO achieves $f_0 = 16.2 \text{ MHz}$ and $k_d = 3.04 \text{ V}^{-1}$, which are very close to the target values mentioned in Section 2. Figure 9 shows a predicted DR for the differential oscillator configuration, which has been estimated from the equations presented in [29]. To get these estimations, the RO simulation setup included the noise contribution of the impedance converter supplied at $V_{DDA} = V_{bias} = 1.8 \text{ V}$. The peak signal-to-noise and distortion ratio (SNDR) predicted is 80 dB-A. Note that the TDC quantization noise is not considered here and also has an impact on the overall VCO-ADC SNDR, as will be shown in Section 4.

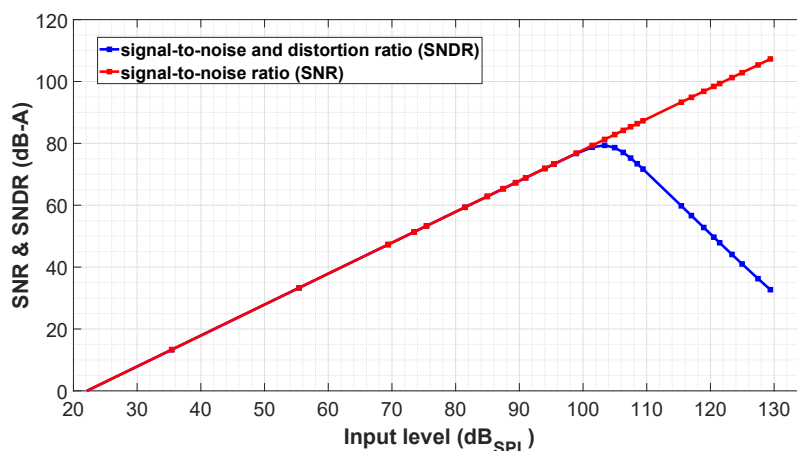


Figure 9. Simulated analog core dynamic range in the differential configuration for different input levels referred to $94 \text{ dB}_{\text{SPL}} = 12 \text{ mV}_{\text{rms}}$ (A-Weighting filter applied).

Figure 10 illustrates some of the digital blocks of the proposed VCO-ADC. The frequency division of the RO output is performed by the two D-type Flip-Flops of Figure 10a. Here, the inverted output terminal of each Flip-Flop is connected to the data input terminal, resulting in a division by a factor of four of the first Flip-Flop clock signal. The composition of the 31-stage delay line is shown in Figure 10b. Every delay unit is formed by two digital buffers, each one implemented with four inverters, where $W/L(M1) = 750 \text{ nm}/400 \text{ nm}$, $W/L(M2) = 500 \text{ nm}/400 \text{ nm}$, $W/L(M3-M5) = 500 \text{ nm}/500 \text{ nm}$, $W/L(M4-M6) = 500 \text{ nm}/1 \mu\text{m}$, $W/L(M7) = 1.42 \mu\text{m}/400 \text{ nm}$, and $W/L(M8) = 920 \text{ nm}/400 \text{ nm}$. Post-layout simulations show a total delay time of the entire chain equal to 47 ns, which is very close to the specified ADC sampling period of 50 ns. This leads to an individual delay time $T_d = 1.52 \text{ ns}$ in each unit. It is important to note that to achieve a total delay time closer to T_s requires a big effort, since the delay time of each unit is highly dependent on its layout implementation. Monte Carlo simulation results show that the T_d standard deviation value is within 5% of the margin, so the delay cell mismatch does not cause a negative impact on the system performance, as proven in Section 2.

In the proposed VCO-ADC, the specified f_s is higher than twice the maximum oscillation frequency after the divider. This allows the use of the XOR-based demodulation circuit of Figure 10c to compute the first-order difference for the delayed copies of the RO output [19,34]. This circuit accounts for the oscillation rising and falling edges, as already described in Figure 5. The remaining blocks of the digital core that process the demodulated single-bit sequences $s1[n]-s31[n]$ are the T2B and the differential two's-complement subtractor. Both of them are implemented with an array of full adders to generate the 6-bit ADC output, without carry propagate functions.

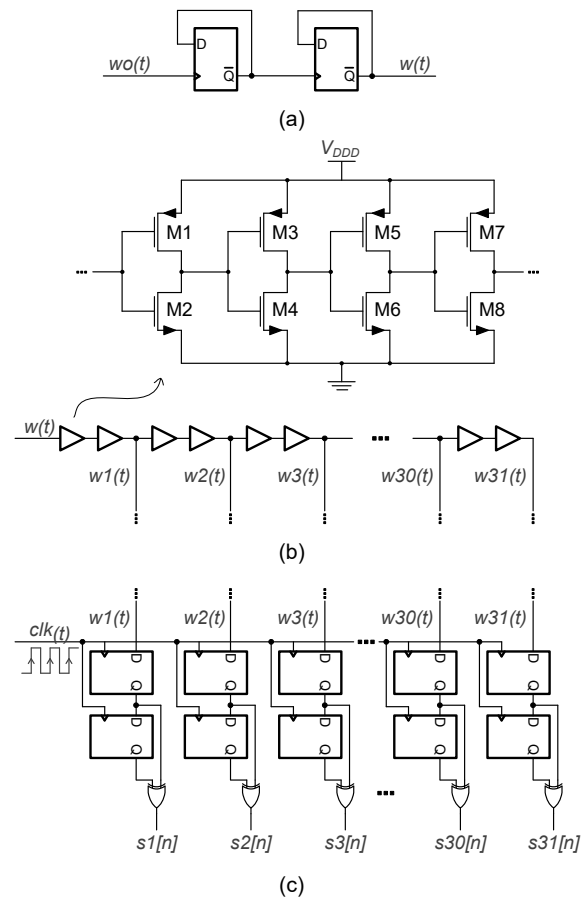


Figure 10. Single-ended digital circuitry of the proposed VCO-ADC: (a) Frequency divider; (b) 31-stage delay line; (c) sampling and demodulation circuit.

4. Experimental Results

The proposed VCO-ADC has been fabricated in a 130 nm standard CMOS process. Figure 11 shows the die dimensions, occupying a total area of 1.69 mm^2 . As can be observed from the block distribution, only 7% of the die area is used by the ADC components, resulting in an active area of 0.12 mm^2 . In the layout, both ROs have been well spaced to avoid the injection-locking effect between them. In addition, for this purpose, the ROs have been protected using guards rings. The ASIC pads include the MEMS microphone interface, the digital data output, the voltage supplies, the clock input, and some test signals like the ROs output.

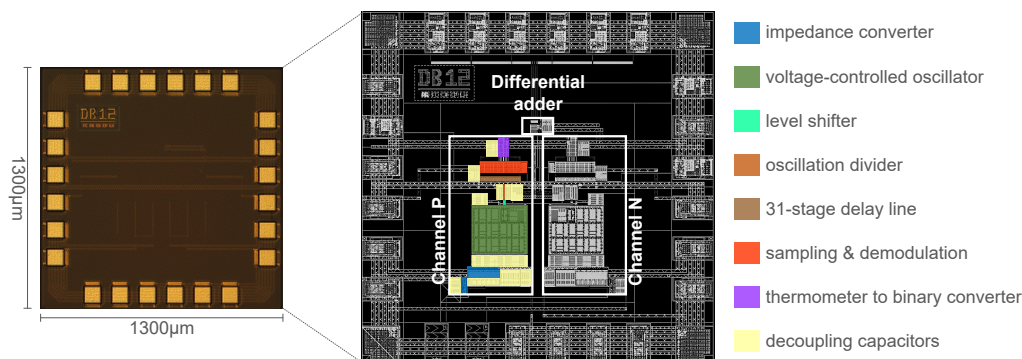


Figure 11. Die micrograph and area distribution.

4.1. Electrical Measurements

To evaluate the performance of the proposed VCO-ADC architecture, the implemented ASIC has been packaged together with a silicon capacitor array directly bonded to the ADC input, in order to emulate the real capacitance of a DBP MEMS microphone. Then, the differential ADC input signal is injected through these capacitors using the balanced output of an audio function generator. This way, by applying the proper input signal levels, the ADC behaves as if the MEMS microphone would be connected to the converter input. The 1.8 V for the V_{bias} , V_{DDA} , and V_{DDD} have been generated with batteries and using discrete LDO regulators to avoid the impact of the noise present in switching power supplies. To minimize the clock jitter, a commercial crystal oscillator of 20 MHz was employed as the system *clk*. The 6-bit VCO-ADC digital output was acquired using a logic analyzer. All the data postprocessing was done on a PC using MATLAB®.

Figure 12 shows the measured DR for a level amplitude sweep of a differential input tone at 1 kHz and applying the A-Weighting filter, as usual in audio applications. In this case, the DR reaches 100 dB-A, with a peak SNR equal to 90.82 dB-A and a peak SNDR of 77.89 dB-A. The acoustic overload point (AOP) (when the maximum allowed distortion is reached) is at 130 dB_{SPL}. The obtained AOP for a SNDR = 40 dB-A is good enough for low-cost digital microphones [20]. This translates into a reduced complexity of the proposed architecture since there is no need for linearity compensation techniques, which may have a negative impact on area and power consumption [22].

The spectra of Figure 13 are obtained applying in the function generator the signal equivalent to 1 Pa of sound pressure in the MEMS microphone, that is, the 94 dB_{SPL} reference at 1 kHz. The achieved SNDR is 59 dB or 64 dB-A if the A-Weighting filter is applied (Figure 13b). At this level, the SNDR limit is imposed only by the flicker, thermal, and quantization noise. Note that the flicker noise is attenuated by the A-Weighting curve. The sidebands of the VCO appear as high-frequency components.

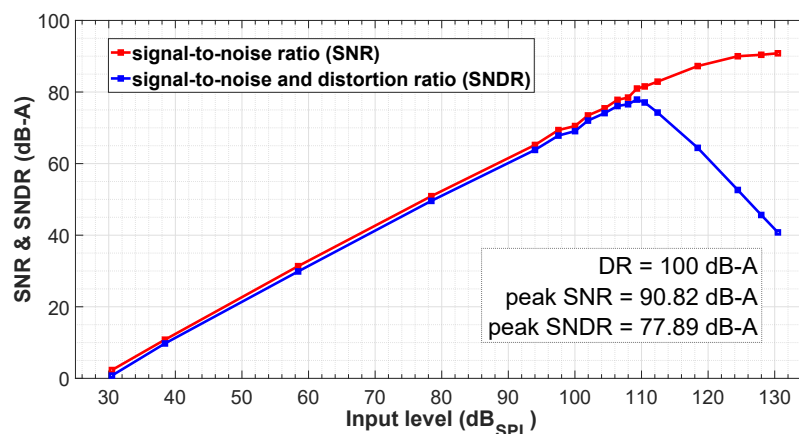


Figure 12. Measured dynamic range for different input levels referred to 94 dB_{SPL} = 12 mV_{rms} (A-Weighting filter applied).

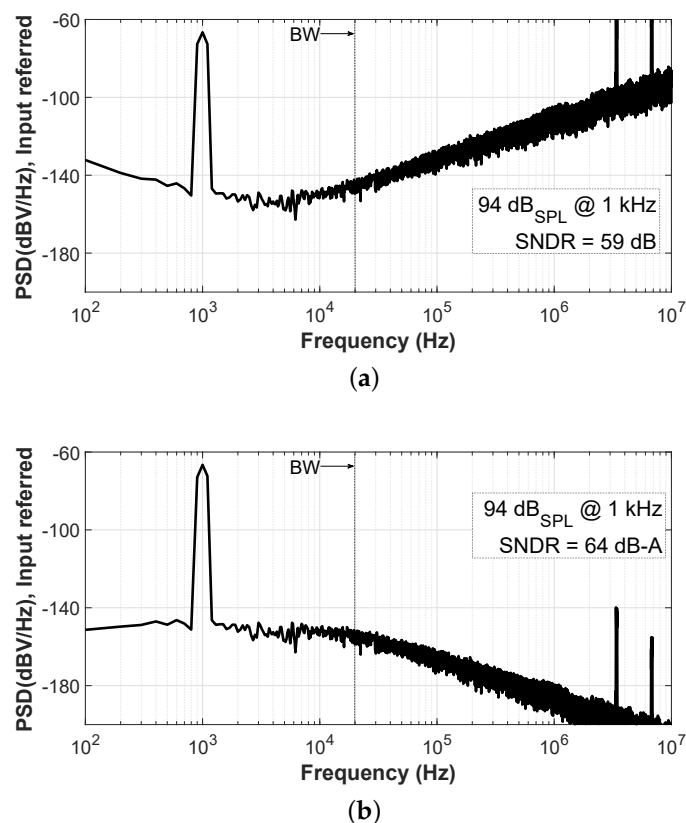


Figure 13. Measured spectrum for an input signal of 94 dB_{SPL} (12 mV_{rms}) at 1 kHz: (a) Non-A-Weighted; (b) A-Weighted.

Another interesting point corresponds to the level for the maximum SNDR. This condition happens when the acoustic input level reaches 109 dB_{SPL} in the sensor. Figure 14 shows the ADC output spectra when the SNDR is maximized. It can be seen that, due to the pseudo-differential configuration, the 2nd harmonic component is canceled but the 3rd one starts to be visible. The distortion for higher input levels is limited by the nonlinearity of the ROs. Moreover, different input signal levels produce wider or narrower modulation sidebands between spectra in Figures 13 and 14, as shown in [24].

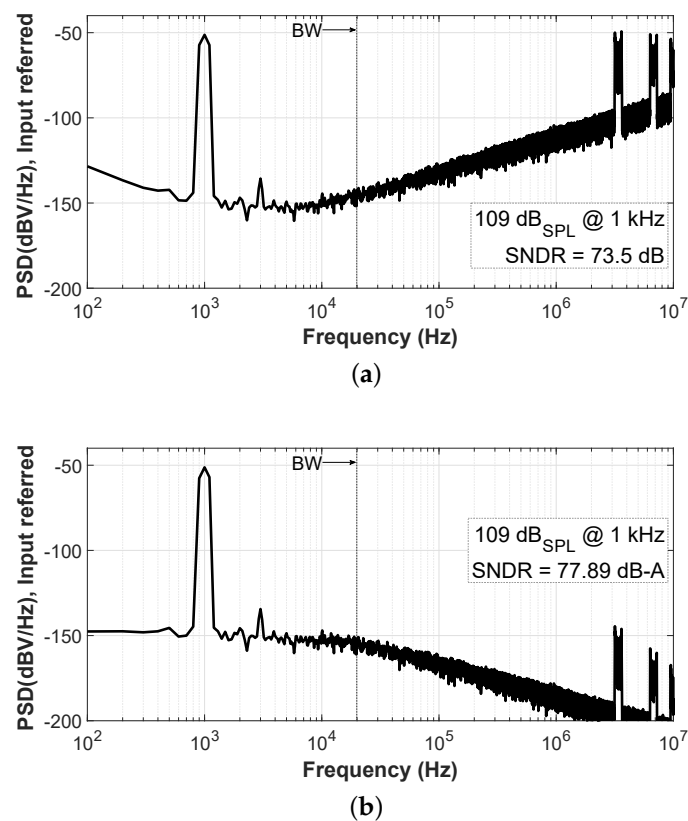


Figure 14. Measured spectrum for an input signal of 109 dB_{SPL} (67.5 mV_{rms}) at 1 kHz: (a) Non-A-Weighted; (b) A-Weighted.

Figure 15 shows the VCO-ADC frequency response from 500 Hz to 15 kHz for a 94 dB_{SPL} equivalent input. In this range, the SNDR shows a maximum variation close to 1 dB. Note that the A-Weighting filter is not applied here, in order to avoid the nonflat characteristic of the A-Weighting curve in the measured frequency response.

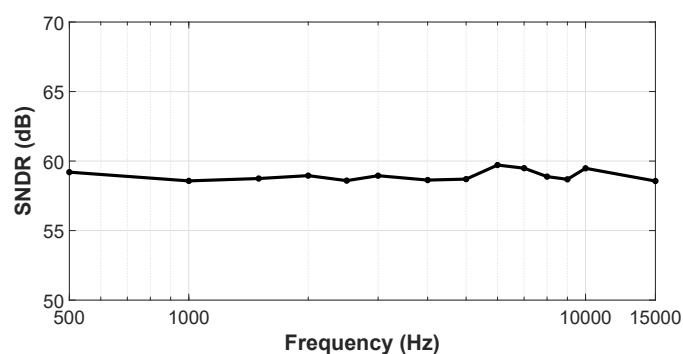


Figure 15. Measured frequency response (500 Hz to 15 kHz) for an input signal of 94 dB_{SPL} (12 mV_{rms}).

4.2. Acoustical Measurements

Apart from the described electrical evaluations, some acoustical measurements have been performed. This time, the implemented ASIC and the DBP MEMS microphone have been directly bonded over a low-leakage PCB, which includes a sound port in the sensor bottom, enabling the contact of sound pressure against the MEMS membrane. To exclude the external acoustic noise and to keep the level of the audio signal applied during the measurements under control, an anechoic test box has been used. A box built-in speaker was employed to generate the audio test tone. Given that

the TDC performance was checked in the electrical measurements, in order to keep the simplicity of the test PCB and to reduce the wire connections out of the box, only the ROs test output was acquired with an oscilloscope and then postprocessed in MATLAB[®]. Figure 16 depicts the test fixture used for the acoustical characterization of the sensor.

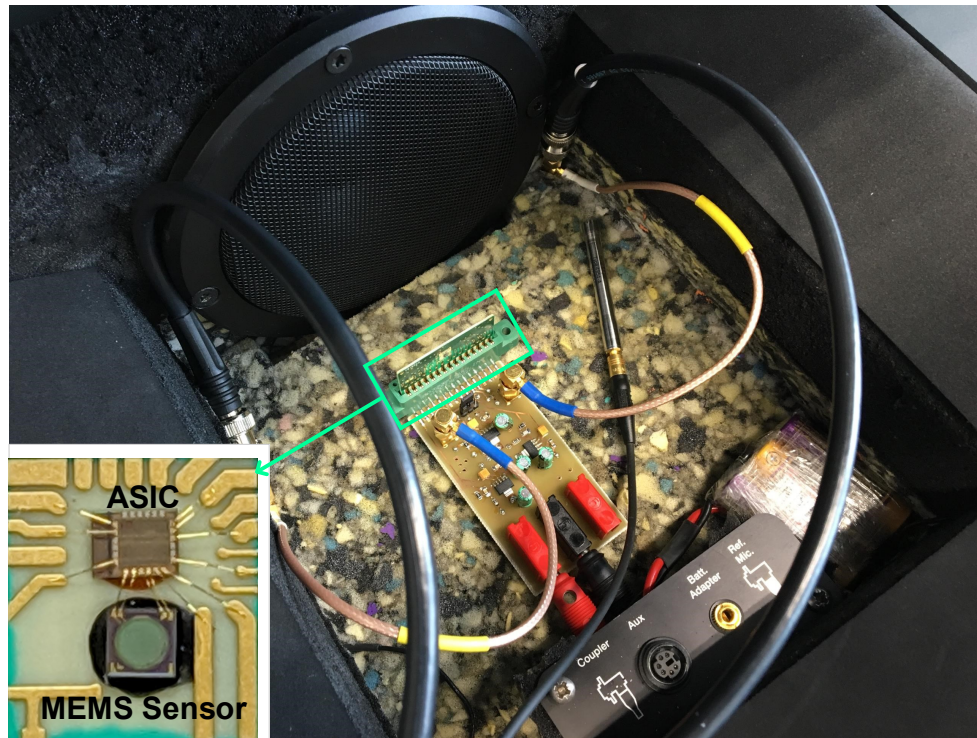


Figure 16. Test fixture used in the acoustical measurements.

Figure 17 shows the differential ROs output spectra for an audio tone of 94 dB_{SPL} at 1 kHz, achieving a SNR = 46.3 dB and the SNDR = 44.6 dB (Figure 17a). With the A-Weighting correction, the SNR reaches 52.7 dB-A and the SNDR equals 47.2 dB-A (Figure 17b). The difference in sensitivity and distortion with the results presented in Figure 13 is due to two main facts. First, in the test fixture shown in Figure 16, a MEMS acoustic package is missing, so the back volume of the MEMS microphone becomes infinite. The optimum mechanical sensitivity of the MEMS is achieved for a specific back volume, which is accurately defined in the packaging process. Moreover, to obtain a good sensitivity, the MEMS membrane should be biased with a high-voltage signal in the order of 6–9 V, depending on the MEMS characteristics. Usually this is achieved with an on-chip charge pump, which has not been included in this test chip. Anyhow, the most important outcome from the acoustical measurements is that the proposed VCO-ADC architecture is audio-responsive, presenting fully compatibility with the MEMS microphone sensors.

Measurements show that the implemented VCO-ADC architecture has a current consumption of 750 μ A at 1.8 V, including all the blocks of Figure 11. The Schreier figure-of-merit (FoM), expressed as $\text{FoM}_S = \text{DR} + 10\log_{10}(\text{BW}/\text{Power})$, is 171.7 dB.

The measurement results presented in this section are valid for the case when a sampling clock with a reduced jitter is employed. As shown in Section 2, the proposed VCO-ADC shows a good sensitivity against clock jitter but SC- $\Sigma\Delta$ s are less tolerant to this problem. Another disadvantage of the proposed oscillator-based architecture is the possible injection-locking between ROs. Some actions should be taken in the layout implementation to avoid this effect.

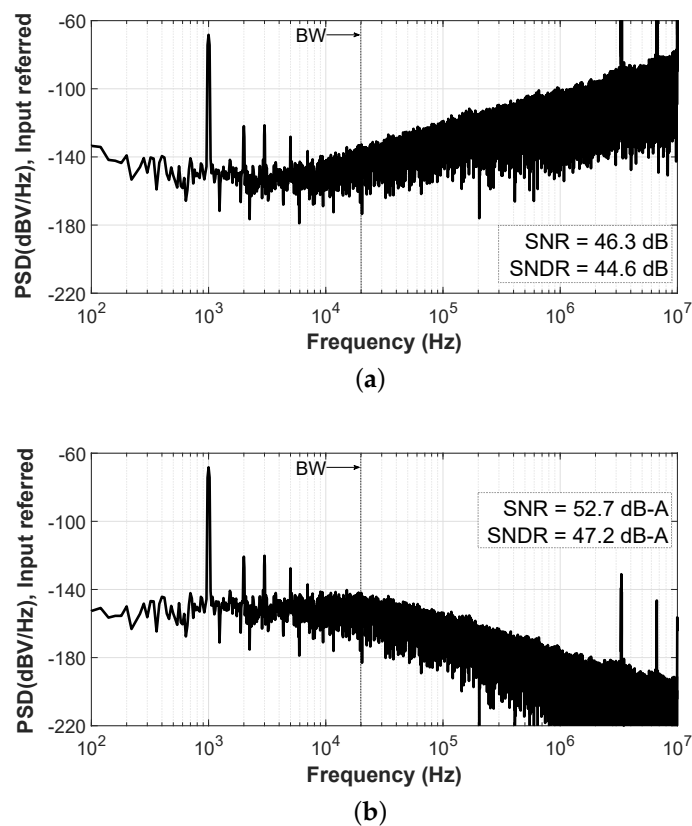


Figure 17. Measured spectrum for an acoustic tone of 94 dB_{SPL} at 1 kHz: (a) Non-A-Weighted; (b) A-Weighted.

5. Conclusions

This paper presents a pseudo-differential VCO-based readout circuit for a capacitive MEMS sensor, suitable for low-cost digital microphones. The proposed VCO-ADC architecture is mostly digital, being a CMOS scalable alternative solution in terms of area and power consumption, in contrast to SC- $\Sigma\Delta$ -based readout circuits for MEMS microphones. It is mainly composed of a stacked-ring oscillator and a time-to-digital converter. A prototype has been fabricated in 130 nm CMOS process to validate the proposed circuit by means of electrical and acoustical measurements, occupying an effective area of 0.12 mm². Electrical measurements exhibit a peak SNR of 90.8 dB-A and a peak SNDR of 77.9 dB-A. The dynamic range reached is 100 dB-A and the acoustic overload point is 130 dB_{SPL}, with a current consumption of 750 μ A powered at 1.8 V. Finally, acoustical measurements using a DBP MEMS microphone, show that the proposed ADC architecture is a good candidate to replace the traditional $\Sigma\Delta$ -based readout circuits in audio applications. A future line of research may concentrate on improving the power consumption of the digital architecture by extending the time-to-digital converter to all the VCO phases or implementing a higher-than-sampling frequency VCO coupled to some phase-counting circuit.

Author Contributions: A.Q., F.C. and L.H. are responsible for the VCO-ADC architecture design. A.Q. and C.P. implemented the CMOS prototype. A.Q. conceived and performed the prototype measurements. A.Q. and L.H. analyzed the data. A.Q. wrote the paper. C.B. managed and supported the prototype implementation and measurements. A.W. and L.H. supervised the project development and proofread the paper.

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