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# An Improved Scheduling Algorithm for Data Transmission in Ultrasonic Phased Arrays with Multi-Group Ultrasonic Sensors

Wenming Tang <sup>1</sup>, Guixiong Liu <sup>1,\*</sup>, Yuzhong Li <sup>1</sup> and Daji Tan <sup>2</sup>

<sup>1</sup> School of Mechanical & Automotive Engineering, South China University of Technology, Guangzhou 510641, China; tang.wm@mail.scut.edu.cn (W.T.); JDXlyz@hzcollege.com (Y.L.)

<sup>2</sup> Guangzhou Doppler Electronic Technologies Co., Ltd., Guangzhou 510663, China; tandaji@cndoppler.cn

\* Correspondence: megxliu@scut.edu.cn; Tel.: +86-020-8711-0568

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**Abstract:** High data transmission efficiency is a key requirement for an ultrasonic phased array with multi-group ultrasonic sensors. Here, a novel FIFOs scheduling algorithm was proposed and the data transmission efficiency with hardware technology was improved. This algorithm includes FIFOs as caches for the ultrasonic scanning data obtained from the sensors with the output data in a bandwidth-sharing way, on the basis of which an optimal length ratio of all the FIFOs is achieved, allowing the reading operations to be switched among all the FIFOs without time slot waiting. Therefore, this algorithm enhances the utilization ratio of the reading bandwidth resources so as to obtain higher efficiency than the traditional scheduling algorithms. The reliability and validity of the algorithm are substantiated after its implementation in the field programmable gate array (FPGA) technology, and the bandwidth utilization ratio and the real-time performance of the ultrasonic phased array are enhanced.

**Keywords:** ultrasonic phased array; scheduling algorithm; FIFOs; multi-group sensors; FPGA; bandwidth utilization

## 1. Introduction

The technology of multi-group ultrasonic sensors that consist of lots of piezoelectric elements and various scanning patterns of an ultrasonic phased array (UPA) have recently attracted widespread attention in the non-destructive testing area [1,2]. The UPA produces a series of the ultrasonic waves controlled by the amplitudes and phases of the electrical pulses to excite a series of elements of the sensors. The waves can easily penetrate inside some materials by adjusting their radiation direction to synthesize flexible and rapidly focused scanning ultrasonic beams. The parameters of beams such as angles, focal distances, and focal spot sizes can be readily tuned with suitable software. Therefore, the beams can be used to detect defects that possibly occur at random positions of the materials [3–6].

To increase the focusing ability, a UPA instrument is often equipped with multiple ultrasonic sensors to collect the ultrasonic echo data from different directions. Each sensor can work in one or more groups so that a variety of scanning modes are generated [7–10], which can be called as a multi-group scanning, and each group scanning includes many focused beams. Hence, the number of the sensors and the scanning groups are two important factors to determine detection accuracy [11,12], such as size, location, and orientation of defects. For example, Song et al. verified that a large-aperture hemispherical phased array can restore a sharp focus and maximize acoustic energy delivery at target tissue [11]. Regardless of the orientation of individual focused beams, the multiple focused beams can change their focal depths and sweeping angles through the phase interference. As a consequence, it is possible to precisely detect the position and the size of defects by means of increasing the number of the

sensors, the scanning groups, and the focused beams. However, this strategy will in turn significantly increase the amount of scanning data in the process of the defect detection, which makes these data difficult to be transmitted to a peripheral through a single (or small quantity) high-speed serial bus, and subsequently produces an ultrasound image.

Each focused beam often brings different sampling rates and sizes of data stream. During the transmission process, different data streams compete against each other to gain access to the unique high-speed serial bus. An excellent transmission scheduling algorithm should allow all the data streams to be transferred to a peripheral without any blocking in a serialized way. Otherwise, the data streams would be blocked or severely delayed. Therefore, it is very desirable to design an effective algorithm to serially transmit a great amount of the data streams. Several well-known scheduling algorithms have been proposed, such as Time Division Multiple Access (TDMA) [13] and Round Robin (RR) [14]. The verification, analysis, and comparison of the two algorithms were presented in literature [15], which proves that the TDMA strategy based on the fixed allocation of a time slot to each master process may lead to important latencies as a time slot, and the RR protocol allows any unused slots to be reallocated to a master process to provide higher bandwidth. Unfortunately, the process of the reallocation will make the time slice resources more fragmented, and increase the complexity of the scheduling algorithm. Multiple examples of implementation for the scheduling algorithm are available in the open literatures [16–23]. Srinivasan et al. designed a self-configuring scheduling protocol for ultrasonic sensor systems by using an algorithm of the timeslot allocation, which simplified the deployment of the present detection system [16]. Long et al. proposed a time-division-multiple-access-based energy consumption balancing algorithm for the general k-hop wireless sensor networks, where one data packet is collected in one cycle, and the results demonstrated the effectiveness of the algorithm in terms of energy efficiency and time slot scheduling [19]. However, although these strategies can effectively improve the efficiency of the data transmission, they increase the complexities of both hardware and software, and their application scopes are limited, which makes such strategies not suitable for UPA of the multi-group sensor scanning system because of limited hardware and software resources and high real-time request.

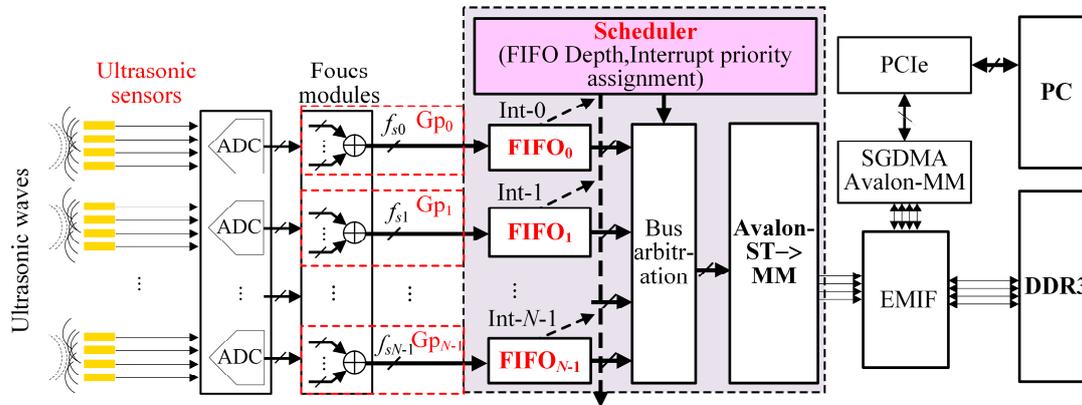
FPGA, which is short for the term field programmable logic gate array, has the characteristics of static system repeatable programming and dynamic system reconfiguration, so that hardware can be modified programmatically, and FPGA also is a special kind of ASIC with the advantages of parallel processing, high speed and flexibility. In this paper, we used a series of FIFOs as high-speed caches and cache times as weights to propose a novel FIFOs and bandwidth-sharing scheduling (MFBSS) algorithm of the data transmission, where the lengths of the FIFOs are achieved by a series of multivariate equations. Actually, the algorithm shows many advantages such as real-time and high efficiency when it is implemented by FPGA technology. As far as the UPA system of the array sensors is concerned, we designed a data stream transmission scheduling mode based on the MFBSS algorithm, with which reading operations among all the FIFOs shares a fast reading bus without time slot waiting when the reading bus switches between any two FIFOs. Hence, such algorithm gives the maximum bandwidth utilization ratio and improves the real-time performance of the UPA instruments with minimal consumption of time and space resources.

In Section 2 of the paper, we will describe the data transmission of ultrasonic scanning for UPA [24–26]. In Section 3, we will study scheduling mechanism of the MFBSS algorithm for the data transmission. Section 4 will describe the results of implementation for the scheduling algorithm by FPGA technology. Finally, Section 5 will summarize the research to derive the conclusion.

## 2. Multi-Group Sensor Scanning Ultrasonic Data Transmission

Figure 1 shows the UPA data transmission framework of the bandwidth-sharing with multiple scanning patterns [7–10]. In order to realize the optimal sampling of the UPA's echoes, different frequency echoes should be digitized with different sampling frequencies [27–29]. A sensor with a frequency of  $f_p$  Hz produces ultrasonic echoes with the same frequency after excitation, and thus the

sampling frequency is  $f_s = K \times f_p$  Hz ( $K$  is a scaling factor, and  $K \geq 2$ ). Hence,  $N$ -group sensors can form  $N$ -group scanning patterns, generating  $N$  sampling frequencies ( $f_{s0} \sim f_{sN-1}$ , where 0 and  $N - 1$  represent the numbers of sampling) and forming  $N$  focusing beams with specific speeds and sizes.



**Figure 1.** The diagram of the ultrasonic data transmission for the multi-sensor scanning.

As shown in Figure 1, the data of various scanning groups such as  $Gp_0, Gp_1, \dots, Gp_{N-1}$  produced from the ultrasonic sensors are written into  $FIFO_0, FIFO_1, \dots, FIFON-1$ , respectively, which are cached by a DDR3 through the Avalon bus in the bandwidth-sharing way [30]. Then, the data from the DDR3 are transmitted to the host computer through the PCIe bus [31,32]. The entire data transmission process is controlled by a bandwidth scheduler, which is composed of a controller with all the FIFOs' lengths and a reading arbiter, and usually runs the following scheduling algorithms such as First Come First Serve (FCFS), TDMA and Equal Time Slice Polling Scheduling (ETSPS) based on the principle of the RR scheduling which will be mentioned in Section 4, and so on. This paper will adopt the MFBSS algorithm to realize reading operations from every FIFO without time slot waiting through adjusting the lengths of FIFOs, timings of the reading and writing, and priority of the interrupts. Therefore, this algorithm can not only ensure the data transmission synchronization but also maximize the bandwidth utilization in all groups, which is readily implemented by FPGA technology with parallel processing.

### 3. Data Transmission Scheduling Mechanism of MFBSS Algorithm

#### 3.1. The principle of the Maximal Bandwidth Utilization

To evaluate the utilization ratio of the data transmission bandwidth of the  $N$ -group scanning in the multi-input and single-output interfaces of the UPA system, the following requirements are satisfied:

- Data transmission models  $Gp(n), n = 0, 1, \dots, N - 1$  are independent from each other and have identical distributions for every group.
- The sum of the data bandwidth  $[\sum_{n=0}^{N-1} B_{v-Gp}(n)]$  of all the groups and the sum of the memory bandwidth ( $\sum B_{v-RAM}$ ) and the sum of the transmission bandwidth ( $\sum B_{v-Trans}$ ) of the peripheral need to satisfy the following inequality:

$$\sum_{n=0}^{N-1} B_{v-Gp}(n) \leq \min(\sum B_{v-RAM}, \sum B_{v-Trans}) \quad (1)$$

The defined parameters of the  $N$ -group scanning and the  $N$  FIFOs caches are listed in Table 1. The writing bandwidth and the reading bandwidth of the  $n$ th  $FIFO_n$  are  $V_W(n) [V_W(n) = f_{sn} \times \Delta B]$  and  $V_R$

bit/s, respectively. The sum of the writing bandwidth of all the FIFOs [ $\sum_{n=0}^{N-1} V_W(n)$ ] should equal to the sum of the transmission bandwidth of the  $N$ -group scanning data [ $\sum_{n=0}^{N-1} B_{v-Gp}(n)$ ], i.e.,  $\sum_{n=0}^{N-1} V_W(n) = \sum_{n=0}^{N-1} B_{v-Gp}(n)$ . Likewise, the sum of the reading bandwidth ( $V_R$ ) of all the FIFOs should equal to the sum of the transmission bandwidth of the DDR3 bandwidth ( $\sum B_{v-RAM}$ ), i.e.,  $V_R = \sum B_{v-RAM}$ . When the Equation (1) becomes an equality, the maximum bandwidth utilization ratio is achieved, i.e., the single-output bandwidth equals to the sum of the multi-input bandwidths from the FIFOs. Consequently, the mathematical principle of the maximal bandwidth utilization ratio can be written as Equation (2).

**Table 1.** The parameters of the  $N$  groups and the  $N$  FIFOs caches.

Group Number	Sampling Rate (Hz)	Bit Width	Cache	Length of FIFO	Input Width of FIFO (bit)	Writing Bandwidth (bit/s)	Output Width of FIFO (bit)	Reading Bandwidth (bit/s)
0	$f_{s0}$	$\Delta B$	FIFO <sub>0</sub>	$L(0)$	$\Delta B_W$	$V_W(0)$	$\Delta B_R$	$V_R$
1	$f_{s1}$	$\Delta B$	FIFO <sub>1</sub>	$L(1)$	$\Delta B_W$	$V_W(1)$	$\Delta B_R$	$V_R$
2	$f_{s2}$	$\Delta B$	FIFO <sub>2</sub>	$L(2)$	$\Delta B_W$	$V_W(2)$	$\Delta B_R$	$V_R$
...	...	...	...	...	...	...	...	...
$N - 1$	$f_{sN-1}$	$\Delta B$	FIFO <sub><math>N-1</math></sub>	$L(N - 1)$	$\Delta B_W$	$V_W(N - 1)$	$\Delta B_R$	$V_R$

$$\begin{cases} \sum_{n=0}^{N-1} B_{v-Gp}(n) \leq \sum B_{v-RAM} \\ \sum_{n=0}^{N-1} B_{v-Gp}(n) = \sum_{n=0}^{N-1} V_W(n) \\ \sum B_{v-RAM} = V_R \end{cases} \Rightarrow V_R = \sum_{n=0}^{N-1} V_W(n) \tag{2}$$

### 3.2. Realization of the Maximal Bandwidth Utilization Ratio

According to Equation (2), the mathematical model of the  $N$  FIFOs' length functions of  $L(i)$ ,  $i = 0, 1, \dots, N - 1$ , [ $L(0) \leq L(1) \leq \dots \leq L(N - 1)$ , FIFO<sub>0</sub>, FIFO<sub>1</sub>, ..., FIFO <sub>$N-1$</sub> ] can be described as follows:

- Assuming that at the moment  $T_i^j$ , when the FIFO <sub>$i$</sub>  is read until empty, the reading operation of the FIFO <sub>$i$</sub>  will be disabled.
- At the next  $T_i^{j+1}$ , when the FIFO <sub>$i$</sub>  is full and the amount of the data is  $L(i)$  ( $i = 0, 1, \dots, N - 1$ ), the reading operation of the FIFO <sub>$i$</sub>  will be enabled.

When the FIFO <sub>$i$</sub>  transfers from empty to full (where the consumed time is  $\Delta T_i = T_i^{j+1} - T_i^j = \frac{L(i)}{V_W(i)}$  and a reading interrupt is produced), the FIFO <sub>$i$</sub>  will gain access to the reading of the Avalon bus. During this process, the other FIFOs with the number of  $0, 1, \dots, i + 1, i + 2, \dots, N - 1$  have also transferred from full to empty with the consumed time of  $\Delta T'_i = \sum_{k=0, k \neq i}^{N-1} \frac{L(k)}{V_R - V_W(k)}$ . The time slot transition diagram of the  $N$  FIFOs reading operations is shown in Figure 2. Because  $\Delta T_i = \Delta T'_i$ , i.e.,  $\Delta T'_i - \Delta T_i = 0$ ,  $i = 0, 1, \dots, N - 1$ , the mathematical equations of the  $N$  FIFOs' length functions of  $L(i)$ ,  $i = 0, 1, \dots, N - 1$  can be easily described in Equation (3).

$$\left\{ \begin{array}{l} -\frac{L(0)}{V_W(0)} + \frac{L(1)}{V_R - V_W(1)} + \frac{L(2)}{V_R - V_W(2)} + \dots + \frac{L(N-1)}{V_R - V_W(N-1)} = 0 \\ \frac{L(0)}{V_R - V_W(0)} - \frac{L(1)}{V_W(1)} + \frac{L(2)}{V_R - V_W(2)} + \dots + \frac{L(N-1)}{V_R - V_W(N-1)} = 0 \\ \vdots \\ \frac{L(0)}{V_R - V_W(0)} + \frac{L(1)}{V_R - V_W(1)} + \dots + \frac{L(N-2)}{V_R - V_W(N-2)} - \frac{L(N-1)}{V_W(N-1)} = 0 \end{array} \right. \quad (3)$$

where  $L(i) \neq 0, i = 0, 1, \dots, N - 1$  in Equation (3). A series of new variables are given in Equation (4) for the simplification of Equation (3).

$$\left\{ \begin{array}{l} K'_0 = \frac{1}{V_W(0)}, \quad K'_1 = \frac{1}{V_W(1)}, \dots, K'_{N-1} = \frac{1}{V_W(N-1)} \\ K_0 = \frac{1}{V_R - V_W(0)}, K_1 = \frac{1}{V_R - V_W(1)}, \dots, K_{N-1} = \frac{1}{V_R - V_W(N-1)} \\ V_R = \sum_{i=0}^{N-1} V_W(i) \end{array} \right. \quad (4)$$

Equation (3) is transformed into a matrix of Equation (5):

$$\begin{pmatrix} -K'_0 & K_1 & \dots & K_{N-1} \\ K_0 & -K'_1 & \dots & K_{N-1} \\ \vdots & \vdots & \ddots & \vdots \\ K_0 & K_1 & \dots & -K'_{N-1} \end{pmatrix} \begin{pmatrix} L(0) \\ L(1) \\ \vdots \\ L(N-1) \end{pmatrix} = \begin{pmatrix} 0 \\ 0 \\ \vdots \\ 0 \end{pmatrix} \quad A = \begin{pmatrix} -K'_0 & K_1 & \dots & K_{N-1} \\ K_0 & -K'_1 & \dots & K_{N-1} \\ \vdots & \vdots & \ddots & \vdots \\ K_0 & K_1 & \dots & -K'_{N-1} \end{pmatrix}, \vec{L} = \begin{pmatrix} L(0) \\ L(1) \\ \vdots \\ L(N-1) \end{pmatrix}, \vec{0} = \begin{pmatrix} 0 \\ 0 \\ \vdots \\ 0 \end{pmatrix} \quad A \cdot \vec{L} = \vec{0} \quad (5)$$

The matrix  $A$  is achieved by elementary row transformation, and then the triangular array is applied:

$$A \sim \begin{pmatrix} -K'_0 & K_1 & \dots & \dots & K_{N-1} \\ K_0 + K'_0 & -(K_1 + K'_1) & 0 & \dots & 0 \\ 0 & \vdots & \vdots & \vdots & \vdots \\ \vdots & \vdots & K_{N-3} + K'_{N-3} & -(K_1 + K'_{N-2}) & 0 \\ 0 & \dots & 0 & K_{N-2} + K'_{N-2} & -(K_{N-1} + K'_{N-1}) \end{pmatrix} \sim \begin{pmatrix} f_K(x_0) & K_1 & \dots & K_{N-1} \\ 0 & f_K(x_1) & \dots & K_{N-1} \\ \vdots & \vdots & \ddots & \vdots \\ 0 & \dots & 0 & f_K(x_{N-1}) \end{pmatrix} \quad (6)$$

$f_K(x_{i+1}) = \frac{K_{i+1} + K'_{i+1}}{K_i + K'_i} \cdot f_K(x_i) + K_{i+1}, i = 0, 1, \dots, N - 2, f_K(x_0) = -K'_0$ , and  $f_K(x_{i+1})$  can be done by using the following recursion:

$$\begin{aligned} f_K(x_{i+1}) &= \frac{K_{i+1} + K'_{i+1}}{K_i + K'_i} \cdot \left( \frac{K_i + K'_i}{K_{i-1} + K'_{i-1}} \cdot \left( \dots \left( \frac{K_1 + K'_1}{K_0 + K'_0} \cdot f_K(x_0) + K_1 \right) + \dots \right) + K_i \right) + K_{i+1} \\ &= \frac{K_{i+1} + K'_{i+1}}{K_i + K'_i} \cdot \frac{K_i + K'_i}{K_{i-1} + K'_{i-1}} \cdot \dots \cdot \frac{K_1 + K'_1}{K_0 + K'_0} \cdot f_K(x_0) + \frac{K_{i+1} + K'_{i+1}}{K_i + K'_i} \cdot \frac{K_i + K'_i}{K_{i-1} + K'_{i-1}} \cdot \dots \cdot \frac{K_2 + K'_2}{K_1 + K'_1} \cdot K_1 \\ &\quad + \frac{K_{i+1} + K'_{i+1}}{K_i + K'_i} \cdot \frac{K_i + K'_i}{K_{i-1} + K'_{i-1}} \cdot \dots \cdot \frac{K_3 + K'_3}{K_2 + K'_2} \cdot K_2 + \dots + \frac{K_{i+1} + K'_{i+1}}{K_i + K'_i} \cdot K_i + K_{i+1} \\ &= \frac{K_{i+1} + K'_{i+1}}{K_0 + K'_0} \cdot f_K(x_0) + \frac{K_{i+1} + K'_{i+1}}{K_1 + K'_1} \cdot K_1 + \frac{K_{i+1} + K'_{i+1}}{K_2 + K'_2} \cdot K_2 + \dots + \frac{K_{i+1} + K'_{i+1}}{K_{i+1} + K'_{i+1}} \cdot K_{i+1} \\ &= (K_{i+1} + K'_{i+1}) \cdot \left( \frac{K_{i+1}}{K_{i+1} + K'_{i+1}} + \frac{K_i}{K_i + K'_i} + \dots + \frac{K_2}{K_2 + K'_2} + \frac{K_1}{K_1 + K'_1} - \frac{K'_0}{K_0 + K'_0} \right) \\ &= (K_{i+1} + K'_{i+1}) \cdot \left[ \left( \sum_{j=1}^{i+1} \frac{K_j}{K_j + K'_j} \right) - \frac{K'_0}{K_0 + K'_0} \right] \end{aligned}$$

According to Equation (4),  $f_K(x_{i+1})$  can be described as Equation (7).

$$f_K(x_{i+1}) = \left( \frac{1}{V_R - V_W(i+1)} + \frac{1}{V_W(i+1)} \right) \cdot \left( \sum_{j=1}^{i+1} \frac{\frac{1}{V_R - V_W(j)}}{\frac{1}{V_R - V_W(j)} + \frac{1}{V_W(j)}} - \frac{\frac{1}{V_W(0)}}{\frac{1}{V_R - V_W(0)} + \frac{1}{V_W(0)}} \right) \tag{7}$$

$$= \frac{1}{(V_R - V_W(i+1)) \cdot V_W(i+1)} \cdot \left( \sum_{j=0}^{i+1} V_W(j) - V_R \right)$$

For the  $N$ -group scanning of the UPA system, when  $i = N$ , according to the Equation (2),  $V_R = \sum_{n=0}^{N-1} V_W(n)$ , and  $f_K(x_{N-1}) = \frac{1}{(V_R - V_W(N-1)) \cdot V_W(N-1)} \cdot \frac{1}{V_R} \cdot \left( \sum_{j=0}^{N-1} V_W(j) - V_R \right) \Big|_{V_R = \sum_{j=0}^{N-1} V_W(j)} = 0$ . The matrix  $A$  can be transformed to  $A'$  through the primary row transformation:

$$A = \begin{pmatrix} -K'_0 & K_1 & \cdots & K_{N-1} \\ K_0 & -K'_1 & \cdots & K_{N-1} \\ \vdots & \vdots & \vdots & \vdots \\ K_0 & K_1 & \cdots & -K'_{N-1} \end{pmatrix} \sim \begin{pmatrix} f_K(x_0) & K_1 - f_K(x_1) & 0 & 0 & \cdots & 0 \\ 0 & f_K(x_1) & K_2 - f_K(x_2) & 0 & \cdots & 0 \\ \vdots & \vdots & \vdots & \vdots & \vdots & 0 \\ 0 & \cdots & \cdots & 0 & f_K(x_{N-2}) & K_2 - f_K(x_{N-1}) \\ 0 & \cdots & \cdots & \cdots & 0 & f_K(x_{N-1}) \end{pmatrix}$$

$$\underline{f_K(x_{N-1}) = 0} \begin{pmatrix} f_K(x_0) & K_1 - f_K(x_1) & 0 & 0 & \cdots & 0 \\ 0 & f_K(x_1) & K_2 - f_K(x_2) & 0 & \cdots & 0 \\ \vdots & \vdots & \vdots & \vdots & \vdots & 0 \\ 0 & \cdots & \cdots & 0 & f_K(x_{N-2}) & K_2 \\ 0 & \cdots & \cdots & \cdots & 0 & 0 \end{pmatrix} = A'$$

Because the rank  $R(A)$  of the matrix  $A$  and the rank  $R(A')$  of the matrix  $A'$  have the following relation  $R(A) = R(A') < N$ , Equation (5) has an infinite number of the solutions, and because  $A \cdot \vec{L} = \vec{0} \Leftrightarrow A' \cdot \vec{L} = \vec{0}$ , and the solutions can be expressed as follows:

$f_K(x_i) \times L(i) + (K_{i+1} - f_K(x_{i+1})) \times L(i+1) = 0$ , ( $i = 0, 1, \dots, N - 2$ ), and  $L(i) = \frac{f_K(x_{i+1}) - K_{i+1}}{f_K(x_i)} \cdot L(i + 1)$ , ( $i = 0, 1, \dots, N - 2$ ), and  $L(i)$  can be further deduced forward:

$$L(i) = \frac{f_K(x_{i+1}) - K_{i+1}}{f_K(x_i)} \cdot \frac{f_K(x_{i+2}) - K_{i+2}}{f_K(x_{i+1})} \cdot \dots \cdot \frac{f_K(x_{N-1}) - K_{N-1}}{f_K(x_{N-2})} \cdot L(N - 1)$$

$$= \prod_{j=i}^{N-2} \frac{f_K(x_{j+1}) - K_{j+1}}{f_K(x_j)} \cdot L(N - 1) \tag{8}$$

Substituting the expression of  $f_K(x_{i+1})$  from Equation (7) into Equation (8). The values of  $L(i)$ ,  $i = 0, 1, \dots, N - 1$  are obtained, as shown in Equation (9):

$$\begin{cases} L(0) = \frac{(V_R - V_W(0)) \cdot V_W(0)}{(V_R - V_W(N - 1)) \cdot V_W(N - 1)} \cdot L(N - 1) \\ \vdots \\ L(i) = \frac{(V_R - V_W(i)) \cdot V_W(i)}{(V_R - V_W(N - 1)) \cdot V_W(N - 1)} \cdot L(N - 1) \\ \vdots \\ L(N - 2) = \frac{(V_R - V_W(N - 2)) \cdot V_W(N - 2)}{(V_R - V_W(N - 1)) \cdot V_W(N - 1)} \cdot L(N - 1) \\ L(N - 1) = L(N - 1) \end{cases} \tag{9}$$

when Equation (9) is multiplied by a term of  $\frac{(V_R - V_W(N - 1)) \cdot V_W(N - 1)}{L(N - 1)}$ , a set of fundamental solutions  $\vec{\xi}$  to the equations of  $A \cdot \vec{L} = \vec{0}$  will be obtained:

$$\vec{\xi} = ((V_R - V_W(0)) \cdot V_W(0), (V_R - V_W(1)) \cdot V_W(1), \dots, (V_R - V_W(N - 1)) \cdot V_W(N - 1))^T.$$

Therefore, the solutions to the equations of  $A \cdot \vec{L} = \vec{0}$  can be expressed as  $\vec{L} = \alpha \cdot \vec{\xi}$  ( $\alpha \in \mathbf{R}^+$ ). The length function of  $L(i), i = 0, 1, \dots, N - 1$  of the FIFOs has a proportional relation, as showed in Equation (10).

$$L(0) : L(1) : \dots : L(N - 1) = (V_R - V_W(0)) \cdot V_W(0) : (V_R - V_W(1)) \cdot V_W(1) : \dots : (V_R - V_W(N - 1)) \cdot V_W(N - 1) \tag{10}$$

Equation (10) can be used to describe the most critical conclusion to realize the MFBSS algorithm, which shares the transmission bandwidth for the  $N$ -group scanning of the UPA system. Therefore, according to the ratios of the FIFOs' lengths, i.e., the cache time of each FIFO, the reading operation can be switched among each FIFO without time slot waiting, thus maximizing the bandwidth utilization ratio.

When the algorithm is implemented by an FPGA, in order to make the consumed resources of the FIFOs minimal, the ratio of  $L(0):L(1): \dots :L(N - 1)$  can often be simplified to a series of the suitable integer ratios. In the system of the  $N$ -group scanning and the  $N$  FIFOs caches, if the sampling rate  $f_{sn}$  ( $n = 0, 1, \dots, N - 1$ , and unit is 100 MHz) of the  $N$  groups linearly increases,  $V_R = \sum_{n=0}^{N-1} f_{sn} \cdot \Delta B$ , and  $\Delta B = \Delta B_W = \Delta B_R$ . The ratios of  $L(0):L(1): \dots :L(N - 1)$  of the FIFOs' lengths are calculated from Equation (10), and the results are listed in Table 2.

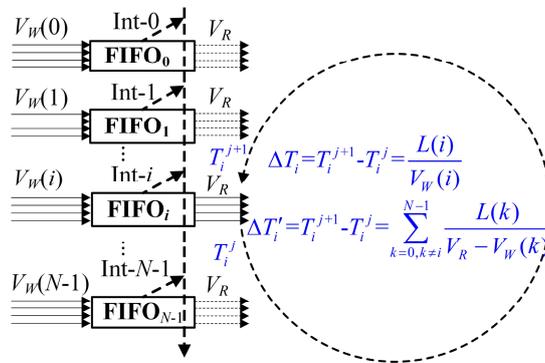


Figure 2. The time slot transition diagram of the  $N$  FIFOs reading operations.

Table 2. The  $N$ -group scanning and the  $N$ -FIFO caches depth ratios.

$N$	$f_{s0}$	$f_{s1}$	$f_{s2}$	$f_{s3}$	...	$f_{sN-1}$	$L(0):L(1): \dots :L(N - 1)$
2	1	2	×	×	×	×	1:1
3	1	2	3	×	×	×	5:8:9
4	1	2	3	4	×	×	9:16:21:24
...	...	...	...	...	...	×	...
$N$	1	2	3	4	...	$N - 1$	$(V_R - f_{s0}) \times f_{s0} : (V_R - f_{s1}) \times f_{s1} : \dots : (V_R - f_{sN-1}) \times f_{sN-1}$

Figure 3 shows the time slot switching flow chart with the sharing reading bus of the  $N$ -group scanning and the  $N$ -FIFO caches ( $N = 3$  or  $4$ ). The horizontal axis represents the time (unit: s).

In the initialization phase, the  $FIFO_{N-1}$  caches the maximum sampling rate beam, which is filled with the length  $L(N - 1)$  data. Meanwhile, the other caches  $FIFO_{N-2} \sim FIFO_0$  are filled with the lengths  $[L(i) - (\sum_{n=i+1}^{N-1} K_n \cdot L(n)) / K'_i](i = N - 2, N - 3, \dots, 1, 0)$ , respectively. The working principle is described as follows:

When an FIFO is full, it will be immediately read until empty (the symbol R represents the reading state of the FIFO), and subsequently switches to the next FIFO without any time slot in the process of the data transmission. Likewise, when the next FIFO is just written fully, it will be read immediately. Therefore, the whole process is carried out in cycles without any delay, maximizing the utilization ratio of the data transmission bandwidth.

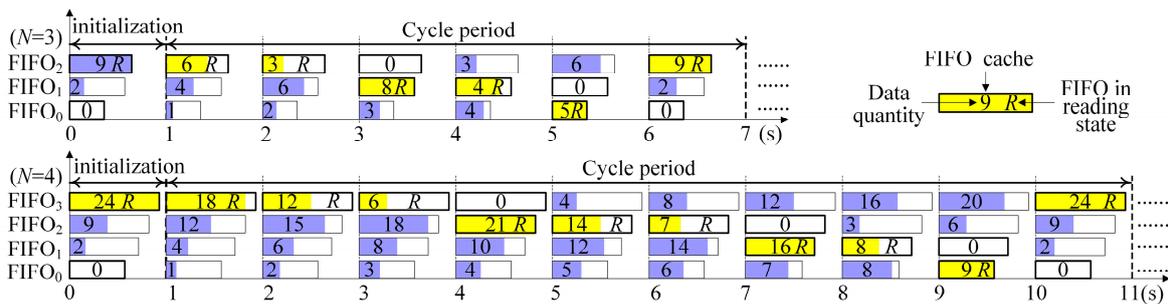


Figure 3. No time-gap switching flow chart of the  $N$ -group scanning and the  $N$ -FIFO caches shared.

#### 4. Implementation and Performance Evaluation of the Scheduling Algorithm

The scheduling algorithm is realized by using a UPA instrument (PA2000 model), which was made by Guangzhou Doppler Electronic Technologies Co., Ltd. (Guangzhou, China), and a Cyclone V GT FPGA Development Board made by Intel Corporation (Santa Clara, CA., USA) as the PCIe communication module with the PC. The UPA data are transmitted to the PC through the PCIe interface, and the multi-group scanning images are processed.

The UPA system with a work clock frequency ( $f_s$ ) of 100 MHz is mounted with four sensors with four different frequencies ( $f_s$ ) of 2, 2.5, 5, or 10 MHz, and thus the system can implement 4-group scanning patterns. The echoes of all the groups are up-sampled ( $f_s = 10 \times f_p$ ) by using digital signal processing technology, and thus the actual sampling frequencies of  $f_{s0} \sim f_{s3}$  become 20, 25, 50, or 100 MHz. The bit-width ( $\Delta B$ ) of the echo data is 8 bits, and both widths of the input ( $\Delta B_W$ ) and the output ( $\Delta B_R$ ) ports of the FIFOs are 64 bits. Table 3 lists the parameters of the writing frequency [ $V_{Wf}(n)$ ] and the reading frequency ( $V_{Rf}$ ) of the  $FIFO_n$  caches. Obviously,  $V_W(n)$  equals to  $V_{Wf}(n) \times \Delta B_W$ , and  $V_R$  equals to  $V_{Rf} \times \Delta B_R$  for this case, hence, the scheduling algorithm can be used to allow the 4-FIFO caches to realize sharing transmission bandwidth. The capacities of the FIFOs are  $L(n) \times \Delta B_W$ , and the length ratios of the FIFO caches can be calculated from Equation (10), i.e.,  $L(0):L(1):L(2):L(3) = 14:17:29:38$ . As listed in Table 3, the value of  $V_{Rf}$  is calculated to be 24.375 MHz, but it is relatively easier to implement the value of  $V_{Rf} = 25.0$  MHz ( $V_{Rf} = f_s / 4 = 25.0$  MHz  $\approx V'_{Rf}$ ) by the FPGA than the value of  $V_{Rf} = 24.375$  MHz, and thus we design the value of  $V_{Rf} = 25.0$  MHz for the experiment.

Table 3. The parameters of the 4 groups scanning and the 4 FIFO caches.

$f_p$ (MHz)	$f_{sn}$ (MHz)	$V_{Wf}(n) = f_{sn} \times \Delta B / \Delta B_W$ (MHz)	$V_{Rf} = \sum V_{Wf}(n)$ (MHz)	$L(n) \times \Delta B_W$ (bit)
2	20	2.5	24.375	$14 \times 64$
2.5	25	3.125	24.375	$17 \times 64$
5	50	6.25	24.375	$29 \times 64$
10	100	12.5	24.375	$38 \times 64$

Figure 4 shows the 4 FIFOs reading timing waves of the MFBSS algorithm from Signaltap, and a soft oscilloscope is used to observe FPGA internal signals. The signals of FIFO0\_rd ~FIFO3\_rd respectively control the reading operation of the 4 FIFOs, allowing it to enable output data in a time slice polling way. The times for reading the 4 FIFOs until empty are  $\Delta T_0 \sim \Delta T_3$ . The variables of  $\Delta T_0 : \Delta T_1 : \Delta T_2 : \Delta T_3$  have the following relation:

$$\Delta T_0 : \Delta T_1 : \Delta T_2 : \Delta T_3 \approx \frac{L(0)}{V_{Rf} - V_{Wf}(0)} : \frac{L(1)}{V_{Rf} - V_{Wf}(1)} : \frac{L(2)}{V_{Rf} - V_{Wf}(2)} : \frac{L(3)}{V_{Rf} - V_{Wf}(3)}$$

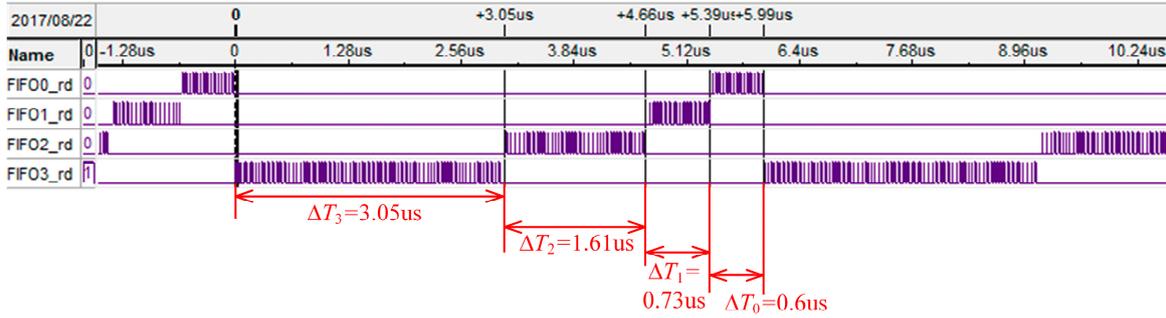


Figure 4. The 4 FIFOs read timing waves of the MFBSS algorithm from Signaltap.

All the FIFOs are readed in turn until empty in every cycle. The sum of data ( $D_{W-sum}$ ) for writing into the FIFOs and the sum of data ( $D_{R-sum}$ ) for reading out from the FIFOs are given by the two formulas  $(\Delta t_0 \cdot V_{Wf}(0) + \Delta t_1 \cdot V_{Wf}(1) + \Delta t_2 \cdot V_{Wf}(2) + \Delta t_3 \cdot V_{Wf}(3)) \cdot \Delta B_W$  and  $(\Delta t_0 + \Delta t_1 + \Delta t_2 + \Delta t_3) \cdot V_{Rf} \cdot \Delta B_W$ , respectively. As a result, the experimental results show that  $D_{W-sum}$  equals to  $D_{R-sum}$ , which meets the relation  $V_R = \sum_{n=0}^{N-1} V_{Wf}(n)$  of Equation (2), and also agrees well with the theoretical analysis.

In the  $N$ -group scanning system, the bandwidth utilization ratio  $\eta_{bw}(N)$  of the MFBSS algorithm can be expressed by Equation (11):

$$\eta_{bw}(N) = \frac{\sum_{i=0}^3 V_{Wf}(i)}{V'_{Rf}} \times 100\%. \quad (11)$$

Therefore, in the experiment, when  $N = 4$ , the utilization ratio  $\eta_{bw}(4)$  of the MFBSS algorithm used in the UPA system can be calculated by Equation (12):

$$\eta_{bw}(4) = \frac{\sum_{i=0}^3 V_{Wf}(i)}{V'_{Rf}} \times 100\% = \frac{V_{Rf}}{V'_{Rf}} = \frac{24.375}{25} \times 100\% = 97.5\%. \quad (12)$$

The ETSPS scheduling algorithm based on the equal allocation of a time slot to each task. As compared with the MFBSS algorithm in this work, the ETSPS scheduling algorithm has four characteristics: (i) The lengths of all the FIFO $_i$  ( $i = 0, 1, 2, \dots, N - 1$ ) are the same as each other, i.e.,  $L(0) = L(1) = \dots = L(N - 1)$ . (ii) All the time slice resources of the reading operation of the  $N$  FIFOs are also equal to each other. (iii) All the FIFOs have the reading speed ( $V'_{Rf}$ ) which is equal to the maximum of the writing speed [ $V_{Wf}(i)$ ], same as that of the individual FIFO, i.e.,  $V'_{Rf} = \max[V_{Wf}(i)]$ ,  $i = 0, 1, \dots, N - 1$ . (iv) When the FIFO $_i$  ( $i = 0, 1, 2, \dots, N - 1$ ) is filled by writing, the reading operations of the

FIFO<sub>*i*</sub> will be immediately performed. Therefore, the general utilization ratio of the bandwidth-sharing transmission with *N*-group scanning of the UPA system can be calculated by Equation (13):

$$\eta'_{bw}(N) = \frac{\sum_{j=0}^{N-1} V_{Wf}(j)}{N \cdot V'_{Rf}} \times 100\% = \frac{\sum_{j=0}^{N-1} V_{Wf}(j)}{N \cdot \max(V_{Wf}(i))} \times 100\%. \tag{13}$$

$i = 0, 1, \dots, N - 1$

For *N*-group scanning data stream with bandwidths {*V<sub>W</sub>(0), V<sub>W</sub>(1), . . . , V<sub>W</sub>(N - 1)*} (unit: Byte/s), we use the FPGA technology to implement the MFBSS algorithm together with the the traditional ETSPS scheduling algorithm, and analyze their bandwidth utilization ratios  $\eta_{bw}(N)$  and  $\eta'_{bw}(N)$ . For example, the FPGA (Arria-II EP2AGX65DF29I5) with a work clock frequency of  $f_{clk} = 100$  MHz. So, it is easy to produce the clock frequencies such as  $F_1 = \{1, 2, 3, \dots, f_{clk}\}$  and  $F_2 = \{f_{clk}/100, f_{clk}/99, f_{clk}/98, \dots, f_{clk}/1\}$  (unit: MHz) by using the clock  $f_{clk}$  by Digital Phase Locked Loop technology.

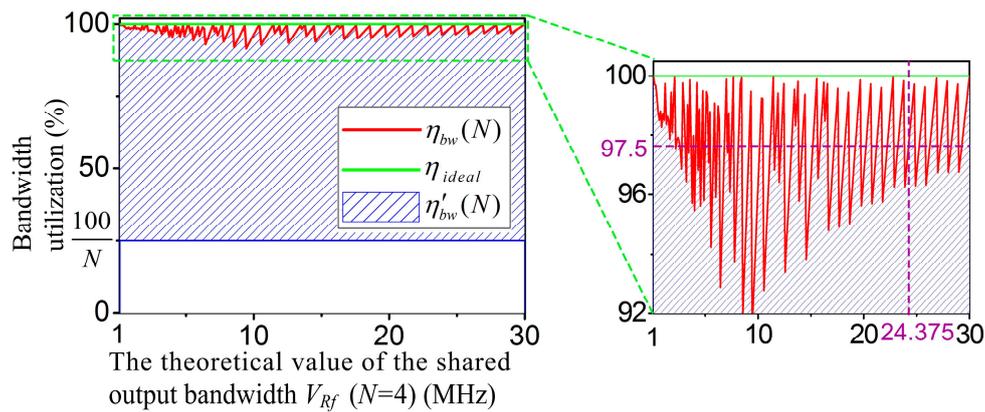
- The MFBSS algorithm. According to Equation (11), the theoretical value of the shared output bandwidth is  $V_{Rf}$  or  $(\sum_{i=0}^3 V_{Wf}(i))$ . The actual value of the shared output bandwidth is  $V'_{Rf}$ , which satisfies the following conditions:  $V'_{Rf} \geq V_{Rf}$ ,  $V'_{Rf} \in F_1$  or  $V'_{Rf} \in F_2$ , and the value of  $(V'_{Rf} - V_{Rf})$  is minimized. For instance, when  $V_{Rf} = 24.375$  HMz, and  $V'_{Rf} = f_{clk}/4 = 25$  MHz, and thus the actual bandwidth utilization ratio is  $\frac{V_{Rf}}{V'_{Rf}} \times 100\%$  which equals to 97.5%.
- The ETSPS algorithm. According to Equation (13), the larger the value of  $\max(V_{Wf}(i))$  is, the smaller the value of  $\eta'_{bw}(N)$  is. The smaller the value of  $\max(V_{Wf}(i))$  is, the larger the value of  $\eta'_{bw}(N)$  is. So, when the value of  $\max(V_{Wf}(i))$  equals to  $\frac{1}{N} \cdot \sum_{j=0}^{N-1} V_{Wf}(j)$ , i.e.,  $V_W(0) = V_W(1) = \dots = V_W(i) = \dots = V_W(N - 1)$ , the maximum theoretical value of  $\eta'_{bw}(N)$  can be expressed by Equation (14).

$$\max(\eta'_{bw}(N)) = \frac{\sum_{j=0}^{N-1} V_{Wf}(j)}{N \cdot \max(V_{Wf}(i))} \times 100\% = \eta_{bw}(N) \tag{14}$$

when the value of  $\max(V_{Wf}(i))$  is close to  $\sum_{j=0}^{N-1} V_{Wf}(j)$ , i.e.,  $V_{Wf}(i) \rightarrow \sum_{j=0}^{N-1} V_{Wf}(j)$ , the minimum theoretical value of  $\eta'_{bw}(N)$  can be expressed by Equation (15).

$$\min(\eta'_{bw}(N)) \approx \frac{\sum_{j=0}^{N-1} V_{Wf}(j)}{N \cdot \max(V_{Wf}(i))} \times 100\% \approx \left(\frac{100}{N}\right)\% \tag{15}$$

Figure 5 shows the bandwidth utilization ratio curves of the two scheduling algorithms (cross axis: the theoretical value of the shared output bandwidth  $V_{Rf}$  ( $N = 4$ ), and vertical axis: the bandwidth utilization).  $\eta_{bw}(N)$  and  $\eta'_{bw}(N)$  are the bandwidth utilization ratios of the MFBSS algorithm and the ETSPS algorithm, respectively.



**Figure 5.** Comparison of the bandwidth utilization ratios of the MFBSS algorithm and the ETSPS algorithm.

The symbols  $\eta_{bw}(N)$  and  $\eta_{ideal}$  represent the experimental and ideal values of the algorithm MFBSS, respectively. The results show that the value of  $\eta_{bw}(N)$  is between 92% and 100%, for example, for the above experiment of 4-group scanning based on the MFBSS algorithm, when  $V_{Rf}$  equals to 24.375 MHz,  $\eta_{bw}(N)$  equals to 97.5% and  $\eta_{ideal}$  equals to 100%. Whereas the value of  $\eta'_{bw}(N)$  is relevant to the value of  $N$ , its value is between  $(100/N)\%$  and  $\eta_{bw}(N)$ . For  $N$ -group scanning patterns, only when all groups have the same bandwidth,  $\eta_{bw}(N)$  equals to  $\eta'_{bw}(N)$ . Otherwise,  $\eta'_{bw}(N)$  would be much smaller than  $\eta_{bw}(N)$ .

Similarly, we use FPGA to implement the traditional ETSPS algorithm with the same parameters in Table 3, and collected reading timing waves of the 4 FIFOs by using Signaltap. As shown in Figure 6, the signals FIFO0\_rd ~FIFO3\_rd control the reading operation of the four FIFOs, and the time resources occupied by the signals are assigned by the signal FIFO\_rd.

Assuming that the symbols  $f_{FIFO\_rd}$ ,  $f_{FIFO0\_rd}$ ,  $f_{FIFO1\_rd}$ ,  $f_{FIFO2\_rd}$ , and  $f_{FIFO3\_rd}$  represent the frequencies of signals FIFO\_rd, FIFO0\_rd, FIFO1\_rd, FIFO2\_rd, and FIFO3\_rd, respectively, the following results can be easily obtained, as shown in Figure 6:  $f_{FIFO\_rd} = \frac{1}{\Delta T} = 50$  MHz,  $f_{FIFO0\_rd} = \frac{1}{\Delta T_0} = 2.5$  MHz,  $f_{FIFO1\_rd} = \frac{1}{\Delta T_1} = 3.125$  MHz,  $f_{FIFO2\_rd} = \frac{1}{\Delta T_2} = 6.25$  MHz,  $f_{FIFO3\_rd} = \frac{1}{\Delta T_3} = 12.5$  MHz.

So, the utilization ratio of the data transmission with the 4-group scanning of the ETSPS algorithm can be calculated by Equation (16):

$$\begin{aligned} \eta'_{bw}(4) &= \frac{f_{FIFO0\_rd} + f_{FIFO1\_rd} + f_{FIFO2\_rd} + f_{FIFO3\_rd}}{f_{FIFO\_rd}} \times 100\% = \frac{\sum_{j=0}^{N-1} f_{sj}}{N \cdot \max(f_{s0}, \dots, f_{s3})} \times 100\% \\ &= \frac{2.5 + 3.125 + 6.25 + 12.5}{50} \times 100\% \\ &= 48.75\% \end{aligned} \quad (16)$$

As a consequence, the bandwidth utilization ratio of the MFBSS algorithm  $\eta_{bw}(4)$  reaches to 97.5% as shown in the inset of Figure 5, while the bandwidth utilization of the ETSPS algorithm  $\eta'_{bw}(4)$  is only 48.75%. The experimental results demonstrate that the MFBSS algorithm is efficient when used in the multi-group sensors scanning UPA system.

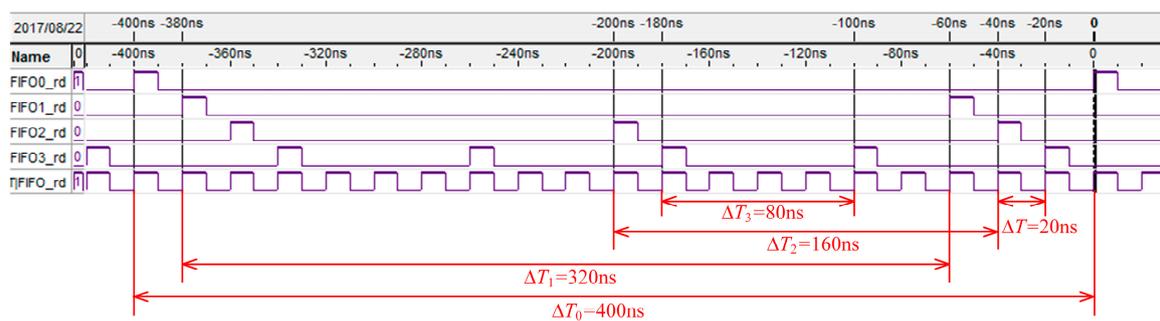


Figure 6. The 4 FIFOs reading timing waves of the ETSPS algorithm from Signaltap.

## 5. Conclusions

The novel MFBSS algorithm was proposed on the basis of the FIFOs variable lengths by FPGA technology, and was used for the multi-sensor scanning UPA system to maximize the bandwidth utilization ratio. The mathematical modeling of the MFBSS algorithm was established, and the formula  $V_R = \sum_{n=0}^{N-1} V_W(n)$  of maximizing bandwidth transmission utilization ratio in the  $N$ -group scanning patterns was successfully deduced. The lengths of the  $N$ -group FIFOs were achieved by using the designed equations, from which the length ratios were readily calculated. The algorithm was realized by FPGA technology, which made the reading operation of one FIFO switch to another FIFO without any time slot waiting, and thus it obtained the data transmission bandwidth utilization of no less than 92% hence allowing the UPA system to have the bandwidth utilization higher than that of the traditional ETSPS algorithm. In order to improve transmission efficiency of the large data generated by the sensor systems and the real-time performance of the algorithm through the multi-FPGA technology, the MFBSS scheduling algorithm based on data transmission has important applications in the multi-sensor systems, and the future research is likely to focus on designing some special scheduling algorithm module for different sensor systems.

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