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New Analysis and Design of a RF Rectifier for RFID and Implantable Devices

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Abstract: New design and optimization of charge pump rectifiers using diode-connected MOS transistors is presented in this paper. An analysis of the output voltage and Power Conversion Efficiency (PCE) is given to guide and evaluate the new design. A novel diode-connected MOS transistor for UHF rectifiers is presented and optimized, and a high efficiency N-stage charge pump rectifier based on this new diode-connected MOS transistor is designed and fabricated in a SMIC 0.18- μm 2P3M CMOS embedded EEPROM process. The new diode achieves 315 mV turn-on voltage and 415 nA reverse saturation leakage current. Compared with the traditional rectifier, the one based on the proposed diode-connected MOS has higher PCE, higher output voltage and smaller ripple coefficient. When the RF input is a 900-MHz sinusoid signal with the power ranging from -15 dBm to -4 dBm, PCEs of the charge pump rectifier with only 3-stage are more than 30%, and the maximum output voltage is 5.5 V, and its ripple coefficients are less than 1%. Therefore, the rectifier is especially suitable to passive UHF RFID tag IC and implantable devices.

Keywords: radio frequency identification; passive transponders; diode-connected MOS transistor; rectifier; power conversion efficiency

1. Introduction

The rapidly increasing range of applications of radio frequency identification (RFID) technology includes supply chain management, access control to buildings, public transportation, airport baggage handling, and express parcel logistics [1-3]. Use of a RFID system is a good approach for automated identification of products. The need for lower cost, higher data rates, and longer communication distances is increasing, while severe regulation of transmission power and bandwidth have to be met. RFID tags (or transponders) are often classified as passive or active. Passive tags are powered by an electromagnetic wave transmitted by the reader, while the active tag is powered by a battery. Passive tags have the advantages of low cost and long life. As the passive tag is remotely powered by a reader's RF signal, it must be able to operate at very low power levels ($\sim \mu\text{W}$) [1,3].

In 1999 the FCC allocated the Medical Implant Communication Service (MICS) band to the 402–405 MHz range. However, due to the low transmitted power of the MICS band ($\text{EIRP} = 25 \mu\text{W}$), this band cannot be used to power implanted system. This has motivated research on implantable transceiver architectures operating in other ISM bands, such as in the 902 to 928 MHz and 2.4 GHz ISM bands [4-6]. For example, [6] presented a wireless neural interface which harvests RF power from a standard commercial ultra-high frequency (UHF, 902 MHz–928 MHz) RFID reader.

The ultra-high-frequency (UHF) passive RFID tag or implantable device has to work at a considerably long distance from the transmitter (or reader). As the RF energy received by the tag (or implantable device) decreases rapidly with distance, the induced voltage across the tag antenna is often very small [6-9]. In order to obtain a high output voltage, an N-stage charge pump rectifier (also called a charge pump multiplier) is typically used [6,10,11]. Schottky diodes with low potential barrier are widely used for achieving a high output voltage and a high Power Conversion Efficiency (PCE), but Schottky diodes are not compatible with the standard CMOS process. Instead of Schottky diodes, diode-connected MOS transistors with very low threshold voltages are used in the N-stage voltage multiplier [7,8]. The weakness of using MOS transistors is that the threshold voltage is increased by the body effect. There were many publications regarding the design of RF rectifiers using diode-connected MOS transistors [7,8,12-17], however, there have been almost no technical papers regarding the design issue of providing a new diode-connected CMOS for substituting the Schottky diode. For example, the design strategy and efficiency optimization of UHF micro-power rectifiers using diode-connected MOS transistors with very low threshold voltage is presented in [7], but it didn't solve the problems generated by the substrate bias effect of diode-connected MOS transistors.

In this paper, a novel diode-connected MOS transistor for replacing the Schottky diode was presented, and a high efficiency N-stage charge pump voltage rectifier circuit based on this new diode-connected MOS transistor was designed and implemented. Section 2 starts with the analysis of the N-stage rectifier using Schottky diodes. Section 3 describes the design and optimization of a new diode-connected MOS transistor. Section 4 gives simulation results for the N-stage rectifier using the novel diode-connected MOS transistor, and compares our new design with the traditional rectifier through these simulation results. Section 5 compares the simulation results with the theoretical analysis. Section 6 concludes our research efforts.

2. Analysis of an N-Stage Rectifier

Figure 1 shows an N-stage charge pump voltage rectifier consisting of a $2N$ peak value detector [1]. The input is assumed to be sinusoidal, with $U_{in} = V_0 \cos(\omega_0 t)$ [10]. To reduce the ripple voltage, the load capacitance C_L is assumed to be large enough, so as to make the time constant much bigger than the input signal cycle:

$$\frac{I_L}{CU_L} \ll \omega_0 \quad (1)$$

where U_L is output voltage, I_L is load current.

The equivalent circuit of the diode working at high frequency consists of two parts, which are an ideal diode and a parasitic capacitance C_D , connected in parallel [11]. According to the V-I characteristics of the PN junction index model, the current of each diode is given by:

$$\begin{aligned} i_D &= I_s (e^{v_D/V_T} - 1) + C_D \frac{dV_d}{dt} \\ &= I_s \left[\exp \left(\pm \frac{V_0}{V_T} \cos(\omega_0 t) - \frac{U_L}{2NV_T} \right) - 1 \right] \\ &\quad + C_D \frac{dV_d}{dt} \end{aligned} \quad (2)$$

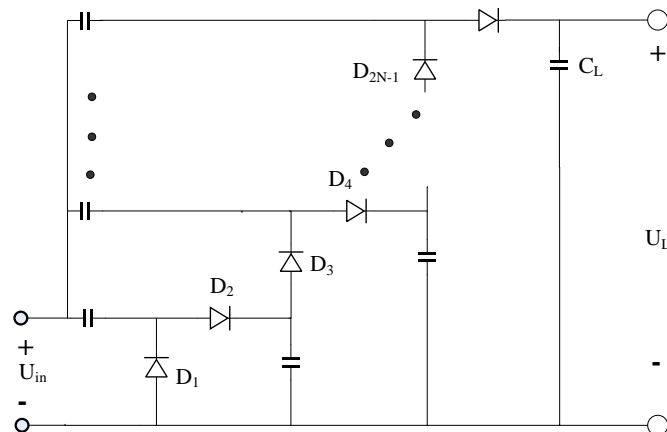
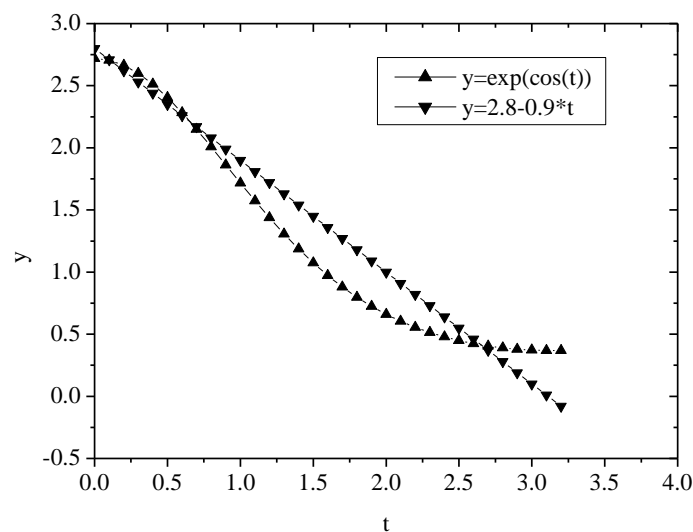
where, V_T is the thermal voltage, I_s is the reverse saturation current.

Because the capacitance doesn't dissipate power, we ignore the parasitic capacitance when we study the large-signal characteristics. For the $2N$ nd diode, we have:

$$\begin{aligned} I_d &= I_s \left[\exp \left(\frac{V_0 \cos(\omega_0 t) - \frac{U_L}{2N}}{V_T} \right) - 1 \right] \\ &= I_s \left[\exp \left(\frac{V_0 \cos(\omega_0 t)}{V_T} \right) \exp \left(\frac{-\frac{U_L}{2N}}{V_T} \right) - 1 \right] \\ &= I_s \left[\left(\exp(\cos(\omega_0 t)) \right)^{\frac{V_0}{V_T}} \exp \left(\frac{-\frac{U_L}{2N}}{V_T} \right) - 1 \right] \end{aligned} \quad (3)$$

As the approximation shown in Figure 2, we assume $e^{\cos(\omega_0 t)} \approx 2.8 - 0.9\omega_0 t$, where $t \in [0, \frac{T}{2}]$, Equation (3) can be rewritten as:

$$I_d = I_s \left[(2.8 - 0.9\omega_0 t)^{\frac{V_0}{V_T}} \exp \left(\frac{-\frac{U_L}{2N}}{V_T} \right) - 1 \right] \quad (4)$$

Figure 1. N-stage charge pump voltage rectifier.**Figure 2.** Linear approximation of exponential trigonometric function.

Integrating Equation (4) in one cycle gives:

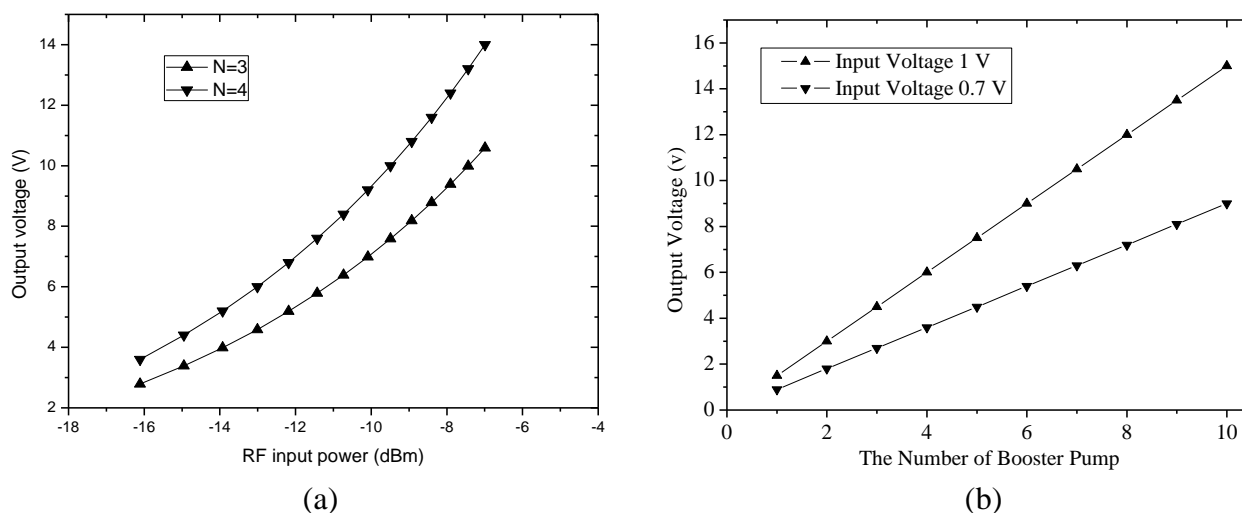
$$\begin{aligned}
 I_L \times T &= \int_0^T I_d dt \\
 &\approx 2 \times I_s \int_0^{T/2} \left[(2.8 - 0.9\omega_0 t)^{\frac{V_0}{V_T}} \exp\left(\frac{-U_L}{2N V_T}\right) - 1 \right] dt \\
 &= 2 \times I_s \exp\left(\frac{-U_L}{2N V_T}\right) \frac{(2.8)^{\frac{V_0}{V_T}+1}}{\left(\frac{V_0}{V_T} + 1\right) 0.9\omega_0} - I_s \times T
 \end{aligned} \tag{5}$$

So, the output voltage is:

$$U_L = -2N V_T \ln \left[\frac{5.652 \times (I_L + I_s) \left(\frac{V_0}{V_T} + 1\right)}{2I_s \times (2.8)^{\frac{V_0}{V_T}+1}} \right] \tag{6}$$

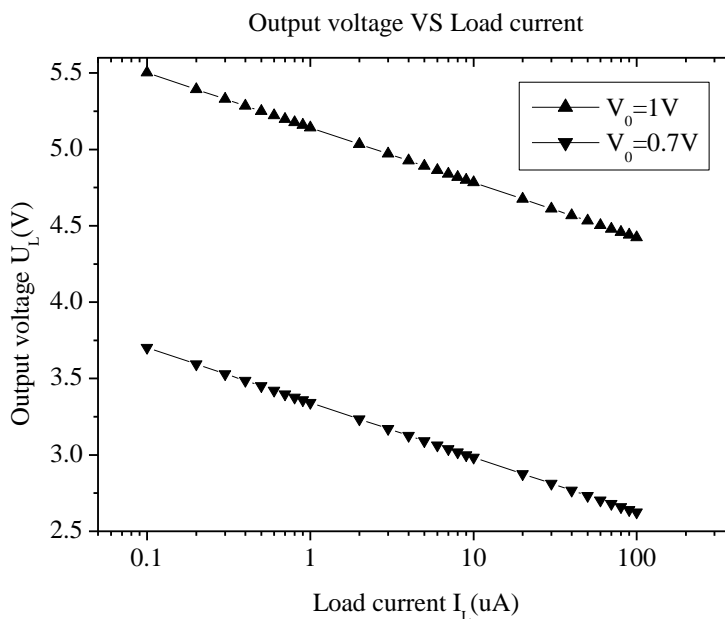
Assuming that the load resistor R_L and I_S of Equation (6) are $10\text{ K}\Omega$ and 1 a A ($1\text{ a} = 10^{-18}$) respectively, the input impedance of the rectifier is $10\text{ K}\Omega$. The characteristic output voltage response is shown in Figure 3. Figure 3(a) shows that the output voltage increases approximately linearly with the RF input power. Figure 3(b) shows that the output voltage increases with rectifier stages N .

Figure 3. Output voltage curves of the charge pump rectifier (a) Output voltage with different input power (b) Output voltage with different number of charge pump stage.



Because the charge pump multiplier is usually used under light load conditions, the primary emphasis is placed on the law of output voltage with different output load current. As shown in Figure 4, output voltage decreases logarithmically with the load current increase.

Figure 4. Output voltage of charge pump rectifier with different load currents.



Taking the strategy of linearly approximation as shown in Figure 2, to an N -stage rectifier, the power dissipated on all diodes in a cycle is:

$$\begin{aligned}
P_{diode} &= 2 \times N \times 2 \int_0^{T/2} I_s \left[\left(2.8 - 0.9\omega_0 t \right)^{\frac{V_0}{V_T}} \exp \left(\frac{-\frac{U_L}{2N}}{V_T} \right) - 1 \right] \\
&\quad \times \left(V_0 - 0.64V_0\omega_0 t - \frac{U_L}{2N} \right) dt \\
&= 4NI_s \left[\frac{0.791V_0}{\left(\frac{V_0}{V_T} + 1 \right) \left(\frac{V_0}{V_T} + 2 \right) \omega_0} \times \exp \left(-\frac{U_L}{2NV_T} \right) \right. \\
&\quad \times \left(2.8 \right)^{\frac{V_0}{V_T}+2} + \frac{\left(V_0 - \frac{U_L}{2N} \right)}{0.9\omega_0 \left(\frac{V_0}{V_T} + 1 \right)} \times \exp \left(-\frac{U_L}{2NV_T} \right) \\
&\quad \times \left(2.8 \right)^{\frac{V_0}{V_T}+1} + \frac{3.15V_0}{\omega_0} - \left(V_0 - \frac{U_L}{2N} \right) \frac{3.14}{\omega_0} \left. \right]
\end{aligned} \tag{7}$$

The power dissipated on the load in one cycle is:

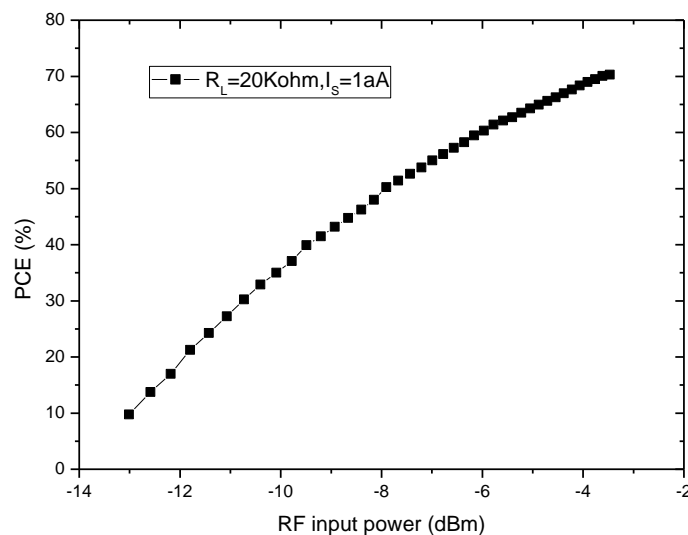
$$P_L = \int_0^T I_L U_L dt = \frac{I_L U_L \times 2\pi}{\omega_0} \tag{8}$$

The power conversion efficiency is given by:

$$PCE = \frac{P_L}{P_L + P_{diode}} \tag{9}$$

Figure 5 shows the power conversion efficiency with different RF input power. PCE increases with the input power, but PCE tends to saturation as the rate of the increase gradually decreases.

Figure 5. Power conversion efficiency with different input power.



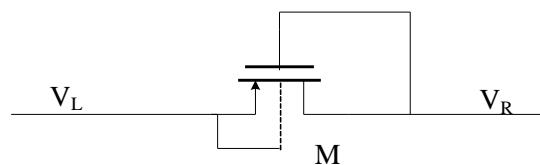
3. Design and Analysis of a New Diode-Connected MOS Transistor

3.1. Design of Diode-Connected CMOS with Low Turn-On Voltage

When replacing a diode with a diode-connected MOS transistor, we have to assure that the new structure will turn on when it is forward-biased and will cut off when it is reverse-biased, so not only should the NMOS substrate connect to the lowest voltage, but also the PMOS substrate should connect to the highest voltage.

As shown in Figure 6, the substrate of a diode-connected PMOS is connected to its source. Then, when V_L is higher than V_R , there will be a current from V_L to V_R . It means that the diode turns on when it is forward-biased. On the other hand, when V_R is higher than V_L , the voltage of drain is higher than that of the substrate, so the drain-body junction starts to conduct. It means that the diode doesn't cut off when it is reverse-biased.

Figure 6. Diode-connected PMOS.

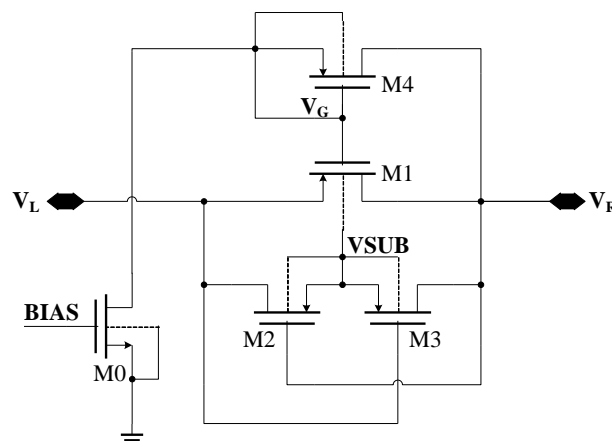


This can be solved by connecting the substrate of PMOS to the highest potential. But this will cause two problems in practice:

- (1) MOS transistor works in dynamic status, so it is difficult to decide the highest voltage.
- (2) Substrate bias effect will result in an increase of the threshold voltage, and make the turn-on voltage increase ultimately.

The structure of improved diode-connected CMOS for replacing the Schottky diode is shown in Figure 7. The improved diode-connected CMOS could decrease the turn-on voltage and ensure that the substrate is connected to the highest voltage.

Figure 7. The schematic diagram of improved diode-connected CMOS.



In Figure 7, M0 supplies an exiguity bias current via bias voltage BIAS. So VG will bias at a level of $V_R - V_{TH}$, where V_{TH} is the drain-body junction turn-on voltage. PMOS M2 and M3 are used to assure that the substrate of M1 is connected to the highest voltage. If V_L is higher than V_R , M2 will turn on while M3 will cut off, and the potential of M1, M2 and M3's substrate VSUB will rises up to V_L . Otherwise, if V_R is higher than V_L , M3 will turn on while M2 will cut off, and the potential of M1, M2 and M3's substrate VSUB will rise up to V_R . All these ensure that the substrate of M1, M2 and M3 is always connected to the highest potential, so that the drain-body junction is reverse-biased all the time.

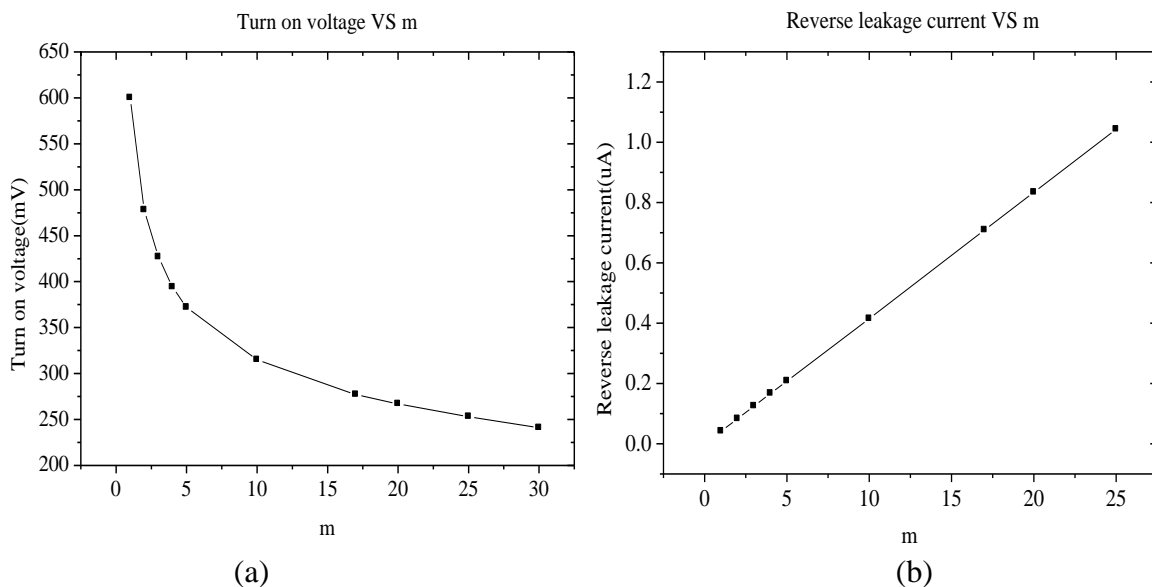
When V_L is high, M1 works in the linear region and the turn-on resistance is small, so V_R can be as high as V_L . On the other hand, when V_L is low, V_G is about $V_R - V_{in}$. The absolute value of V_{GD} of M1 will be smaller than its threshold voltage, and M1 will cut off. In this way, we realize a diode which will turns on when it's forward-biased with small voltage. In this diode, M0 is high voltage zero-threshold NMOS, whose threshold voltage is 0.31 V. M1, M2 and M3 are all high-voltage PMOS, whose threshold voltage is -0.92 V. The drain-body junction turn-on voltage of all these transistors is 0.7 V. It is notable that the absolute value of the threshold voltage V_{TH} of the PMOS is higher than the drain-body junction turn-on voltage V_{th} . This new diode-connected CMOS has some advantages:

- (1) The problem of body-potential connecting is solved by the body-switching technique.
- (2) The control of M1's gate voltage is realized by a simple bias circuit, which makes M1 be in the linear region rather than the saturation region when it is turned on. Therefore, this structure has a small forward voltage, which is applicable to a UHF RFID tag. When the voltage amplitude of the antenna in UHF RFID tag is small, high conversion efficiency and high output voltage are important to the rectifier of a UHF RFID tag.

3.2. Analysis and Optimization of Parasitic Effect for the New Diode-Connected CMOS

M2 and M3 always work in the linear region, in order to connect the substrate voltage. So they don't need big (W/L), actually, it's 2/1 in this design. For M1, if the number of the multiple transistors is bigger, *i.e.*, the W/L will be bigger, the turn-on resistance will be smaller, and then the turn-on voltage will be lower. However, bigger (W/L) brings a greater reverse leakage current, so we need a tradeoff between turn-on voltage, reverse leakage current and area. Figure 8 shows the different turn-on voltage (when conduction current is 100 μ A) and different reverse leakage current (when reverse voltage is 1 V) with different number of parallel connection transistors. From Figure 8, we can see that the reverse leakage current gets greater with the increase of the number m of parallel connection transistors, and the reverse current is directly proportional to the m value. From the analysis above, 10 could be the probable number of multiple transistors. When the number is 10, the turn-on voltage is only 315 mV, and the reverse leakage current is 415 nA.

Figure 8. Characteristic curve of diode-connected CMOS (a) Turn-on voltage with different m (b) Reverse leakage current with different m .



As shown in Figure 7, $C_P = C_{GS1}$ is a relatively large parasitic capacitance, and is about 0.1 pf. When V_L changes, because of the coupling of C_P , the gate voltage of M4 V_G will also change. Two situations are analyzed here under the condition that the RF input was a 900-MHz sinusoid.

- (1) If V_L decreases suddenly, the gate voltage of M4 V_G will decrease too. Then drain-body junction of M4 turns on, and C_P is charged to $V_R - V_{TH}$ (where V_{TH} is the turn-on voltage of M4's drain-body junction) by the current of drain-body junction of M4. If V_G rises rapidly, the duration of low potential of V_G will be short, and then the conduction time of M1 will be short too. It means that the reverse leakage current will be small. Besides, the charging rate depends on the current through the drain-body junction of M4. If the drain—body junction area is large, the turn-on current will be big, thus the charging rate will be high. Because the area of M4's drain-body junction is directly related to the width of the transistor, the width of M4 should be as big as possible, so as to decrease the reverse leakage current. Assuming that the falling amplitude of V_L is V , the charging current to C_P through the drain-body junction I is constant, charging time is t , and the capacitance seen from V_G is C_X , we have:

$$\frac{C_P C_X}{C_P + C_X} V = It \quad (10)$$

If C_X is comparable with C_P , $V = 1$, t is ten percent of the RF signal cycle, I will be 450 μA , which is easy to gain for a turn-on diode.

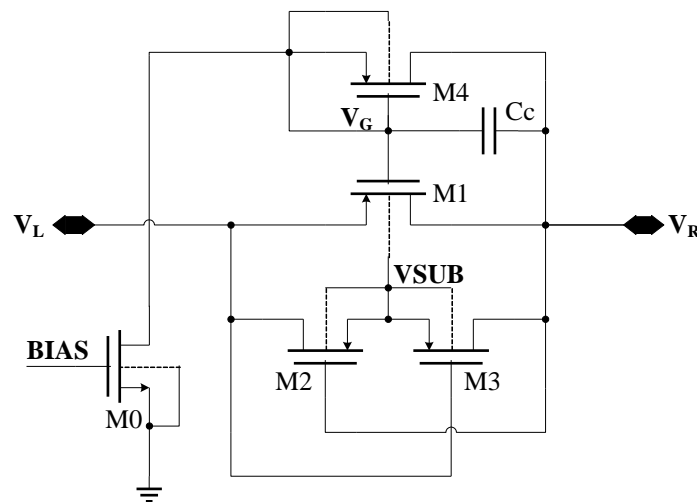
- (2) If V_L rises suddenly, the gate voltage of M4 V_G will rise too. The capacitance C_P discharges through M0 and M4. The shorter the discharging time is, the lower the turn-on voltage of the diode-connected MOS will be. The discharging time is determined by the current through M0 and M4. However, as long as V_G rises to no more than $V_{TH} + V_{th}$, (where V_{TH} is the absolute value of PMOS threshold voltage, V_{th} is the turn-on voltage of drain-body junction,) M4 will cut off, the current will be close to 0, so that the discharging time depends mainly on the

current I_0 through M_0 . As the parasitic capacitance of MOS transistors, V_R changes little when it tends to stability. Therefore, V_R can be regarded as ground in the AC analysis. The parasitic capacitances of M_1 are consisted the gate-drain parasitic capacitance C_{gd1} and gate-source parasitic capacitance C_{gs1} . The effect of V_L on V_G is $C_{gs1} \times V_L / (C_{gs1} + C_{gd1})$. C_{gs1} and C_{gd1} is nearly equal. So if the rise amplitude is V , V_G rise up about $1/2 V$:

$$\frac{1}{2}V = I_0 t \quad (11)$$

When V is 1, t is ten percent of the RF signal cycle, I_0 is 450 μA . For bias transistor M_0 , I_0 is huge and will make the power consumption much bigger, so it's not advisable to increase I_0 . Fortunately, we could solve this problem by a compensatory capacitance C_c . With the C_c , the effect of V_L on V_G is $C_{gs1} \times V_L / (C_{gs1} + C_{gd1} + C_c)$, reducing the power consumption caused by coupling effect of parasitic capacitances. Actually we add a 10 pf capacitance between V_R and V_G in this design. The final schematic diagram of the optimized diode-connected MOS is shown in Figure 9.

Figure 9. Schematic diagram of optimized diode-connected CMOS.



4. Simulation Results and Discussions for N-Stage Rectifier

The N-stage rectifier using the novel diode-connected MOS transistor will be discussed in this Section. Figure 10 shows the structure of a 3-stage charge pump rectifier in which we use the optimized diode-connected MOS which is represented by a rectangle symbol. When the RFID tag enters an electromagnetic field, the input voltage is in negative half-cycle, current charges C_2 , C_4 and C_5 through NMOS M_1 , M_2 and drain-body junction diode of M_3 . In positive half-cycle, current charges C_1 , C_3 and C_L through diode-connected MOS D_1 , D_2 and D_3 . Compared with the traditional CMOS charge pump rectifier (shown in Figure 11), the proposed structure has the advantages of high PCE, low power consumption, high output voltage, and low ripple coefficient. When the RF input is a 900-MHz sinusoid, the two rectifiers are all designed and implemented in SMIC 0.18- μm 2P3M CMOS embedded EEPROM process. The simulation results of the key performance parameters is given in the same process, with the same load resistance 20 k Ω and the same input powers, compared with the traditional CMOS 3-stage charge pump multiplier. According to the key simulation data, we

get the curves of output voltage, PCE and ripple coefficient with different the input powers as shown in Figure 12.

Figure 10. A improved 3-stage charge pump rectifier.

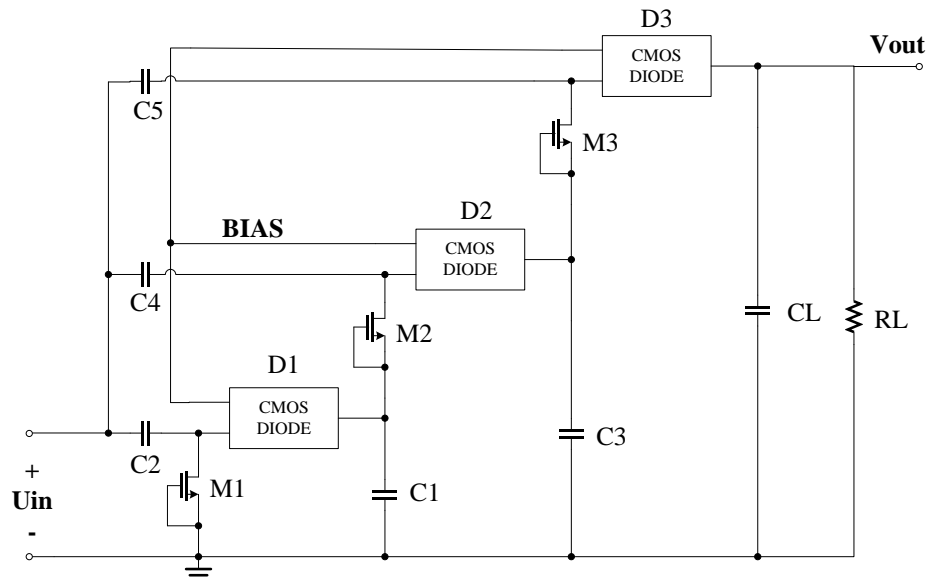


Figure 11. Traditional CMOS charge pump rectifier.

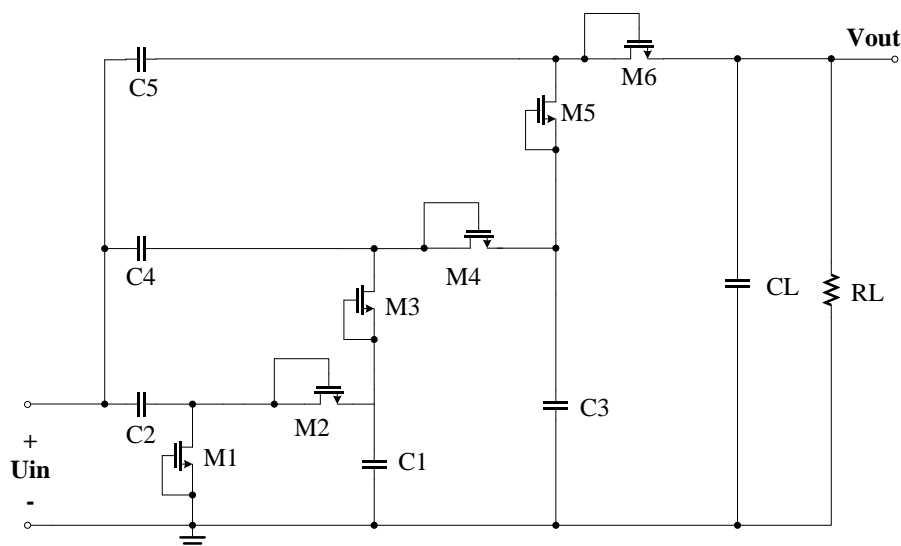
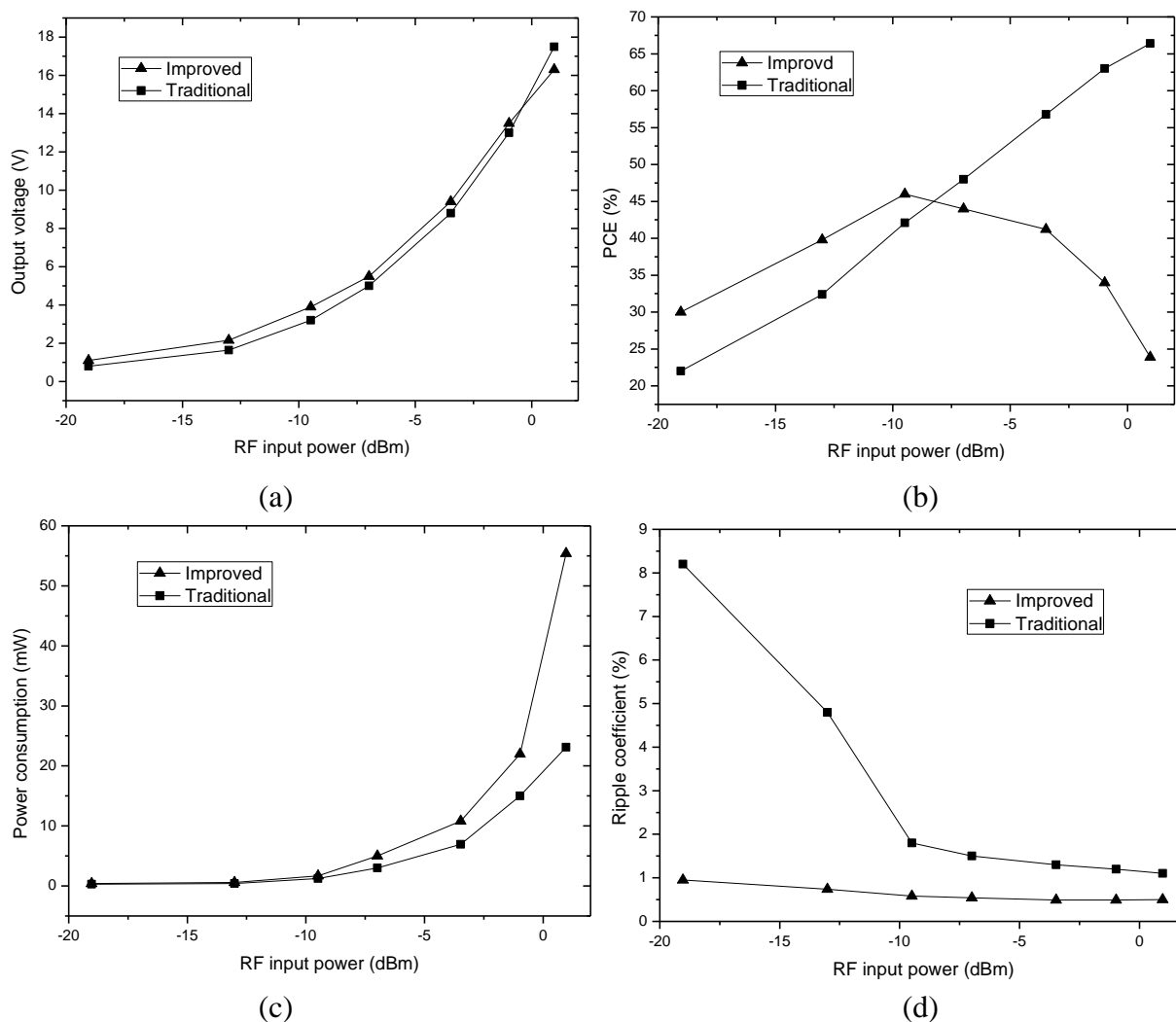


Figure 12 shows that the improved charge pump multiplier has a very small ripple coefficient, always below 1%. When the voltage amplitude is small, this novel charge pump multiplier has a distinct high output voltage and high PCE, compared with traditional rectifier. When the RF input is a 900-MHz sinusoid and the input power is -13 dBm (the input impedance of the rectifier is $10\text{ K}\Omega$, peak-to-zero amplitude is 1 V), conversion efficiency is 39.8% , and output voltage is 2.16 V , the ripple coefficient is below 1% . When the RF input is a 900-MHz sinusoid and the input power is -7 dBm, conversion efficiency is 46.9% , and output voltage is 5.76 V , the ripple coefficient is also below 1% . When the induced voltage across the antenna gets bigger, the improved rectifier's power consumption increases markedly, and at the same time, the conversion efficiency decreases. The main reason can be

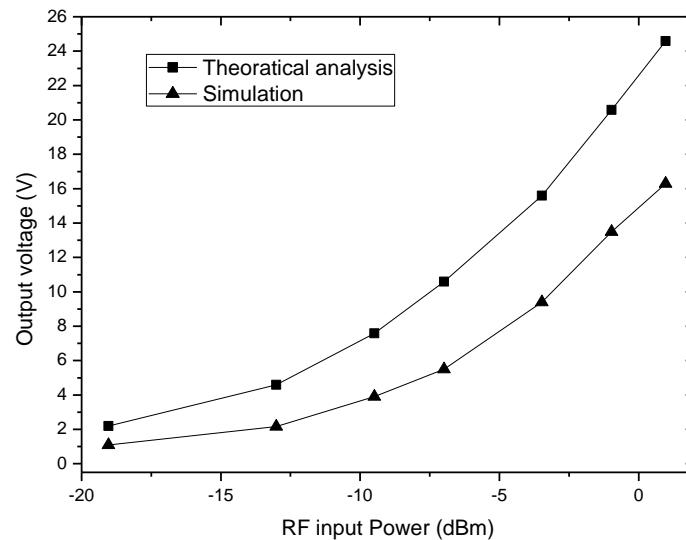
explained by Figure 9: when the output voltage is very high, the reverse voltage on the drain-body junction diode of the bias transistor M0 is close to its reverse breakdown voltage, so the current of M0 can no longer be calculated in accordance with the mirror current. However, in practice, we can limit the output voltage smaller than 8 V through a regulator, so as to protect the chip.

Figure 12. The curves of output voltage, PCE, power consumption and ripple coefficient with different the input power (a) Output voltages with different input power (b) PCEs with different input power (c) Power consumption with different input power (d) Ripple coefficients with different input power.



5. Comparison between the Simulation Results and the Theoretical Analysis

The comparison between Figure 12(a) and Figure 3(a) is plotted in the same figure, as shown in the Figure 13, which indicates their trends are identical, meaning the theoretical analysis in Figure 3(a) is correct.

Figure 13. Comparison of the output voltage of the theoretical analysis and simulation results.

The relationship between PCE and input voltage is simulated, when the RF input is a 900-MHz sinusoid and output load is 20 k Ω . According to the simulation results, we get the PCE of the charge pump multiplier curve with different input voltages as shown in Figure 14. The comparison between Figures 5 and 14 is plotted in the same figure, as shown in Figure 15, which indicates some differences. The simulation results show that PCE increases at the beginning of the input power and then decreases, whereas, the theoretical analysis in Figure 5 shows that PCE increases all the time and tends to saturation. The explanation is as follows: in this paper, we use a diode-connected NMOS and mirror NMOS. Their reverse voltage on drain-body junction rises with input voltage, their leakage current increases when the reverse voltage is close to its breakdown voltage, this bring superfluity power consumption. While in the theoretical model, we don't take into account of breakdown model, which is the origin of difference between PCE curves.

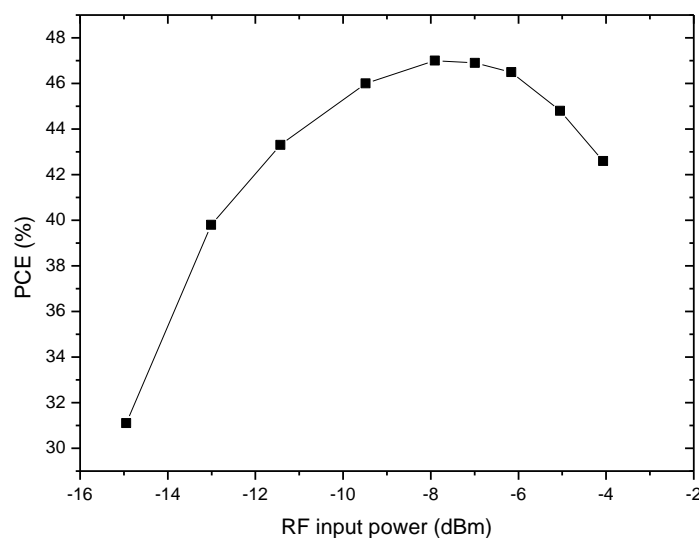
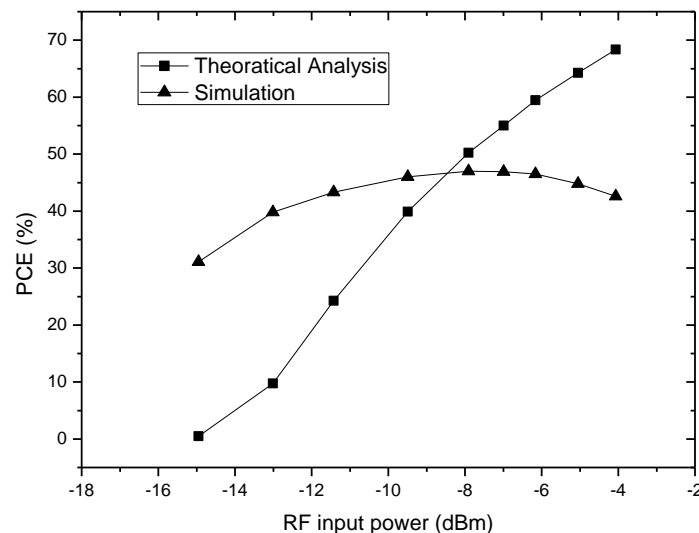
Figure 14. PCE of the 3-stage rectifier with different input power.

Figure 15. Comparison of the PCE of the theoretical analysis and simulation results.

6. Conclusions

The output voltage and PCE of the N-stage rectifier based on the equivalent model of diode are discussed. To optimize the output voltage and PCE, we analyze the disadvantages of the traditional diode-connected MOS rectifier, and propose a novel diode-connected MOS transistor for UHF micro-power rectifiers. The turn-on voltage of the novel structure is only 315 mV, and its reverse saturation leakage current is 415 nA. The proposed diode-connected MOS transistor has been successfully applied in passive RFID tags for PMOS bridge rectifiers [12] and N-stage charge pump rectifiers.

After that, a charge pump multiplier using the presented diode-connected MOS is designed and fabricated in the SMIC 0.18- μm three-metal two-poly mixed signal CMOS technology with embedded EEPROM process. Compared with a traditional rectifier, this circuit has higher PCE, higher output voltage and smaller ripple coefficient. When the RF input is a 900-MHz sinusoid signal with the power ranging from -15 dBm to -4 dBm, PCEs of the charge pump rectifier with only 3-stages are stable between 30% and 47%, achieving much higher efficiency than charge pump rectifier designs reported in journals or conferences. For example, [16] also employed the SMIC 0.18- μm process, but the PCEs are stable between 26% and 36%. Such performances might open promising perspectives for the deployment of passive RFID tag IC and implantable device in standard CMOS process without Schottky diodes.

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