A Report on Testing of ThermaWatts Prototype Ambient Thermal Electric Converter Devices

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Acknowledgments

I would like to acknowledge and thank the following contributors to this work:
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Revision History

Number	Date	Notes (by Section)	By
1.1	12/06/13	Cosmetic and stylistic changes	PMO
1	12/02/13	Initial release	FMO

Section 1. Executive Summary

ThermaWatts Ambient Thermal Electric Converter (ATEC) devices generate electric power directly from heat, *without a cold sid*e, as predicted from models. They use well-known characteristics of semiconductors in a patented layered structure.

This report provides an overview of the conceptual design, the models used prior to prototype development, the results found during prototype testing, and detailed descriptions of the various test rigs that were used to get those results.

This report presents evidence that the ATEC structure converts heat directly to electricity. Data analysis shows a good correspondence between modeled current and measured current. The analysis also shows an exponential increase in output current with increasing temperature. The report explains how EMI and Seebeck effect were aggressively mitigated and addresses the limitations of the prototype ATECs for testing.

Methods of analysis include I–V (current under applied voltage) sweeps, noise injection and test equipment verification. A series of known voltages was applied across the prototype and a precision load across a range of temperatures. An amplifier was used at the load to minimize Seebeck and EMI effects. The resulting I–V sweeps were collected and analyzed. Test equipment performance was further analyzed with noise injection for both a prototype and a blank, and I–V sweeps with known resistors.

We must emphasize that the prototype devices were built and tested to establish the *principle* of direct conversion. The material set for these prototype devices was chosen for its familiarity in making semiconductor structures. The same kind of modeling that predicted that the device would generate power further predicts that other material sets should produce practical amounts of power.

Recommendations based on this report include:

- Replication of these tests with better facilities on similar prototypes
- Construction new prototypes from higher performance materials.
- Testing the new prototypes to verify practical amounts of power output.

Section 2. Ambient Thermal Electric Converter Basic Concept

The Ambient Thermal Electric Converter (ATEC) converts heat into electricity without a cold side. This introduction assumes a familiarity with solid state physics.

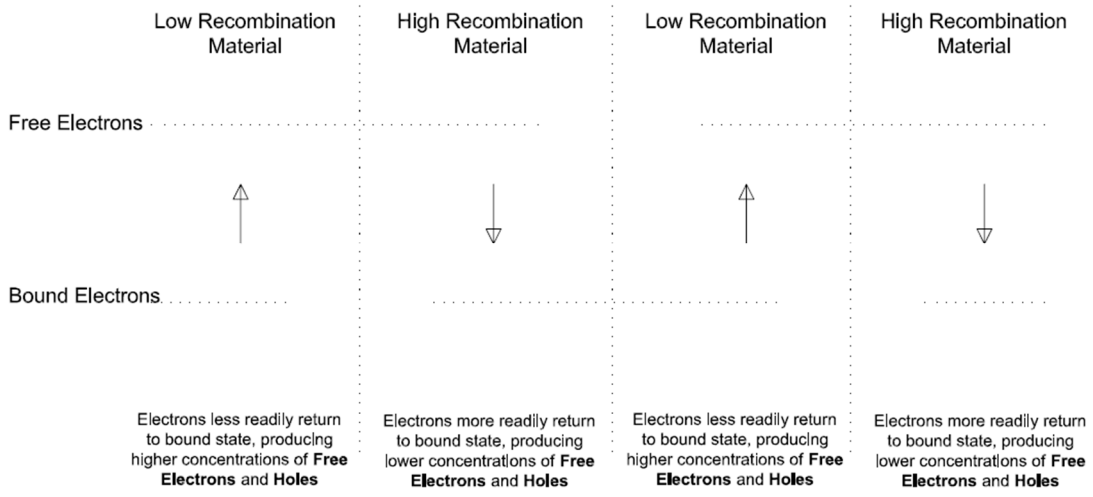
The ATEC uses statistical differences in the properties of semiconductor materials and electrons within these materials. Heat pushes electrons through the structure, consuming the heat and giving us electricity. The following will be presented in this document:

- A simplified model of semiconductor materials
- How electrons move without doping
- The effect of doping on electron flow
- The resulting flow of electrons.

The ATEC is built around the combined properties of pairs of carriers in pairs of materials. The equilibrium carrier density in semiconductors follows the formula:

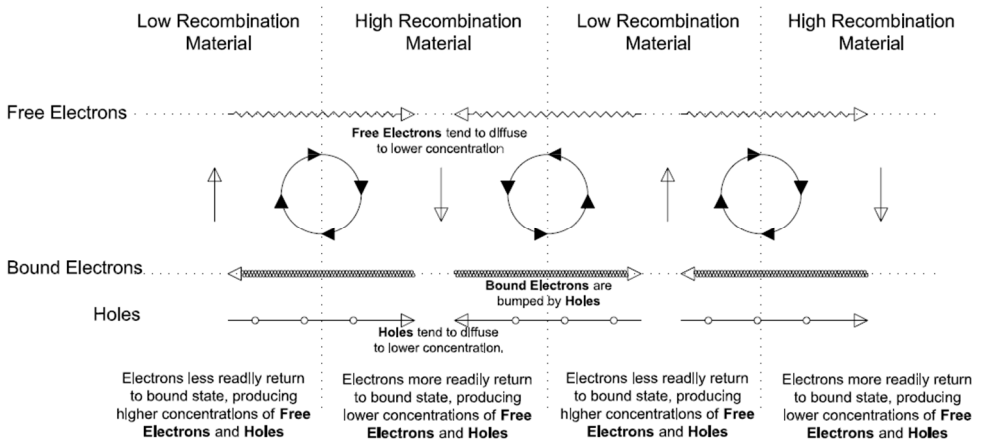
$$n*p = C*T^3*\exp(-E_G/k_B*T)$$

The equilibrium values are for thermal generation only, without the photovoltaic effect, and take into account all recombination (indirect, direct, and Auger) paths. Most of the variation in the material-specific constant C corresponds to different recombination paths. For this reason, we describe the ATEC in terms of high and low recombination materials.



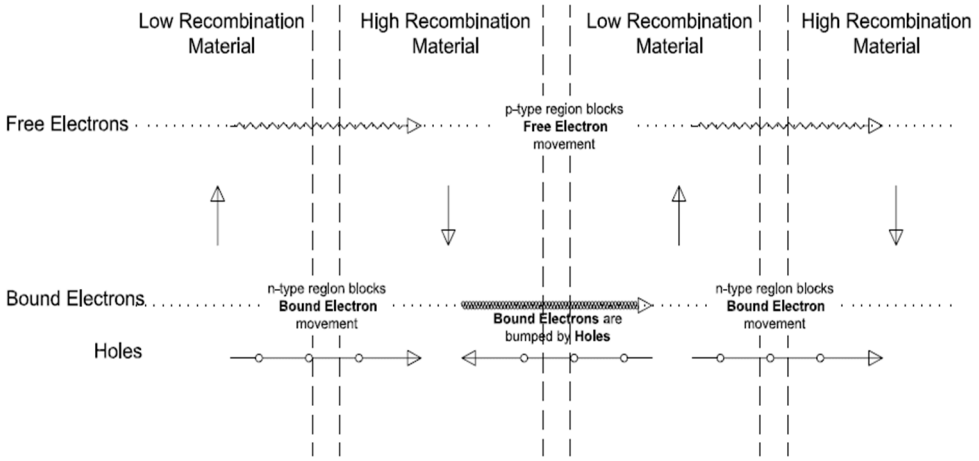
The figure above shows a higher intrinsic carrier density in a low recombination material and a lower intrinsic carrier density in a high recombination material.

An ATEC consists of layers of semiconductor materials (heterostructure), joined at a heterojunction. There is an equilibrium for both electrons and holes across the heterojunction. This equilibrium is dominated by the energy level of each band in a way that approximately offsets the differences in band gaps between the materials. It is not, however, inherently matched to the combined differences of band gaps and densities of states. As a result, there is a net flow from the low recombination material to the high recombination material.



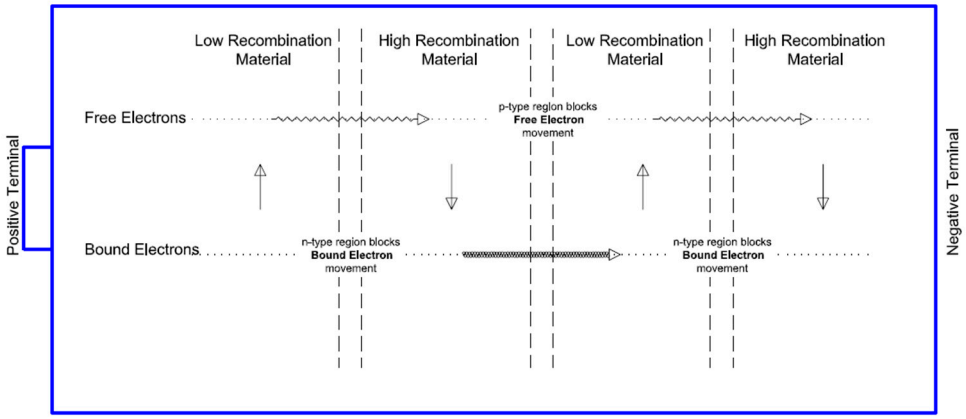
The figure shows that electrons and holes diffuse across the heterojunctions.

Doping is used to select which carrier passes through a layer of material, effectively creating separate paths for holes and electrons. N-type doping adds extra electrons, which allows electrons to diffuse from a low recombination material to a high recombination material while blocking the flow of holes. The effect is a net flow of electrons in that direction. P-type doping adds extra holes and therefore it has the reverse effect on the movement.



The effect of doping is shown above. With positive (p-type) and negative (n-type) doped layers between the low recombination and high recombination layers as shown, the circular flows are broken.

The ATEC layers are assembled into a convenient package for particular applications. The following figure represents a common and easily recognizable package that we might use in a flashlight:



There are many other possible configurations for other applications. Output voltage is increased by adding more layers, in much the same way as stacking batteries increases the voltage. Increasing the temperature also generally increases the current and voltage. The maximum obtainable current depends on the doping and thickness of the layers. For production, consideration should be given to performance, which depends heavily on the materials used and the layering of the materials.

Summary

The ATEC converts heat into electricity by using the known properties of semiconductors wherein heat and differing recombination rates cause different concentrations of electrons and holes. Heat pushes the electrons and holes through separate paths to recombine, which creates an electric current.

Unlike an alkaline or lead-acid battery, the structure and materials of the ATEC are not consumed by the process. Instead, heat is consumed, leaving the structure unchanged. Replacing the consumed heat recharges the ATEC.

Section 3. Modeling the ATEC Structure

3.1. Summary

Silvaco's ATLAS software readily models the ATEC functionality. Each of the elements of the ATEC is well understood, but assembling them together is not within the normal design objectives for solid state physics.

Models of the ATEC structure were created for four purposes before prototypes were fabricated:

1. Generate specific testable predictions based on the theoretical structure.
2. Support engineering of optimal configurations of available materials.
3. Assist in visualizing the internal operation of the structure.
4. Determine if sufficient performance can be achieved to make the undertaking worthwhile.

3.2. Models and Plots

Models were generated using Silvaco's ATLAS version 5.16.3.R. Graphs were generated with TonyPlot 3.8.18.R

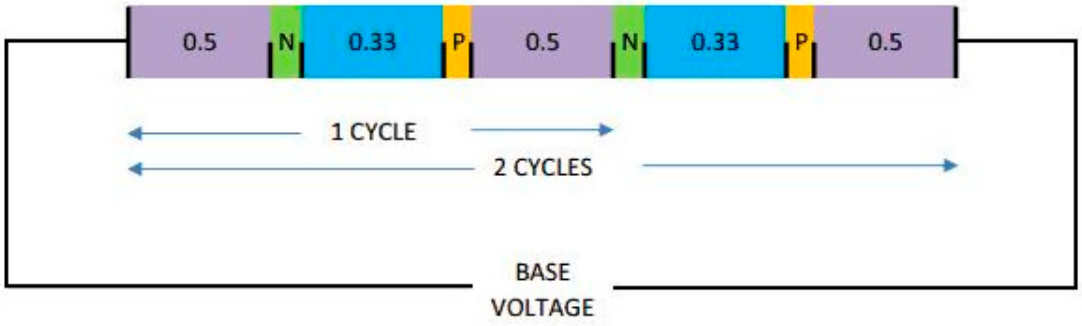
The following graphs were generated to support engineering of Series 2, "S2P1" part. The model predicted a current of 1.2 micro-amps for a complete wafer. For models AlGaAs12 and AlGaAsn17, the structure is as follows:

Contact, named "El1"
AlGaAs y.min= 0.00 y.max= 0.250 x.composition=0.5
AlGaAs y.min= 0.250 y.max= 0.275 x.composition=0.33 donors = 1e+17
AlGaAs y.min= 0.275 y.max= 0.475 x.composition=0.33
AlGaAs y.min= 0.475 y.max= 0.500 x.composition=0.33 acceptors = 1e+17
AlGaAs y.min= 0.500 y.max= 0.750 x.composition = 0.5
AlGaAs y.min= 0.750 y.max= 0.775 x.composition = 0.33 donors = 1e+17
AlGaAs y.min= 0.775 y.max= 0.975 x.composition = 0.33
AlGaAs y.min= 0.975 y.max= 1.000 x.composition = 0.33 acceptors = 1e+17
AlGaAs y.min= 1.000 y.max= 1.225 x.composition = 0.5
Contact, named "Base"

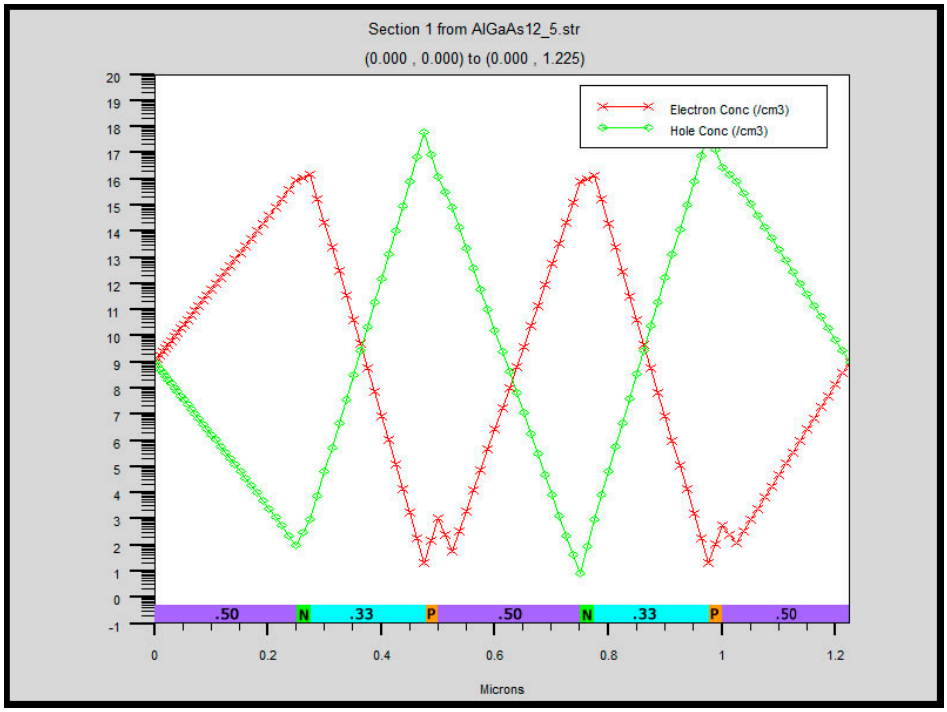
Model AlGaAs8 was an earlier model which used a somewhat different syntax for defining the doped regions. The significant difference is that the doping was on both sides of the heterojunction. For model AlGaAs8 the structure is as follows:

```
region    num=1   material=AlGaAs y.min= 0.00 y.max= 0.25 x.composition=0.5
region    num=2   material=AlGaAs y.min= 0.25 y.max= 0.50 x.composition=0.33334 LED
region    num=3   material=AlGaAs y.min= 0.50 y.max= 0.75 x.composition=0.5
region    num=4   material=AlGaAs y.min= 0.75 y.max= 1.00 x.composition=0.33334 LED
region    num=5   material=AlGaAs y.min= 1.00 y.max= 1.25 x.composition=0.5
region    num=6   material=AlGaAs y.min= 1.25 y.max= 1.50 x.composition=0.33334 LED
region    num=7   material=AlGaAs y.min= 1.50 y.max= 1.75 x.composition=0.5
region    num=8   material=AlGaAs y.min= 1.75 y.max= 2.00 x.composition=0.33334 LED
region    num=9   material=AlGaAs y.min= 2.00 y.max= 2.25 x.composition=0.5
#
elec      num=1   name=el1 x.min=-1.0 x.max=1.0 y.min=0.0 y.max=0.0
elec      num=2   name=base x.min=-1.0 x.max=1.0 y.min=2.25 y.max=2.25
#
doping    uniform y.min= 0.225 y.max= 0.250 n.type conc=1.e18
doping    uniform y.min= 0.250 y.max= 0.275 n.type conc=1.e18
doping    uniform y.min= 0.475 y.max= 0.525 p.type conc=1.e18
doping    uniform y.min= 0.725 y.max= 0.750 n.type conc=1.e18
doping    uniform y.min= 0.750 y.max= 0.775 n.type conc=1.e18
doping    uniform y.min= 0.975 y.max= 1.025 p.type conc=1.e18
doping    uniform y.min= 1.225 y.max= 1.250 n.type conc=1.e18
doping    uniform y.min= 1.250 y.max= 1.275 n.type conc=1.e18
doping    uniform y.min= 1.475 y.max= 1.525 p.type conc=1.e18
doping    uniform y.min= 1.725 y.max= 1.750 n.type conc=1.e18
doping    uniform y.min= 1.750 y.max= 1.775 n.type conc=1.e18
doping    uniform y.min= 1.975 y.max= 2.025 p.type conc=1.e18
```

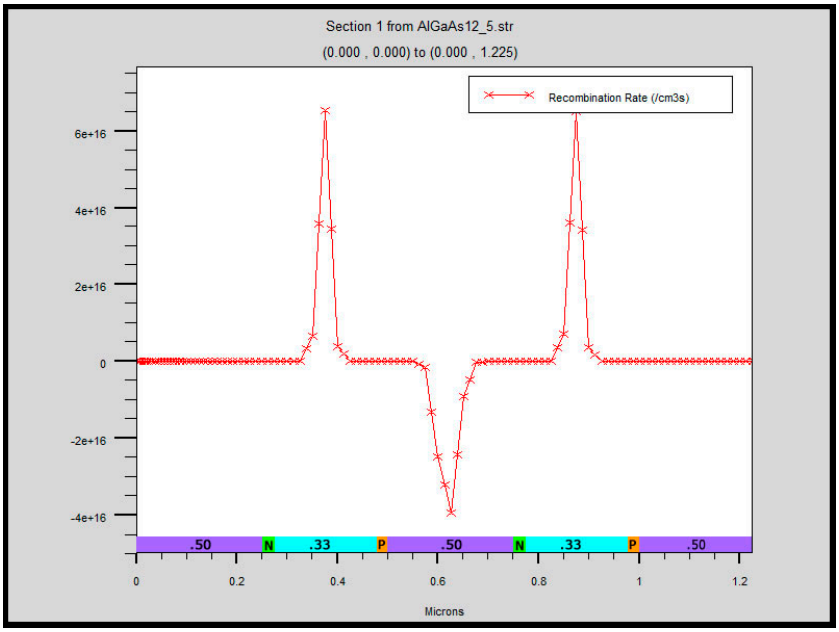
The figure below shows a conceptual view of cycles and "Base Voltage".



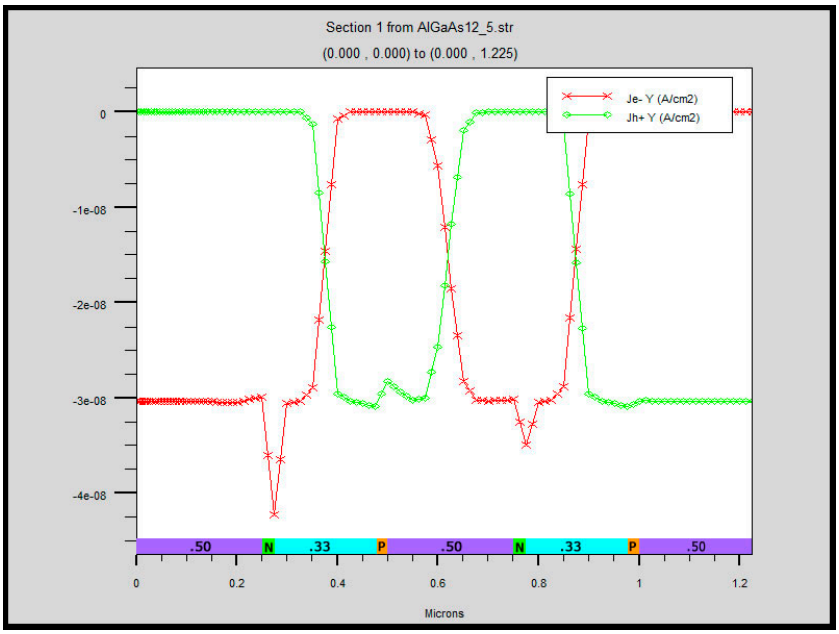
The figure below shows carrier densities through the structure for the model with 10e+18 doping, referred later as Model 18. The *y*-axis is on a log scale. The *x*-axis corresponds to y.min numbers above. N and P indicate n-type and p-type doping, respectively. Doped layers correspond to peaks in the carrier densities. Model run AlGaAs12_5 was at 200 °C.



The figure below shows where carrier generation and recombination occurs. The two peaks of recombination are within the $Al_{0.33}Ga_{0.67}As$ region. The peak of generation is in center the $Al_{0.5}Ga_{0.5}As$ region.

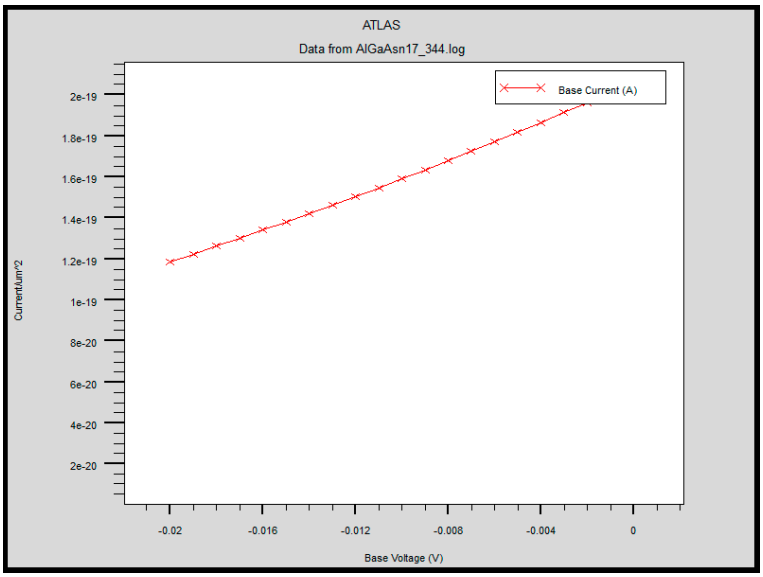


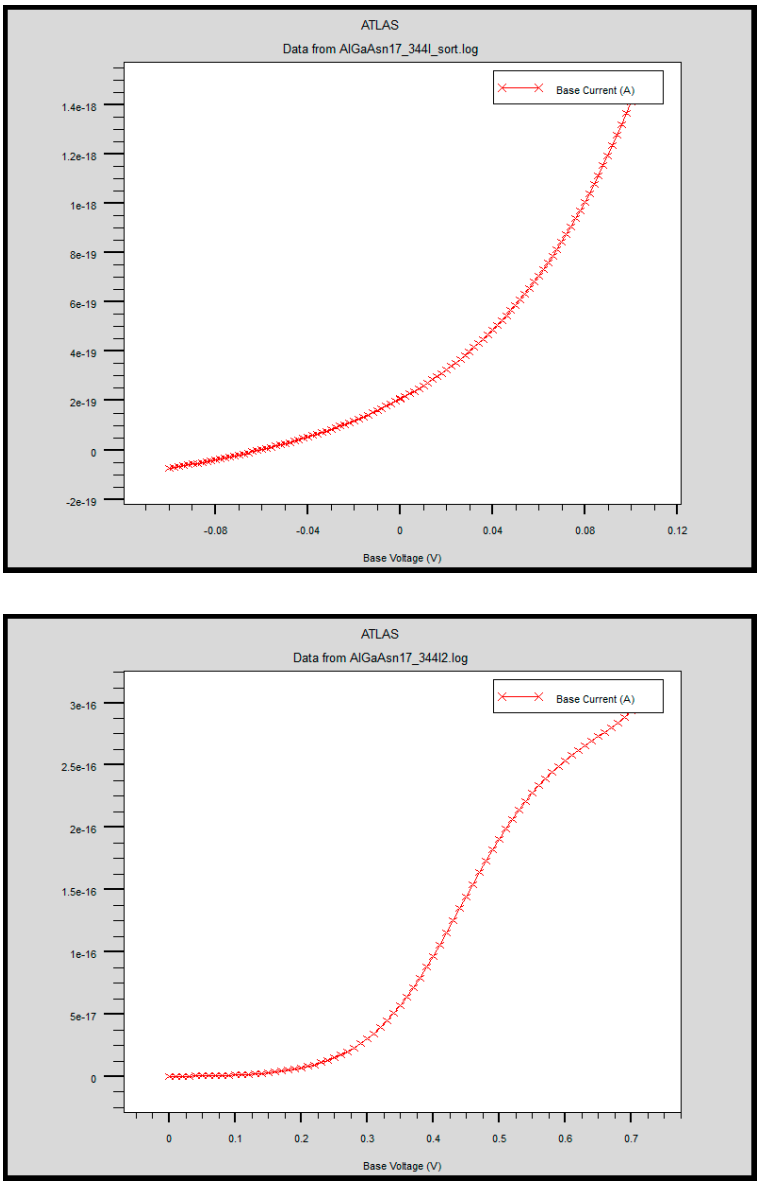
The figure below shows current through the structure. Looking from left to right across the figure, the current flips at the crossover between hole-dominated (in green) flow and electron-dominated (in red) flow at each region of generation or recombination. The spikes on the bottom line are artifacts of the numerical method (Newton's Method) reaching "close enough" and stopping.



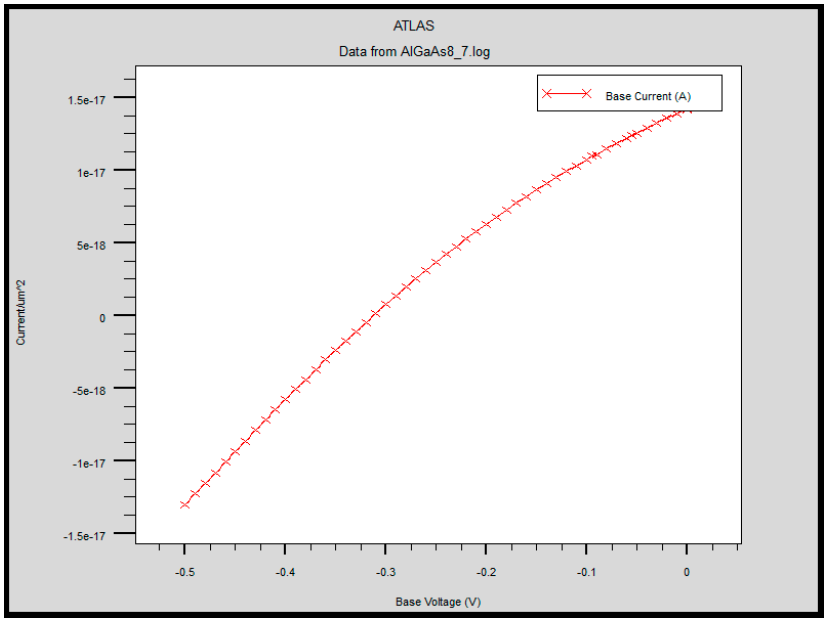
3.3. Responses of Models with Loads

The figures below shows an I–V curve for a modeled Series 2 part at 344 K (160 °F). In this model, the voltage applied to "Base" contact is changed, and the current is recorded. The current displayed is per square micron. At 0 current, the part has an effective series resistance of 56 MΩ over 2 cycles or 280 MΩ for 10 cycles (S2P1). The diode ideality factor here is 2.6 over 2 cycles. For a 10 cycle ATEC, it should have an ideality factor of about 13. The lower figures provide additional context for the first figure. Above 0.7 V, the part experiences diode breakdown, and a rapid increase in current.





The figure below shows a Series 1 ATEC with 4 cycles at 422 K. The current displayed is per square micron and displays both resistance and a diode response. The resistance shown is 77 MΩ for 4 cycles, or 192 MΩ for 10 cycles. The diode ideality factor here is 3.7, which is reasonable for 4 cycles (effectively 4 diodes). Series 1 prototypes had 10.5 cycles. Prototypes should therefore have an ideality factor of approximately 10. A diode with a high ideality factor would show very little rectification of AC.



3.4. Code Used for an ATEC in the Atlas Model

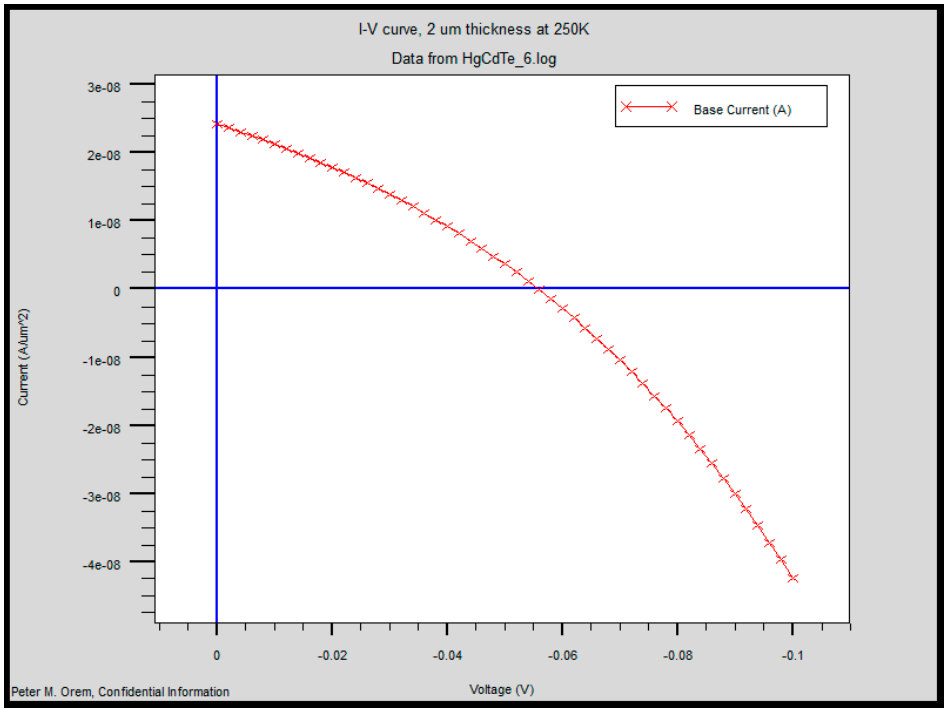
The following is the actual code used to generate the model data, configured for 344.26 K (160 F).

```
go atlas
#
# Proprietary information of Peter M. Orem
#
# SECTION 1: Mesh input

mesh auto

x.mesh loc=-0.5 spac=0.2
x.mesh loc=0.5 spac=0.2
y.mesh loc=0.01 spac=0.01

# SECTION 2: Structure Specification

region num= 1 material=AlGaAs y.min= 0.00 y.max= 0.250 x.composition=0.5

region num= 2 material=AlGaAs y.min= 0.250 y.max= 0.275 x.composition=0.33 donors = 1e+17
region num= 3 material=AlGaAs y.min= 0.275 y.max= 0.475 x.composition=0.33
region num= 4 material=AlGaAs y.min= 0.475 y.max= 0.500 x.composition=0.33 acceptors = 1e+17

region num= 5 material=AlGaAs y.min= 0.500 y.max= 0.750 x.composition = 0.5

region num= 6 material=AlGaAs y.min= 0.750 y.max= 0.775 x.composition = 0.33 donors =
```

```
1e+17
region     num= 7    material=AlGaAs y.min= 0.775 y.max= 0.975 x.composition = 0.33
region     num= 8    material=AlGaAs y.min= 0.975 y.max= 1.000 x.composition = 0.33 acceptors =
1e+17

region     num= 9    material=AlGaAs y.min= 1.000 y.max= 1.225 x.composition = 0.5
#
elec       num=1    name=el1 x.min=-0.5 x.max=0.5 y.min=0.0 y.max=0.0
elec       num=2    name=base x.min=-0.5 x.max=0.5 y.min=1.225 y.max=1.225
#
# modeling thermionic emissions across semiconductor boundaries is required.
interface s.s thermionic

# SECTION 3: Material Models
#
model temp=344.26 srh
Models print

# SECTION 4: Initial solution
#
solve init
save outf=AlGaAs12.str

log outf=AlGaAs12_0.log master

#
method newton trap itlim = 50 maxtrap = 2
solve vbase = 0
save outf = AlGaAs12_0.str
```

3.5. Modeling HgCdTe

The following figure is from a model of $Hg_{1-x}Cd_xTe$ at 250 K (−10 °F). The structure is 2 cycles, for a total thickness of 2 microns, with the same structure as Series 1, and alternates between x = 0.24 and x = 0.14. It shows a short circuit current of 24 μA/μm^2, or 2.4 A/cm^2 and an open circuit voltage of 55 mV. Peak power output is at 30.0 mV and 1.38 A/cm^2, for a total output power of 207 W/cm^3. There is room for further optimization.



Section 4 .Test Results

4.1. Overview of Test Results

Several series of tests were run on prototype ATECs and other test targets to ascertain whether the ATECs exhibit a voltage across them as predicted by models. The models predict that at low voltages, the current will be linear with an offset from zero. The ATECs and other test targets were put in a test jig and subjected to a sweep of input voltage or AC noise while electrical inputs to and outputs from the test target were recorded (see Section 5—Test Setup and Procedures for details).

Four types of tests were run:

1. Qualification of test jig for scaling of its amplifier and for Seebeck effect (see 5.5.1.1)
2. Assessment of the effect of noise on the test jig (see 5.5.1.2)
3. Assessment of the effect of noise on an ATEC (see 5.5.1.3)
4. Measurement of ATEC outputs (see 5.4)

The results and conclusions from these tests are described below. The test data logs from which these results were derived are available online at www.ThermaWatts.com/testlogs/refs.html. The computational steps are described in Section 5.4.

4.2. Voltage Sweeps on Resistors

4.2.1. Purpose

The purpose of these tests is to establish baseline behavior of the test jig, well-understood passive devices (resistors) are run at test targets in the test jig. The results may be used to identify the level of Seebeck effect in the test jig, to calibrate the amplifier and its input resistors, and as a basis for comparison with the prototype ATEC.

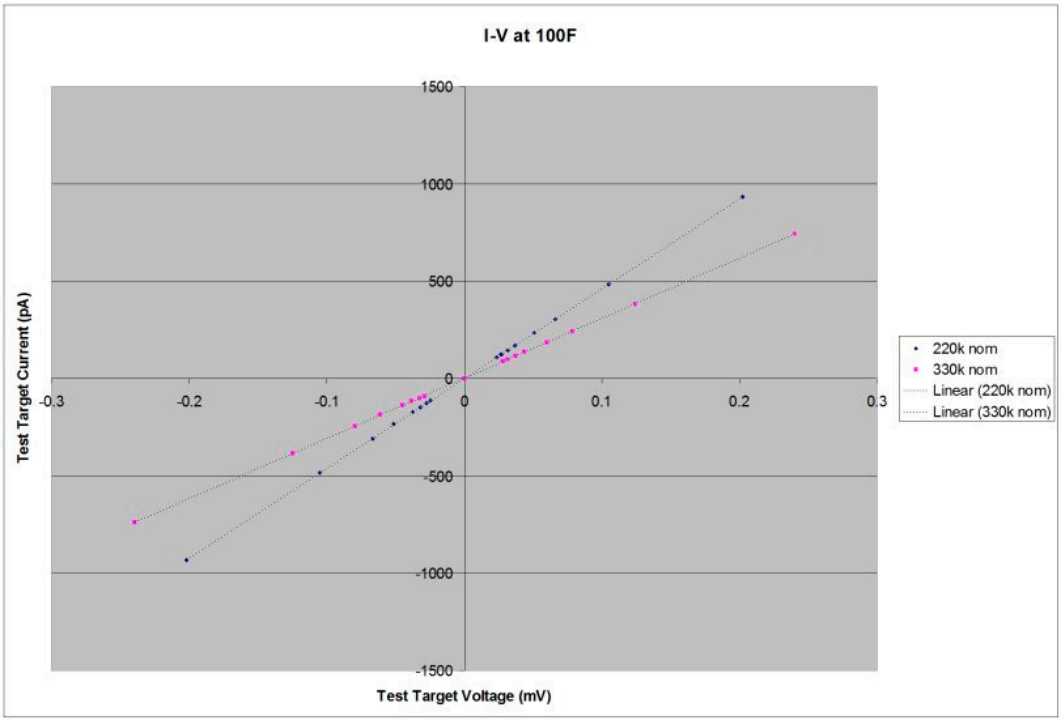
4.2.2. Test Results on Resistors

The configuration for this test is described in 5.8.1.

The graph below is an example of I–V curves of resistors in the test jig. It is one of several run at 100 to 160 °F in 10 °F steps for resistors of 160 kΩ, 220 kΩ, and 330 kΩ. The horizontal axis shows the sweep voltage imposed by the Test Jig across a resistor as a test target. The amplified voltage as measured is converted to current through the test target, in picoamps (pA).

For the two resistors in the 100 °F test, the computed resistances for 220 kΩ and 330 kΩ were 216.9 kΩ and 323.7 kΩ respectively, both well within the 5% tolerances for the resistors.

A least-squares fit is shown through the data points. It passes very nearly through zero current at zero applied voltage—less than 1 pA of error on a scale of more than 1000 pA as indicated by the y-intercept from the fit. See the Summary Tab, cell AU5 of the R_2_ ResistorsNNN.xls files for the results at each test temperature.

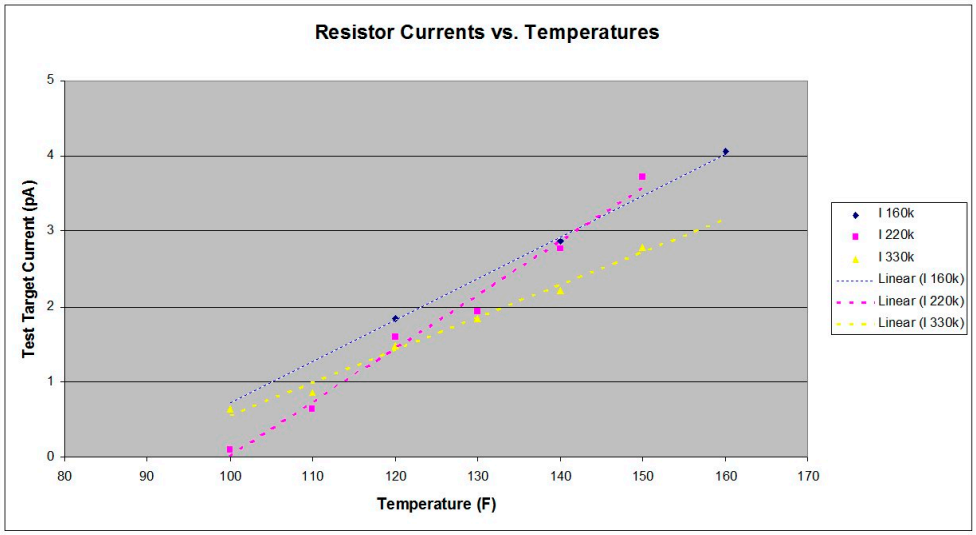


The table below shows the computed resistance for each of the temperatures used in ATEC testing. These are all within the 5% tolerance for the resistors. They all show a downward drift in measured resistance of around 1% with increasing temperature. This is probably from the test target resistor, which is a 5% part of unknown provenance, rather than from amplifier resistors, which are 25 ppm/K. In any case, the source of error from nominal values is not significant for our purposes since bias is eliminated in the output computation.

Computed Resistances for Resistor Tests

Temperature ºF	160k	220k	330k
100		216,843	323,568
110		216,195	323,194
120	161,832	215,638	322,189
130		215,155	321,543
140	161,081	214,566	320,790
150		213,984	320,061
160	160,358	213,631	

The next graph combines the current at zero applied voltage (y-intercept of fit) of the all the tests with resistors at the various temperatures. It shows sensitivity to both resistor size and temperature. Current offset errors are in the range of 0 to 4 pA at zero voltage. These data points are roughly consistent with the data sheet on the Op-Amps (see 5.3.1.1) in the Amplifier.



4.2.3. Comments on Tests on Resistors

The regular behavior, low current at zero sweep voltage, and slopes of the I–V curves-compared to resistor values confirm that the test jig is operating properly.

The match between the resistor values and the computed resistances confirm the scaling of the amplifier.

The deviations from zero current at zero applied voltage is the result of:

- Seebeck effect between the amplifier, which is inside the temperature chamber, and the meter, which is outside the temperature chamber. Any Seebeck effect, which appears to be small, applies to the same extent in later tests against ATECs because the same test jig is used.
- Normal variance in the amplifier input resistors, which are 0.1% tolerance.
- Thermal variance in the amplifier input resistors, which are 25 ppm/K tolerance.
- Imbalance between amplifier input resistors and the test target, as expected.
- Sensitivity of amplifier components and amplifier input resistors to temperature which affect scaling.

The test jig is suitable for measurements in the microvolt range.

4.3. Voltage Sweeps on ATECs

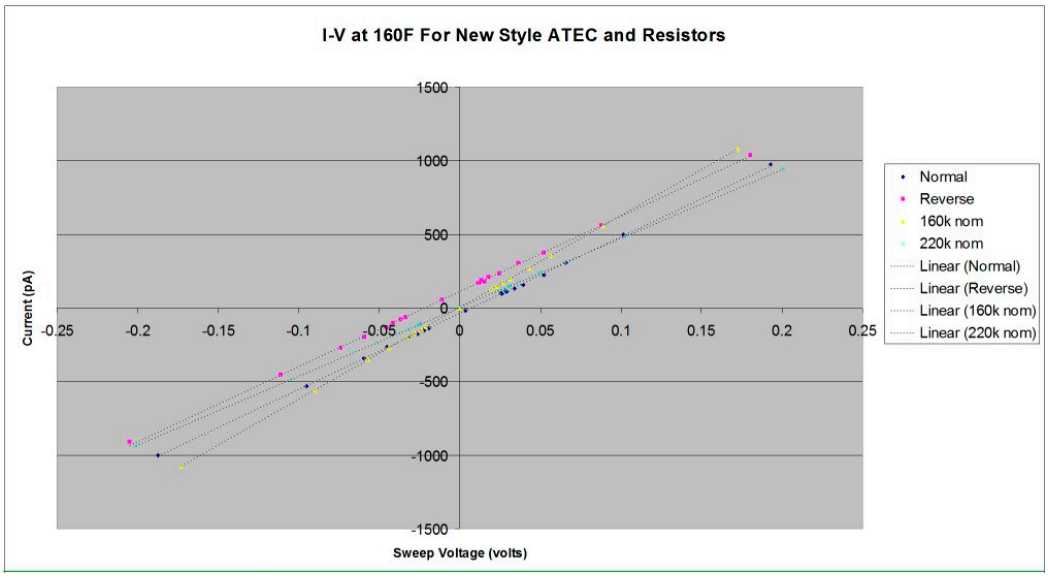
4.3.1. Purpose

The purpose of these tests is to determine whether ATECs produce a voltage, current is measured through each prototype ATECs as it is subjected to a voltage sweep. This establishes a pattern of behavior.

4.3.2. Test Results for ATECs

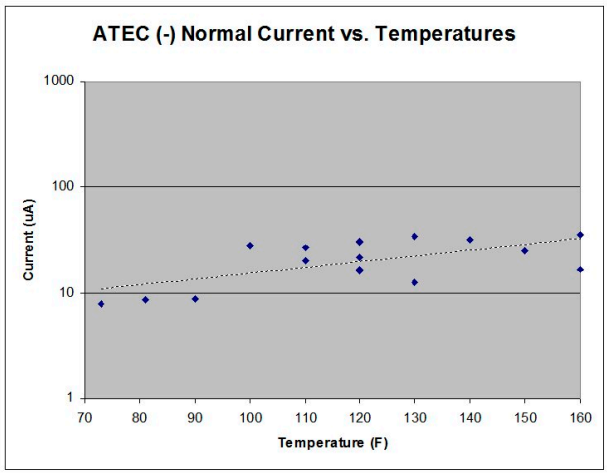
The configuration for this test is described in 5.7.2.

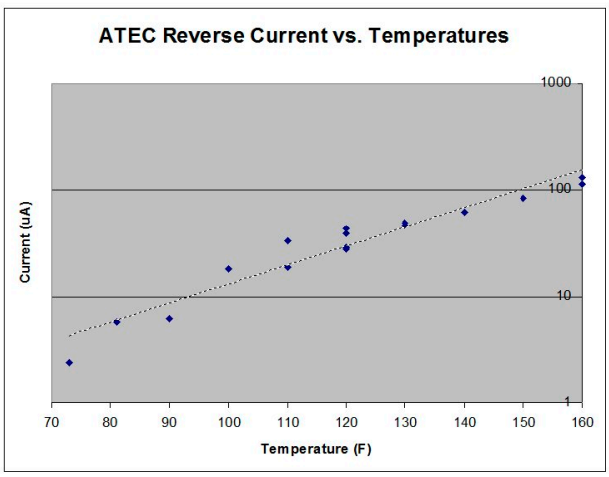
The graph below is an example pair of I–V curves of ATECs in the test jig at the temperature shown. For comparison purposes, the graph includes the plot of resistors.



At the zero sweep voltage, the ATEC is measured as putting out 36 picoamps in one direction in Normal Orientation and 112 picoamps in the opposite direction in reverse orientation.

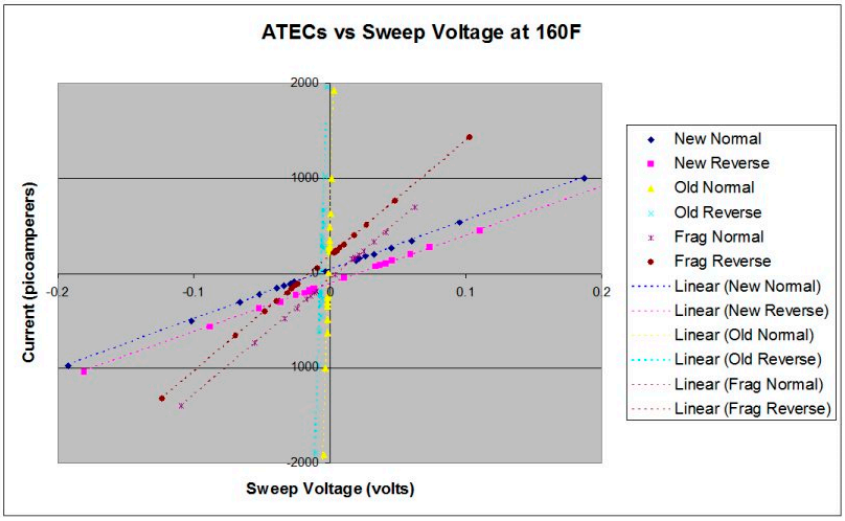
The graph below shows the current as a function of temperature. Current is computed as the intercept from a least squares fit for the S2P1 ATEC at zero sweep voltage and across the temperature range for the ATEC in the normal and reverse orientation (with several runs at some temperatures). This revealed distinctly different responses to the environment as shown by the different line slopes of power versus temperature on a logarithmic scale.





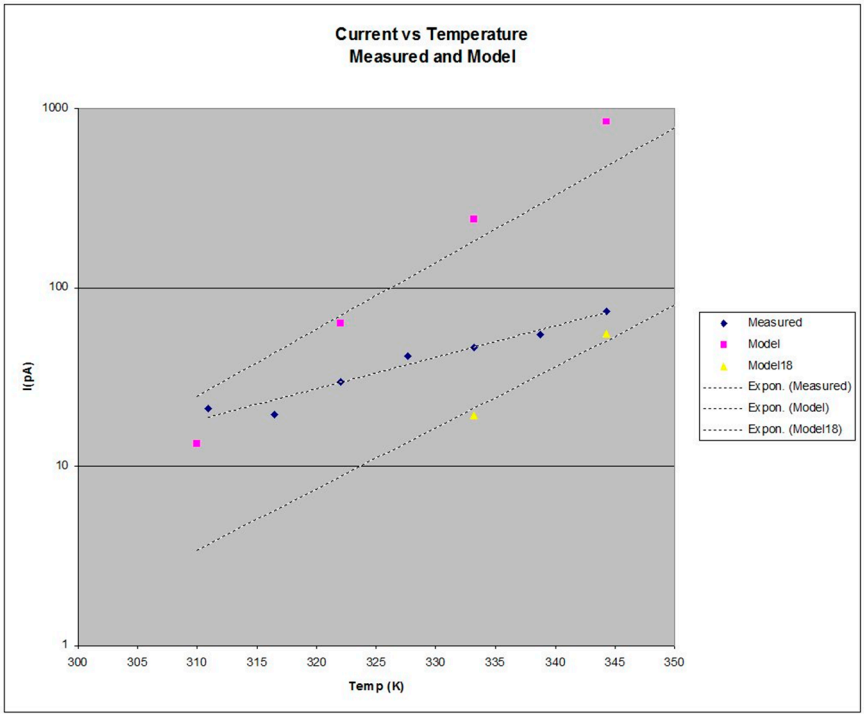
The ATEC responses to the temperature sweeps for normal orientation and reverse orientation are fairly consistent within orientations and distinctly different between orientations.

The graph below shows the current versus voltage for three different ATEC prototypes at 160 °F. The pairs of plots (Normal and Reverse Orientations) show consistent vertical separation in the current. The actual net voltage produced by the ATEC was half the difference between the measured voltages. $V_{nor} = V_{bias} + V_{atec}$ and $V_{rev} = V_{bias} - V_{atec}$, therefore $V_{nor} - V_{rev} = 2 * V_{atec}$.



4.3.3. Comparison of Modeled to Measured Results

The measured output from the S2P1 ATEC is somewhat lower than the modeled output, as shown in the plot below. Voltage of prototype ATECs is much lower (3 orders) than the modeled voltage. The current is between the modeled currents for doping levels of 10^{17} and 10^{18}, as shown in the figure below.



4.4. Tests of Induced Noise through Plates

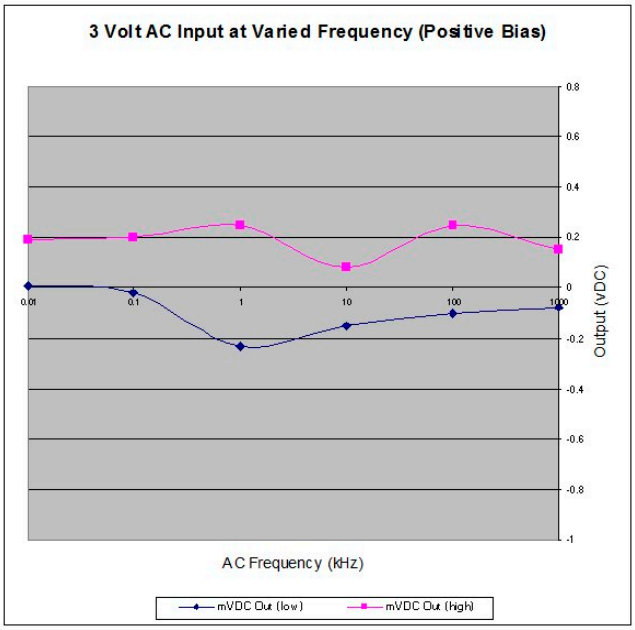
4.4.1. Purpose

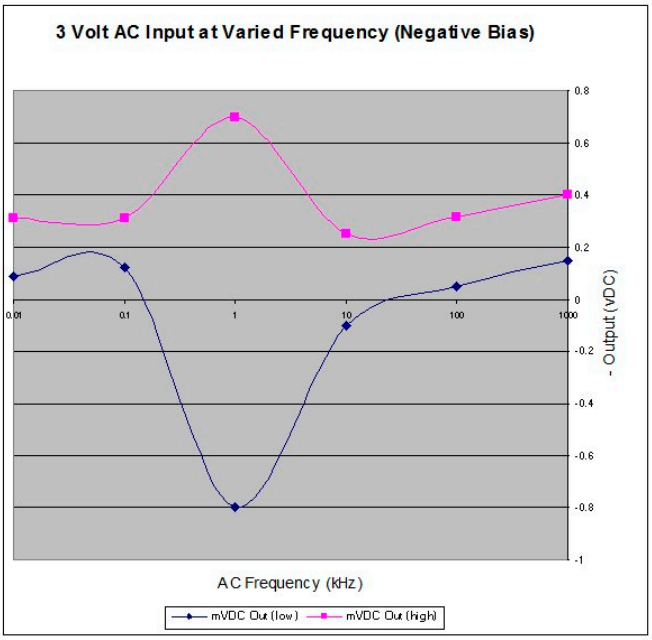
The purpose of these tests was to determine how a high level of induced electrical noise affected the blank and test jig. This established a baseline for the effect of noise on an ATEC, which has the same size, substrate, and contact layers as the blank, and is therefore similarly susceptible to picking up noise.

4.4.2. Test Results of Induced Noise with Blank

The configuration for this test is described in 5.7.4.

The graphs below show the results of applying a 0.2 volt DC bias across the blank while applying 3 V AC noise of varied frequencies with plates parallel and near the blank. The high/low results show the range of DC output, which drifted up and down over time periods ranging from approximately 10 s to more than a minute.





4.4.3. Conclusions from Induced Noise with Blank

This test set shows that the amplifier of the test jig, which is seeing the induced AC voltage, responds with a DC output. Since the Blank has a very low impedance (~1 Ω) compared to the rest of the DC input circuit, we know that the measured drop is not from the DC bias. Consequently, the DC output was coming from the amplifier, with the slow-moving swings caused by time delays in the Op-Amps.

4.4.4. Test of Induced Noise with ATEC

The configuration for this test is described in 5.7.4

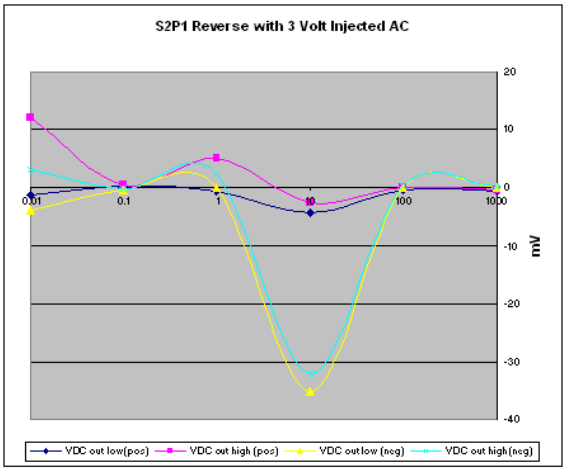
The snippet below shows the results with the prototype ATEC in the forward orientation and the DC bias in the positive direction.

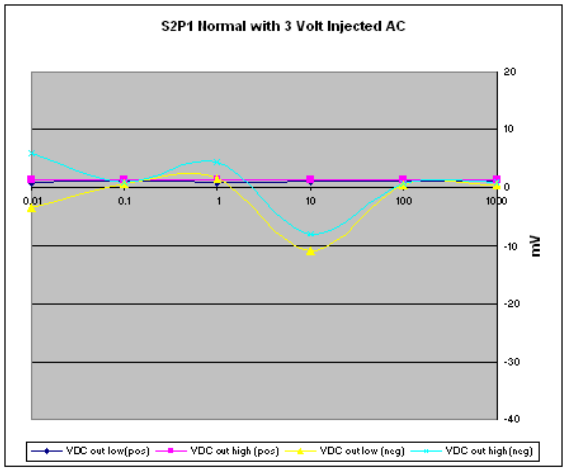
	B	C	D	E	F	G	H	I
4	VDC in(V)	VAC in(V)	F(kHz)	VDC out low (mV)	VDC out high (mV)	VACout (mV)	Part Orient	Drive Orient
5	0	0		3.1	3.3	0.8	Normal	
9		1	0.01	-2	6.8	24	Normal	Positive
10	0.12	1	0.1	2.7	2.9	14	Normal	Positive
11	0.11	1	1	-1	9.6	50	Normal	Positive
12	0.12	1	10	0.7	3.5	13	Normal	Positive
13	0.12		100	2.5	2.8	13	Normal	Positive
14	0.12		1000	2.3	2.6	13	Normal	Positive

Like the similar test using the Blank as the test target, these frequency sweeps exhibit a range of measured DC output at each frequency, and again the swings between high and low output take up to a minute.

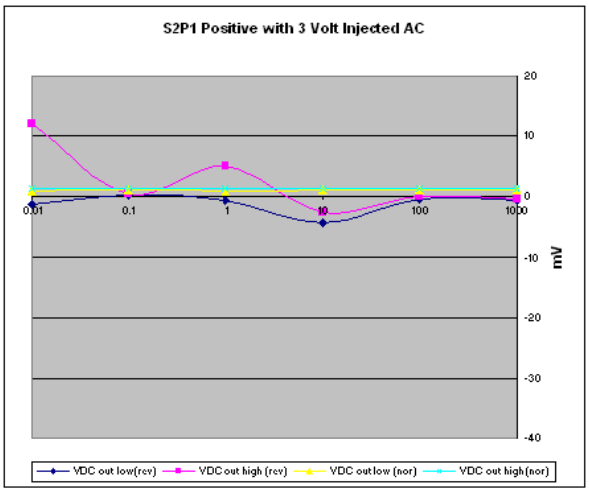
The graphs below, from Induced AC Noise.xls, show the results of applying a 0.3 V DC bias across the S2P1 ATEC while applying 3 V AC noise of varied frequencies with plates parallel and near the ATEC. These graphs combine plots of positive and negative DC bias for each orientation to help show strong similarities of frequency depending on the connection of the signal generator. Again, the high/low results show the range of DC output, which drifted up and down periods from about 10 s to about a minute. Following S2P1 results at 3 V AC, test was repeated on S2P1 at 1 V AC, and on F1 at 3 V AC.

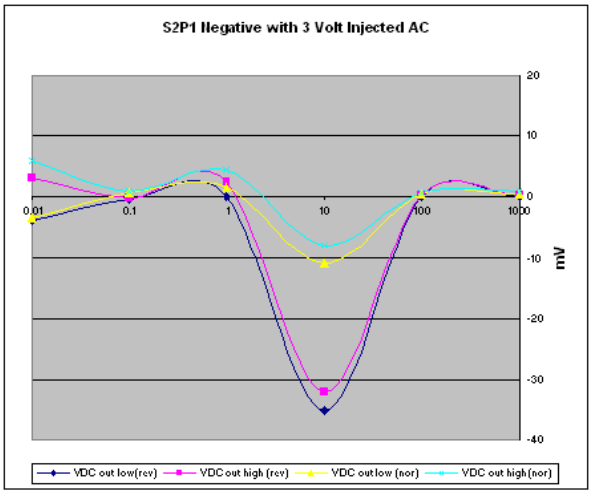
S2P1, 3 V AC, sorted by part orientation:



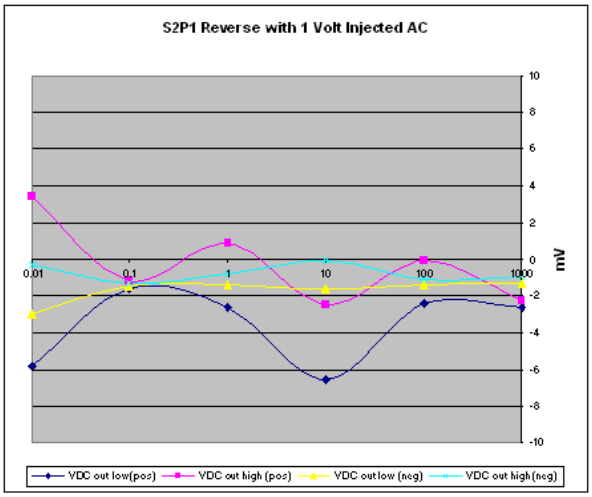


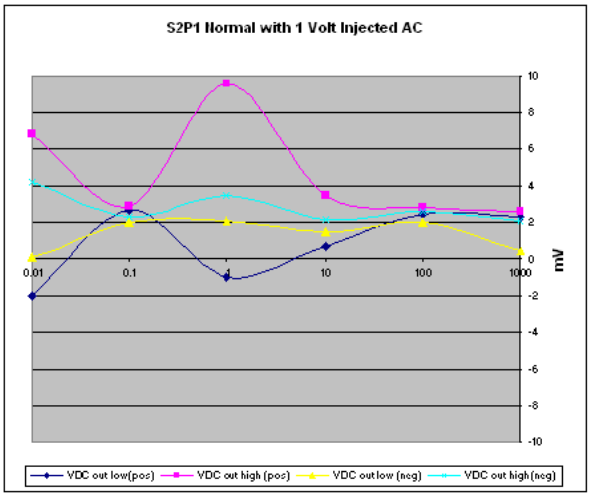
S2P1, 3 VAC, sorted by signal generator connection:



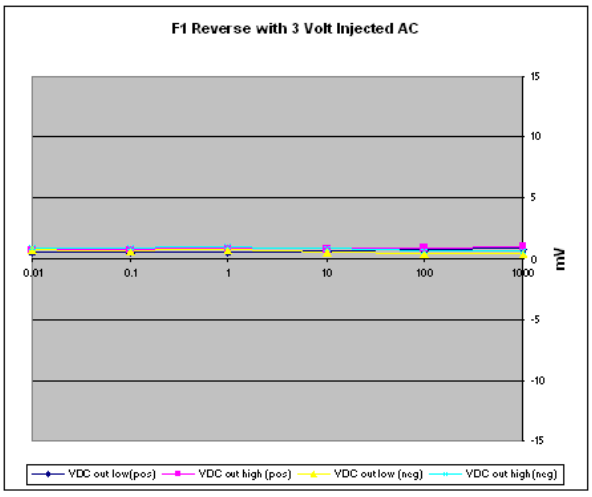


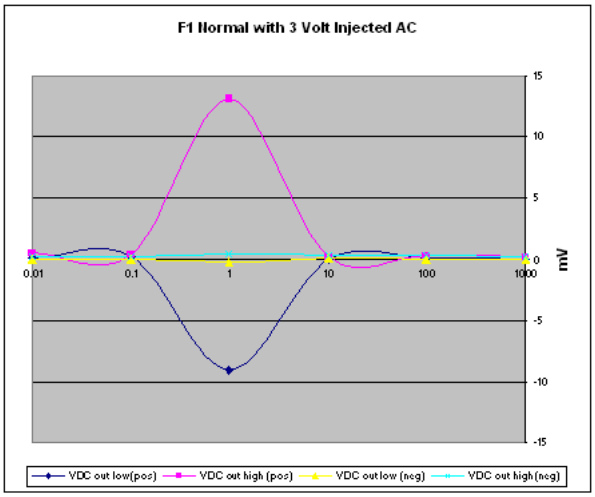
S2P1, 1 VAC, sorted by part orientation:





F1, 3 VAC, sorted by part orientation:





4.4.5. Conclusions from Induced Noise against ATEC

The graphs in 4.4.5 show a clear anomalous response at 10 kHz with 3 VAC_{RMS} for S2P1. The anomaly follows the polarity (grounded vs. driven) of the signal generator. The anomaly disappears at lower voltages and on lower impedance parts. This points to some interaction between the signal generator and the amplifier at high signal levels.

We conclude that induced noise is not the source of our detected voltage.

4.5. Tests with Injected Noise through Voltage Divider

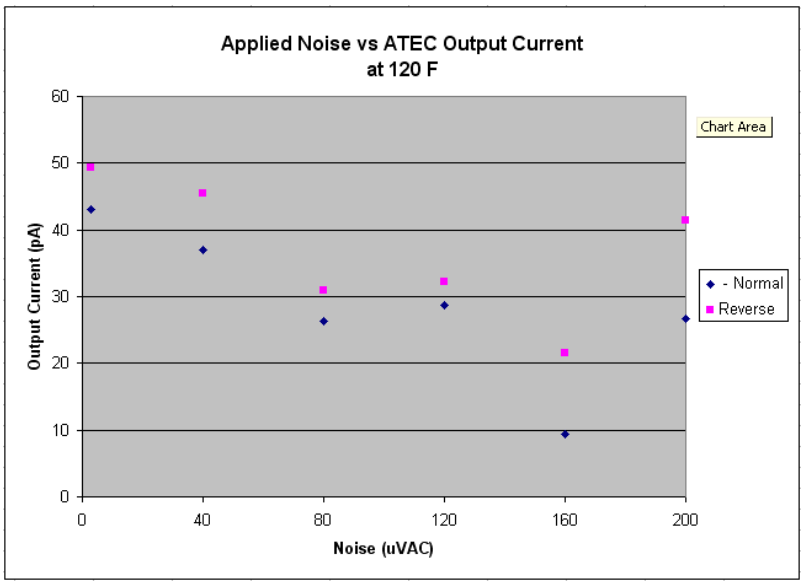
4.5.1. Purpose

The purpose of these tests is to determine whether electrical noise from the environment invalidate the test results. This could be because noise is interpreted as ATEC behavior or because the noise is masking the true behavior of the ATEC. The effect of extreme noise needs to be compared with the effect of extreme noise on the Blank to determine whether the ATEC measurements are being skewed by noise. The effect of moderate noise needs to be measured to see what adjustments might be needed for later tests on ATECs.

4.5.2. Injected Noise through Voltage Divider with Sweep against ATEC

The configuration for this test is described in 5.7.3.

The graph below, from R_2_New120Sweep.xls, shows the effect of exposing the S2P1 ATEC to varying moderate levels of AC driven into the ATEC by a signal generator. At these levels of noise, the output does not exhibit the oscillations seen in extreme noise. Notice that normal orientation output has its sign reversed so that results can be more easily compared.



4.5.3. Conclusions for Injected AC Sweep against ATEC

The first pair of graphs reflect results of extreme noise on an ATEC that are quite similar in nature to the results on the Blank, including slow-moving oscillations. This points conclusively to the amplifier as the source of the oscillations. Any ATEC output is overwhelmed by extreme noise, which results in clear swings in measured output.

The last graph shows that the measured output of the ATEC is affected by moderate noise. In fact, the measured output decreases significantly with noise, so that noise is reducing the measured output of the ATEC rather than contributing to it.

4.6. Additional Tests on ATECs

Additional tests were performed on ATECs to explore their properties. These tests were not as rigorous as other tests.

4.6.1. Photosensitivity

The S2P1, F1 and S1P2 ATECs were tested for photosensitivity.

The configuration for this test is described in 5.7.5.

With direct lighting, S2P1 and F1 both went to amplifier rail (±1.5 V) in both orientations, except for S2P1 in reverse orientation, where it only went to 0.5 V. Voltages matched the output voltages from the Voltage Sweeps in Section 4.4. This means that the photovoltaic effect cannot be ruled out completely, and tests must be run in dark environments.

S1P2 was also tested for photosensitivity during preparation for mechanical stressing in Section 4.6.2. Output polarity was also consistent with sweep voltage, however the amplified output voltage varied from 100 mV to 1.5 V. No clear pattern was identified.

For $Al_{0.33}Ga_{0.67}As$, the bandgap is 1.76 eV. For $Al_{0.50}Ga_{0.50}As$, the bandgap is 1.97 eV. Photons with these energies are visible as red or red-orange light respectively. The ATEC materials do not absorb photons with less energy.

For light sources with a low color temperature, (under 1000 K), the spectrum should contain substantially more 1.76 eV photons than 1.97 eV, which should drive the ATEC backwards. We have not tested this.

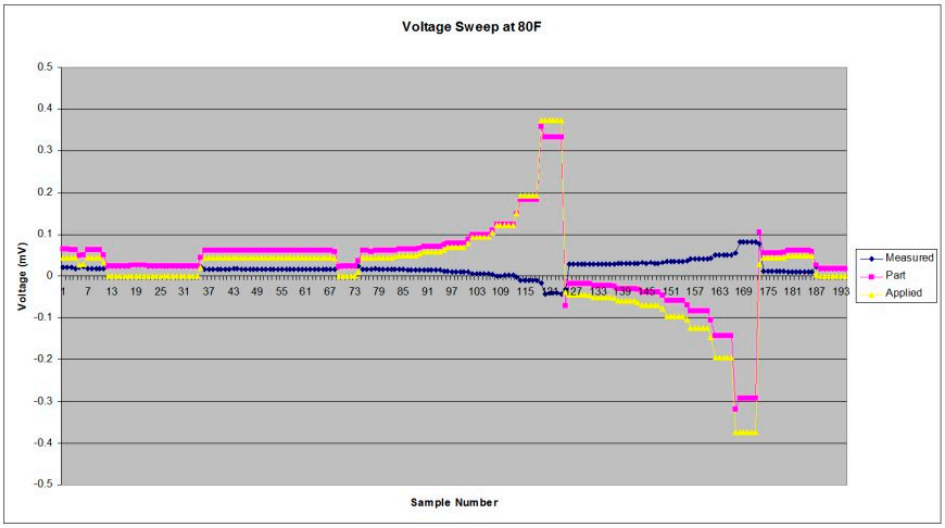
For light sources with a high color temperature (e.g., fluorescent lights), it seems reasonable that contamination would drive the ATEC forward by stimulating extra carrier generation in the $Al_{0.50}Ga_{0.50}As$ layers. Care was taken during testing to prevent light contamination. Further, casual testing was performed turning office lights on and off, and looking for a change in output. No change was observed. Office lights were generally left low as a precaution.

4.6.2. Mechanical Stressing

The configuration for this test is described in 5.7.6.

The results below, from R_3_Old8081_20131023.xls, show the S1P2 ATEC being tested with static mechanical stressing. This is not considered a high quality test result, but it may be indicative. Significant variations in output voltage were observed during testing, with Fluke 8846A readings ranging from approximately 0 to over 0.5 V. Voltage sweeps were run for several different variations of mechanical stress.

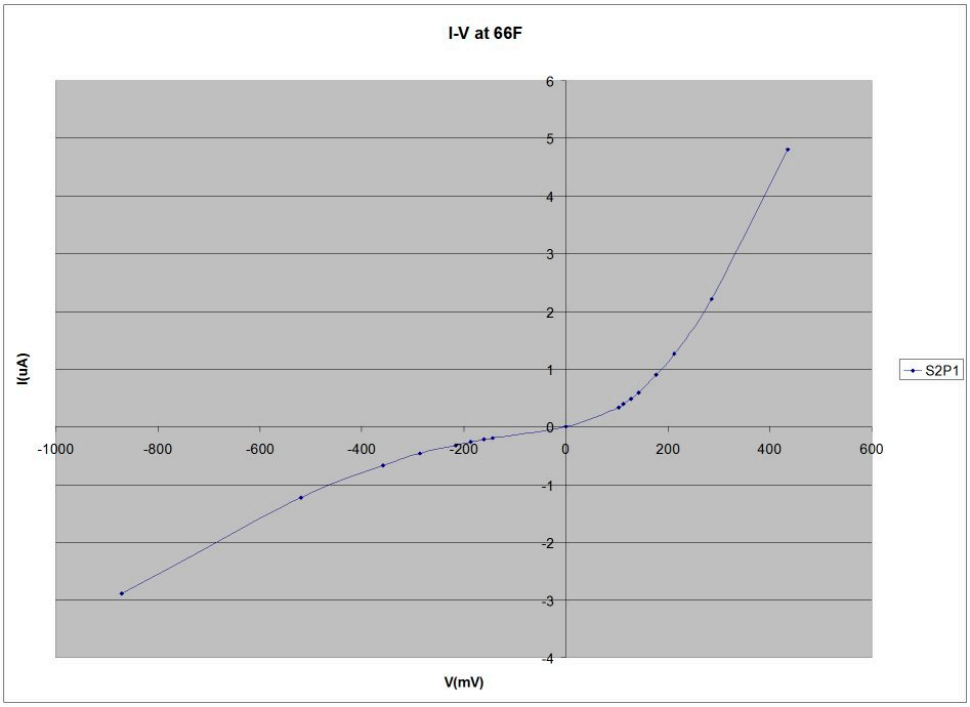
One such sweep is shown below. The yellow line is the calculated voltage applied through the divider. The blue line is the measured voltage at the amplifier inputs. The magenta line is the calculated voltage of S1P2. This run shows 122 pA short-circuit or 126 μV open-circuit, with an effective output impedance of 1.0 MΩ. In unstressed runs, most of the applied voltage would be dissipated across the amplifier, rather than across the part. This probably indicates that some kind of mechanical deformation is altering the electrical properties of S1P2.

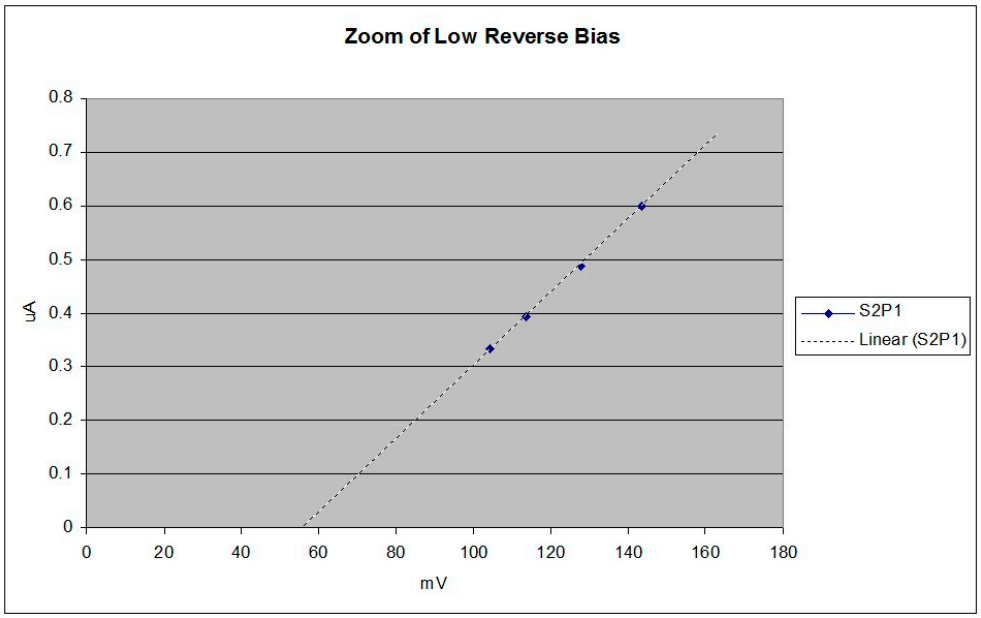


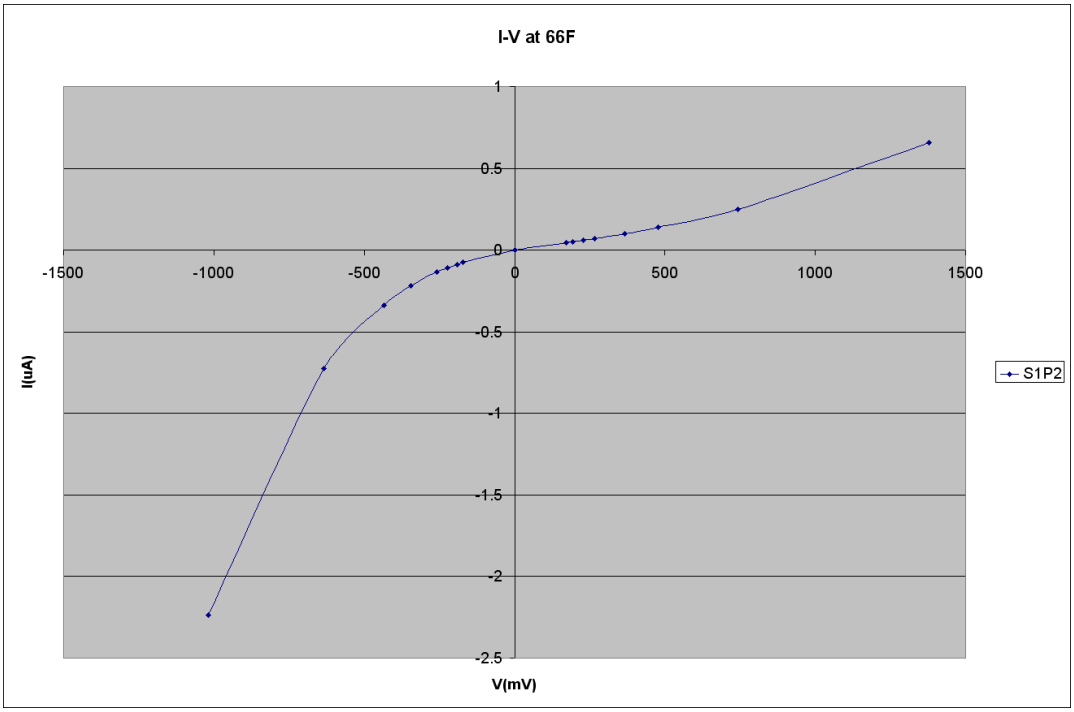
4.6.3. Wide Range Voltage Sweeps

The configuration for this test is described in 5.7.7.

The purpose of these tests was to explore the curve shapes and diode ideality factors in Section 3.3. Data files are R_Wide_OldAmb.xls and R_Wide_NewAmb.xls. S2P1 shows (by first-differences) diode ideality factors of 16 forward and 7.7 reverse. The reverse ideality is lower than predicted by models, and is not shaped like a diode in the zoom image. S1P2 shows diode ideality factors of 14 forward and 26 reverse. The figures below are reversed (−V and −I) from the corresponding figures in Section 3.3 in order to remain consistent with other graphs in this section.







4.7. Conclusions from ATECs and Resistors Test Results

We concluded from the test results shown above:

- I–V curves for the S2P1 ATEC shows distinctly different behavior than those for resistors. We believe that the ATEC is making a contribution to voltage across the entire sweep voltage range, and that the contribution changes direction depending on ATEC orientation. The resistors do not.
- ATECs vs. sweep voltage at 160 °F shows that the S2P1, S1P2 and Fragment ATECs show distinctly different behaviors.
- For tests other than 4.5, the voltage is roughly 4 orders below the model predicted voltage, though still non-zero. Current increases with temperature and is within a factor of 2 of model predictions across the temperature range. Obvious possibilities are that the models overstate the voltage, or that there is some manufacturing defect.
- Whereas the model predicts ATEC S2P1 as having an output impedance of $2.8*10^8$ ohms at 160 °F, the measured output impedance was $1.9–2.1*10^5$ Ω. The same wafer initially measured as 37 ohms prior to post-contact etching. Its impedance 160 °F appears to have consistently increased from $1.68*10^5$ Ω during early tests to $2.11*10^5$ Ω during the last test. These results indicate that S2P1 remains partially shorted.
- The test results of 4.6.2 show voltages closer to model predictions. These results suggest the lower outputs from other tests are a result of manufacturing defects, and that the models are valid.

Therefore, the tests confirm that the ATECs are producing a voltage and supplying a current.

Section 5. Test Setups and Procedures

5.1. Overview of Test Setups and Procedures

This section contains:

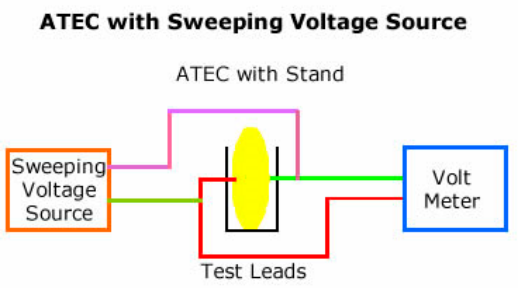
1. The purpose and approach to testing ATECs
2. A description of the test jig and supporting units used to run tests on prototype ATECs

3. Descriptions of the test logs
4. Test results on the test jig itself
5. Specifications of the prototype ATECs
6. Location and list of the test log files

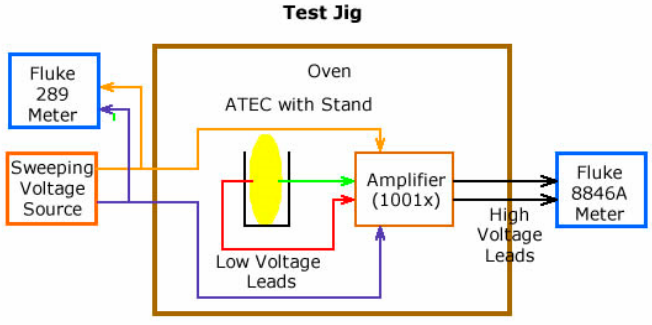
5.2. Purpose and Approach to Testing ATECs

The goal of testing the prototype ATECs was to confirm that they exhibit a measurable, repeatable power output at various temperatures as predicted from models. There are several sources of error that could mask the true behavior or could be mistaken for positive results. These sources include Seebeck effect, rectified EMI and various meter effects. Consequently, the testing process designed to mitigate or assess such errors to isolate accurately the microvolt and picoamp outputs expected.

Testing was run on a test jig that was essentially the same for all tests, varying only as needed for changing the test target, injecting noise, or such. Testing was centered on measuring the voltage across a test target (usually an ATEC) in both normal orientation and reverse orientation. "Orientations" differ by physically reversing the part under test. The normal orientation is defined as having the structure side of the wafer connected to the positive input. To mitigate the effects of test jig bias, the ATEC was subjected to a sweeping voltage across a wide range at each selected temperature. At zero sweep voltage, the measurement in one orientation contains ATEC output plus whatever test jig bias there may be. In the reverse orientation, it contains the same bias minus the ATEC output. Subtracting one measurement from the other cancels out the bias and doubles the ATEC output contribution. Consequently, the difference between measured voltages of an ATEC, divided by 2 because of the doubled contribution, was taken as the actual net voltage produced by the ATEC.



A signal amplifier was developed and situated in the measurement setup, as sketched below, to mitigate the errors from Seebeck effect and from EMI-induced voltages on the low voltage leads. The amplifier boosts the microvolt output expected to more accurately measured millivolt range while mitigating most of the erroneous inputs to the volt meters of the above figure. Both effects are still present, but become less important compared to the amplified signal voltages. This Amplifier needed to be qualified as part of the testing process.



The test jig figure above shows the connections of elements of the test setup. The Fluke 289 measures the output of the voltage source, with any feedback from the test apparatus attenuated at 4001:1. The Fluke 8846A is measuring the same combined voltages, amplified 1001 times (with most noise removed with by-pass capacitors). Sweep measurements for ATEC in normal and reverse orientation with both meters contain an offset at each measurement point of the voltage source at each point.

The Amplifier (1001x) enabled the following mitigations of error:

Error Source	Mitigation
Temperature changes and thermal gradients (Seebeck effect)	Prototype ATEC, amplifier, and low voltage connections are held at nearly uniform temperatures in a Tenney Junior or Binder FD53 Oven able to hold to a specified temperature within about 0.5 °F (see Section 5.3.5)
Induced voltages or currents from EMI on the test circuits (long leads)	Low voltage leads are about 4″ long (1 1/2″ twisted) to minimize exposure to EMI. Amplifier includes noise-suppression circuitry.
Meter precision limits (high precision not readily available for this low-performance material set)	Measured voltage is amplified by 1001, bringing it easily within range of Fluke 8846A (see Section 5.3.4 for meter specifications)
Meter bias (inherent in meters)	This is controlled by reversing the prototype between tests. It is also quantified by tests on resistors.
Meter noise (inherent in meters and interaction with circuits under test)	Meter noise was measured in 10 microvolt range, which—without amplification-would overshadow expected measurements

5.3. Test Jig Components

The test jig is made up of the following components:

1. Amplifier
2. Voltage Source
3. Inputs Meter
4. Outputs Meter
5. Ovens
6. Signal Generator
7. AC Induction Plates
8. Test Target Stand

The subsections below describe design or performance of these components.

5.3.1. Amplifier

This section contains the rationale for the amplifier and enough information to replicate it.

Design Basis

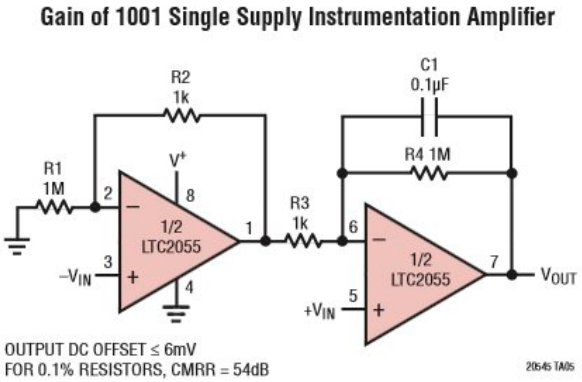
The amplifier was designed to minimize the errors inherent in measuring low-level electrical signals from a test target being subjected to elevated temperatures and in an environment of EMI generated by nearby electrical equipment. The primary test involved measuring the voltage across a known load while applying a known voltage to the combined target and load. This allows the tests to map the I–V characteristics of the test target. Consequently, the amplifier needed to:

- Provide amplification of voltage by about 1000 to take inputs of about 10 μV and put out about

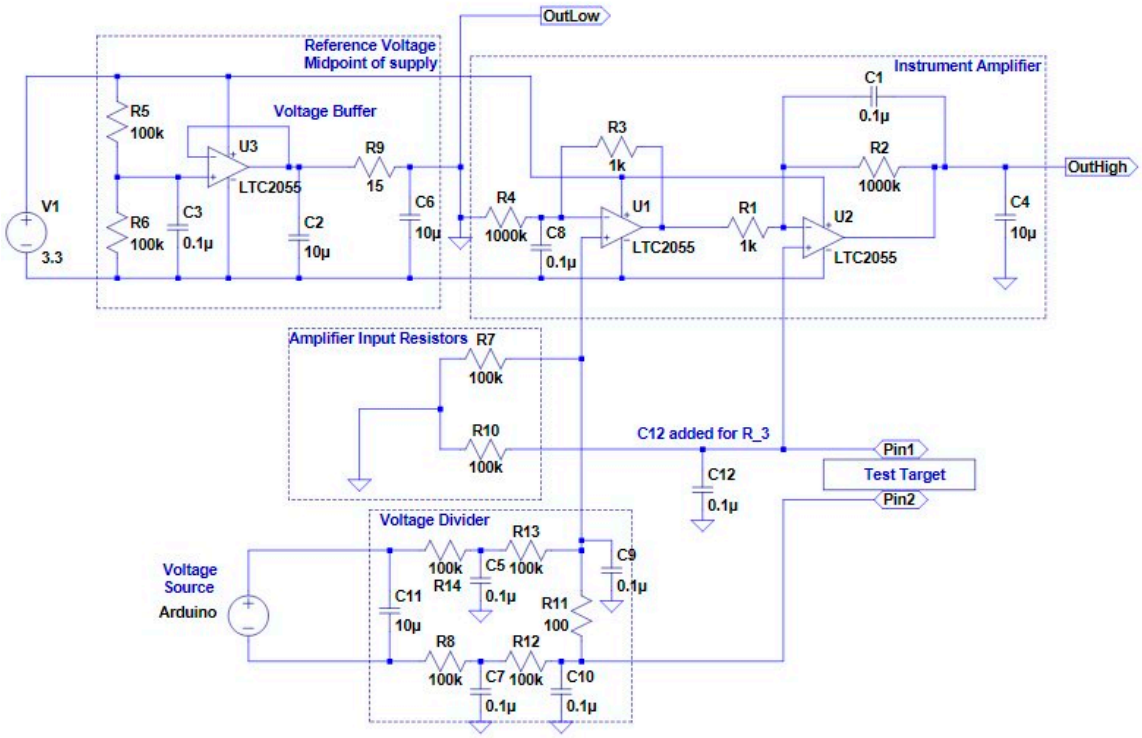
10 mV for reliable results from a Fluke 8846A meter.

- Be able to operate at the same temperatures of the test targets, up to 180 °F to avoid Seebeck effect.
- Remove noise through filtering and through use of a differential input circuit. The amplified noise level as measured as AC voltage across the ATEC or a resistor is typically in the range of 5 mV to 40 mV, very high compared to the DC signal expected of 10 μV. The test location has many noise sources, including nearby computers and other electronics equipment, the test oven, lighting, and electromechanical equipment.

The Amplifier design is based upon application notes from Linear Technology Corporation. http://www.linear.com/docs/5176, page 12 (see U1, U2, etc., in Instrument Amplifier section of Circuit Diagram, below).



Circuit Diagram



Amplifier Inputs

Inputs Pin1 and Pin2 are connected to the test target by twisted pair to the extent practical (and through gold contacts on the prototype ATECs).

Two AA batteries produce V1 to power the Op-Amps U1, U2, and U3. These batteries are located outside the oven and therefore their delivered output may include Seebeck effect, but this effect only matters if the amplifier is putting out its maximum voltage (which does not occur in practice). Otherwise, the effect is cancelled out by putting the voltage differences into the instrument amplifier.

Amplifier Outputs

Output signals OutHigh and OutLow are the output signals connected to Fluke 8846A meter outside of oven. Their voltage difference is 1001 times larger than the difference between Pin1 and Pin2, the voltage across the test target.

Reference Voltage Midpoint of Supply

R5 and R6 produce a reference voltage at the midpoint of the supply voltage.

Voltage buffering takes the reference voltage and supplies that voltage level to other portions of the circuit while protecting those circuits against overvoltages. The combination of C2 and C6 provide filtering to prevent "chopper noise" from entering the rest of the amplifier. Chopper Noise is an artifact of high precision chopper-type zero-drift Op-Amps. Adding R9 and C6 was sufficient in bench testing, as measured AC noise with the 289 went from over 100 mVAC to under the 289's noise floor.

Instrument Amplifier

All components in this section except C4 and C8 are from the LTC2055 reference design as noted above. As configured, the instrument amplifier has a gain of 1001 as shown in the Linear Technologies application notes. That is, the voltage output at U2 will be 1001 times the (U2+ - U1+), up to the limit of V1.

All resistors are 0.1% tolerance, ± 25 ppm/K.

C4 and C8 control chopper noise.

Amplifier Input Resistors

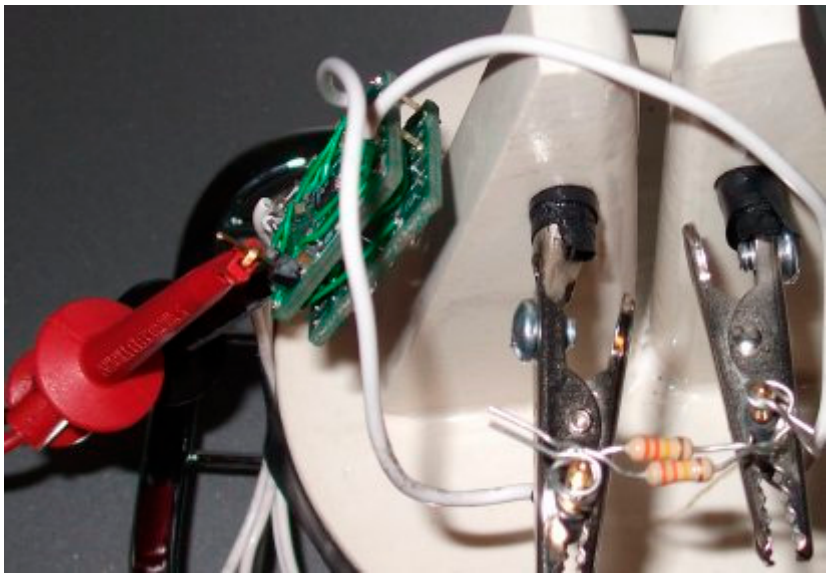
R7 and R10 provide the input buffering to pull the Amplifier inputs towards midpoint. The Op-Amp inputs leak current (on the order of 1 pA max), and will drift to the positive rail without sufficient pull-down. R7 and R10 provide an effective resistance across the instrument amplifier of 200.0 kΩ. They are 0.1% tolerance.

Amplifier Voltage Divider

The voltage divider allows relatively high voltages from outside the oven to control precise voltages inside the oven. R8, R12, R13, R14 and R11 divide the input voltage by 4001 (derived from: 100 Ω/(100 Ω + 4*100 kΩ)). These are 0.1% parts, with 25 ppm/K variation. The voltage divider also serves as a low pass filter.

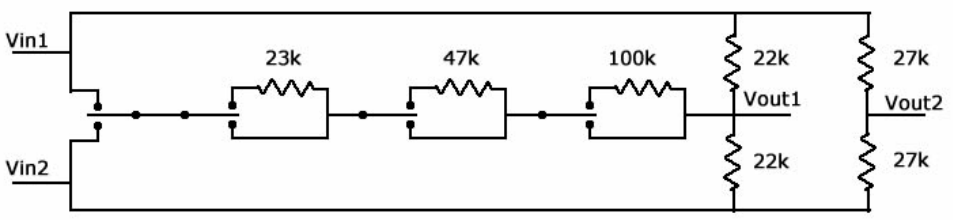
Amplifier Construction

The amplifier is constructed on two SchmartBoard 204-0006-1 "0.65 mm Pitch SOIC to DIP" adapters assembled back to back, with standoffs.



5.3.2. Voltage Source

The voltage for sweeping through the test target is produced from batteries by a network of resistors and relays, controlled by an Arduino Uno controller (see http://arduino.cc/en/Main/ArduinoBoardUno).



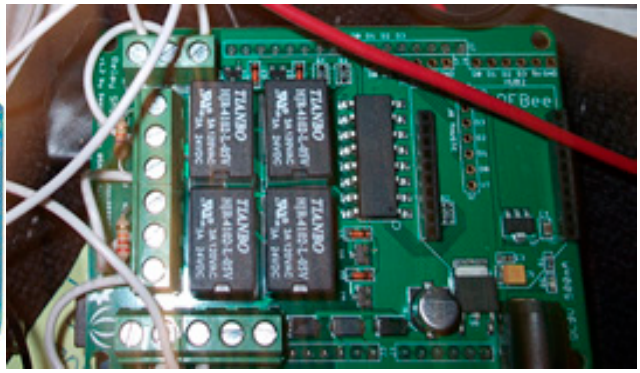
The Arduino Uno controller steps through 16 relay configurations to make test points, one step per a minute, starting when power is applied. It repeats the first two test voltages and halts. The last test point (nominally 0 V) comes from removing power to both the batteries and the Arduino Uno controller.

The voltage values from the voltage source are not precise because the tolerances on the resistors are 5%, and the batteries which drive it discharge over time. This imprecision does not affect the measurements because its measured value is what is used in calculations. Rather, it provides a series of measurement points used to observe the behavior of the prototype ATEC.

Connecting power to the Arduino injects 1–35 μV of AC noise, as measured and recorded by the Fluke 8846A at the Amplifier output. This is most likely 60 Hz, coupled through the voltage source relays. The amplitude varies from test to test.

Vin1 and Vin2 come from a battery with an Arduino-controlled voltage source, and are measured outside the oven, so they are not at that point subject to Seebeck effect. However, their connections to the voltage divider are, so the Seebeck effect needed to be estimated. Assuming 20 μV/K Seebeck and a 50 K difference on the wire gives 1 mV Seebeck on a 1 V signal. Variations in Seebeck should be even smaller, taking it well below the sensitivity of the test jig. Therefore, impact on the voltage is not an issue.

Arduino controller and Seeed relay board are shown below:



5.3.3. Inputs Meter

A Fluke 289 was used to measure input DC voltage to the voltage divider and amplifier and record to a computer. It is capable of 0.025% accuracy. See specifications at http://www.fluke-direct.com/shop/itemDetail.do?itm_id=307737&itm_index=0&item=289&manufacturerItemNumber=2675778.

FlukeView Forms software was used to record all voltages.

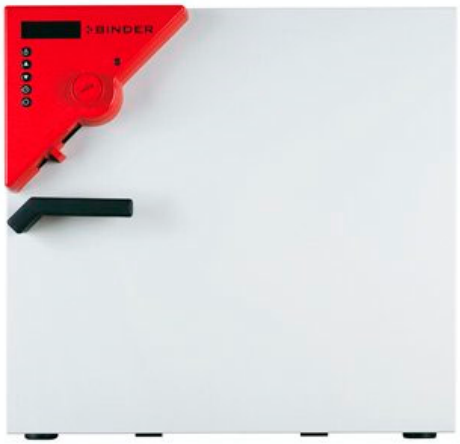
5.3.4. Outputs Meter

A Fluke 8846A was used to measure the output AC and DC voltages at the test target and record them to a computer. It is capable of 6.5 digit resolution. See specifications at http://www.fluke-direct.com/shop/itemDetail.do?itm_id=154822&itm_index=0&item=8846A.

5.3.5. Ovens

The primary oven is a Tenney Junior from SPX Thermal Products Solutions of SPX Corporation. Its specifications are at http://www.thermalproductsolutions.com/products/compare.aspx?cType=1.

The secondary oven, used as a Faraday Cage in noise tests, is a Binder FD53. Its specifications are at http://www.binder-oven.us/oven/drying-ovens/fd-series-forced-air/fd53/.



5.3.6. Signal Generator

EZ Digital FG-7002C is capable of putting out a sine wave for range of frequencies and voltage amplitudes. Its specification may be found at http://ezdgt.en.ec21.com/Sweep_Function--2139379_303061.html and http://www.testequipmentdepot.com/ezdigital/fg7002c.htm

Notice that both frequency and amplitude controls (7 and 18) are knobs, so those values are not precisely reproducible. Also of note, signal ground is tied to chassis ground, giving a single-ended

signal, rather than differential. This means that when the signal generator is used, a record must be kept whether the signal is on the positive or negative input of the amplifier.

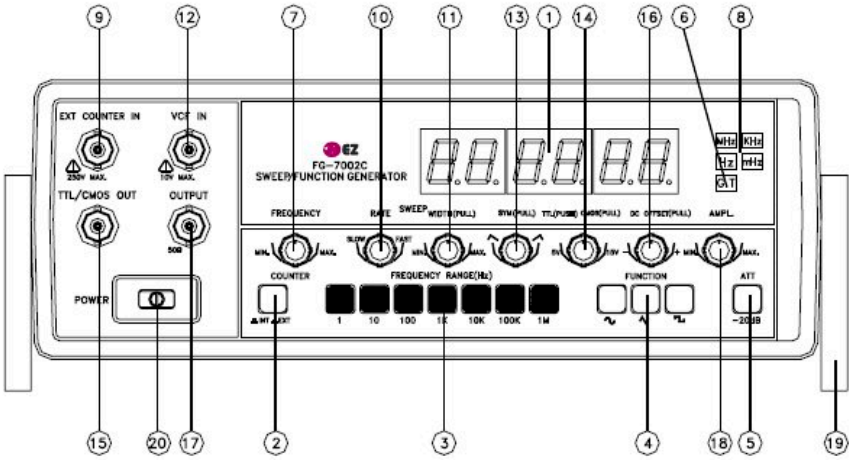


FIG 1. FRONT PANEL OPERATOR'S CONTROLS

5.3.7. AC Injection Plates

The image below shows two copper plates with insulating tape on the interior surfaces. In test, the wafer is inserted between the plates, allowing a voltage to be capacitively coupled onto the wafer.

5.3.8. Test Target Stand

With the exception of resistors, test targets were mounted in a custom ceramic device designed to minimize scratching and to provide stable wire and contact positions. They were built by James Anderson (www.artman.biz).

5.4. Test Log Contents and Computations

This section describes what was recorded from prototype ATEC testing, how the measurements were captured, where the data are displayed in files, and how summary data were computed and displayed.

5.4.1. Test Procedure Summary

For a given test, the test target was set (with a ATEC in normal orientation and then reverse orientation), the oven set for successive temperatures, and then voltage sweeps made within each temperature. For a sweep, start of sweep and the recording meters was done manually, resulting in skewed start times. Time tags on the recordings were used to synchronize the data used for analysis. Recorded data were captured off the recording meters after each sweep and assembled into Excel files and tabs.

A test run for a prototype ATEC consists of one (or more) sweep(s) of the voltage source for each orientation (normal and reverse) for each of several temperatures. A test run for a resistor consists of one sweep at each of the same several temperatures.

5.4.2. Test Results Data Files

The test results data files are organized around test target and test temperatures. Excel files are gathered from the recording meters and named for the target and temperature. For example, the file for the runs for the S2P1 ATEC at 160 °F is named R_2_New160.xls.

The complete Excel files may be downloaded from links on http://www.ThermaWatts.com/TestLogs/.

Data are assembled into tabs in the Excel files with a name with the following parts:

Logyyyymmdd (year, month, day)

a target designation (New, Old, F1 or resistance)

ttt, the temperature in °F

Test target orientation (Nor, Rev)

Voltage source from Fluke 289 or results from the Fluke 8846A (_Vin, _Vout)

Thus, the log of measurements from the Fluke 8846A on May 6, 2013 for the S2P1 part at 160 °F with normal orientation is Log20130506New160Nor_Vout.

A tab named Summary contains computed summary data and graphs for the test target and temperature.

Below are shown the beginning records of recordings for samples of each of the tab types, with notes for interpreting the columns.

Input Voltage Log Tabs Format

Input tabs in the Excel files for a test are named with a text string that concatenates:

- "Log"
- Test date, as yyyymmdd
- Test Target: "New", "Old", "F1", or "Blank" for prototype ATEC designations (see 5.6), or nnnk for resistors of nnn kOhms
- A visual separator "_"
- Test run temperature ttt in °F
- "Nor" or "Rev" for normal orientation or reverse orientation, respectively

"Vin" for input voltage measurements

The snippet below is from the tab Log20130522New160_NorVin of R_2_New160A.xls. It shows the Fluke 289 recording of the Source Voltage. Note the meter identification upper left.

	A	B	C	D	E	F	G	H	I	J	K
1	FLUKE 289	V1.12	15100066 Peter M Orem								
2											
3	Start Time	Stop Time	Elapsed Ti	Interval	Total readings	Intervals	Input Events	Session Name			
4	5/22/2013 17:06	5/22/2013 18:15	1:09:33	0:00:10	424	418	7				
5	Max Time	Max	Average	Min	Min Time	Scaling					
6	5/22/2013 18:03	1.5526 V DC	0.1366 V D	-1.5503 V	5/22/2013 18:11	(none)					
7											
8	To display full timestamps use Format Cells 'm/d/y hh:mm:ss.0'										
9											
10	Reading	Sample	Start Time	Duration	Max Time	Max	Average	Min Time	Min	Description	Stop Time
11	1	0.1820 V DC	06:15.2	00:09.9	06:21.0	0.1821 V DC	0.1820 V DC	06:15.2	0.1820 V DC	Interval	06:25.1
12	2	0.1821 V DC	06:25.1	00:10.3	06:25.1	0.1821 V DC	0.1820 V DC	06:25.6	0.1820 V DC	Interval	06:35.3
13	3	0.1820 V DC	06:35.3	00:10.1	06:35.3	0.1820 V DC	0.1820 V DC	06:35.3	0.1820 V DC	Interval	06:45.5
14	4	0.1820 V DC	06:45.5	00:09.6	06:48.5	0.1821 V DC	0.1820 V DC	06:45.5	0.1820 V DC	Interval	06:55.1
15	5	0.1820 V DC	06:55.1	00:10.2	06:55.1	0.1820 V DC	0.1820 V DC	06:55.1	0.1820 V DC	Interval	07:05.3

About the Row 10 column header descriptions, from left to right:

- Reading is a sequence number from start of recording
- Sample is the measured value at Start Time
- Start Time is minutes:seconds.tenth seconds. See cell A4 for date:hour:minute
- Duration is sample width, nominally 10 s, but startup and occasional other noise may fragment the duration (see Description column)
- Max Time is the one-tenth second slice of a sample where the maximum sample is seen. This value is not significant here.
- Max is the value at the Max Time sample time. It is some measure of jitter seen, but otherwise not used.
- Average is the average of one-half second slices. This value is used.
- Min Time and Min are minimum slices analogous to Max Time and Max.
- Description indicates the meter's sample type. We disregard any entries not shown as "Interval", which are input events rather than 10-s samples.
- Stop Time shows end of 10-ssample time. It appears also as start of next sample.

Note that only the samples in NorVin and RevVin that show an "Interval" under Description (column J) are taken into the Summary Tab. Samples with "Stable" or "Unstable" occur during Arduino relay transitions.

Output Voltage Log Tabs Format

Output tabs are named in the same way as input tabs, except substituting "Vout" for "Vin".

The next snippet is from the tab Log20130506New160_Vout of R_2_New160A.xls. It shows the Fluke 8846A recording of the Output Voltage. The meter identification upper left says 45 rather than 8846A.

	A	B	C	D	E	F	G	H	I	J	K
1	FLUKE 45	2.0 D2.0	2072006								
2											
3	Start Time	Stop Time	Elapsed Ti	Interval	Total readings	Intervals	Input Events	Session Name			
4	5/22/2013 17:06	5/22/2013 18:15	1:09:33	0:00:10	419	418	2				
5	Max Time	Max	Average	Min	Min Time	Scaling					
6	5/22/2013 18:11	201.970 mV DC	-7.9325 m\	-198.656 n	5/22/2013 18:03	(none)					
7	5/22/2013 18:04	51.296 mV AC	7.4951 mV	4.9726 mV	5/22/2013 17:09	(none)					
8											
9	To display full timestamps use Format Cells 'm/d/y hh:mm:ss.0'										
10											
11	Reading	Sample	Start Time	Duration	Max Time	Max	Average	Min Time	Min	Description	Stop Time
12	1	30.2081 mV DC	06:16.1	00:09.0	06:16.1	30.2081 mV DC	29.5032 mV DC	06:21.5	28.8665 mV DC	Interval	06:25.1
13	1	6.5963 mV AC	06:16.1	00:09.0	06:21.5	7.3710 mV AC	6.7609 mV AC	06:16.8	5.6623 mV AC	...	06:25.1
14	2	29.1751 mV DC	06:25.1	00:10.2	06:25.1	29.1751 mV DC	27.9588 mV DC	06:32.7	27.2743 mV DC	Interval	06:35.3
15	2	7.2659 mV AC	06:25.1	00:10.2	06:25.1	7.2659 mV AC	6.5378 mV AC	06:28.2	6.0389 mV AC	...	06:35.3

The columns for this log are identical to those for the Fluke 289, except for Excel column N which is just a copy of the numeric value of Average. The rows starting with Excel 12 show alternating samples labeled as mV DC and mv AC. The 8846A presents the direct current component of the amplified input (the source voltage plus any ATEC contribution) and everything else, which is probably induced noise from EMI.

Summary Tab

The first snippet from the Summary tab contains copies of some of the data from Log tabs, along with some computation, as shown below. This section is from an ATEC in normal orientation (see file R_2_F1_120). The rows from 6 to 52 generally show the temperature ramping and coming to equilibrium, which are not included in the analysis.

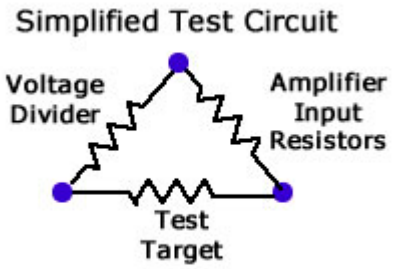
	A	B	C	D	E	F	G	H	I	J	K	L
1		Normal										
2		Input sample time (hh:mm:ss)	Voltage Source (vDC)	Output sample time (mm:ss)	Signal Out (mVDC)	Noise Out (mVAC)	Voltage Divider output (VDC)	Scaled Signal (mVDC)	Scaled Noise (mVAC)	Selected sample across Amplifier (mV)	Test Target Voltage	Test Target Current
3									0.00054434			
4												
5		17:56:16	0.1825	17:56:17	-35.667	0.2871	0.04561360	-0.03563137	0.00028681			
53		18:04:15	0.1824	18:04:17	-25.650	0.3507	0.04558860	-0.02562438	0.00035035			
54		18:04:25	0.1824	18:04:27	-25.564	0.3481	0.04558860	-0.02553846	0.00034775			
55		18:04:35	0.1824	18:04:37	-25.751	0.3519	0.04558860	-0.02572527	0.00035155			
56		18:04:45	0.1824	18:04:47	-26.062	0.3458	0.04558860	-0.02603596	0.00034545	-0.026035964	0.01955	130.1798202
57		18:04:55	0.2042	18:04:57	-28.442	0.3790	0.05103724	-0.02841359	0.00037862			
58		18:05:05	0.2055	18:05:07	-28.868	0.3256	0.05136216	-0.02883916	0.00032527			
59		18:05:15	0.2055	18:05:17	-28.775	0.3407	0.05136216	-0.02874625	0.00034036			
60		18:05:25	0.2055	18:05:27	-28.837	0.3286	0.05136216	-0.02880819	0.00032827			
61		18:05:35	0.2055	18:05:37	-29.023	0.3583	0.05136216	-0.02899401	0.00035794			
62		18:05:45	0.2055	18:05:47	-28.571	0.4519	0.05136216	-0.02854246	0.00045145	-0.028542458	0.02282	142.7122877
63		18:05:55	0.2393	18:05:58	-33.579	0.5287	0.05981005	-0.03354545	0.00052817			

The columns show the data and computations used to obtain the voltage across the test target:

- Input sample time (column B) and Output sample time (column D) are the time tags recorded by the Fluke meters. They were used to select synchronized data from the respective Vin and Vout tabs in this Excel file so that we are considering results for the same slices of time.
- Voltage source (column C), Signal Out (column E), and Noise Out (column F) are the measurements copied from the Vin and Vout tabs for the times corresponding to Input sample time and Output sample time. Units are volts, millivolts, and millivolts, respectively. The columns occasionally shows 'OL V', reflecting a 8846 scale shift. Such results are not used.
- Voltage divider output (column G) is voltage source scaled back by 4.001 (100 Ω/(100 Ω + 4*100 kΩ)/1000) (from Section 5.3.1.8) to convert it to millivolts delivered by the voltage divider to the test target and amplifier.
- Scaled Signal (column H) is Signal Out, the signal from the amplifier to the 8846A, scaled back by the factor of 1001 created by the amplifier, so that it is unscaled voltage.
- Recorded noise (column I) in millivolts, a copy of column F to allow averaging.
- Selected sample across amplifier (column J) is manually selected by inspection of Scaled Signal, generally the last sample before the next change in voltage source.

- We need to know the voltage across the test target itself (by ATEC activity, if any, or by voltage drop across a resistor). The test jig gives us two related quantities:
  - The sweep voltage delivered from the voltage source as measured by the Fluke 289 and then scaled down by a factor of 4001 by the Voltage Divider.
  - The voltage across the amplifier (and then amplified by 1001).

Per the simplified sketch below of the test, these two with values along with the sought test target voltage must sum to zero (Kirchhoff). Note that we are interested only in DC voltages, so need not consider the various capacitors in the circuits.



Per the sketch, test target voltage (column K) computes the voltage across the test target as the difference what the amplifier sees (in mV DC) and what was delivered by the voltage divider (column G) of the selected sample across amplifier (column J) and the scaled-back voltage source from the voltage divider that is the voltage delivered to the amplifier through the amplifier input resistors.

- Test target current (column L) is the Selected sample across amplifier (column J), multiplied by 5000 to compute the current (in pico-amps) through the amplifier input resistors (see Circuit Diagram in 5.3.1.2), which have an impedance of 200.0 kΩ ± 0.4 kΩ. This factor is derived from R7 and R10 (R7 + R10 = 200k) and used to scale current through the target in picoamps, or 1 picoamp/200 k ohms = 5000 picoamps/microvolt.

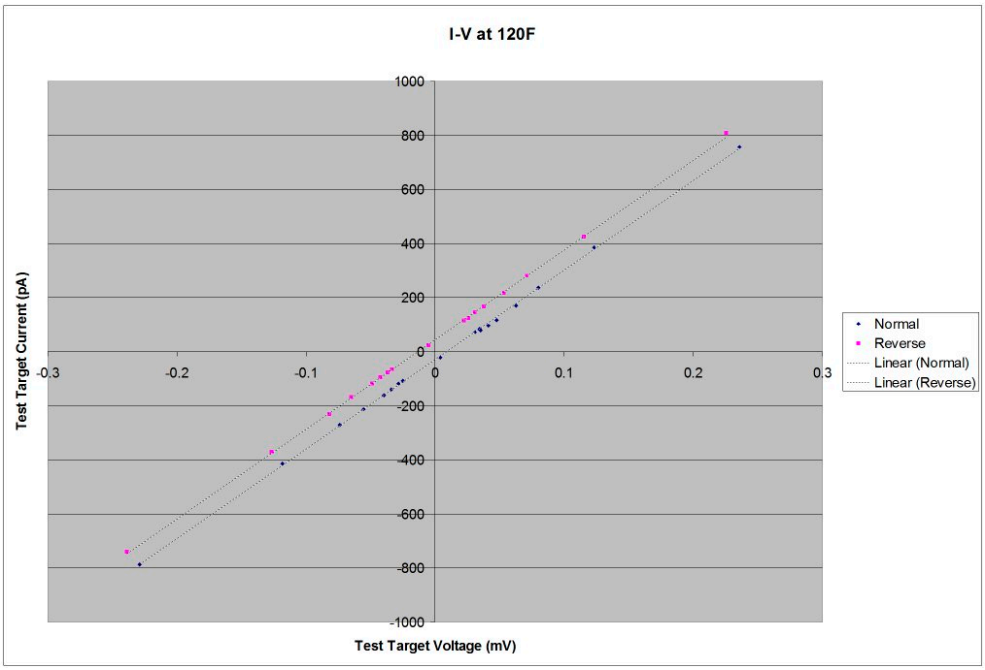
Columns U, V, and W similarly develop the results for the reverse orientation.

Summary Tab Plots

The Summary tab contains a block of 17 rows (5 through 23) in columns AW to AZ which are of copies of the non-zero Measured mV across amplifier and test target data (columns K and L, the derivation of which are shown above). Below is a plot of voltage source against resulting current through the test target in this case at 120 °F from R_2_New120B.xls:

- Test Target current (column AW) against Test Target Voltage (column AX) for Normal orientation
- Test Target current (column AY) against Test Target Voltage (column AZ) for Reverse Orientation.

The plots show the least squares fit line for each orientation.



The tab also contains a block of numbers in columns AW to BA, rows 2 and 3 which are derived from the 17 rows below them and are used in turn to derive the average resistance and average current from measurements at the test temperature:

- AU:2 is the slope of the least squares fit line of normal orientation through a voltage source sweep, which has dimensions of amps/volts.
- AV:2 is the inverse of AU:2, or volts/amps, scaled into ohms, which is the effective resistance of the test target in the forward direction.
- AW:2 is like AU:2, but for the reverse orientation
- AX:2 is line AV:2, but for the reverse orientation.
- AU:3 and AV:3 are y-intercepts of the least square fit lines for normal and reverse orientations, respectively.
- AY:2 is the average resistance, for both directions, for the test target
- AY:3 is half the average distance between the y-intercepts (in picoamps) for normal and reverse orientations, respectively, representing the average net flow generated by the test target.
- AY:4 is the product of AY:2 (resistance in ohms) and AY:3 (current in picoamps), then scaled down by 1,000,000 to average microvolts generated by the test target for this temperature.

AU	AV	AW	AX	AY	AZ
Normal		**Reverse**			
3308.019551	302295.6741	3320.789249	301133.2322	301714.4531	ohms
-29.83593893		43.81900298		-36.82747096	pA
From col. K	From col. L	From col. V	From col. W	-11.11138026	uV
-0.229059893	-787.7172827	-0.238568365	-740.04995		
-0.118273426	-412.6318681	-0.126507093	-371.4635365		
-0.073830489	-270.3126873	-0.08182929	-230.3186813		
-0.05538411	-213.7067932	-0.064648227	-167.2612388		

The values in BA are carried over into a later summary for a target across all temperatures.

Summary Tab Zero Input Point

One more piece of data from these runs that turn out to be significant. The sweeps were actually run substantially out of order: voltages are swept from low to high in one polarity, low to high with the reverse polarity, and the test at zero forcing volts was run last rather than in the middle of the

sweep. This was done to expose any hysteresis effects. The zero voltage was achieved by unplugging the Arduino AC supply and rectifier from its wall plug along with removing the batteries from the Voltage Source. Below are snippets of raw data from one of the runs (this one at 150 °F) around the time of setting the zero voltage (with just sample number, start time, and average values shown). The left hand table shows the forcing voltage as recorded by the Fluke 289, and the right hand table shows what the Fluke 8846A recorded (DC and AC). Note that the Reading column is left in only for reference; for synchronization, look at Start Time.

Reading	Start Time	Average
245	06:11.4	0.2060 V DC
246	06:21.1	0.2060 V DC
247	06:31.4	0.1880 V DC
248	06:41.1	0.0003 V DC
249	06:51.3	0.0001 V DC
250	07:01.5	0.0001 V DC
251	07:11.2	0.0001 V DC
252	07:21.4	0.0001 V DC
253	07:31.1	0.0000 V DC
254	07:41.3	0.0000 V DC

Reading	Start Time	Average
245	06:22.5	-22.6394 mV DC
245	06:22.5	13.5498 mV AC
246	06:32.2	-21.3032 mV DC
246	06:32.2	15.1272 mV AC
247	06:42.3	-5.6583 mV DC
247	06:42.3	13.5454 mV AC
248	06:52.5	2.7156 mV DC
248	06:52.5	6.6091 mV AC
249	07:02.2	2.6891 mV DC
249	07:02.2	7.1037 mV AC
250	07:12.4	2.6331 mV DC
250	07:12.4	6.8619 mV AC
251	07:22.1	2.3196 mV DC
251	07:22.1	7.3343 mV AC
252	07:32.4	2.5511 mV DC
252	07:32.4	7.9380 mV AC
253	07:42.1	2.5366 mV DC
253	07:42.1	7.1743 mV AC
254	07:52.3	2.8813 mV DC
254	07:52.3	6.9024 mV AC

What we see is that the plug on the AC supply and rectifier was pulled at around 06:30, and average voltage from the voltage source drops to near zero. From the 8846, we see that it was measuring about 14 millivolts (mV AC) beforehand, and that afterwards it was measuring just over half that much.

5.5. Tests on Test Jig

This section describes the tests employed to qualify the amplifier.

5.5.1. Amplifier

The amplifier adds its own scaling, bias, and noise to the test jig, which were measured.

Amplifier Scaling

To verify the amplifier scaling, resistors of 160 kΩ, 220 kΩ, and 330 kΩ were used as the test target and subjected to the input voltage sweep. The test results were recorded and reported for the resistor Test Targets in the same manner as described above for prototype ATECs.

	B	C	D	E	F	G	H	I	J	K	L
2	Tin	Vin	Tout	mVout (dc)	mVout (ac)	Scaled Vin (DC input)	Measured mV across Test Target		Sampled mV across Amplifier	Test Target Voltage (mV)	Test Target Current (pA)
3											
131	10:08:27 PM	0.1822	08:28.3	-25.744	18.718	0.045538615	-0.025718282				
132	10:08:37 PM	0.1822	08:38.1	-25.738	18.723	0.045538615	-0.025712288				
133	10:08:47 PM	0.1822	08:48.3	-25.674	18.747	0.045538615	-0.025648352				
134	10:08:57 PM	0.1822	08:58.0	-25.624	18.748	0.045538615	-0.025598402				
135	10:09:07 PM	0.1822	09:08.3	-25.682	18.755	0.045538615	-0.025656344		-0.025634366	0.01990	128.1718282
136	10:09:17 PM	0.1968	09:18.1	-27.113	18.771	0.049187703	-0.027085914				
137	10:09:27 PM	0.2053	09:28.4	-28.833	18.788	0.051312172	-0.028804196				
138	10:09:37 PM	0.2053	09:38.2	-28.740	18.804	0.051312172	-0.028711289				
139	10:09:47 PM	0.2053	09:48.4	-28.659	18.826	0.051312172	-0.02863037				
140	10:09:57 PM	0.2053	09:58.2	-28.701	18.846	0.051312172	-0.028672328				
141	10:10:07 PM	0.2053	10:08.4	-28.788	18.867	0.051312172	-0.028759241		-0.028687313	0.02262	143.4365634
142	10:10:17 PM	0.2283	10:18.0	-30.978	18.865	0.057060735	-0.030947053				

The above snippet from the Summary tab of R_2_Resistors140.xls shows the the title rows and the first sample data, and copied from the Log tabs. The column contents are described fully in Section 7—Test Results. Where the summary tabs for ATEC prototypes have data sets for each orientation (normal and reverse), the resistor Summary tab has sets of columns for each resistor size.

The log summaries are further summarized by resistor size and computation is made from voltage/current relation. The table below, from columns AU and AV, rows 5 to 24 of the Summary tab of the R_2_Resistorsxxx.xls files (xxx = 100, 110, 120, 130, 140, 150, or 160) are copied of the non-zero data Test Target Voltage (column K) and Test Target Current (column L) from the 160 kΩ resistor. Columns AW and AX, and columns AY and AZ are from 220 kΩ and 330 kΩ resistors, respectively.

	AU	AV	AW	AX	AY	AZ
1	160k		220k		330k	
2	6208.053	161081.1	4660.561	214566.5	3117.295	320790.9
3	2.951264		2.815189		2.239619	
4						
5	-0.17331	-1073.21	-0.20112	-934.647	-0.23909	-743.713
6	-0.09015	-556.758	-0.10463	-484.701	-0.12448	-384.835
7	-0.05755	-353.964	-0.06671	-308.312	-0.07934	-244.892
8	-0.04419	-271.295	-0.05133	-235.848	-0.06098	-187.364
9	-0.03243	-198.866	-0.03768	-172.778	-0.04477	-137.203
10	-0.0278	-169.8	-0.03224	-147.748	-0.03833	-117.138
11	-0.02373	-144.769	-0.02754	-125.965	-0.03268	-100.054
12	-0.02114	-128.888	-0.02452	-112.098	-0.02908	-89.296
13	-0.00033	1.752747	-0.00028	1.414918	-0.00017	0.970363
14	0.019904	128.1718	0.023153	112.0513	0.027564	90
15	0.01996	128.017	0.023164	111.9963	0.027599	89.7003
16	0.022625	143.4366	0.026288	125.4962	0.031363	99.74692
17	0.022649	143.5681	0.026289	125.2398	0.031369	99.9667
18	0.022703	143.2934	0.030992	147.2145	0.036958	117.1362
19	0.026691	168.4715	0.036438	172.4709	0.043427	137.2777
20	0.031386	197.4825	0.050133	235.964	0.059726	187.7473
21	0.043172	270.6444	0.065702	308.4565	0.07825	245.3413
22	0.056553	353.9527	0.103764	486.1805	0.123492	387.0396
23	0.089428	557.6091	0.200837	938.8278	0.238942	747.3027
24	0.173077	1077.256				

Row 13 of the table above shows (in the 1st, 3rd, and 5th columns) the amplified and measured voltage across the resistors at the zero imposed voltage point. The values are −0.33, −0.28, and −0.17 μV are measures of the Amplifier bias at 140 F. *For purposes of ATEC testing, the bias is essentially zero.*

For the 160 kΩ resistor, AU:2 contains the least squares fit slope of test target current (in pA) vs. test target voltage (in mV), which is 10^9/resistance. Cell AV2 makes the inversion and scaling, resulting in the computed resistance across the resistor. The value is well within the tolerance of the 160 kΩ resistor. Values of resistance are similarly developed for 220 kΩ and 330 kΩ resistors in AX:2 and AZ:2.

Amplifier and Electrical Noise

In an ideal world, the amplifier would simply multiply its DC inputs per design while filtering out its AC inputs. In reality, the amplifier has internal capacitance, inductance within connectors, and non-linear, time-dependent Op-Amps with diodes that all present opportunity for distortion of the measured DC results.

Most of the electrical noise to which prototype ATECs are subjected during testing is likely (but not confirmed) from surrounding power systems, where 60 Hz dominates.

We investigated possible distortion by the amplifier by plotting current (computed from measured voltage) vs. temperature for normal and for reverse orientation of the S2P1 ATEC.

The effect of orientation of the ATEC on the measured responses could be from:

- Noise response of the ATEC.

- Noise response from the amplifier.
- Both.

We chose to focus on the Amplifier response to noise because:

- There seems little opportunity within an ATEC to set up resonance at frequencies in the 10 Hz to 1 MHz range (carrier lifetimes are in the order of 10–7 s)
- We can isolate the amplifier from the ATEC by using the Blank (see 5.6.4) as the test target and thus get some measures of the amplifier's behavior.

Amplifier Response to Noise on Blank

The test jig was configured as shown in 5.7.3 to induce AC noise.
The test approach was to apply a high noise level to the Amplifier by:

- Putting the amplifier and the Blank in an otherwise low-noise environment which consisted of a Faraday Cage—using the oven, an ungrounded (unplugged), double-walled steel chamber - to capture any AC noise from the general environment.
- Putting a pair of copper plates around the Blank and connected to a sine wave signal generator capable of putting out a range of frequencies and voltage amplitudes.
- Driving the AC voltage across the copper plates at approximate selected levels and at frequency decades from 10 Hz to 1 MHz. Note that the signal generator uses dial (analog) settings which are not precisely reproducible.
- Providing a DC bias across the Blank to emulate the test environment used for ATECs in one and then the other direction. Note that the Blank has a very low impedance (on the order of 1 ohm). Since the amplifier input is only capacitively coupled to the Blank, there should be no effect of DC bias on the amplifier. Test values at zero and the extremes of DC input (points 0–2 in the measurements in the summary snippet shown below) verify this.
- Measuring and manually recording the applied DC bias with the Fluke 289
- Measuring and manually recording both the AC and DC components of the amplifier output with the Fluke 8846A.

The following measurements, from Injected AC Noise.xls, were recorded for zero and the same extreme DC bias used in voltage sweeps on prototype ATECs:

	A	B	C	D	E	F	G	H	I
4	Point	VDC in(V)	VAC in(V)	F(kHz)	VDC out low (mV)	VDC out high (mV)	VACout (mV)		Drive Orient
5	0	0	0		0	0.25	0.2		Positive
6	1	-11.6	0.4	1	0	0.16	0.25		Positive
7	2	10.8	0.4	1	0.05	0.2	0.26		Positive

Note that VDC output shows both a high and low reading. The 8846A showed oscillating DC outputs, with cycles for the low frequency noise of several tens of seconds, probably arising from processing lags within the Op-Amps.

Amplifier Response to Noise on ATEC

To assess the effects of moderate AC noise on an ATEC, we ran frequency sweeps on the S2P1 prototype ATEC using the otherwise same setup as was used on the Blank. Results were measured and manually recorded.

5.5.2. Voltage Source

The voltage source device used for voltage sweeps also has potential to introduce bias and noise. The leads from it to the voltage divider inside the oven are fairly long and therefore antennae for EMI. The leads also have a temperature gradient and metal-to-metal connections which may cause Seebeck effect. However, these are made inconsequential because the amplifier operates on differentials as described in Section 5.3 along with other pertinent details. For the same reason, reproducibility is not an issue.

5.6. Prototype ATEC Specifications

Below are the technical specifications and supporting notes for building the prototype ATECs used in testing. They should be sufficient to build additional ATECs for testing. Please contact ThermaWatts, LLC, at www.ThermaWatts.com for license permissions to use the ATEC technology.

5.6.1. Series 1 Prototype ATEC

GaAs substrate, n-type

Repeating pattern, repeated 10.5 times

AlGaAs, x=0.5, n-type 10^18, 25 nm

AlGaAs, x=0.5, undoped, 200 nm

AlGaAs, x=0.5, p-type 10^18, 25 nm

AlGaAs, x=0.33, p-type 10^18, 25 nm

AlGaAs, x=0.33, undoped, 200 nm

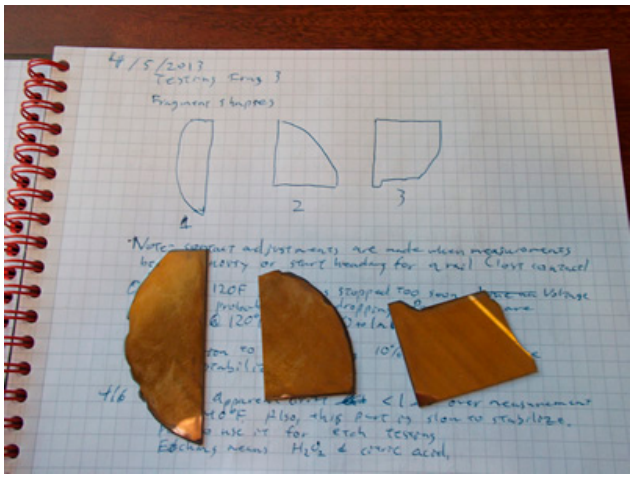
AlGaAs, x=0.33, n-type 10^18, 25 nm

Final layer doped 10^20

Fabrication was completed by depositing an n-type contact (AuGe/Ni/Au) on the back of the wafer and a p-type contact (Ti/Pt/Au) on the front of the wafer. This resulted in a complete short across the structure. Edges were mechanically removed to reduce the short circuit.

5.6.2. Fragments

Handling S1P1 during testing eventually resulted in shattering of the part. Some of the fragments of that were still large enough to be testable. The major fragments are shown below, sitting on an 8 ½ by 11 inch lab record book. Edges were processed mechanically (buffing) to remove short-circuits. We used Fragment 1 (F1) for this series of tests. It was chemically etched on 6/2/2013, and logs for subsequent test log files are named F1A.



5.6.3. Series 2 Prototype ATECs

After initial testing of the Series 1 part, a pair of additional parts were fabricated. These parts were intended to include lessons learned from Series 1. Contacts were deposited using a different process, including masking the edges of the structure to prevent shorts. Masking was not wholly effective for S1P2.

Specifications for "S2P1":

GaAs substrate, n-type

Repeating pattern, repeated 10 times:

AlGaAs, x = 0.5, undoped, 250 nm

AlGaAs, x = 0.33, p-type 10^17, 25 nm

AlGaAs, x = 0.33, undoped, 200 nm

AlGaAs, x = 0.33, n-type 10^17, 25 nm

Final layer doped 5*10^18

Fabrication was completed by depositing an n-type contact (AuGe/Ni/Au) on both sides of the wafer. A metal ring was used to keep the contact from overlapping the edge of the structure. This left a clearance of 1–3 mm between the edge of the contact and the edge of the structure. The heavily doped top layer was removed around the perimeter of the contact with a combination of 3% Hydrogen Peroxide and dilute Citric Acid. The surface was then treated with 3% Hydrogen Peroxide to leave a thin layer (less than 10 nm) of Gallium Oxide as an insulator.

Specifications for S1P2

One of the Series Two ATECs was made to match the structure specification of the Series One prototype ATEC, and hence is called "S1P2".

GaAs substrate, n-type

AlGaAs, x = 0.5, n-type 10^18, 25 nm

AlGaAs, x = 0.5, undoped, 200 nm

AlGaAs, x = 0.5, p-type 10^18, 25 nm

AlGaAs, x = 0.33, p-type 10^18, 25 nm

AlGaAs, x = 0.33, undoped, 200 nm

AlGaAs, x = 0.33, n-type 10^18, 25 nm

Final layer doped 10^20

Notes on Series 2 Prototypes

The contact layer on the ATEC structure side was supposed to be centered such that it did not overlap and short out onto the substrate. This layer was not laid down correctly. Trenches were cut across the structure side to a depth of roughly 50 microns in order to isolate the edges. Wafer was then treated with 3% Hydrogen Peroxide and dilute Citric Acid in an attempt to duplicate the results on "S2P1". Observation during treatment and subsequent testing indicate that treatment was not as effective as on "S2P1". Significant Oxygen bubble formation occurred along the edges of the trenches, possibly due to exposed Platinum. Key problems are the path length from contact to substrate (5.5 μm vs. 1 mm) and the difficulty in getting sufficient quantity of Hydrogen Peroxide to the exposed surface.

A number of lessons are indicated by the manufacturing differences between S2P1 and S1P2:

- Surface conductivity at the edge of the structure is important.
- Providing a gap between the contact and the edges improves performance.

- A properly planned process for construction is required.

5.6.4. Blank

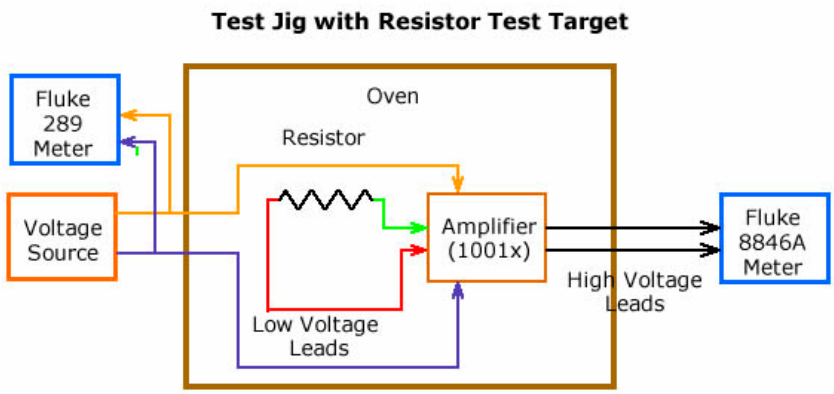
We put contact layers on a GaAs substrate, n-type, without the ATEC structure, to use for baseline testing of the test jig. It proved to be of too low an impedance to be useful when testing with the amplifier. However, it proved useful in noise testing as described in 5.5.1.3.

5.7. Specific Configurations

5.7.1. Voltage Sweep on Resistor

Components used:

- Test Stand
- Amplifier
- Arduino as voltage source
- Resistor connected to contacts

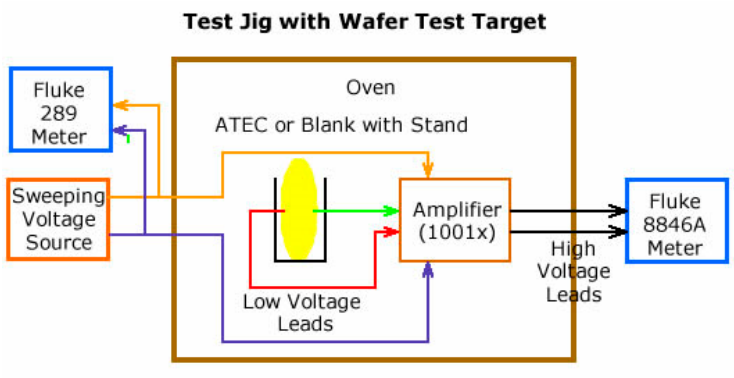


5.7.2. Voltage Sweep on Wafer

Components used:

- Test Stand

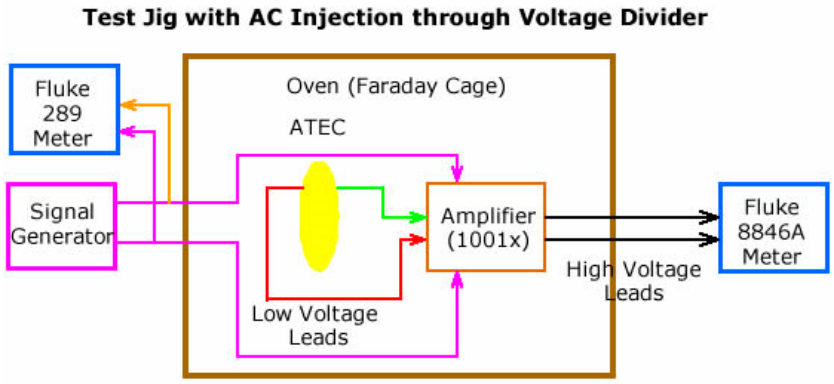
- Amplifier
- Arduino and battery as voltage source
- Wafer mounted between contacts



5.7.3. Injected Noise through Divider

Components used:

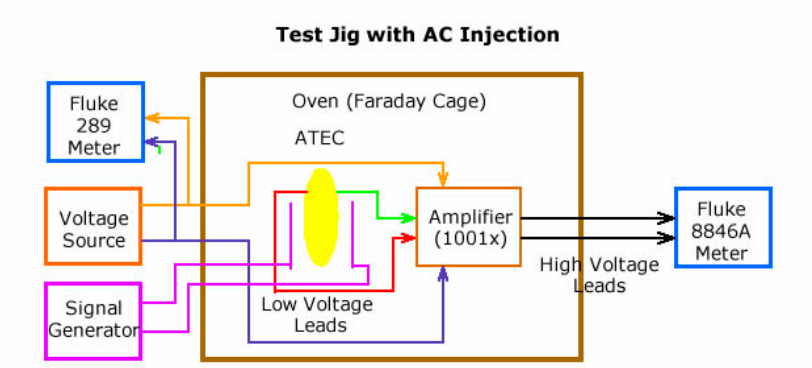
- Test Stand
- Amplifier
- Signal generator as voltage source
- Wafer mounted between contacts



5.7.4. Induced Noise through Plates

Components used:

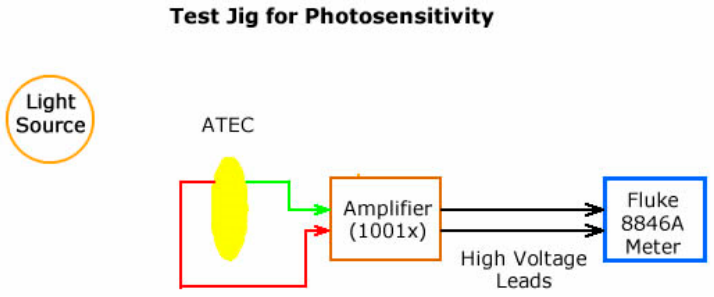
- Test Stand
- Amplifier
- No voltage source
- Wafer mounted between contacts
- Copper plates on either side of wafer
- Signal generator connected directly to copper plates



5.7.5. Photosensitivity

Components used:

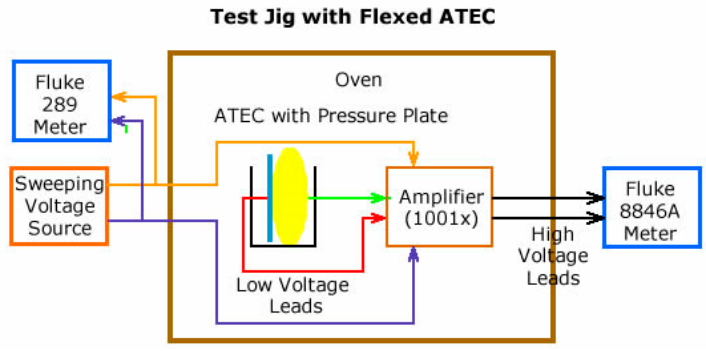
- Test Stand
- Amplifier
- No voltage source
- Wafer mounted between contacts
- Oven open to local lighting



5.7.6. Mechanical Flexing

Components used:

- Test Stand
- Amplifier
- Arduino as voltage source
- Wafer mounted between contacts
- Copper plate on substrate side of wafer, between wafer and contact



5.7.7. Wide Range Voltage Sweeps

Components used:

- Test Stand
- Arduino as voltage source
- Voltage Divider not used
- Amplifier not used

5.8. Test Log Files

Below is the list of files of collected or derived data from ATEC testing. These Excel files Thermawatts.com/TestLogs/.

File Name	Notes
Induced AC noise	tabs with frequency sweeps on Blank, S2P1 @ 3v, http://thermawatts.com/TestSeries2/Files/S2P1 @ 1v, and Fragment 1
R_2_F1_120	IV for Fragment 1 @ 120 °F
R_2_F1_140	IV for Fragment 1 @ 140 °F
R_2_F1_160	IV for Fragment 1 @ 160 °F
R_2_F1A_120	IV for Fragment 1 @ 120 °F after it was etched
R_2_F1A_140	IV for Fragment 1 @ 140 °F after it was etched
R_2_F1A_160	IV for Fragment 1 @ 160 °F after it was etched
R_2_F1A_72	IV for Fragment 1 @ 72 °F after it was etched
R_2_F1A_73	IV for Fragment 1 @ 73 °F after it was etched
R_2_F1_Summary	Summary of F1 and F1A for several temperatures.
R_2_New_073	IV for S2P1 @ ambient
R_2_New081	IV for S2P1 @ 81 °F
R_2_New090	IV for S2P1 @ 90 °F
R_2_New100	IV for S2P1 @ 100 °F
R_2_New110	IV for S2P1 @ 110 °F
R_2_New110A	IV for S2P1 @ 110 °F (further runs)
R_2_New120	IV for S2P1 @ 120 °F
R_2_New120A	IV for S2P1 @ 120 °F (further runs)
R_2_New120B	IV for S2P1 @ 120 °F (further runs)
R_2_New130	IV for S2P1 @ 130 °F
R_2_New130A	IV for S2P1 @ 130 °F (further runs)
R_2_New140	IV for S2P1 @ 140 °F
R_2_New150	IV for S2P1 @ 150 °F
R_2_New160A	IV for S2P1 @ 160 °F
R_2_NewSummaryBL	Summary of S2P1 for all temperatures
R_4_New120	IV for S2P1 @ 120 °F
R_4_New160	IV for S2P1 @ 160 °F
R_2_Old_Summary	Summary of S1P2 for 120, 140, 160 F.
R_2_Old120	IV for S1P2 @ 120 °F
R_2_Old140	IV for S1P2 @ 140 °F
R_2_Old140A	IV for S1P2 @ 140 °F (further runs)
R_2_Old160	IV for S1P2 @ 160 °F
R_2_Resistors100	IV for 220 kΩ and 330 kΩ @ 100 °F
R_2_Resistors110	IV for 220 kΩ and 330 kΩ @ 110 °F
R_2_Resistors120	IV for 160 kΩ, 220 kΩ, and 330 kΩ @ 120 °F
R_2_Resistors120_low	IV for 2.2 kΩ and 3.3 kΩ @ 120 °F
R_2_Resistors130	IV for 220 kΩ and 330 kΩ @ 130 °F
R_2_Resistors140	IV for 160 kΩ, 220 kΩ and 330 kΩ @ 140 °F

R_2_Resistors140_low	IV for 2.2 kΩ and 3.3 kΩ @ 140 °F
R_2_Resistors150	IV for 220 kΩ and 330 kΩ @ 150 °F
R_2_Resistors160_low	IV for 2.2 kΩ and 3.3 kΩ @ 160 °F
R_2_Resistors160A	IV for 220 kΩ and 330 kΩ @ 160 °F
R_2_ResSummaryA	Summary of all resistor runs
R_3_Blank_120	IV for Blank @ 120 °F
R_3_Blank_160	IV for Blank @ 160 °F
R_3_New120	IV for S2P1 @ 120 °F
R_3_NewB_120	IV for S2P1 @ 120 °F
R2_AC_New72	IV for AC against S2P1 @ ambient
R2_AC_New120	IV for AC against S2P1 @ 120 °F
R_2_New120Sweep	IV for S2P1 @ 120 °F with noise (AC) vs. current
R_3_New120Sweep	IV for S2P1 @ 120 °F with noise (AC) vs. current
RB3_OldAmb_20131003	Impressive, but not reproducible.
R_3_Old8081_20131023	S1P2 with static mechanical stressing
R_Wide_NewAmb.xls	IV for wide sweep voltage on S2P2, testing Ideality
R_Wide_OldAmb.xls	IV for wide sweep voltage on S2P1, testing Ideality

Section 6. Recommendations for Next Steps

6.1. Recommendations

This paper has presented the ATEC, a semiconductor structure that we believe will produce a useable voltage. The theory behind it is based on well-developed technologies and the test results presented here offer a proof of the concept.

We see two stages for further work on the ATEC:

- A higher level proof of concept, using the AlGaAs and better material sets
- Further development into practical products

The subsections below outline recommended steps for the first stage.

6.2. AlGaAs Material Set

The conclusions drawn from the tests reported here need to be confirmed or overturned by independent testing.

- Run tests on AlGaAs prototype ATECs similar to the specifications of Section 5, using better measurement techniques and environmental controls. It would be good science if the experimenter were to run the tests as described in Section 5 before looking at the test results in Section 4.
- Explore parameters of design and construction through models and prototypes, such as:
    - High and low carrier density layer composition and thickness
    - Doping level and thickness
    - Alternate methods for building layers
    - Alternate geometries of layers

6.3. Specific Application Requirements

It should be helpful to know what applications are most likely to be practical for ATEC technology in order to guide exploration and evaluation of higher performance material sets than AlGaAs:

- Identify broad application areas
- Identify performance, environmental and packaging requirements for the application areas

6.4. Higher Performance Material Sets

A few material sets have been explored for their potential to enable practical application of ATEC structures. Narrow band-gaps and wide separation of carrier densities for closely-related materials were the primary search criteria. PbS/PbSe and HgCdTe emerged as candidates, but there are many more possibilities which should give practical performance for specific application areas.

- Research new materials and their characteristics
- Model potential material sets
- Construct new prototypes from higher performance material sets.
- Test the new prototypes to verify practical amounts of power output.

Section 7. Glossary

AlGaAs: Aluminum Gallium Arsenide, a semiconductor material.

ambient: existing or present on all sides; encompassing; surrounding; encircling.

ATEC (Ambient Thermal Electric Converter): Truly direct conversion of heat to electricity, where the conversion system is surrounded by and is working from a single temperature environment. Contrast this with what is widely called "direct thermal electric conversion", which uses Seebeck Effect and is inherently inefficient.

ATLAS (by Silvaco): From http://www.silvaco.com/products/device_simulation/atlas.html: a device simulation framework [software] that "enables device technology engineers to simulate the electrical, optical, and thermal behavior of semiconductor devices."

blank: A null version of an ATEC consisting of a substrate and gold contact layers.

charge carriers (electrons and holes): see http://en.wikipedia.org/wiki/Charge_carrier

differential input circuit:

EMI (electromagnetic interference): disturbance such as induced voltage that affects an electrical circuit due to electromagnetic induction from an external source

Faraday cage: An enclosure formed by conducting material. Such an enclosure blocks external static and non-static electric fields, providing constant voltage on all sides of the enclosure and no current within.

I–V (current/voltage) curve: A relationship, represented as a graph, between the electric current through a device and the corresponding voltage across it.

holes: In semiconductors, regions in atoms where electrons normally reside.

Hertz, Hz: Cycles per second.

least squares fit: A mathematical process that fits a straight line to a collection of data points with a minimum of error. It is used extensively to examine the test run measurement sets of ATECs.

molecular beam epitaxy: deposition of a crystalline overlayer on a crystalline substrate in a high-vacuum environment for high purity films of semiconductor.

Mercat (Mercury Cadmium Telluride): a semiconductor material.

n-type Semiconductor: Semiconducting material to which impurity atoms have been added which cause an excess of electrons to be present, in turn creating a region that conducts electron flow and blocks holes flow.

Orientation (either Normal or Reverse): refers to the connection of a prototype ATEC with the positive terminal of the Voltage Source. Arbitrarily, Normal Orientation connects positive to the polished side (back) and Reverse connects positive to the matte finished side (front).

Op-Amp (Operational Amplifier): a high-gain electronic voltage amplifier with an input which is the difference of two measured quantities. An op-amp produces an output voltage that is typically hundreds of thousands of times larger than the voltage *difference* between its input terminals.

p-type Semiconductor: Semiconducting material to which impurity atoms have been added which cause a deficiency of electrons to be present, in turn creating a region which conducts Holes flow and blocks Electron flow.

Seebeck effect: Electric potential found in a construct of metals in a circuit as a metal-to-metal junction in the circuit is heated while the matching reverse junction is kept relatively cool.

shunt: A device allowing electrical current to pass around a point in a circuit.

substrate: The physical material upon which a semiconductor device, e.g., an integrated circuit or ThermaWatts ATEC structure, is applied.

test target: The part being tested for its electrical characteristics in the Test Jig (a prototype ATEC, resistor, diode, etc.)

ThermaWatts, LLC: A limited liability corporation registered in the State of Washington.