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Characteristics of Offset Corbino Thin Film Transistor: A Physical Model

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Abstract: Offset Corbino thin film transistor is a good candidate for high voltage thin film transistor (HVTFT) due to the uniform drain electric field distribution benefiting from the circular structure. The physical model of offset Corbino thin film transistor characteristics has yet to be clarified. In this study, Equations are derived to describe the current–voltage relations of Corbino TFT with offset at the drain or source sides. The influence of offset position and parameters on the saturation voltage and the saturation current was described quantitatively. Three-dimensional Computer-Aided Design simulation and experiment results verify the theoretical physical model. Our physical model provides design rules for high voltage offset Corbino TFT when considering the voltage tolerance and saturation current balance.

Keywords: thin film transistor; Corbino; drain offset; high voltage; model

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1. Introduction

High voltage thin film transistors (HVTFT) have applications as driving components for field-emission display [1], dielectric elastomer actuators (DEA) [2], piezoelectric actuators [3], triboelectric nanogenerators [4], etc. Two approaches have been adopted to increase the breakdown voltage (V_{BD}) of TFT. One is to use materials of wide bandgap (E_g > 3 eV) as the active layer, such as ZnO, IGZO and Ga_2O_3 [5,6]. The other is to use specific structures such as drain offset [7–9] or field-plate (FP) structure [10,11]. The drain offset structure uses the ungated channel region to undertake much of the drain voltage, which reduces the voltage on the gated channel region [12,13]. While in the field-plate structure, a plate located above the gate edge near the drain offset region is used to suppress the current collapse phenomena by restraining the gate edge electric field concentration [14–18]. Sometimes, these two approaches are used together to increase the breakdown voltage of TFT [19,20].

Many researchers have reported HVTFT based on conventional TFT with rectangular channels [21–26]. Martin, et al., fabricated high-voltage amorphous silicon TFT with a drain offset structure, operating at over 400 V [22]. Unagami, et al., reported high-voltage TFT fabricated in recrystallized polycrystalline silicon with a breakdown voltage above 100 V at an offset drain length of 20 µm [23]. Yu, et al., used amorphous InGaZnO (a-IGZO) as the active layer and high-k Al_2O_3 as the gate dielectric layer to fabricate HVTFT, which demonstrated a gate breakdown voltage (V_{BD_G}) of 45–50 V and a source-drain channel breakdown voltage (V_{BD_SD}) exceeding 100 V [24]. Chow, et al., fabricated rectangular a-Si HVTFT to operate voltage above 300 V with an offset of 6 µm [25]. Li, et al., reported a-IGZO HVTFT with a high breakdown voltage of over 1.1 kV [26] and over 1.9 kV [27]. The results in the literature show that breakdown voltage can be improved if the drain offset structure is used. Although the drain offset structure can improve the breakdown voltage, it may reduce the operating current and occupy a larger area. The saturation

currents of rectangular TFTs with offset at the drain side are approximately the same, and at the source side decrease with offset length [12,21].

Corbino TFT is a circular TFT consisting of inner and outer concentric ring electrodes, superior to the rectangular-shaped TFT in some properties. Due to the uniform electric field distribution in the channel region, Corbino TFT can potentially work at higher drain bias [28,29] and achieve better mechanical bending stability [30,31]. In addition, the output resistance of Corbino TFT behaves almost infinitely beyond pinch-off with the outer-ring electrode as drain [32–34]. Mativenga, et al., showed that Corbino TFT could provide bending direction independence and achieve better stability under mechanical bending strain than rectangular-shaped TFTs [30]. Huo, et al., reported the fabrication of flexible and transparent IGZO Corbino TFT on muscovite mica substrates, which can keep electrical performances stable when exposed to tensile bending cycles up to 10,000 times [31]. Mativenga, et al., first reported a-IGZO Corbino TFT with almost infinite output resistance beyond pinch-off. They attributed this advantage to the nearly unchanged channel width to channel length ratio in Corbino TFT when the outer-ring electrode is the drain electrode [32]. Due to the high output resistance, Joo, et al., fabricated the high-gain complementary logic inverter composed of Corbino p-type SnO and n-type IGZO TFTs [33], and Geng, et al., reported a high-performance active image sensor pixel design by utilizing a-IGZO Corbino TFTs [34]. Furthermore, the concentric electrodes of Corbino TFT can be easily achieved using inkjet printing, taking advantage of the coffee ring effect [35,36].

In contrast, research about high-voltage Corbino thin film transistors is limited [28,29]. Hong, et al., demonstrated magnesium zinc oxide (MZO) based Corbino HVTFT [28] and ZnO-based flexible Corbino HVTFT [29], which show a blocking voltage of 609 V and 150 V, respectively. As for the physical model of offset Corbino thin film transistor, Huo, et al., [19] gave a simplified expression of saturation voltage and saturation current for Corbino TFT with offset at the drain side. In contrast, the detailed theoretical analysis was not given, and the model of Corbino TFT with offset at the source side was not mentioned. The physical model of offset Corbino thin film transistor characteristics has not been clarified before. Obviously, the length and the position of offset play an essential role in the transfer characteristic and output characteristic of Corbino TFT, but the exact mechanism of how to offset influences the electrical characteristics, including the saturation current of Corbino TFT, has yet to be reported.

In this study, we put forward a physical model of offset Corbino TFT according to the basic resistance formula and electric potential analysis. The mathematical expression of current-voltage relations in offset Corbino TFT was derived. Both simulation and experiment are carried out to verify the model.

2. Device Structure of Model

According to the position of the offset region to the drain electrode, offset Corbino TFT can be classified into Drain-Offset Corbino TFT and Source-Offset Corbino TFT, in which the offset locates at the drain side and source side, respectively. The electrical characteristics of Corbino TFT vary when choosing the inner or outer ring electrode as the drain. Therefore, Drain-Offset Corbino TFT can be further divided into Source-Gate-Offset-Drain TFT (SGOD TFT) and Drain-Offset-Gate-Source TFT (DOGS TFT). Source-Offset Corbino TFT can be further divided into Drain-Gate-Offset-Source TFT (DGOS TFT) and Source-Offset-Gate-Drain TFT (SOGD TFT). The three-dimensional cross-sectional structures and top views of the four types of offset Corbino TFT are shown in Figure 1a–d. The inner and outer radiuses of the gated channel are denoted as R_{cir} and R_{cor}, and the inner and outer radiuses of the offset region are denoted as R_{oir} and R_{oor}. Due to the coupling of the gated channel region and offset region in offset Corbino TFT, $R_{cir} = R_{oor}$ can be found in Figure 1a,c, and $R_{oir} = R_{cor}$ can be found in Figure 1b,d. In addition, we label the length of the gated channel region and offset region as $L_{channel}$ (R_{cor}–R_{cir}) and L_{offset} (R_{oor}–R_{oir}). Although SGOD TFTs and DOGS TFTs (also for DGOS TFTs and SOGD TFTs) have the same $L_{channel}$ and L_{offset}, their gated channel and offset region differ due to the rotation symmetry of Corbino TFTs,

as shown in the top views. In addition, the direction of the drain current is also different for SGOD TFTs and DOGS TFTs. The charge carriers are injected from the outer electrode to the inner electrode in SGOD TFTs but from the inner electrode to the outer electrode in DOGS TFTs.

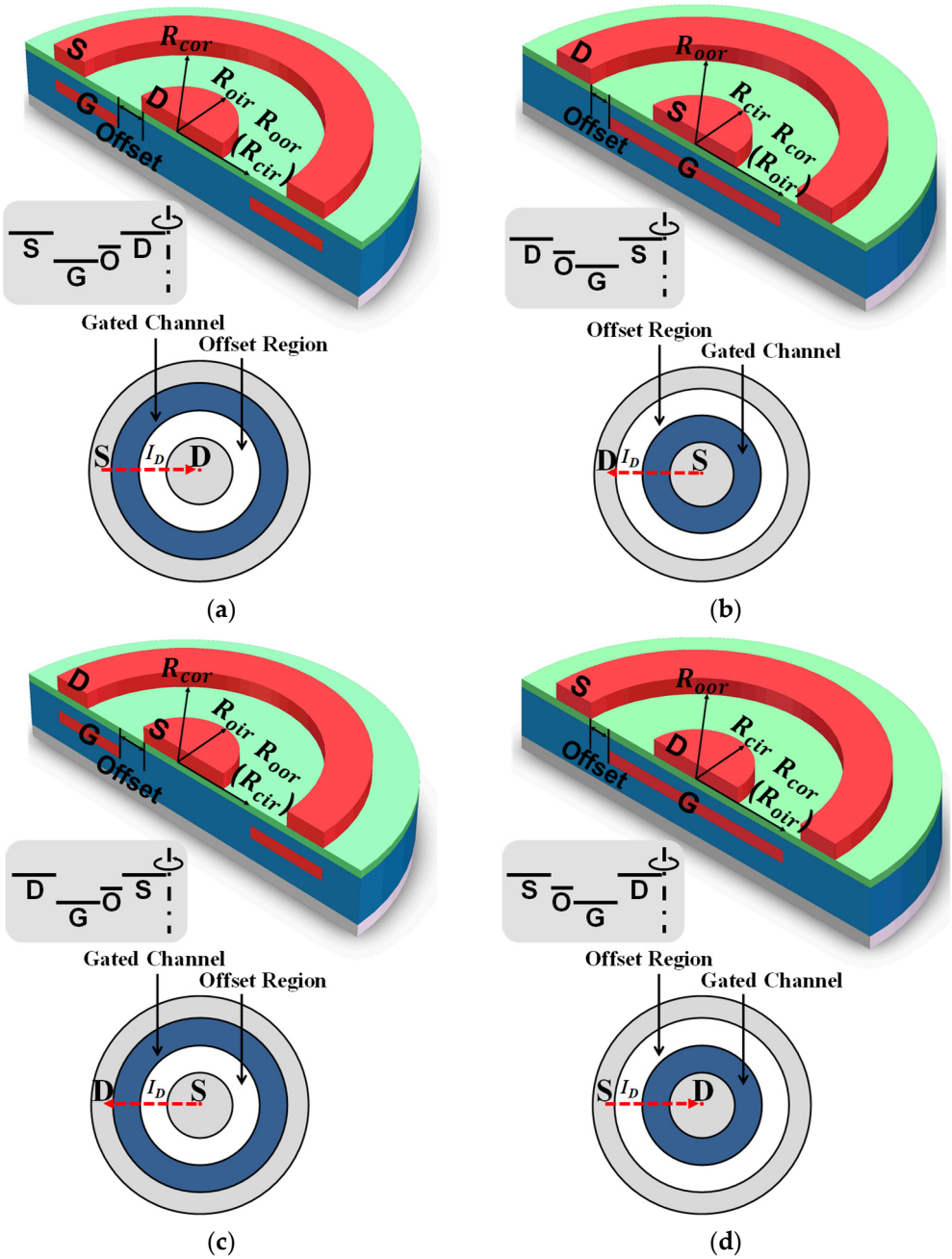


Figure 1. The three-dimensional cross-sectional structures and top views of offset Corbino TFTs. (**a**) SGOD TFT. (**b**) DOGS TFT. (**c**) DGOS TFT. (**d**) SOGD TFT. Insets of (**a**–**d**) are the corresponding schematic of offset Corbino TFTs.

3. Results and Discussion

3.1. Formula

According to the gradual channel approximation, we can derive Equation (1) to describe the drain current of TFTs [37]:

$$I_D = \begin{cases} \frac{W}{L}\mu_1 C_i\left(V_G - V_{th} - \frac{V_D}{2}\right)V_D; \\ \frac{W}{L}\mu_1 C_i\left(V_G - V_{th} - \frac{V_1+V_S}{2}\right)(V_1 - V_S). \end{cases} \quad (1)$$

The first form of Equation (1) describes the drain current of TFTs without offset, and the second form of Equation (1) is the general Equation to describe the current of gated channel applicable for all offset TFTs (rectangular and Corbino structure). Here, I_D is the drain current, W and L refer to the width and length of the gated semiconductor, μ_1 is the carrier mobility in the gated semiconductors, $C_i = \varepsilon_{ox}/t_{ox}$ with ε_{ox} as permittivity and t_{ox} as the thickness of the insulating layer below or above the gated semiconductor, and V_G and V_{th} refer to the gate voltage and threshold voltage. The threshold voltage is the gate voltage axis intercept of the linear extrapolation of the transfer characteristics at its maximum first derivative (slope) point [38]. V_D is the drain voltage, V_1 is the potential at the end of gated semiconductors, and V_S is the source potential as transistors with organic or low-dimensional semiconductors usually have injection barriers, unlike MOSFETs. Therefore, the values of V_1 and V_S depend on the specific structure of FETs with non-trivial gates. In addition, we derived the following Equation to describe the current of the offset region, calculated as the area of non-gated semiconductor times the current density [37]: $I_D = Q_0 S\mu_2(V_D - V_0 - V_1)^\alpha/d^\beta$. Here, Q_0 is the charge density factor, and μ_2 is the carrier mobility in the non-gated semiconductors. S and d are the current area and length of the non-gated semiconductor. V_0 is the onset voltage for the non-gated channel (due to injection barriers or trap states). The injection barriers or trap states are related to the material of the active layer and metal electrode. Therefore, V_0 is mainly related to material properties and film quality rather than transistor bias. Here, V_0 is omitted for simplicity and could be included by replacing V_D with V_D–V_0 whenever needed. α is referred to as the charge transport factor and $\beta \approx 2\alpha - 1$. The current density of the offset region is the product of Q_0 and $\mu_2(V_D - V_0 - V_1)^\alpha/d^\beta$. Reference [35] shows our detailed analysis of Q_0, α and β according to different conduction mechanisms, including Ohmic, SCLC, and other cases. According to the continuity principle, the current of the gated channel is equal to that of the offset region, so we have

$$I_D = \frac{W}{L}\mu_1 C_i\left(V_G - V_{th} - \frac{V_1 + V_S}{2}\right)(V_1 - V_S) = Q_0 S\mu_2\frac{(V_D - V_0 - V_1)^\alpha}{d^\beta}. \quad (2)$$

Here we consider the non-gated semiconductor with low resistance in the offset region. Thus, we assume that the carriers in the non-gated semiconductor of offset Corbino TFT obey Ohm's law. In this case, the value of α is 1, $\beta \approx 2\alpha - 1 = 1$, and $Q_0 = n_0 q$ with n_0 as the intrinsic carrier concentration and q as the elementary charge. From this perspective, we can derive the physical model of Drain-Offset Corbino TFT and Source-Offset Corbino TFT by analyzing Vs and V_1 in the corresponding situation.

The cross-section image of Drain-Offset Corbino TFT and Source-Offset Corbino TFT are shown in Figure 2a,b. For either cross-section image structures, we can choose the drain pole or the source pole to rotate the circle's center to obtain two types of offset Corbino TFT.

Drain-Offset Corbino TFT could be equivalent to the series of traditional TFT and offset resistance, as shown in Figure 2c. We define R_{offset} as the non-gated offset region resistance, and the source serves as the reference point of the potential and is grounded instead of biased. We assume the contact in thin film-based transistors between the electrode and active layer is ohmic contact, and thus V_S is set as zero. Thus, we approximate $V_1 + V_S$ and $V_1 - V_S$ to V_1 and obtain $V_1 = V_D - I_D R_{offset}$. By considering a radial electric field in Corbino TFT, the width-to-length ratio of Corbino TFT without offset can be written as

$2\pi/\ln(R_2/R_1)$ according to previous work [39], where R_2 and R_1 refer to the radius of the outer electrode and inner electrode. For Corbino offset resistance, we have:

$$R_{offset} = \frac{L_{offset}}{\sigma S} = \frac{L_{offset}}{q\mu_2 n_0 W_{offset} t} = \frac{\ln(R_{oor}/R_{oir})}{2\pi q\mu_2 n_0 t}. \quad (3)$$

Here, σ is electrical conductivity, and W_{offset} and t are the width and thickness of the offset semiconductor. It is worth noting that there are no geometric concepts of length and width in Corbino TFT with offset structure. Equation (3) considers that the geometrical factor of rectangular resistance is L_{offset}/W_{offset}, while Corbino-type offset resistance is $\ln(R_{oor}/R_{oir})/2\pi$. We know the gate voltage, V_G, could affect the carrier of the gated channel and the offset region. However, the Debye length in various semiconductors with low resistance at room temperature is in tens of nanometers. As a result, it is reasonable to ignore the effect of gate voltage when considering the resistance of the offset region of the micron scale.

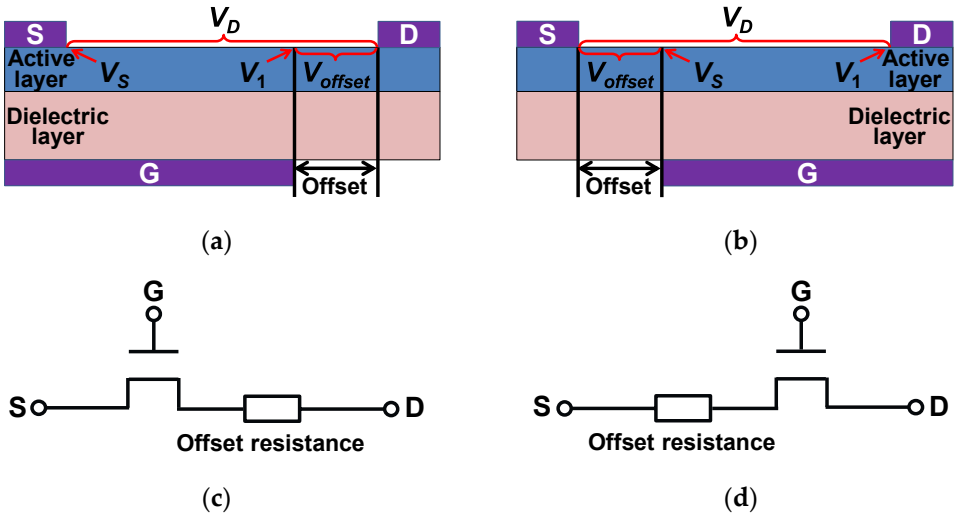


Figure 2. The cross-section image of (**a**) Drain-Offset Corbino TFT, and (**b**) Source-Offset Corbino TFT. The schematic diagram of the equivalent circuit of (**c**) Drain-Offset Corbino TFT, and (**d**) Source-Offset Corbino TFT.

According to Equations (2) and (3), we have the drain current of Drain-Offset Corbino TFT in the linear region as:

$$I_D = K_n\left[2V_{GT}\left(V_D - I_D R_{offset}\right) - \left(V_D - I_D R_{offset}\right)^2\right]. \quad (4)$$

where $V_{GT} = V_G - V_{th}$ and K_n refers to the transconductance coefficient of the device as $\pi\mu_1 C_i/\ln(R_{cor}/R_{cir})$. Equation (4) is rewritten into:

$$I_D = \left(-b + \sqrt{b^2 - 4ac}\right)/(2a) = \frac{V_D - V_{GT}}{R_{offset}} + \frac{\sqrt{\left(2K_n R_{offset} V_{GT} + 1\right)^2 - 4K_n R_{offset} V_D} - 1}{2K_n R_{offset}^2}. \quad (5)$$

where $a = R_{offset}^2$, $b = K_n^{-1} + 2V_{GT}R_{offset} - 2V_D R_{offset}$ and $c = V_D^2 - 2V_{GT}V_D$. From Equation (5), we can obtain the saturation drain current (I_{Dsat}) and saturation drain voltage (V_{Dsat}) when $\partial I_D/\partial V_D = 0$.

For TFTs in the saturation region, we denote the depletion length due to the channel length modulation effect as ΔL. The ΔL in a non-doped TFT is predicted to increase with V_D [37], similar to the classic doped MOSFETs [40]. For simplicity, we use a simple one-dimensional depletion model in doped MOSFET, i.e., $\Delta L \cong \sqrt{2\varepsilon(V_D - V_{Dsat})/qN^*}$. Here ε

is the permittivity of the active layer, and N^* is the effective dopant concentration. Unlike rectangular TFT, the position of the depletion region is significant for Corbino TFT, which is with drain near the inner or outer electrode. Therefore, we have the drain current in the saturation region in Corbino TFT with the drain at the inner electrode or outer electrode, respectively:

$$\frac{I_D}{I_{\mathrm{Dsat}}} = \begin{cases} \frac{\ln(R_{\mathrm{cor}}/R_{\mathrm{cir}})}{\ln(R_{\mathrm{cor}}/(R_{\mathrm{cir}}+\Delta L))}, & \text{For SGOD and SOGD TFT;} \\ \frac{\ln(R_{\mathrm{cor}}/R_{\mathrm{cir}})}{\ln((R_{\mathrm{cor}}-\Delta L)/R_{\mathrm{cir}})}, & \text{For DOGS and DGOS TFT.} \end{cases} \quad (6)$$

Similarly, Source-Offset Corbino TFT could be equivalent to the series of traditional TFT and offset resistance, as shown in Figure 2d. However, in the case of Source-Offset Corbino TFT, V_1 is $V_{D,}$ and V_S is $I_D R_{offset}$ in Equation (2). Therefore, we have the current-voltage (*I-V*) Equation of Source-Offset Corbino TFT in the linear region as:

$$I_D = K_n\left(2V_{GT} - V_D - I_D R_{offset}\right)\left(V_D - I_D R_{offset}\right). \quad (7)$$

From Equations (6) and (7), I_{Dsat}, V_{Dsat}, and the drain current of Source-Offset Corbino TFT in the saturation region could be obtained likewise.

We derive the current–voltage (*I-V*) Equations (listed in Table 1) of four types of offset Corbino TFT in the linear region and saturation region independent of the active layer material, from which we can derive important parameters such as the saturation drain voltage (V_{Dsat}) and the saturation drain current (I_{Dsat}). The position and length of the offset region are the key parameters influencing the electrical characteristics. Therefore, the derived equations listed in Table 1 are helpful when designing offset Corbino TFT for specific applications.

Table 1. The current-voltage equations of four types of offset Corbino TFT and other important parameters.

Drain-Offset Corbino TFT		
	SGOD TFT	DOGS TFT
V_1	$V_D - I_D R_{offset}$	
V_S	0	
I_D in the linear region	$\frac{V_D - V_{GT}}{R_{offset}} + \frac{\sqrt{\left(2K_n R_{offset} V_{GT}+1\right)^2 - 4K_n R_{offset} V_D} - 1}{2K_n R_{offset}^2}$	
I_D in the saturation region	$I_{Dsat}\frac{\ln\left(\frac{R_{cor}}{R_{cir}}\right)}{\ln\left(\frac{R_{cor}}{R_{cir}+\Delta L}\right)}$	$I_{Dsat}\frac{\ln\left(\frac{R_{cor}}{R_{cir}}\right)}{\ln\left(\frac{R_{cor}-\Delta L}{R_{cir}}\right)}$
V_{Dsat}	$K_n R_{offset} V_{GT}^2 + V_{GT}$	
I_{Dsat}	$K_n V_{GT}^2$	
Source-Offset Corbino TFT		
	DGOS TFT	SOGD TFT
V_1	V_D	
V_S	$I_D R_{offset}$	
I_D in the linear region	$\frac{V_{GT}}{R_{offset}} - \frac{\sqrt{4K_n^2 R_{offset}^2 (V_{GT}-V_D)^2 + 4K_n R_{offset} V_{GT}+1} - 1}{2K_n R_{offset}^2}$	
I_D in the saturation region	$I_{Dsat}\frac{\ln\left(\frac{R_{cor}}{R_{cir}}\right)}{\ln\left(\frac{R_{cor}-\Delta L}{R_{cir}}\right)}$	$I_{Dsat}\frac{\ln\left(\frac{R_{cor}}{R_{cir}}\right)}{\ln\left(\frac{R_{cor}}{R_{cir}+\Delta L}\right)}$
V_{Dsat}	V_{GT}	
I_{Dsat}	$\frac{V_{GT}}{R_{offset}} - \frac{\sqrt{4K_n R_{offset} V_{GT}+1} - 1}{2K_n R_{offset}^2}$	

The theoretical output characteristics of 4 types of offset Corbino TFT were drawn for different L_{offset}, and the results are shown in Figure 3. The corresponding structure parameters and other parameters used are given in Table 2. For Drain-Offset Corbino TFTs, the V_{Dsat} increases with L_{offset}. The I_{Dsat} of DOGS TFT remains unchanged independent of L_{offset}. The I_{Dsat} of SGOD TFT is larger for longer L_{offset} because of larger K_n for longer L_{offset} in SGOD TFT with the same $L_{channel}$. For Source-Offset Corbino TFT, including DGOS TFT and SOGD TFT, I_{Dsat} decreases with longer L_{offset} while V_{Dsat} remains unchanged. As shown in Figure 3, the primary influence of offset in Drain-Offset Corbino TFT is to increase the saturation voltage, and in Source-Offset Corbino TFT is to reduce the saturation current. The offset in Drain-Offset Corbino TFT undertakes a great part of drain voltage, and thus Drain-Offset Corbino TFT can operate at higher drain voltage. The SGOD TFT can endure higher potential due to a larger R_{offset} compared with DOGS TFT with the same L_{offset} and $L_{channel}$. Our derived model can also demonstrate the influence of the inherent conductivity of semiconductors (such as n_0, μ_1 and μ_2) on I_D. When the semiconductor is more conductive, the I_D of offset Corbino TFT is higher. The influence of offset on drain current shown in transfer characteristics is the same as in output characteristics, so we only show the relevant output curves in the manuscript for a concise presentation.

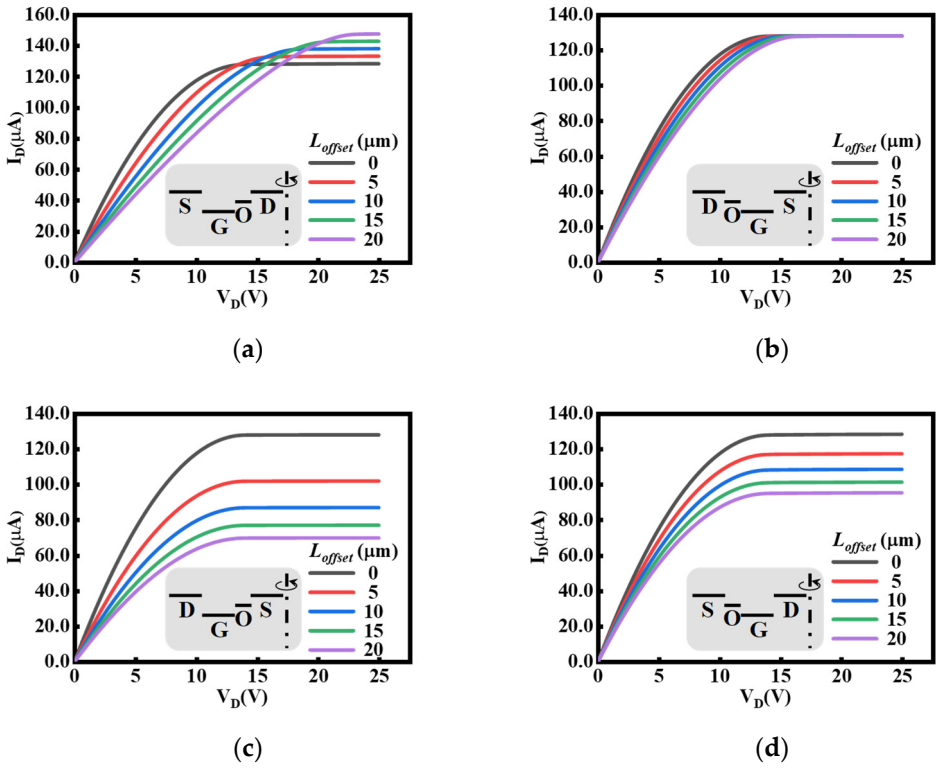


Figure 3. The theoretical output characteristics of offset Corbino TFT when V_G is 15 V: (**a**) SGOD TFT. (**b**) DOGS TFT. (**c**) DGOS TFT. (**d**) SOGD TFT. Insets of (**a**–**d**) are the corresponding schematic of offset Corbino TFT.

The position of the offset region affects the current–voltage characteristics of offset Corbino TFT, as shown in Figure 4. With the same L_{offset} and $L_{channel}$, the I_{Dsat} of Source-Offset Corbino TFT is smaller than that of Drain-Offset Corbino TFT because the offset in Source-Offset Corbino TFT reduces the saturation current. The DGOS TFT has the lowest I_{Dsat}, and the SOGD TFT has the second lowest I_{Dsat}. In the formula of I_{Dsat} of Source-Offset Corbino TFT, the value of R_{offset} exists as a denominator. The V_{Dsat} and I_{Dsat} of SGOD TFT are greater than those of DOGS TFT on account of larger K_n and R_{offset}, which can be explained directly using the formula of V_{Dsat} and I_{Dsat} of Drain-Offset Corbino TFT shown in Table 1.

Table 2. The structure parameters and other parameters of offset Corbino TFT used for theoretical characteristics plotting.

Parameter	Value	Parameter	Value
V_{th}(V)	1.0	$n_0\left(\mathrm{cm}^{-3}\right)$	1.5×10^{17}
$\mu_1\left(\mathrm{cm}^2\mathrm{V}^{-1}\mathrm{s}^{-1}\right)$	5.0	$\mu_2\left(\mathrm{cm}^2\mathrm{V}^{-1}\mathrm{s}^{-1}\right)$	5.0
$C_i\left(\mathrm{F/cm}^2\right)$	5.0×10^{-8}	t(cm)	0.05×10^{-4}
ε(F/cm)	8.5×10^{-13}	$N^*\left(\mathrm{cm}^{-3}\right)$	1.0×10^{17}
L_{offset}(μm)	0, 5, 10, 15, 20	$L_{channel}$(μm)	175
Inner electrode radius (μm)	75		

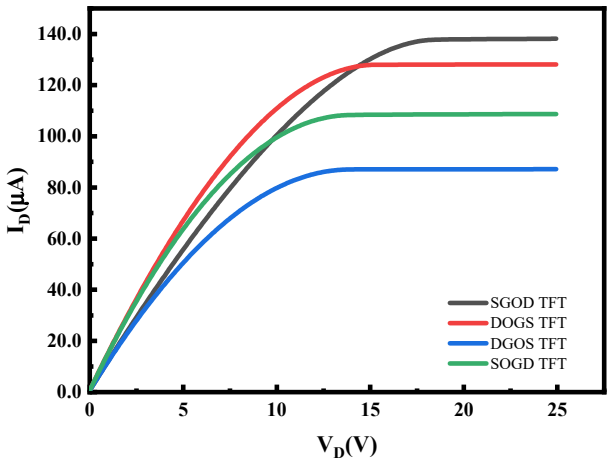


Figure 4. The theoretical output characteristics of different offset Corbino TFTs with the same L_{offset} of 10 μm and the same $L_{channel}$ of 175 μm when V_G is 15 V.

It is worth mentioning that, as shown in Figures 3 and 4, ideal Corbino TFTs have almost infinite output resistance when the outer-ring electrode is the drain, which has been reported in previous literature [32]. As for this phenomenon, the expression of I_D in the saturation region shown in Table 1 gives direct quantitative theoretical proof. Channel length modulation in the device leads to variations in the I_D of offset Corbino TFT in the saturation region. As shown in Table 1, the I_D of offset Corbino TFT in the saturation region relates to the R_{cor} and R_{cir}. In our one-dimensional depletion model, the same drain voltage increment in the saturation region results in the same ΔL. In the case of R_{cor} to R_{cir} ratio greater than one and with the same ΔL, our Equations show that I_D of Corbino TFT with the drain at the outer electrode in the saturation region increases more slowly than that of Corbino TFT with the drain at the inner electrode. The output conductance is expressed as $\partial I_D / \partial V_D$, so the Corbino TFT with the drain at the outer electrode has higher output resistance than Corbino TFT with the drain at the inner electrode.

3.2. Simulation

In order to further validate the theoretical derivation, we used the three-dimensional technology Computer-Aided Design (TCAD) by Silvaco tool to simulate the characteristics of offset Corbino TFT. The material we choose as the active layer is amorphous indium-gallium-zinc-oxide (a-IGZO). For the TCAD simulation, density of states (DOS) parameters such as conduction and valence band tail states (N_{TD} and N_{TA}), conduction and valence band tail state slopes (W_{TD} and W_{TA}), donor-like and acceptor-like states (N_{GD} and N_{GA}) with Gaussian distributions, and their respective full width at half maximums (W_{GD} and W_{GA}) are listed in Table 3. The corresponding structure parameters for simulation are the same as the theoretical characteristics plotting, as shown in Table 2.

Table 3. Silvaco TCAD simulation density of states parameters for IGZO.

Parameter	Value	Parameter	Value
$N_{TA}\left(cm^{-3}eV^{-1}\right)$	5.5×10^{18}	$N_{GA}\left(cm^{-3}eV^{-1}\right)$	1.85×10^{16}
$W_{TA}\left(eV^{-1}\right)$	0.015	$W_{GA}\left(eV^{-1}\right)$	0.3
$N_{TD}\left(cm^{-3}eV^{-1}\right)$	5.5×10^{18}	$N_{GD}\left(cm^{-3}eV^{-1}\right)$	1.225×10^{17}
$W_{TD}\left(eV^{-1}\right)$	0.22	$W_{GD}\left(eV^{-1}\right)$	0.13

TCAD simulation results also show that offset has a similar effect on Corbino TFT with theoretical results. The simulated and theoretical fitting output characteristics of 4 types of offset Corbino TFT are shown in Figure 5. The theoretical fitting parameters used different from Table 2 are V_{th} = 0 V, $C_i = 8.7 \times 10^{-9}$ F/cm^2, $n_0 = 5.0 \times 10^{16}$ cm^{-3} for the curves of L_{offset} = 2 µm in Figure 5c,d and $n_0 = 3.8 \times 10^{15}$ cm^{-3} for other fitting curves in Figure 5s and 6, μ_2 = 11 cm^{2}V^{-1}s^{-1} for Figure 6 and μ_2 = 8 cm^{2}V^{-1}s^{-1} for other fitting curves in Figure 5. Comparing Figure 5 with Figure 3, we found that the simulation results show that the characteristics of the TFT exhibit similar trends when offset length (L_{offset}) increases. Offset in Drain-Offset Corbino TFT makes no difference to I_{Dsat} with the same K_n, as shown in Figure 5b. I_{Dsat} decreases with offset length more rapidly in Source-Offset Corbino TFT, as shown in Figure 5c,d. Longer L_{offset} significantly increases V_{Dsat} in Drain-Offset Corbino TFT, as shown in Figure 5a,b. In the same way, we study the effect of the position of the offset region with the same L_{offset} and $L_{channel}$ by TCAD simulation, as shown in Figure 6. The feature and trend of V_{Dsat} and I_{Dsat} with offset in Figure 6 are consistent with Figure 4, although their exact values are different. We can conclude that the TCAD simulation results prove the correctness of the formula of offset Corbino TFT we derived.

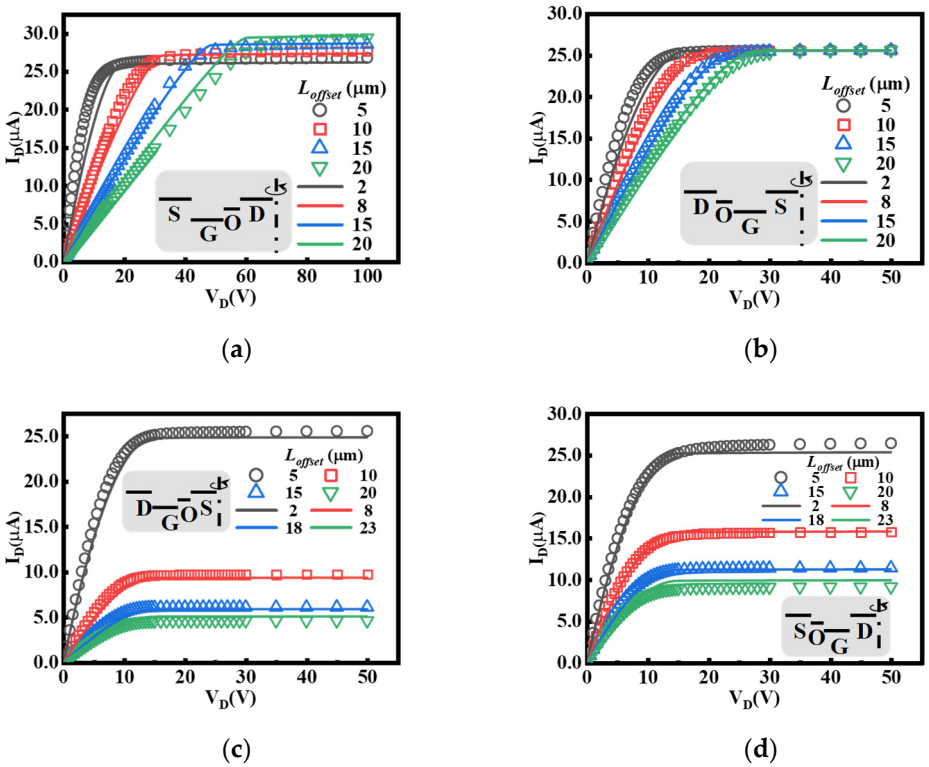


Figure 5. The simulation output characteristics of offset Corbino TFT when V_G is 15 V: (**a**) SGOD TFT. (**b**) DOGS TFT. (**c**) DGOS TFT. (**d**) SOGD TFT. Insets of (**a**–**d**) are the corresponding schematic of offset Corbino TFT. The TCAD simulated data are drawn in dots, and relevant results using the derived Equations are drawn in curves.

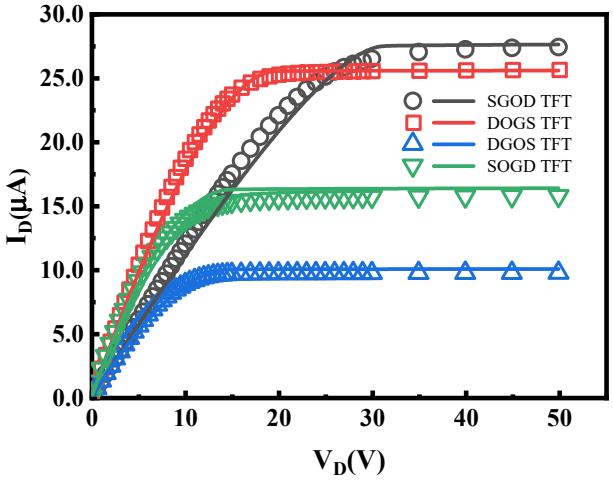


Figure 6. The simulation output characteristics of different offset Corbino TFTs with the same L_{offset} of 10 µm and the same $L_{channel}$ of 175 µm when V_G is 15 V. The TCAD simulated data are drawn in dots, and fitting results by using the derived Equations are drawn in curves.

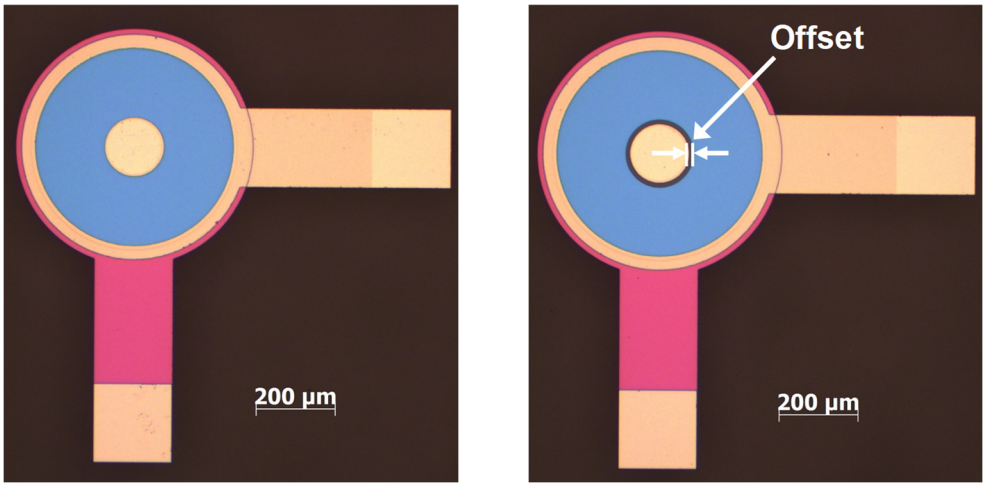
Although TCAD simulation and theoretical formula help design and predict offset Corbino TFT characteristics, the physical model's theoretical formula is more convenient and practical. First, the three-dimensional Silvaco TCAD simulation of offset Corbino TFT is time-consuming. We could not simplify the three-dimensional Corbino TFT simulation to a two-dimensional one to save software run time because it is not translational symmetrical in Corbino TFT. Even if we can simplify to two-dimensional TCAD simulation, formula calculation without calculus operation always runs faster than TCAD simulation. Secondly, TCAD simulation may encounter problems such as limiting materials and non-convergence in operation. Thus, we could employ formulas to help design device characteristics in most cases.

3.3. Experimental Verification

Apart from theoretical Equation derivation and TCAD simulation, experiment results can also add credibility to the physical model of offset Corbino TFT. We fabricated a-IGZO offset Corbino TFT to verify the physical model. The fabricated a-IGZO Corbino TFTs have a bottom-gate, inverted-staggered structure prepared on glass substrates. The circular gate electrode was a 200 nm thick Mo layer by depositing and patterning via wet etching. The gate insulator of 400 nm thick SiO_2 was deposited by plasma-enhanced chemical vapor deposition (PECVD). A 50-nm-thick IGZO film was sputtered and etched to form the active layer on top of the gate insulator. Both the source and drain electrodes were formed by sputtering and lift-off processes. A SiO_2 passivation layer was deposited by PECVD and etched by reactive ion etching (RIE) to form contact holes. We fill the contact holes with indium tin oxide (ITO) by magnetron sputtering and patterning it via a lift-off process. There are two annealing steps in device fabrication. IGZO film was annealed by thermal oxidation at 350 °C for 1 hour in N_2 atmosphere, and ITO was annealed by thermal oxidation at 470 °C for 2 hours in air atmosphere.

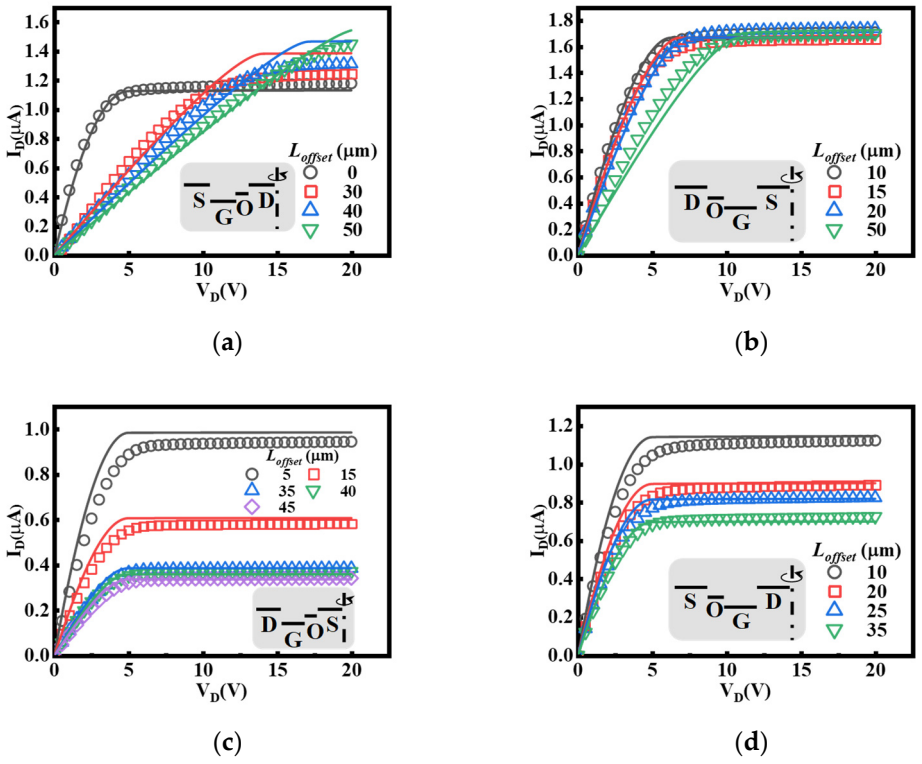
We fabricate four types of offset Corbino TFT with 15 different values of L_{offset}, i.e., 0, 5, 10, 15, 20, 25, 30, 35, 40, 45, 50, 55, 60, 75, 100 µm. The optical images of two fabricated devices are shown in Figure 7. The electrical characteristics of the a-IGZO Corbino TFT were measured using a semiconductor analyzer (Agilent B1500A). The typical experimental and theoretical fitting output characteristics of fabricated offset Corbino TFTs are shown in Figure 8. The theoretical fitting parameters different from Table 2 are $V_{th} = -1$ V, $n_0 = 3.8 \times 10^{15}$ cm^{-3}, $\mu_2 = 2.7$ cm^{2}V^{-1}s^{-1}, $C_i = 6.4 \times 10^{-9}$ F/cm^2, $\mu_1 = 2.7$ cm^{2}V^{-1}s^{-1} for Figure 8a and $\mu_1 = 4$ cm^{2}V^{-1}s^{-1} for Figures 8b–d and 9. Different positions of offset region in offset Corbino TFT with the same L_{offset} and $L_{channel}$ are also studied in the experiment.

The experimental and theoretical fitting output characteristics of different types of offset Corbino TFT with the same L_{offset} and $L_{channel}$ are shown in Figure 9.



(**a**) (**b**)

Figure 7. Optical images of fabricated a-IGZO Corbino TFTs: (**a**) without offset; and (**b**) with an offset of 10 μm.



(**a**) (**b**)

(**c**) (**d**)

Figure 8. The experimental output characteristics of offset Corbino TFT when V_G is 4 V: (**a**) SGOD TFT. (**b**) DOGS TFT. (**c**) DGOS TFT. (**d**) SOGD TFT. Insets of (**a**–**d**) are the corresponding schematic of offset Corbino TFT. The dots are experimental data, and the curves are the fitting results using the derived Equations.

For Drain-Offset Corbino TFT, the experiment results in Figure 8a,b show that the V_{Dsat} increases with the L_{offset}. SGOD TFT with longer L_{offset} has larger I_{Dsat}, and different DOGS TFT almost have the same I_{Dsat} despite different L_{offset}. Despite the slight variance in I_{Dsat}, the experimental results verify the theoretical derivation and TCAD simulation, where

different DOGS TFT have identical I_{Dsat} for different values of L_{offset}. For Source-Offset Corbino TFT, experimental TFTs with longer L_{offset} have smaller I_{Dsat}. In addition, the V_{Dsat} of experimental Source-Offset Corbino TFTs is almost the same despite different L_{offset}, as demonstrated in the formula. In Figure 9, the regulation of V_{Dsat} and I_{Dsat} with offset is the same as expected from the theoretical formula and simulation. Overall, the experiment results indicate that our physical model of offset Corbino TFT is reasonable.

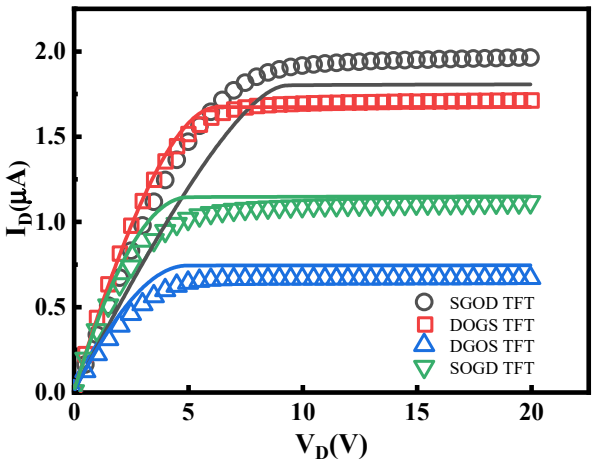


Figure 9. The experimental output characteristics of different offset Corbino TFTs with the same L_{offset} of 10 μm and the same $L_{channel}$ of 175 μm when V_G is 4 V. The dots are experimental data, and the curves are the fitting results by using the derived Equations.

4. Conclusions

According to the basic resistance formula and electric potential analysis, we derived a physical model of offset Corbino TFT, including Drain-Offset Corbino TFT and Source-Offset Corbino TFT. We explored how the offset's position and length influence the transfer and output characteristics of Corbino TFT. For Drain-Offset Corbino TFT, the saturation voltage increases with offset length, but the saturation current remains the same as long as the gated channel region is the same. When offset length increases, Source-Offset Corbino TFT has the same saturation voltage but a much smaller saturation current. TCAD simulation and experiment results verified the physical model of offset Corbino TFT. Our physical model is beneficial to device design for which the saturation voltage and saturation current must be considered. Offset Corbino TFT is a good candidate for high-voltage applications, and our model could provide guidelines for balancing voltage tolerance and the saturation current in device design.

Author Contributions: J.C. and C.L. conceived the idea and proposed the experimental scheme. J.C., C.L. and J.K initiated this study. J.C., C.L. and J.K. established the model. J.K. carried out the simulations. J.K., X.L. and H.O. carried out the experiments. J.C., C.L., S.D., J.S. and J.K. discussed and interpreted the results. J.C., C.L. and J.K. co-wrote the manuscript. All authors have read and agreed to the published version of the manuscript.

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Conflicts of Interest: The authors declare no conflict of interest.

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