energies

MDPI

Article

A New Vertical JFET Power Device for Harsh Radiation Environments

Pablo Fernández-Martínez *, David Flores, Salvador Hidalgo, Xavier Jordà, Xavier Perpiñà, David Quirion, Lucia Ré, Miguel Ullán and Miquel Vellvehí

Instituto de Microelectrónica de Barcelona, Centro Nacional de Microelectrónica (IMB-CNM, CSIC), Campus UAB, 08193 Bellaterra, Barcelona, Spain; david.flores@csic.es (D.F.); salvador.hidalgo@csic.es (S.H.); xavier.jorda@imb-cnm.csic.es (X.J.); xavier.perpinya@imb-cnm.csic.es (X.P.); david.quirion@imb-cnm.csic.es (D.Q.); lucia.re.blanco@gmail.com (L.R.); miguel.ullan@csic.es (M.U.); miquel.vellvehi@imb-cnm.csic.es (M.V.)

* Correspondence: pablo.fernandez.martinez@cern.ch; Tel.: +34-93-594-7700

Academic Editor: Alberto Castellazzi

Received: 15 December 2016; Accepted: 15 February 2017; Published: 20 February 2017

Abstract: An increasing demand for power electronic devices able to be operative in harsh radiation environments is now taking place. Specifically, in High Energy Physics experiments the required power devices are expected to withstand very high radiation levels which are normally too hard for most of the available commercial solutions. In this context, a new vertical junction field effect transistor (JFET) has been designed and fabricated at the Instituto de Microelectrónica de Barcelona, Centro Nacional de Microelectrónica (IMB-CNM, CSIC). The new silicon V-JFET devices draw upon a deep-trenched technology to achieve volume conduction and low switch-off voltage, together with a moderately high voltage capability. The first batches of V-JFET prototypes have been already fabricated at the IMB-CNM clean room, and several aspects of their design, fabrication and the outcome of their characterization are summarized and discussed in this paper. Radiation hardness of the fabricated transistors have been tested both with gamma and neutron irradiations, and the results are also included in the contribution.

Keywords: rad-hard power devices; JFET; vertical power devices; power distribution; electronics for High Energy Physics

1. Introduction

In the last years, there is an increasing demand for power devices able to tolerate very high radiation levels [1–3]. This is particularly relevant in the field of High Energy Physics (HEP) [4] experiments, where a large spectrum of power devices and systems are required to operate the particle accelerator machines and the particle detectors. In those applications, the electronics is expected to withstand extremely harsh radiation fields and, in some cases, such as the future upgrade for High-Luminosity of the Large Hadron Colider (HL-LHC) at European Organization for Nuclear Research (CERN), in Geneva (Switzerland), with an unprecedented level of radiation [5,6]. Among the large variety of power electronics applications in such a huge experiment, the sensor biasing circuitry [7] requires high voltage but not high current, since they consist of reverse biased diodes, with typical leakage currents below the order of microamperes before being irradiated [8]. Although the current demand increases to the milliampere range after irradiation, the challenging factor for the associated electronics is typically related with the voltage demand (up to 1000 V), and the performance degradation due to the high radiation level.

A careful search for suitable power switches is mandatory for reliable operation of the final application. Wide bandgap semiconductors, such as GaN or SiC, may offer good performance in some

specific cases [9]. Vertical JFET SiC devices with voltage capability up to 1700 V have been successfully fabricated and tested in harsh conditions [10,11]. Although these devices integrated on SiC substrates a better than Silicon counterparts in terms of ionization hardness due to the wider bandgap, suffer from performance degradation due to displacement damage, similar to that of Silicon devices. In this contest, solutions based on Silicon technology are still preferred, because the maturity of this technology is crucial to design and fabricate power devices that have to be fully operative and not accessible during several years, when the experiment is in operation. Besides, radiation effects in Silicon technologies have been studied for years, and the subsequent performance degradation on the electronic devices is well understood and predictable to a greater extent. Among the high voltage Silicon power devices, those based on MOS technology (Metal Oxide Semiconductor Field Effect Transistor, MOSFET, and Insulated Gate Bipolar Transistor, IGBTs) are very sensitive to ionizing radiation [12,13] although new designs are continuously produced to improve the radiation hardness [14]. Thyristors are current controlled devices with two low-doped regions (p- and n-type). Although these devices are harder in terms of ionization damage, the fast degradation of the low-doped regions because of the non-ionizing radiation [15] make not advisable their use.

In this context, the IMB-CNM has proposed a new Vertical JFET (V-JFET) transistor based on a 3D deep trenched technology [16] implemented on p-type substrates to minimize the displacement damage at high radiation fluences.

2. Device Structure

The proposed V-JFET power device has a highly adaptable design, which allows the transistor to exhibit very different performance depending on the values of the relevant geometrical parameters. The active area of the device is arranged with a large number of paralleled cells with vertical conduction. The channel is confined by a ring-shaped trench, deeply etched into the silicon substrate. As shown in Figure 1, where a schematic cross section through the center of two basic cells is depicted, the trenches are filled with highly doped polysilicon to work as the Gate electrode. A Source electrode is placed on the channel surface at the center of each cell, and then connected to the Source metal. Drain electrode is placed at the opposite face of the substrate. The trenches are all connected to the same polysilicon layer, which is then reached elsewhere by a metal pad, well isolated from the Source metal to avoid short-circuit among the electrodes.

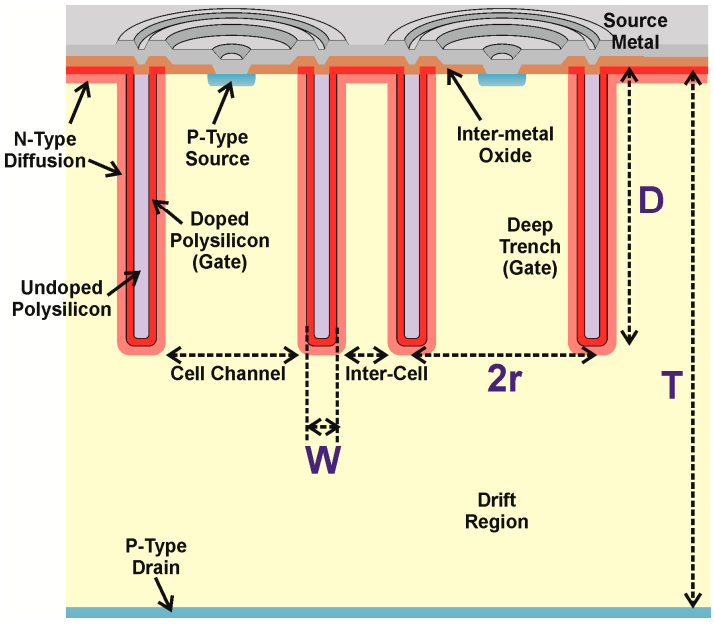

Figure 1. Schematic cross section through the center of two adjacent V-JFET cells.

In order to gain structural stability and to attain well filling and sealing of the trenches, a ring-shaped layout with a certain separation among adjacent cells was preferred. Other arrangements, missing cell-to-cell separation or even considering hexagonal cells, turned out unsuitable [17], since many of the channels collapsed and the trenches were not satisfactorily filled. In this sense, the characteristic width uniformity in the trenches of the ring-shaped layout helps to improve the filling process. In addition, a second polysilicon layer (undoped) is included to refill the trenches, thus ensuring a complete sealing. The separation between adjacent cells does not deteriorate the connection of the cells to a common Gate, since the doped polysilicon layer is not interrupted. Besides, the diffusion of the n-type dopant impurities from the polysilicon into the p-type substrate contributes to interconnect the Gates of the individual cells.

From the electrical point of view, the V-JFET is a depletion mode transistor, with channel conduction at zero Gate-to-Source bias (V_{GS}). Each cell acts as an individual JFET transistor, with vertical conduction and switching properties very close to the pentode characteristics expected for an ideal long-channel JFET [18]. Thanks to the deeply etched Gate surrounding the silicon channel, the conduction is mainly controlled by the Gate voltage and a relatively high current level can be obtained for low Drain voltages (V_{DS}), whereas for higher V_{DS} values a current saturation is observed. The proposed structure is switched-off at low V_{GS} values due to the fast depletion of the narrow channels of the individual cells. Besides, the long distance that separates the drain electrode from the bottom of the trenches, the so-called drift region in Figure 1, provides the high voltage capability of the cell, at the cost of adding a series resistance to the conduction channel. Although a single cell is not able to drive a large amount of current, the additive effect of the parallel cell arrangement hugely expands the total current handling capability.

The performance of the V-JFET transistor strongly depends on several geometrical and technological parameters. Among them, the trench depth (D), the cell radius (r), and the substrate doping concentration (N_A) have been identified as the more relevant for finding an optimum design. Other important parameters, such as the trench width (W) and the substrate thickness (T), are fixed or limited by technological constrains. Finally, the desired active area of the device (A) determines the number of basic cells connected in parallel and the resulting current handling capability of the V-JFET transistor.

The electrical performance and the process technology of the proposed transistor has been extensively simulated with the aid of Sentaurus TCAD software (Synopsys Inc., Mountain View, CA, USA), using the physical models typical from power devices. The dependence on the trench depth is illustrated in Figure 2, where the switch-off voltage (V_{OFF}) and breakdown voltage ($V_{BD|CELL}$) of an individual cell within the arrangement (a so-called "inner cell") are represented as a function of D. Deep trenches are generally preferred to obtain pentode-like characteristics. However, as D is increased, the drift region becomes shorter and $V_{BD|CELL}$ decreases. For any inner cell, the highest voltage capability is achieved at the lowest D value, when the performance approaches the triode-like characteristics [16]. Nevertheless, the strongest influence of the Drain potential in such a short-channel transistor would increase the Gate voltage required to deplete the cell, leading to a drastic increase of the V_{OFF} value. Considering a substrate thickness of T = 300 μm, the optimum D value ranges between 60 and 100 μm.

Dependences on r and N_A are more directly correlated. In general, higher current levels can be obtained for higher N_A values, although this is strongly modulated by r, since the wider is the cell channel, the higher is the current handling capability. This is in contrast with the switching performance, because low N_A and r values are required to deplete the cell channel at low voltage values. The switching versus current capability trade-off is illustrated in Figure 3, where V_{OFF} and the forward current value at saturation (I_{ON}) are represented as a function of N_A, for two different channel diameters ($2r$ = 23 and 35 μm) in a V-JFET transistor with $A = 5 \times 5$ mm^2. In this example, a convenient V_{OFF} = 3 V can be easily obtained for the $2r$ = 23 μm transistor as long as N_A is lower than 1×10^{14} at/cm^3. Still, I_{ON} will be always below 30 mA. The current level can be significantly increased

if the $2r$ = 35 µm design is considered, although for $N_A = 1 \times 10^{14}$ at/cm^3, V_{OFF} will increase up to almost 10 V. To regain the previous V_{OFF} value of 3 V, N_A should be reduced below 4×10^{13} at/cm^3, with the consequent I_{ON} reduction.

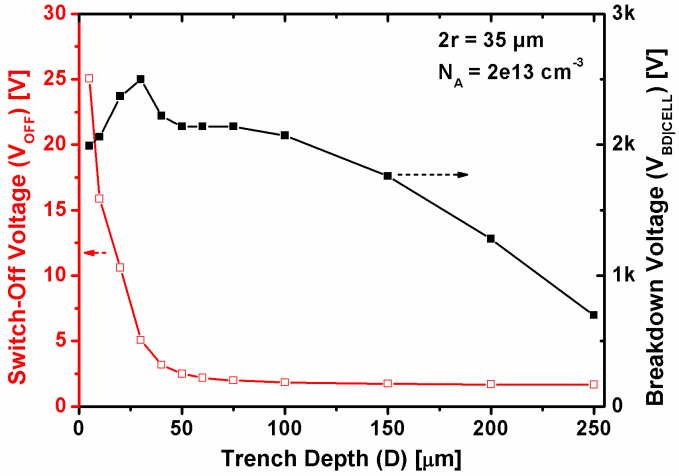

Figure 2. Simulated switch-off voltage, V_{OFF}, (**red curves**) and inner-cell breakdown voltage, $V_{BD|CELL}$, (**black curves**) as a function of the trench depth, D, for a given V-JFET cell with $2r$ = 35 µm, $N_A = 2 \times 10^{13}$ at/cm^3, and T = 300 µm.

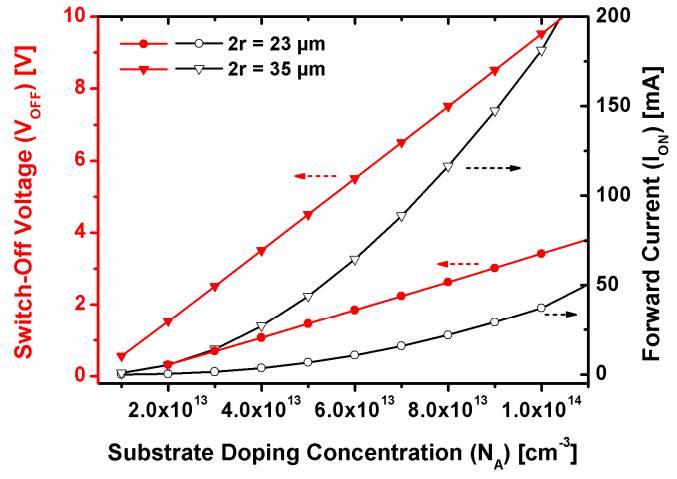

Figure 3. Simulated switch-off voltage, V_{OFF}, (**red curves**) and forward current at saturation, I_{ON}, (**black curves**) as a function of the substrate doping concentration, N_A, for a given V-JFET design with two different cell diameters ($2r$ = 23 and 35 µm), and a total active area $A = 5 \times 5$ mm^2.

V_{OFF} is the major limiting factor, since control electronics with low switching voltage is generally preferred. Hence, low r and N_A values are favored. On the other hand, the current handling capability depends also on the total number of parallel cells, i.e., on A. Therefore, if the optimum r and N_A values for attaining low V_{OFF} lead to too low I_{ON} value, a layout with broader A can be considered to achieve the desired current level. Moreover, a device optimization based on N_A is somewhat cumbersome, since working with high resistivity substrates implies low accuracy in their doping level. Higher precision could be achieved by increasing N_A, and this would also produce a remarkable increase of the current handling capability, but the voltage capability will be drastically worsened. This is illustrated in Figure 4, where $V_{BD|CELL}$ and I_{ON} have been represented as a function of N_A. It can be clearly seen that the current capability increases with the cell diameter and the substrate doping concentration. On the contrary, the cell diameter has no relevant effect on the $V_{BD|CELL}$ value, which

is basically determined by the substrate doping concentration. This is a direct consequence of the self-protection between adjacent trenches that moves the weakest point to the last cell of the device. On the whole, if for instance a final $A = 5 \times 5$ mm^2 transistor with $V_{OFF} < 3$ V, I_{ON} ranging between 10 and 100 mA, and $V_{BD|CELL} > 1000$ V is desired, N_A should range between 2 and 8×10^{13} at/cm^3, whereas the optimum cell diameter is valued between $2r = 20$ and 35 μm.

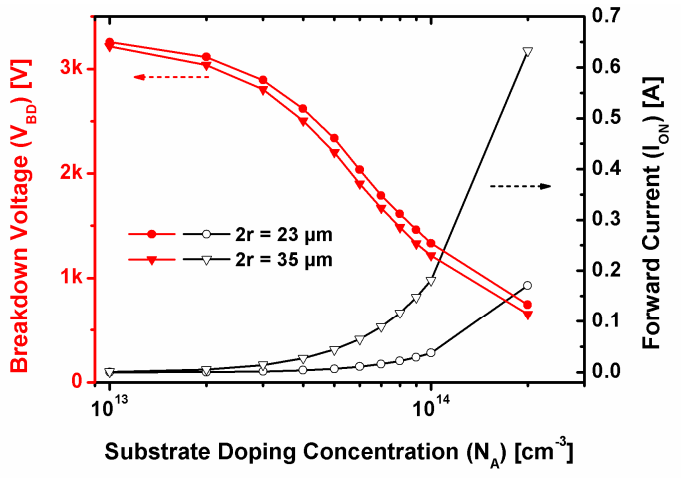

Figure 4. Simulated inner-cell breakdown voltage, $V_{BD|CELL}$, (**red curves**) and forward current at saturation, I_{ON}, (**black curves**) as a function of the substrate doping concentration, N_A, for a given V-JFET design with two different cell diameters ($2r$ = 23 and 35 μm), and a total active area $A = 5 \times 5$ mm^2.

Besides on the features of an optimized active region, the final performance of the V-JFET transistor rests on the suitability of the edge termination design. In contrast with the inner cells, the cells placed at the periphery of the active region show an asymmetric distribution of the electrostatic potential. As a result, the breakdown voltage of these outer cells is significantly lower than $V_{BD|CELL}$, unless a proper termination is implemented. The design of the edge termination region is challenging, as the maximum electric field value is located at the bottom of the trenches, typically ~100 μm far from the silicon surface. Additionally, a gate runner, consisting of a peripheral n-type diffusion connected to the Gate electrode with a maximum doping concentration in the range of 1×10^{18} cm^{-3}, has been placed around the whole active area to ensure uniform Gate bias distribution to all the cells in the layout. Gate runners are always used in the large area power devices with multi-cellular layout, also including the peripheral gate runner. This design approach has been followed in the new V-JFET structure proposed in this paper. The n-type diffusion is placed below the whole gate runner area to avoid premature breakdown as a consequence of the non-uniform cell distribution at the device periphery. Although several technologically elaborated designs are still under study, for the first fabrication batch, a planar solution with 4 floating guard rings has been chosen. This conservative approach allows the full transistor to achieve a useful voltage capability ($V_{BD|FULL}$) of several hundreds of volts, though always lower than $V_{BD|CELL}$.

3. Technological Process

The fabrication of the V-JFET transistors at the IMB-CNM clean room includes more than 90 technological steps, 7 photolithographic mask levels and several ion implantation processes at different doses of Boron, Phosphorus, and Arsenic dopants. Besides, the use of a highly doped polysilicon layer for defining the Gate electrode allows the utilization of just a single additional metal layer to interconnect the Source electrodes of the cells. Among the different steps, two key operations are of major concern: the trench etching and the trench complete sealing. The trenches are etched by means of a deep reactive ion etching (DRIE) technique [19], which gives excellent verticality and

uniformity in trenches even more than 200 µm deep. A complete sealing is then required for structural stability and to permit the following steps of the process (photolithography and layer depositions). Two polysilicon layers are successively deposited to this aim. The first one is doped in a $POCl_3$ ambient immediately after the deposition, to acquire the n-type character required to work as the gate electrode. A second polysilicon layer is then deposited to refill the trench. This second undoped layer is then completely removed from the surface, since it does not play any role in the front-end connections. As seen from SEM images, the trench is not fully filled by the undoped polysilicon since the deposition method causes a premature trench sealing, which is mandatory to continue with the subsequent technological steps. Nevertheless, the incomplete trench filling does not have any relevant impact on the current and voltage capabilities. Before the metal deposition, a thick inter-level oxide layer is deposited to get the required isolation between the Gate and Source electrodes. A BPTEOS oxide of 730 nm is preferred for its good quality and excellent replication of the surface topography. The device is finished with the source and drain metals (Al/Cu of 1.5 and 1 µm, respectively) and the passivation layer consisting of consecutively deposited oxide and nitride layers with a total thickness of 700 nm. The active area of the fabricated devices is fixed at 5×5 mm^2 but the number of paralleled cells depends on the $2r$ value: 9.500 for $2r$ = 35 µm and 14.000 for $2r$ = 23 µm.

Figure 5 shows a SEM image of a V-JFET sample obtained just before the metal deposition. The tilted image allows distinguishing the arrangement of parallel cells, as well as the location of the peripheral gate runner and three of the floating guard rings. A layout scheme is also inset in the figure, for the shake of clarity. The cross section visible in the front confirms the good verticality of the etched trenches and their uniformity in depth.

The sample has been prepared with a reverse engineering technique to highlight the regions with higher doping concentration. In this sense, the amplified SEM image of Figure 6, focused on the top side of an individual cell, shows the different elements present in the cell design. Highly doped regions, such as the doped polysilicon layer or the Source implant are clearly distinguishable. The n-type diffusion layer surrounding the trench edges can be also observed. From the image, it is clear that the second polysilicon layer is not thick enough to fill the entire trench hole. Even so, the combined effect of this layer with the thick inter-level oxide leads to a complete seal of the trench, thus allowing the process to continue with the following fabrication steps.

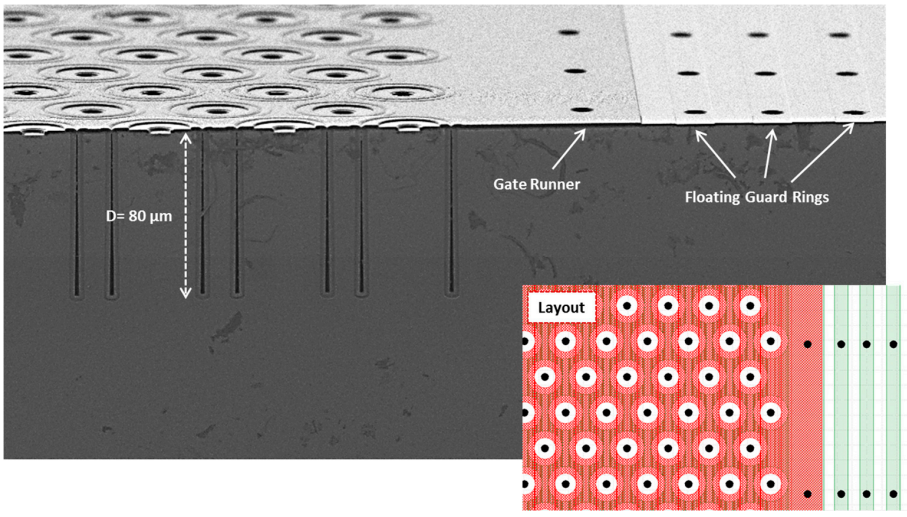

Figure 5. SEM image of a cross section through the center of a row of cells, obtained on a V-JFET sample before the metal deposition. Several peripheral elements (gate runners and guard rings) can be observed together with the arrangement of parallel cells. A depict of the layout is also shown in the bottom right inset.

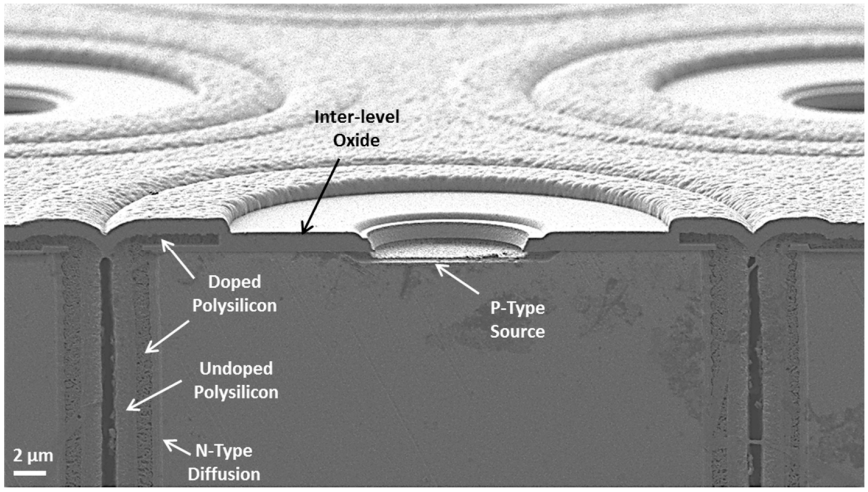

Figure 6. SEM image of a cross section through the center of an individual V-JFET cell, obtained on a sample during the fabrication process. Regions with different doping levels are distinguishable thanks to a preparation of the sample with a reverse engineering technique.

Due to the difficulty of obtaining highly resistive substrates with the good doping concentration precision, two different batches have been used for the fabrication of the first prototypes. The first one contains wafers with a nominal resistivity ranging between 500 and 1000 Ω·cm, which for p-type dopants is equivalent to N_A = 1 to 3 × 10^{13} at/cm^3; the second one presents a nominal resistivity between 150 and 500 Ω·cm, corresponding to N_A ranging from 3 to 9 × 10^{13} at/cm^3. The choice allows covering the whole range of optimum values discussed in the previous section, although the lack of accuracy in the actual N_A value advise against the use of a single value for the other design parameters. Consequently, three different diameters (2r = 23, 29 and 35 µm) have been considered. Concerning the trench layout, values of D = 80 µm and W = 5 µm have been fixed. In addition, two cell-to-cell separation (S) values of 7 and 10 µm have been considered to test the structural stability of the arrangement if S is reduced.

4. Electrical Performance

The particular layout of the V-JFET transistor, with n-type Gate and p-type Source and Drain electrodes, forces the use of a specific measurement set-up. In order to avoid the forward bias of the channel-trench p-n junction, both the Gate-to-Source (V_{GS}) and the Gate-to-Drain (V_{GD}) voltages should be always greater than or equal to zero. A straightforward way to get this conditions is the application of a negative bias to the Drain and Source electrodes, while the Gate bias is always positive. This arrangement allows analyzing the forward conduction mode when $0 \leq V_{GS} < V_{OFF}$ and $V_{DS} \leq 0$, whereas the forward blocking mode is obtained when $V_{GS} \geq V_{OFF}$ and $V_{DS} \leq 0$. The reverse mode can be also explored for $V_{DS} > 0$, provided the $V_{GD} \geq 0$ restriction is always observed.

Taking this into account, the output ($|I_D|$ vs. V_{DS} at V_{GS} = 0 V) and transfer ($|I_D|$ vs. V_{GS} at $V_{DS} > V_{DS|SAT}$) characteristic curves have been measured in all the fabricated prototypes. For devices with equal design (i.e., with the same 2r, S and A values), the measured current scales at different levels depending on the wafer of origin. By way of example, Figures 7 and 8 respectively shown the output and transfer characteristics for three representative 2r = 35 µm samples fabricated on different wafers. The corresponding simulated curves for different N_A values are also included in the figures, and demonstrate great accordance with the observed performance. All the prototypes fabricated on the first batch of wafers, with nominal N_A between 1 and 3 × 10^{13} at/cm^3, show characteristic curves as the ones labeled as Wafer A in the figures. For the prototypes of the second batch, where the nominal N_A ranges from 3 to 9 × 10^{13} at/cm^3, two groups of curves (B and C) have been identified, with all the devices of a given wafer belonging to the same group. According to the simulations, wafers in the

first batch yield in the lower part of the expected range of N_A values, since all the measured curves correspond to N_A between 1 and 2×10^{13} at/cm^3. For their part, wafers used for the second batch had actual N_A values around 6×10^{13} at/cm^3, for the group B, and 7×10^{13} at/cm^3, for the group C, both in the higher side of the expected range. As a consequence, the intermediate values of the optimum range for N_A were not affordable in this study.

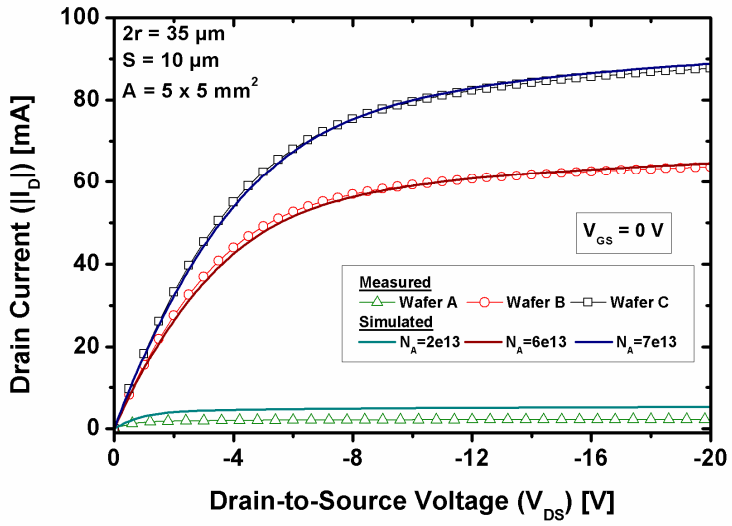

Figure 7. Measured output characteristic curves ($|I_D|$ vs. V_{DS} at $V_{GS} = 0$ V) for several representative V-JFET samples, with $2r = 35$ µm, $S = 10$ µm and $A = 5 \times 5$ mm^2, coming from different wafers (A, B, and C), and compared with the corresponding simulated curves for different N_A values.

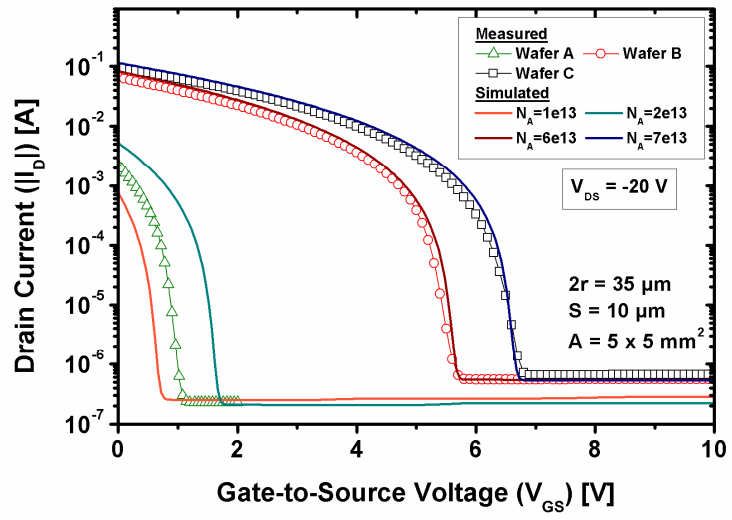

Figure 8. Measured transfer characteristic curves ($|I_D|$ vs. V_{GS} at $V_{DS} = -20$ V) for several representative V-JFET samples, with $2r = 35$ µm, $S = 10$ µm and $A = 5 \times 5$ mm^2, coming from different wafers (A, B, and C), and compared with the corresponding simulated curves for different N_A values.

The average values of the main Figures of Merit (FoM) extracted from the measured characteristics are compiled in Table 1. The values come from the measurement of 360 working VJFET devices. For devices fabricated on wafers of group A, low I_{ON} and V_{OFF} values have been obtained, with only the $2r = 35$ µm designs achieving forward currents over the milliampere order and switching voltages close to 1 V. Besides, the low N_A value led to a relatively high on-state resistance (R_{ON}) in the order

of kΩ. For devices fabricated in the second batch (groups B and C), I_{ON} ranges from more than 10 mA to almost 100 mA, mainly depending on the cell diameter. A significant reduction is observed in R_{ON}, with values below 100 Ω for all the cases. V_{OFF} is strongly dependent on r. Hence, prototypes with $2r$ = 23 μm show V_{OFF} around 2 V, whereas the average V_{OFF} value approaches 4 V for the 29 μm case, and is always higher than 5 V if $2r$ = 35 μm.

Concerning the forward blocking performance, the measured leakage current levels (I_{OFF}) are typically below the microampere order, with the majority of prototypes of group A showing I_{OFF} ~0.2 μA. The Gate leakage (I_G), both in conduction and blocking modes, averages current levels below 1 μA, with similar I_{OFF} values. However, a large I_G increase has been measured in some devices, particularly for high V_{GS}. Other devices show high leakage even at V_{GS} = 0 V. As it is considered a reliability issue, both cases have not been taken into account when extracting the average values listed in Table 1.

Table 1. Measured values for the main Figures of Merit.

Wafer Group	$2r$ (μm)	I_{ON} (mA)	R_{ON} (Ω)	V_{OFF} (V)	I_{OFF} (μA)	I_G (μA)	$V_{BD\|FULL}$ (V)
A	23	0.1 ± 0.0	4.0k ± 1.1k	0.1 ± 0.0	0.3 ± 0.2	0.2 ± 0.2	<675
	29	0.7 ± 0.1	0.7k ± 0.1k	0.5 ± 0.0	0.2 ± 0.1	0.2 ± 0.1	
	35	2.2 ± 0.3	0.4k ± 0.0k	0.9 ± 0.0	0.2 ± 0.2	0.2 ± 0.2	
B	23	13.1 ± 1.5	95.8 ± 8.6	2.0 ± 0.0	1.1 ± 0.4	1.1 ± 0.5	<300
	29	33.0 ± 1.3	70.7 ± 1.6	3.7 ± 0.1	0.8 ± 0.2	0.8 ± 0.2	
	35	65.7 ± 5.9	58.1 ± 3.0	5.5 ± 0.1	0.8 ± 0.2	0.8 ± 0.2	
C	23	17.7 ± 2.6	79.3 ± 10.4	2.4 ± 0.1	1.0 ± 0.2	1.0 ± 0.3	<275
	29	43.0 ± 0.2	60.6 ± 0.1	4.3 ± 0.2	0.9 ± 0.2	0.9 ± 0.2	
	35	87.2 ± 7.9	47.6 ± 2.6	6.8 ± 0.3	0.8 ± 0.2	0.8 ± 0.2	

The voltage capability of the fabricated prototypes has been also measured. The obtained $V_{BD|FULL}$ values show high variability and are too low, even considering that a large reduction with respect to the simulated $V_{BD|CELL}$ was expected. For prototypes of the group A, a maximum $V_{BD|FULL}$ = 675 V has been measured. Meanwhile, $V_{BD|FULL}$ is never higher than 300 V in the group B and group C devices. The breakdown point is located at the bottom of the peripheral trenches and the edge termination was optimized for a low substrate doping concentration (N_A). The dependence of the edge termination efficiency on the substrate doping concentration is very strong and the drastic reduction of the voltage capability is directly related with high N_A values of the available wafers. On the other hand, no correlation has been found between the voltage capability and the size of the cells, as prototypes with different r show similar $V_{BD|FULL}$ values. The variability in the measured $V_{BD|FULL}$ value and the influence of the implemented edge termination strategy are discussed in the next section.

Finally, it has to be noted that the dynamic performance has not been evaluated in this study, since the device is not conceived to work in switching mode.

5. Reliability

Two main reliability concerns have been found during the characterization of the V-JFET prototypes: an abnormal increase in the Gate leakage current in several devices working in forward blocking mode and a large variability of the voltage capability, even for devices with equal design, fabricated on the same wafer. In addition, the measured $V_{BD|FULL}$ values were always below the expectations. Both, issues have been specifically analyzed with the aid of lock-in infrared thermography technique.

Although most of the measured devices show Gate leakage in the order of a few hundreds of nanoamperes, approximately a 30% of the prototypes exhibit higher Gate currents, particularly when they are biased in the blocking mode. Figure 9 shows the Gate current vs. Gate voltage characteristic for one of such malfunctioning devices, compared with the curves of two prototypes with standard performance. A sudden current increase takes place for $V_{GS} > V_{OFF}$, rising the Gate leakage to

almost the milliampere order. Some other samples exhibit an analogous current increment, even with V_{GS} = 0 V. The Gate current drift is observed in devices for all the wafers, irrespective the particular design parameters. It cannot be attributed to a bulk effect, since measurements at low temperature (down to −30 °C) have not shown any scaling of the abnormal current level, whereas the standard Gate leakage was reduced according to the theoretical expectations. In addition, the Gate leakage increase leads to an immediate rise of the Source current, thus pointing to a short-circuit between the electrodes.

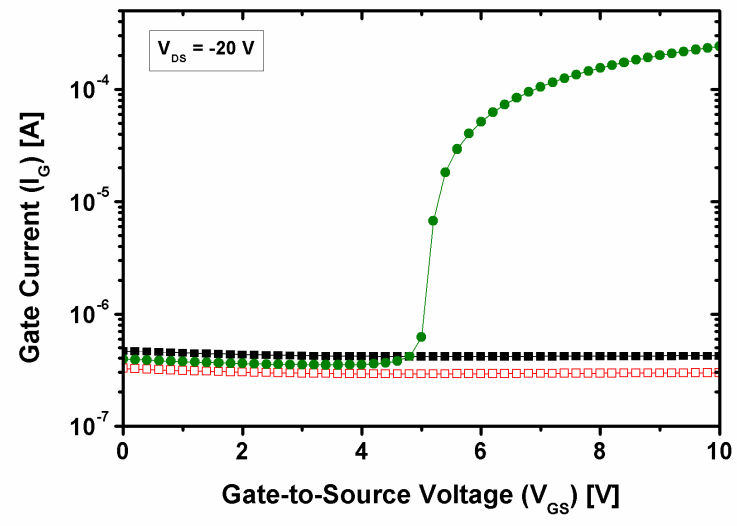

Figure 9. Measured Gate current as a function of the Gate bias (I_G vs. V_{GS} at V_{DS} = −20 V) for several V-JFET samples with equal design, fabricated on the same wafer. The leakage current increase for $V_{GS} > V_{OFF}$, observed in one malfunctioning sample is compared with the curves of other prototypes with standard performance.

To analyze this case, a lock-in infrared measurement [20] was performed on a malfunctioning device by modulating the Gate voltage with a sine-like voltage of certain amplitude (ΔV), around a specific V_{GS} value [21,22]. V_{DS} is held constant well below the $V_{BD|FULL}$ value. For V_{GS} < 2 V, the transistor is biased in the conduction mode and low Gate leakage is observed. An infrared thermography image was composed, by obtaining 15,000 frames while the transistor Gate was being modulated with ΔV = 4 V and lock-in frequency, $f_{lock\text{-}in}$ = 500 Hz. As shown on the top side of Figure 10, uniform dissipation takes place throughout the whole device, and no leakages are observed. Conversely, when the Gate is modulated in the same way around V_{GS} = 7.5 V, a conspicuous hot-spot is clearly observed. The infrared thermography, represented in the bottom side of Figure 10, shows how the Gate leakage increment is completely driven through the hot-spot, with all the heat generation focused on a single location. Although the issue is still under study, a pin-hole in the inter-metal oxide has been identified as the most probable cause of the hot-spot generation, requiring a future improvement of its quality for better yield.

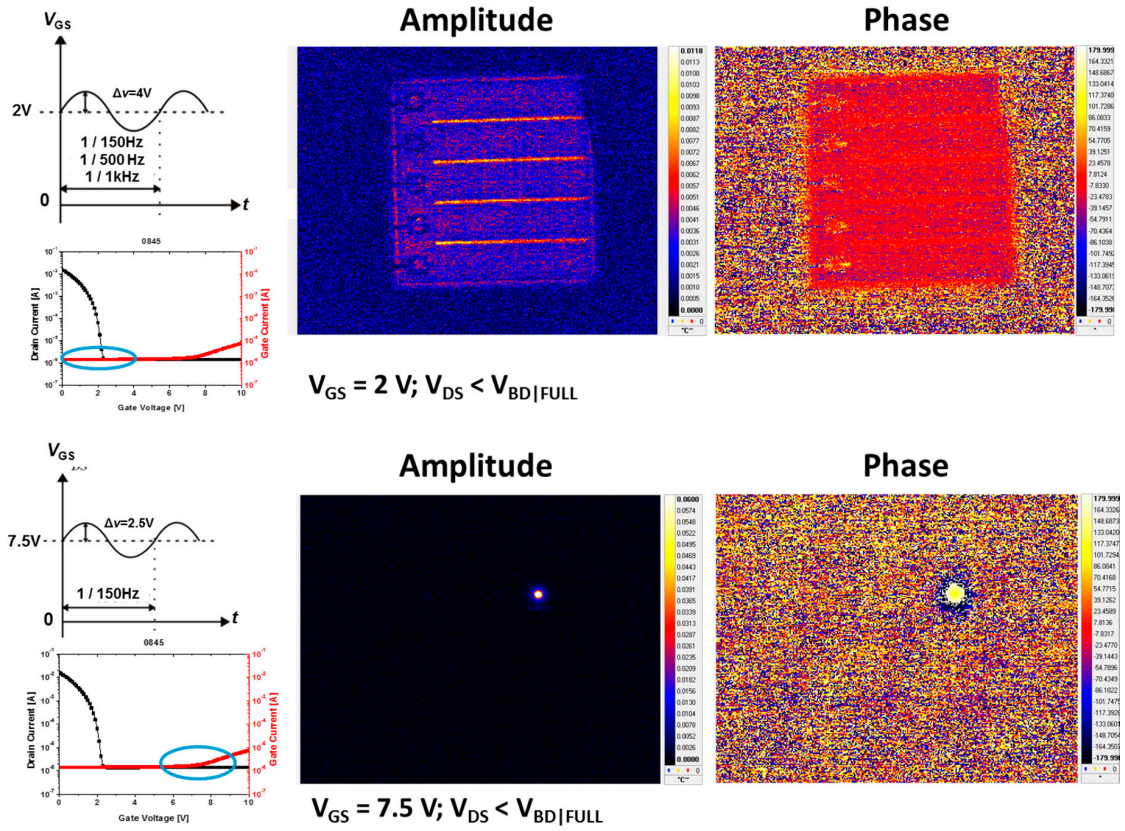

Figure 10. Lock-in thermography amplitude and phase images, obtained with a voltage Gate modulation of ΔV = 4 V, for a V-JFET sample biased at V_{GS} = 2 V (**top side**), and at V_{GS} = 7.5 V (**bottom side**). A hot spot responsible of the Gate leakage increase is observed in the second case.

The low breakdown voltage of the samples was also studied with the aid of the infrared thermography analysis. In this case, Drain voltage modulation was performed, while V_{GS} is held constant at different values to explore both the forward conduction and forward blocking operational modes of the transistor. For $V_{DS} < V_{BD|FULL}$, no signal was discerned, irrespective the V_{GS} considered, since the devices are not dissipating enough power. When the transistor is biased close to the breakdown ($V_{DS} = -300$ V), a higher signal level can be obtained, as a consequence of the increase in power dissipation, as shown in images from Figure 11. For V_{GS} = 0 (top side of the figure), with the transistor working in forward conduction, uniform dissipation is perceived. When the transistor is switched-off into the blocking mode, the dissipation focuses at the periphery. As shown in the bottom side of Figure 11, for $V_{GS} = -10$ V, several hot spots appear on the peripheral Gate runner. Two main conclusions can be extracted from the analysis: The Gate-to-Drain breakdown is located at the peripheral Gate runner, thus indicating that the floating guard rings are not contributing to increase the voltage capability of the device; this can be identified as the main cause of the low $V_{BD|FULL}$ value measured in all the devices. Besides, the power dissipation is not uniformly distributed all around the periphery; on the contrary, several hot-spots of different size can be distinguished. The presence of these weak points in the design may be the origin of the high variability in $V_{BD|FULL}$ observed among different devices. The edge termination strategy is now being revisited to achieve a more robust and uniform breakdown behavior.

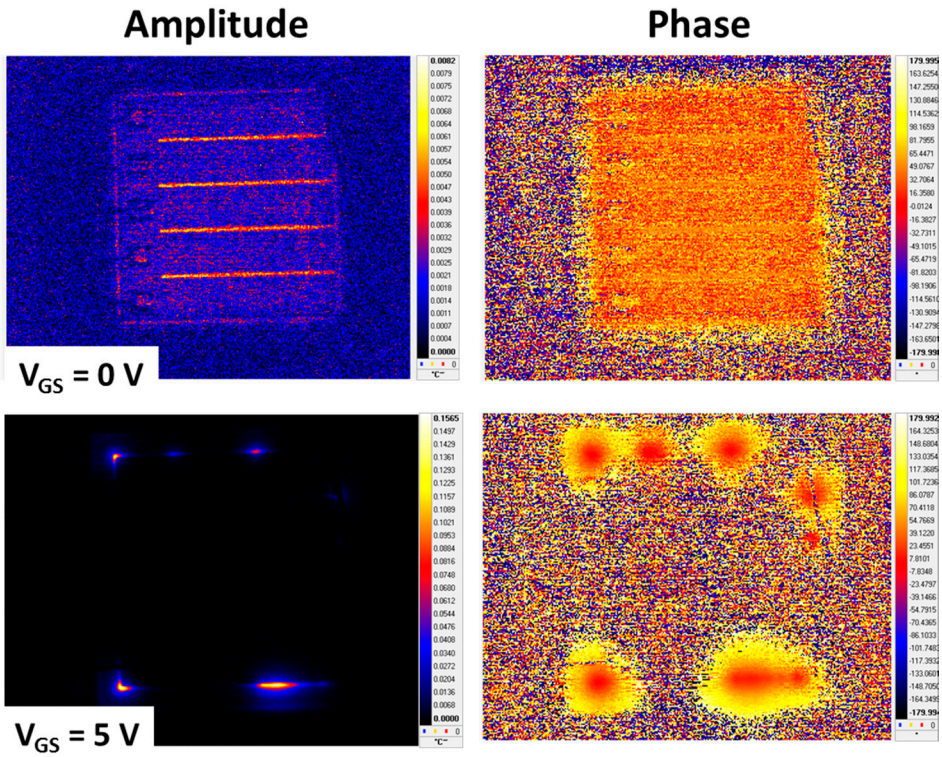

Figure 11. Lock-in thermography amplitude and phase images, obtained with a Drain voltage modulation of ΔV = 5 V around the breakdown value (V_{DS} = −300 V), for a V-JFET sample biased in conduction (V_{GS} = 0 V; **top side**), and blocking (V_{GS} = 5 V; **bottom side**) modes. Hot spots responsible for the breakdown are not uniformly located at the peripheral Gate runner.

6. Radiation Hardness

Two different mechanisms are responsible for the radiation effects on the electronic devices [23]: ionizing radiation introduces ionization damage (ID), whereas non-ionizing radiation induces displacement damage (DD). In both cases, the consequences on the device performance are generally the result of the accumulative effect of the introduced damage. In addition, single event effects (SEE) may occur when a highly energetic particle introduces large amount of damage (usually ID) within a particularly sensitive region of the electronic device [24]. ID is especially harmful for dielectric materials, where the introduced damage leads to the accumulation of trapped charge. This charge, which can eventually become permanently fixed, is able to modify the distribution of the electrostatic potential in the device. In this sense, MOS transistors and other insulated Gate devices are specifically sensitive to ID [25]. On the contrary, DD affects the semiconductor layers into a greater extent, as the semiconductor lattice is affected by the introduction of active defects and dislocations. Bipolar transistors and other devices with large depleted regions, such as the semiconductor radiation detectors, have been reported especially sensitive to displacement damage [26].

High radiation tolerance is expected in the V-JFET thanks to its specific design. The absence of a Gate oxide and other insulator layers within the active regions of the device makes the V-JFET less sensitive to the accumulated effects of the ionizing radiation. Although a certain increase can be expected in the leakage current, the use of a p-type substrate (less sensitive to DD [27]) and the volume conduction through relatively wide channels also prospected radiation hardness as far as the non-ionizing radiation is concern. SEE are not considered a probable cause of fail, thanks to the large number of parallel cells present in the transistor layout: even if an individual cell becomes affected by a SEE, the possible current increase represents a minor alteration in the overall current of the whole arrangement. In this sense, SEE were not tested in this work.

To analyze the effect of ID, 30 V-JFET samples were exposed to different doses of a pure gamma radiation source. Gamma radiation consists of high energetic photons able to produce large amount of ID, although a minor amount of DD can be also introduced into the semiconductor layers, from the secondary electrons released by Compton Effect. Irradiations, up to a total ionizing dose (TID) of 100 Mrad(Si), corresponding to a dose rate of 389 krad(Si)/h, where performed at the NAYADE ^{60}Co water well source of the CIEMAT [28], in Madrid (Spain). Details of the experimental set up and a thorough analysis of the obtained results can be found in [29]. The performance of the irradiated devices was almost the same as before the irradiation. Most of the FoM (e.g., V_{OFF}, I_{OFF}, I_G, or $V_{BD\,|\,FULL}$) remained unaffected even for the highest TID considered. The single relevant effect was a minor reduction of the conduction current in the forward mode, which led to lower I_{ON}, and higher R_{ON} values. Nevertheless, the FoM modification achieved a maximum of ~20% for 50 Mrad(Si) and saturates for higher TID, whereas was almost negligible below 10 Mrad(Si) [29]. All this considered, the V-JFET prototypes have been proved to remain fully operative after a high dose pure ionizing irradiation.

The effects of DD are normally studied in samples irradiated with hadrons, e.g., neutrons, protons or pions. Among them, neutrons are preferred, since the absence of electrical charge leads to almost pure DD effects into the semiconductor devices. Hence, 55 V-JFET samples were irradiated at different neutron fluences in a TRIGA-type nuclear reactor at the Jožef Stefan Institute in Ljubljana (Slovenia) [30]. The particular nature of the irradiation source produces neutrons with a continuous spectrum of energies (including thermal neutrons), which are then normalized according to the NIEL scaling [31], and expressed by means of a 1-MeV neutron equivalent fluence (n_{eq}) magnitude, which takes into account the weighted effect of all the non-ionizing contributions.

After high neutron irradiation fluence up to of 2×10^{13} n_{eq}/cm^2, the V-JFET samples still remained fully operative, although the DD effects were not negligible. The variation in the transistor performance can be observed in Figure 12, where the transfer characteristic of an irradiated sample is compared with the curve measured before the irradiation. The sample was fabricated on a p-type substrate with a doping concentration of 7×10^{13} cm^{-3}. The forward current exhibits a reduction in the range of 60 ma, depending on the sample and on the specific layout, whereas the blocking leakage current increases notably, from 0.1 to 2 µA. Similar increment is observed in the Gate leakage current. Besides, V_{OFF} experiences a reduction of almost 3 V.

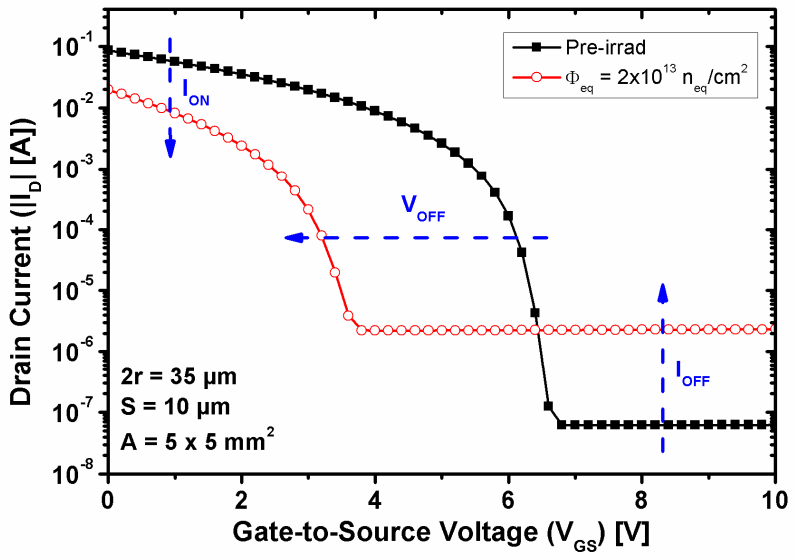

Figure 12. Measured transfer characteristic curves for a V-JFET sample, before and after a neutron irradiation with equivalent fluence of 2×10^{13} n_{eq}/cm^2. The effects on I_{ON}, I_{OFF}, and V_{OFF} are indicated in the figure.

The increase in the blocking and Gate leakage currents were expected, since it is typically observed in radiation detectors fabricated on p-type silicon substrates [32]. This effect is generally associated with the introduction of a large amount of DD defects, which can act as generation-recombination centers in the depleted regions of the affected silicon. In contrast, the observed effects in the undepleted silicon (i.e., the V_{OFF} and the forward current reductions) can be associated with a decrease in the effective doping concentration of the substrate. Although this effect is still under study, it can be due to an acceptor removal process, already reported in the literature [33], and analogous to the well documented donor removal effect, associated to DD effects on n-type silicon substrates [24].

7. Conclusions

A new Vertical JFET technology has been developed at Centro Nacional de Microelectrónica (IMB-CNM, CSIC) in Barcelona, for harsh radiation applications. Fabricated on a p-type silicon substrate, the new V-JFET transistor consists of a large arrange of parallel cells (typically 10,000), each one of then surrounded by a trench of ring shape, deeply etched in the silicon substrate. The trench acts as the Gate electrode thus allowing vertical conduction through the confined silicon channel as well as a low switch-off voltage. The actual characteristics of the whole device are strongly related with the values of several design and technological parameters (i.e., the cell radius, the trench depth, the substrate doping concentration, and the total area of the device). A thorough optimization of the final design according to the values of these parameters has been discussed in this paper. The technological process was also outlined, with a particular emphasis laid on the trench etching and filling steps, which are crucial for attaining working prototypes.

After the fabrication, the V-JFET samples were fully characterized and the main results have been compiled here. The measured performance is in very good agreement with the simulation predictions, with forward current levels up to the 100 mA level, switch-off voltage ranging between 1 and 6 volts, depending on the cell radius and the substrate doping concentration, and blocking current and Gate leakage typically below the microampere order. Two main reliably issues have been held in the article, too: the relatively low voltage capability of the fabricated prototypes, and the rising of the blocking current in several devices. Both cases have been investigated with the aid of the lock-in infrared thermography technique, and the results point to an ineffective design of the edge termination region, in the first case, and to the presence of pin-holes in the inter-metal oxide. Still under study, both issues will be carefully addressed in the next batch production.

The radiation hardness of the V-JFET has been also tested with gamma and neutron irradiations up to total ionizing dose of 100 Mrad(Si) and equivalent fluence of 2×10^{13} n_{eq}/cm^2, respectively. Minor effects have been found as far as the gamma ionizing damage is concern. For its part, the displacement damage introduced by neutrons is able to notably modify the characteristic curves of the irradiated devices. Nevertheless, the evaluated samples remain fully operative under the radiation levels considered in this study.

Acknowledgments: The authors would like to heartily thank the Clean Room staff of the IMB-CNM for their dedicated work and kind availability. This work is supported and financed in part by the Spanish Ministry of Economy and Competitiveness through the Particle Physics National Program, ref. FPA2014-55295-C3-2-R and FPA2015-65652-C4-4-R (MINECO/FEDER, UE), and co-financed with FEDER funds and the European Union's Horizon 2020 research and innovation programme under grant agreement No. 654158. The work is also partially supported by the Generalitat de Catalunya (2014-SGR-1596). The authors want to thank Pedro Valdivieso and co-workers at NAYADE facility (CIEMAT) and the staff on the TRIGA nuclear reactor facilities (JSI), for their efficiency and dedication in performing the managing and irradiation of our devices.

Author Contributions: Pablo Fernández-Martinez, David Flores, Salvador Hidalgo, David Quirion and Miguel Ullán conceived and designed the device under study, as well as the technological process for its fabrication. David Quiron supervised the fabrication at the IMB-CNM clean room. Pablo Fernández-Martínez and Lucía Ré performed all the experimental measurements. Xavier Jordà, Xavier Perpiñà, and Miquel Vellvehí performed the locking IR analysis of the device. Pablo Fernández-Martínez and David Flores wrote the paper.

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Adell, P.C.; Scheik, L.Z. Radiation effects in power systems: A review. *IEEE Trans. Nucl. Sci.* **2013**, *60*, 1929–1952. [CrossRef]
2. Faccio, F.; Allongue, B.; Balnchot, G.; Fuentes, C.; Michelis, S.; Orlandi, S.; Sorge, R. TID and displacement damage effects in vertical and lateral power MOSFETs for integrated DC-DC converters. *IEEE Trans. Nucl. Sci.* **2010**, *57*, 1790–1797. [CrossRef]
3. Weber, M. Power distribution for SLHC trackers: Challenges and solutions. *Nucl. Instrum. Meth. A* **2008**, *592*, 44–55. [CrossRef]
4. Díez, S.; Ullán, U.; Pellegrini, G.; Lozano, M.; Sorge, R.; Knoll, D. Radiation studies of power LDMOS devices for high energy physics applications. *IEEE Trans. Nucl. Sci.* **2010**, *57*, 3322–3328.
5. Gianotti, F.; mangano, M.; Virdee, T. Physics potential and experimental challenges of the LHC luminosity upgrade. *Eur. Phys. J. C* **2005**, *39*, 293–333. [CrossRef]
6. ATLAS Collaboration. ATLAS Phase-II Upgrade Scoping Document 2015. Available online: https://cds.cern.ch/record/2055248?ln=es (accessed on 1 December 2016).
7. Villani, E.G.; Phillips, P.; Matheson, J.; Zhang, Z.; Lynn, D.; Kuczewski, P.; Hommels, L.B.A.; Gregor, I.; Bessner, M.; Tackmann, K.; et al. HVMUX, the high voltage multiplexing for the ATLAS tracker upgrade. *J. Instrum.* **2015**, *10*. [CrossRef]
8. Moser, H.G. Silicon detector systems in high energy physics. *Prog. Part. Nucl. Phys.* **2009**, *63*, 186–237. [CrossRef]
9. Abbate, C.; Alderighi, M.; Baccaro, S.; Busatto, G.; Citterio, M.; Cova, P.; Delmonte, N.; de Luca, V.; Gerardin, S.; Ghisolfi, E.; et al. Radiation performance of new semiconductor power devices for the LHC experiment upgrades. In Proceedings of the 11th International Conference on Large Scale Applications and Radiation Hardness of Semiconductor Detectors, Florence, Italy, 3–5 July 2013.
10. Veliadis, V.; Steiner, B.; Lawson, K.; Bayne, S.B.; Urciuoli, D.; Ha, H.C.; El-Hinnawy, N.; Gupta, S.; Borodulin, P.; Howell, R.S.; et al. Reliable operation of SiC JFET subjected to over 2.4 million 1200-V/115-A hard switch stressing events at 150 °C. *IEEE Electr. Device Lett.* **2013**, *34*, 384–386. [CrossRef]
11. Pushpakaran, B.N.; Hinojosa, M.; Bayne, S.B.; Veliadis, V.; Urciuoli, D.; El-Hinnawy, N.; Borodulin, P.; Gupta, S.; Scozzie, C. High temperature unclamped inductive switching mode evaluation of SiC JFET. *IEEE Electr. Device Lett.* **2013**, *34*, 526–528. [CrossRef]
12. Schwank, J.R.; Shaneyfelt, M.R.; Fleetwood, D.M.; Felix, J.A.; Dodd, P.E.; Paillet, P.; Ferlet-Cavrois, V. Radiation effects in MOS oxides. *IEEE Trans. Nucl. Sci.* **2008**, *55*, 1833–1853. [CrossRef]
13. Lambert, D.; Schmeidl, M.; Wu, X.; Neyer, T. A concise study of neutron irradiation effects on power MOSFETs and IGBTs. *Microelectron. Reliab.* **2016**, *62*, 74–78.
14. Baghaie Yazdi, M.; Desnoyers, F.; Thouvenot, D.; Azais, B. Single event effect in power MOSFETs and IGBTs due 14 MeV and 25 MeV neutrons. *Microelectron. Reliab.* **2016**, *62*, 74–78. [CrossRef]
15. Zebrev, G.I.; Petrov, A.S.; Useinov, R.G.; Ikhsarov, R.S.; Ulimov, V.N.; Anashin, A.S.; Elushov, I.V.; Drosdetsky, M.G.; Galimov, A.M. Simulation of bipolar transistor degradation at various dose rates and electrical modes for high dose conditions. *IEEE Trans. Nuc. Sci.* **2014**, *61*, 1785–1790. [CrossRef]
16. Fernández-Martínez, P.; Ullán, M.; Fores, D.; Hidalgo, S.; Quirion, D.; Lynn, D. Rad-hard vertical JFET switch for the HV-MUX system of the ATLAS upgrade Inner Tracker. *J. Instrum.* **2016**, *11*. [CrossRef]
17. Fernández-Martínez, P.; Flores, D.; Hidalgo, S.; Quirion, D.; Durà, R.; Ullán, M. First Fabrication of A Silicon Vertical JFET for Power Distribution in High Energy Physics Applications. *Nucl. Instrum. Method A* **2017**. under review.
18. Baliga, B.J. *Modern Power Devices*; Wiley-Interscience: Hoboken, NJ, USA, 1987.
19. Wu, B.; Kumar, A.; Pamarthy, S. High aspect ratio silicon etch: A review. *J. Appl. Phys.* **2010**, *108*, 051101. [CrossRef]
20. León, J.; Berthou, M.; Perpiñà, X.; Banu, V.; Monserrat, J.; Vellvehí, M.; Godignon, P.; Jordà, X. Structural analysis of SiC Shottky diodes failure mechanism under current overload. *J. Phys. D Appl. Phys.* **2014**, *47*, 055102. [CrossRef]
21. Ouaida, R.; Berthou, M.; León, J.; Perpiñà, X.; Oge, S.; Brosselard, P.; Joubert, C. Gate oxide degradation of SiC MOSFET in switching conditions. *IEEE Electron Device Lett.* **2014**, *35*, 1284–1286. [CrossRef]

22. Chevalier, F.; Tournier, D.; Jordà, X.; León, J.; Perpignà, X.; Godignon, P. Impact of the design of 4H-SiC JFET on switching delay and gate potential distribution with the aim of a free-wheeling diode integration. In Proceedings of the 10th European Conference on Silicon Carbide and Related Materials, Grenoble, France, 21–25 September 2014.
23. Bräunig, D.; Wulf, F. Atomic displacement and total ionizing dose damage in semiconductors. *Radiat. Phys. Chem.* **1994**, *43*, 105–127. [CrossRef]
24. Baumann, R.C. Radiation-induced soft errors in advanced semiconductor technologies. *IEEE Trans. Device Mater. Reliab.* **2005**, *5*, 305–316. [CrossRef]
25. Ma, T.; Dressendorfer, P. *Ionizing Radiation Effects in MOS Devices and Circuits*; John Wiley and Sons, Inc.: Hoboken, NJ, USA, 1989.
26. Leroy, C.; Rancoita, P.G. Particle interaction and displacement damage in silicon devices operated in radiation environments. *Rep. Prog. Phys.* **2007**, *70*, 493–625. [CrossRef]
27. Lindström, G.; Moll, M.; Fretwurst, E. Radiation hardness of silicon detectors—A challenge from high-energy physics. *Nucl. Instrum. Method A* **1999**, *426*, 1–15. [CrossRef]
28. Centro de Investigaciones Energética, Medioambientales y Tecnológicas (CIEMAT), Centro de la Moncloa, Madrid. Available online: http://www.ciemat.es (accessed on 15 December 2016).
29. Fernández-Martínez, P.; Ré, L.; Flores, D.; Hidalgo, S.; Quirion, D.; Ullán, M. Gamma Irradiation Damage on the Vertical JFET Transistors Fabricated at the IMB-CNM. *J. Instrum.* **2017**. in print.
30. TRIGA Mark II Reactor Centre at Jozef Stefan Institute. Available online: http://www.rcp.ijs.si/ric/index-a.htm (accessed on 15 December 2016).
31. Messenger, S.R.; Burke, E.A.; Summers, G.P.; Xapsos, M.A.; Walters, R.J.; Jackson, E.M.; Weaver, B.D. Nonionizing energy loss (NIEL) for heavy ions. *IEEE Trans. Nucl. Sci.* **1999**, *46*, 1595–1602. [CrossRef]
32. Moll, M.; Fretwurrst, E.; Kuhnke, M.; Lindström, G. Relation between microscopic defects and macroscopic changes in silicon detector properties after hadron irradiation. *Nucl. Instrum. Method B* **2002**, *186*, 100–110. [CrossRef]
33. Wunstorf, R.; Bugg, W.M.; Walter, J.; Garber, F.W.; Larson, D. Investigations of donor and acceptor removal and long term annealing in silicon with different boron/phosphorus ratios. *Nucl. Instrum. Method A* **1996**, *377*, 228–233. [CrossRef]