



Low Power Embedded Memories

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Message from the Guest Editor

Dear Colleagues,

This Special Issue will focus on circuit techniques for low power embedded memories. Nearly all embedded applications require on-chip memory, but the requirements for these embedded memories vary significantly across applications. For many embedded designs, reducing power is a key design concern. A variety of circuit approaches have emerged to meet low power needs for memory blocks. Topics of interest include, but are not limited to:

- reducing V_{min} for low power memory
- circuits and architectures for embedded DRAM
- alternative bit cells for low power SRAM
- sub-threshold memory arrays
- low power non volatile memory technologies and circuits
- circuit assist features for low power
- charge recycling in RAMs
- low power periphery (sense amplifiers, decoders, etc.)
- effects of variability on low power RAM

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Message from the Editor-in-Chief

Journal of Low Power Electronics and Applications (ISSN 2079-9268) is an open access journal which provides an advanced forum for the studies of electronics for low power applications. A special emphasize is made on ultralow power bio-medical applications. It publishes reviews, regular research papers and short communications.

Our aim is to encourage scientists to publish their experimental and theoretical results in as much detail as possible. There is no restriction on the length of the papers. Full experimental and/or methodical details must be provided.

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