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Advances in Low-Voltage Design Techniques for Scaled CMOS Technologies

Guest Editors:

Prof. Dr. Alfio Dario Grasso
Department of Electrical, Electronics and Computer Engineering (DIEEI), University of Catania, 95125 Catania CT, Italy

Dr. Andrea Ballo
Department of Electrical, Electronics and Computer Engineering (DIEEI), University of Catania, 95125 Catania, Italy

Deadline for manuscript submissions:
closed (31 December 2021)

Message from the Guest Editors

Dear Colleagues,

The down scaling of CMOS technology has enabled the implementation of complex analog and digital functions on the same die. This has come with a progressive reduction of the supply voltage below 1 V to reduce the electric field within MOS devices. Even lower supply voltage may be requested for ultra-low-power systems, such as biomedical implantable/wearable electronic devices and energy-autonomous Internet of Things (IoT) nodes.

The aim of this Special Issue is to attract researchers in the area of integrated circuits to highlight the recent advances in low-voltage design techniques. The topics to be covered in this Special Issue include, but are not limited to, the following:

- Conventional and nonconventional low-voltage analog and digital design techniques
- Theory, design, and new applications of sub-1-V analog and digital circuits
- Circuits for IoT nodes and implantable/wearable biomedical devices
- Low-voltage power-efficient analog-to-digital converters
- Circuits and systems for energy harvesting
- Power management of sub-1-V integrated digital and analog systems
- Time-based analog signal processing

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Editor-in-Chief

Prof. Dr. Giulio Nicola Cerullo
Dipartimento di Fisica, Politecnico di Milano, Piazza L. da Vinci 32, 20133 Milano, Italy

Message from the Editor-in-Chief

As the world of science becomes ever more specialized, researchers may lose themselves in the deep forest of the ever increasing number of subfields being created. This open access journal *Applied Sciences* has been started to link these subfields, so researchers can cut through the forest and see the surrounding, or quite distant fields and subfields to help develop his/her own research even further with the aid of this multi-dimensional network.

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Applied Sciences Editorial Office
MDPI, Grosspeteranlage 5
4052 Basel, Switzerland

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