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Solar Photovoltaic System-Based Reduced Switch Multilevel Inverter for Improved Power Quality

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Abstract: This paper deals with a reduced switch multi-level inverter for the solar photovoltaic system-based 127-level multi-level inverter. The proposed technique uses the minimum number of switches to achieve the maximum steps in staircase AC output voltage when compared to the flying capacitor multi-level inverter, cascaded type multilevel inverter and diode clamped multi-level inverter. The use of a minimum number of switches decreases the cost of the system. To eliminate the switching losses, in this topology a square wave switch is used instead of pulse width modulation. Thereby the total harmonic distortion (THD) and harmonics have been reduced in the pulsating AC output voltage waveform. The performance of 127-level MLI is compared with 15 level, 31-level and 63-level multilevel inverters. The outcomes of the solar photovoltaic system-based 127-level multi-level inverter have been simulated in a MATLAB R2009b environment.

Keywords: reduced switch multilevel inverter; power quality; solar photovoltaic system; cost saving



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1. Introduction

In the current generation, the demand for electricity is growing day by day. Nowadays, most electricity is generated through conventional energy sources (thermal, nuclear, etc.), which are not environmentally friendly. Due to these processes of generating electricity, the availability of fossil fuels is being reduced. Therefore, due to the reduction in conventional energy sources, we are unable to meet demand. To meet the demand, the alternative method of generating electricity is via non-conventional energy sources (wind energy, solar energy, hydro, biomass, etc.) which are environmentally friendly.

The Earth grabs a significant amount of solar power, at nearly 173 terawatts. This is around ten thousand times more power than the world's population uses. As such, it is possible that one day the world could be entirely reliant on solar energy, which could present an available, clean, pollution-free, highly efficient, and long-life energy source. With the help of technology, the cost of the SPV panels and associated equipment has reduced tremendously over recent decades [1]. To interface solar energy to the grid, low voltage PV cells are aligned in a series to acquire high DC output voltage [2]. This process needs high-rated voltage equipment for inversion and a step-up transformer, which increases the losses, cost, weight and size of the system [3]. To overcome these issues, the transformer can be eliminated.

Therefore, a multilevel inverter (MLI) uses the power of semiconductor device sources to integrate the staircase waveform near a sine waveform. The multilevel inverter is the best option for the majority of electricity production in an SPV system. The traditional 2-level inverters face high switching voltage stress, less efficiency and low power quality,

as stated in [4,5]. There are many types of inverter, including the neutral clamped, flying capacitor, cascaded H-bridge MLI has been reported [6–9]. The major difficulties related to MLI are the greater number of power switches and difficulty in its design.

In MLI, limiting the number of switches has attained major importance [10,11]. Limiting the number of power switches reduces the difficulty and enhances the performance of MLI [12]. The major benefit of the proposed configuration is the ability to produce multiple output voltage steps using the minimum number of switches at various adjustable magnitudes in DC input sources [13,14]. The 3-phase MLI technique and its design are more difficult compared with the 1-phase technique in terms of minimum switch count [15–17]. An easier assembly of the 3-phase MLI technique with reduced switches is proposed [18]. The key difficulty of the MLI design with a minimized switching technique is associated with the bi-directional power IGBT switches [19]. The least switching losses are attained when using a 3-phase hybrid control-based MLI [20]. In order to avoid the disadvantages of hard switching in a buck converter, a converter with soft switching cells is suggested for PV applications [21]. A transportable solar power generating unit with an inverter is suggested in [22]. In [23], an MLI specially designed for the grid integration of renewable energy sources is reported. Here, the number of switching states and, thus, the losses are reduced by recalculating and modulating the pulse width and height. A 9-level H-bridge MLI with two maximum power point tracking methods is developed in [24]. Different configurations of MLIs with a lower number of switching devices are suggested in [25–28]. A Quasi-Z source inverter is proposed for solar panel applications in [29]. A single-phase MLI with reduced switching stress on the power switches is suggested in [30]. A new MLI topology using a diode half-bridge circuit is explained in [31]. An MLI where the number of DC sources is reduced with the control of the switching scheme is suggested in [32]. A solar-powered electric vehicle parking lot for the optimal operation with respect to efficiency and cost is suggested in [33]. A seventeen-level inverter with less voltage stress and a smaller number of components is suggested in [34]. An H-bridge MLI for a solar power system which can be used for the interconnection of solar PV system with a distribution system is proposed in [35].

In this paper, a configuration is planned which has a lower number of IGBT switches for SPV voltage source based 127-level MLI. The proposed technique has ten IGBT semiconductor switches, which is a fewer amount than in the diode clamped, cascaded, and flying capacitor type MLI. In this proposed configuration, the main discussion is concerned with decreasing the gate-driven circuits and the number of IGBT switches for the most inexpensive 127-MLI. The proposed configuration of MLI uses SPV with DC-DC converters to turn as six dissimilar DC sources which produce 127-level at AC output voltage which, in turn, decreases harmonics and advances the power quality. This proposed configuration of 127-level is used in off-grid applications. The performance of the proposed technique is demonstrated through simulation, using the MATLAB R2009a environment.

2. Solar Photovoltaic System with Battery

The solar PV panels used consist of: 84 series of connected cells; $V_{oc} = 60$ V; $I_{sc} = 7.8$ A; $R_{se} = 0.18$ Ω ; $R_{sh} = 360$ Ω ; a number of series connected modules = 6; and a number of parallel connected modules = 6.

The battery model consists of a battery of V1–V6, in series resistance of 0.1 Ω , both in series with the parallel combination of the capacitor of 50,000 F and a resistor of 10 k Ω .

3. Proposed System Circuit and Its Configuration

3.1. 127-Level Multilevel Inverter Circuit Diagram

Figure 1 shows a 127-level reduced switch multilevel inverter. In this configuration, we are using ten switches to obtain 127 levels at the output voltage. Here we are using SPV as voltage sources, along with a DC-DC converter as the input for obtaining 127 levels of output. Therefore, to stepdown the voltage, these DC-DC converters are used by changing their duty cycle.

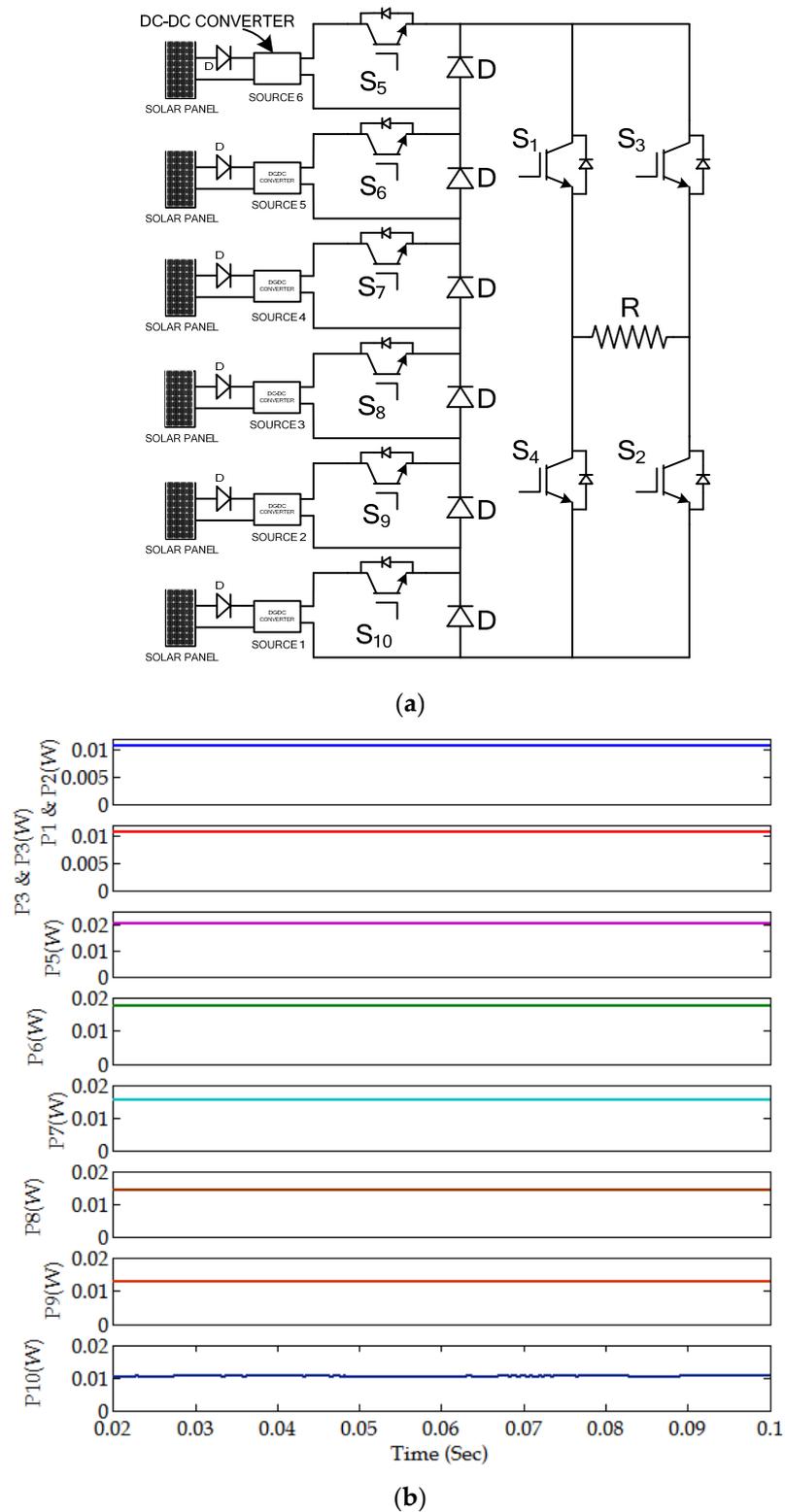


Figure 1. (a) 127-level reduced switch multilevel inverter. (b) Power losses in all the switches 127-level MLI.

3.2. 127-Level Multilevel Inverter Operation and Principle

In this proposed topology of a 127-level reduced switch multi-level inverter, the input is taken from the six solar photovoltaic panels along with the DC-DC converters to control the variations in the output voltage. This system is consisting of ten IGBT switches to

generate 127 levels in one cycle, so that the output waveform has become nearly sinusoidal and THD of the output waveform is reduced to a large extent. Here, diodes are used to avoid the bidirectional flow of the current. According to the requirement of output voltage, the IGBT switches are triggered at different intervals of time. Here the four switches, named S1, S2, S3 and S4, are used to form an inverter circuit that converts DC to AC, and the remaining six IGBT switches (S5, S6, S7, S8, S9 and S10) are used to obtain the desired output level of voltage from the solar panels. To obtain the positive half at the output, switches S1 and S2 should conduct throughout the positive half cycle. To obtain a negative half cycle, S3 and S4 should conduct throughout the negative half cycle.

By considering $V_1 = 10 \times V$, $V_2 = 20 \times V$, $V_3 = 40 \times V$, $V_4 = 80 \times V$, $V_5 = 160 \times V$ & $V_6 = 320 \times V$, where \times is the multiplication factor equal to $325.22/630$ and the solar photo voltaic panels connected in series parallel act as the input.

3.3. Switching Sequence of MLI for Positive Half Cycle

The below Table 1 illustrates the ON and OFF switching pattern of each and every switch, from steps 1 to 63 in the positive half cycle and a negative half cycle of the inverter. Output step voltages of MLI from steps 1 to 63 are shown in Table 1.

Table 1. Switching pattern of S5 to S10 in 127-level MLI.

STEP 1	S ₅	S ₆	S ₇	S ₈	S ₉	S ₁₀	Output (V ₀)
0	0	0	0	0	0	0	0
1	0	0	0	0	0	1	V ₁
2	0	0	0	0	1	0	V ₂
3	0	0	0	0	1	1	V ₂ + V ₁
4	0	0	0	1	0	0	V ₃
5	0	0	0	1	0	1	V ₃ + V ₁
6	0	0	0	1	1	0	V ₃ + V ₂
7	0	0	0	1	1	1	V ₃ + V ₂ + V ₁
8	0	0	1	0	0	0	V ₄
9	0	0	1	0	0	1	V ₄ + V ₁
10	0	0	1	0	1	0	V ₄ + V ₂
11	0	0	1	0	1	1	V ₄ + V ₂ + V ₁
12	0	0	1	1	0	0	V ₄ + V ₃
13	0	0	1	1	0	1	V ₄ + V ₃ + V ₁
14	0	0	1	1	1	0	V ₄ + V ₃ + V ₂
15	0	0	1	1	1	1	V ₄ + V ₃ + V ₂ + V ₁
16	0	1	0	0	0	0	V ₅
17	0	1	0	0	0	1	V ₅ + V ₁
18	0	1	0	0	1	0	V ₅ + V ₂
19	0	1	0	0	1	1	V ₅ + V ₂ + V ₁
20	0	1	0	1	0	0	V ₅ + V ₃
21	0	1	0	1	0	1	V ₅ + V ₃ + V ₁
22	0	1	0	1	1	0	V ₅ + V ₃ + V ₂
23	0	1	0	1	1	1	V ₅ + V ₃ + V ₂ + V ₁
24	0	1	1	0	0	0	V ₅ + V ₄
25	0	1	1	0	0	1	V ₅ + V ₄ + V ₁
26	0	1	1	0	1	0	V ₅ + V ₄ + V ₂
27	0	1	1	0	1	1	V ₅ + V ₄ + V ₂ + V ₁
28	0	1	1	1	0	0	V ₅ + V ₄ + V ₃
29	0	1	1	1	0	1	V ₅ + V ₄ + V ₃ + V ₁
30	0	1	1	1	1	0	V ₅ + V ₄ + V ₃ + V ₂
31	0	1	1	1	1	1	V ₅ + V ₄ + V ₃ + V ₂ + V ₁
32	1	0	0	0	0	0	V ₆
33	1	0	0	0	0	1	V ₆ + V ₁

Table 1. *Cont.*

STEP 1	S ₅	S ₆	S ₇	S ₈	S ₉	S ₁₀	Output (V ₀)
34	1	0	0	0	1	0	V ₆ + V ₂
35	1	0	0	0	1	1	V ₆ + V ₂ + V ₁
36	1	0	0	1	0	0	V ₆ + V ₃
37	1	0	0	1	0	1	V ₆ + V ₃ + V ₁
38	1	0	0	1	1	0	V ₆ + V ₃ + V ₂
39	1	0	0	1	1	1	V ₆ + V ₃ + V ₂ + V ₁
40	1	0	1	0	0	0	V ₆ + V ₄
41	1	0	1	0	0	1	V ₆ + V ₄ + V ₁
42	1	0	1	0	1	0	V ₆ + V ₄ + V ₂
43	1	0	1	0	1	1	V ₆ + V ₄ + V ₂ + V ₁
44	1	0	1	1	0	0	V ₆ + V ₄ + V ₃
45	1	0	1	1	0	1	V ₆ + V ₄ + V ₃ + V ₁
46	1	0	1	1	1	0	V ₆ + V ₄ + V ₃ + V ₂
47	1	0	1	1	1	1	V ₆ + V ₄ + V ₃ + V ₂ + V ₁
48	1	1	0	0	0	0	V ₆ + V ₅
49	1	1	0	0	0	1	V ₆ + V ₅ + V ₁
50	1	1	0	0	1	0	V ₆ + V ₅ + V ₂
51	1	1	0	0	1	1	V ₆ + V ₅ + V ₂ + V ₁
52	1	1	0	1	0	0	V ₆ + V ₅ + V ₃
53	1	1	0	1	0	1	V ₆ + V ₅ + V ₃ + V ₁
54	1	1	0	1	1	0	V ₆ + V ₅ + V ₃ + V ₂
55	1	1	0	1	1	1	V ₆ + V ₅ + V ₃ + V ₂ + V ₁
56	1	1	1	0	0	0	V ₆ + V ₅ + V ₄
57	1	1	1	0	0	1	V ₆ + V ₅ + V ₄ + V ₁
58	1	1	1	0	1	0	V ₆ + V ₅ + V ₄ + V ₂
59	1	1	1	0	1	1	V ₆ + V ₅ + V ₄ + V ₂ + V ₁
60	1	1	1	1	0	0	V ₆ + V ₅ + V ₄ + V ₃
61	1	1	1	1	0	1	V ₆ + V ₅ + V ₄ + V ₃ + V ₁
62	1	1	1	1	1	0	V ₆ + V ₅ + V ₄ + V ₃ + V ₂
63	1	1	1	1	1	1	V ₆ + V ₅ + V ₄ + V ₃ + V ₂ + V ₁

3.4. Voltage Stress Calculation for 127-Level Reduced Switch MLI

The values of the total voltage stress are: $V_{s1} = 325$ V, $V_{s2} = 325$ V, $V_{s3} = 325$ V, $V_{s4} = 325$ V, $V_{s5} = 165$ V, $V_{s6} = 82.5$ V, $V_{s7} = 41.25$ V, $V_{s8} = 20.625$ V, $V_{s9} = 10.3125$ V, $V_{s10} = 5.15625$ V.

3.5. Power Losses for 127-Level Reduced Switch MLI

Figure 1b shows the power losses waveforms of 127-level MLI.

4. Results and Discussion

The proposed configuration of the 127-level MLI has been designed and simulated in the MATLAB R2009a environment. The corresponding output voltages and the switching sequence of switches S₅ to S₁₀ are shown in Table 1. The switching pulses of 10-IGBT switches for one entire cycle are shown in Figure 2. The solar PV output voltage through the DC-DC converter is given to 10-IGBT switches S₁ to S₁₀ to achieve the desired 127 levels. The pulsating AC output voltage of the proposed configuration is shown in Figure 3 with THD.

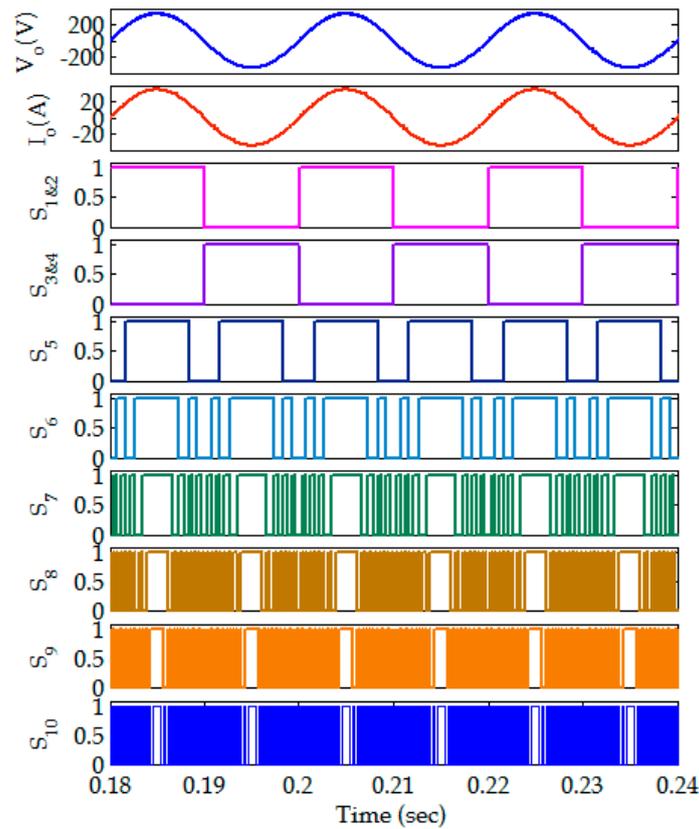


Figure 2. Output waveforms and switching pattern of reduced switch 127-level multilevel inverter.

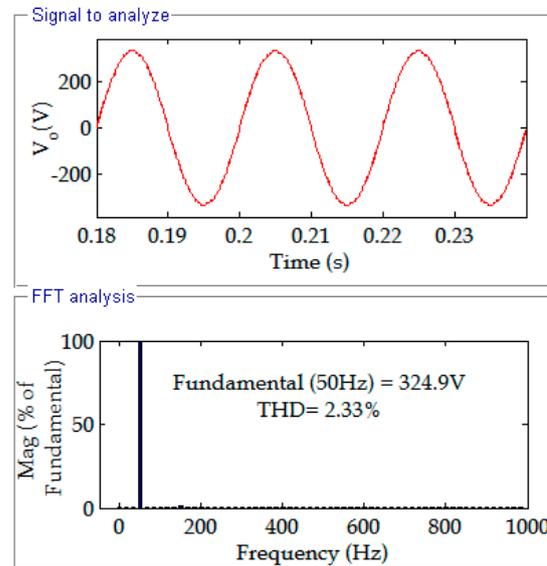


Figure 3. Harmonic spectra of 127-level MLI.

Figure 2 shows the output voltage of the inverter consisting of 127 levels, and for one complete cycle a frequency of 50 Hz is observed. For effective demonstration, the output resistive load is connected across it. The fundamental AC output voltage of the inverter and its % THD are shown in Figure 3, with a fundamental AC output voltage of 324.9 V and THD of 2.33%. These output voltages show harmonics in the output voltage of the inverter, which are well within the limits, according to IEEE-519 standards.

Figures 4–6 show the output voltages and switching pulses of the 15-level, 31-level and 63-level multilevel inverter, using seven, eight and nine IGBT switches, respectively.

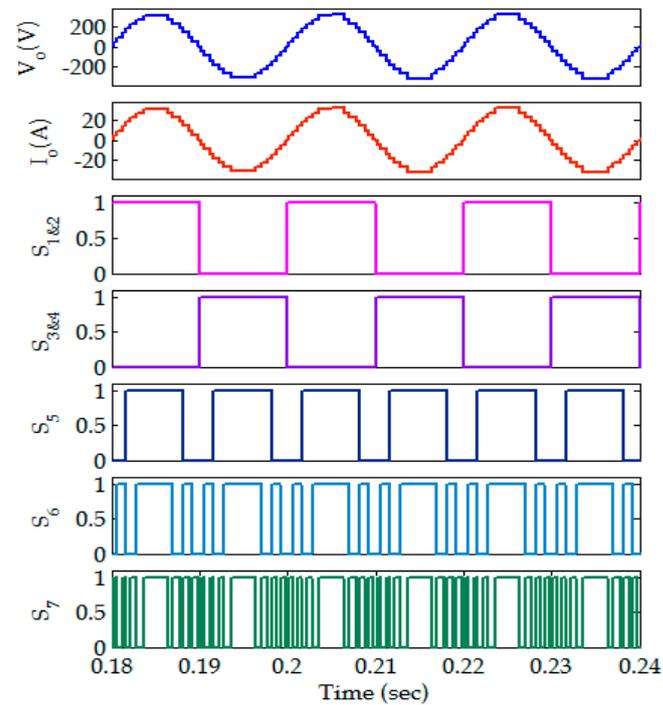


Figure 4. Output waveforms and switching pattern of reduced switch 15-level MLI.

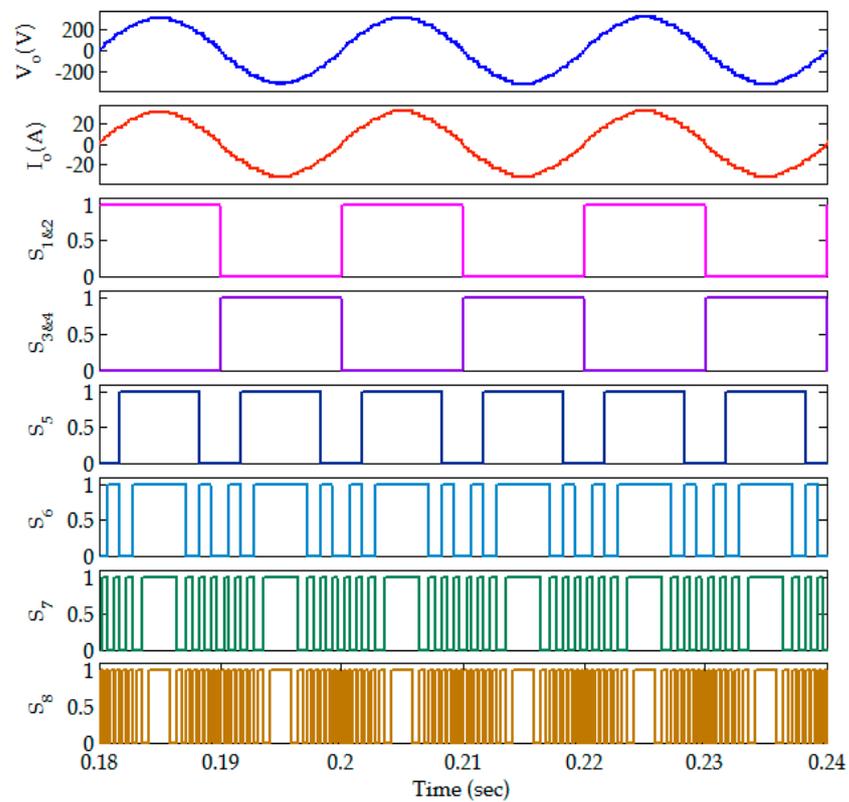


Figure 5. Output waveforms and switching pattern of reduced switch 31-level MLI.

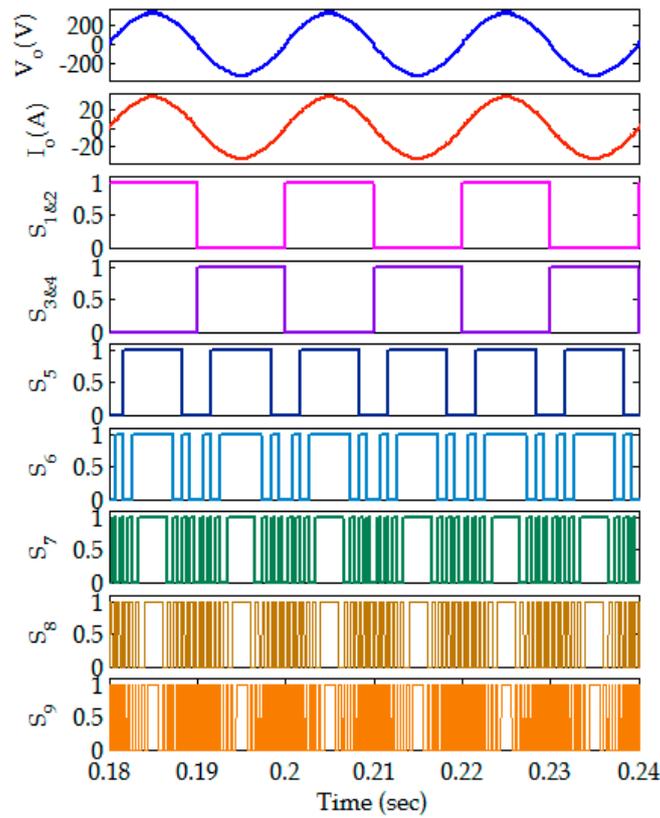


Figure 6. Output waveforms and switching pattern of reduced switch 63-level MLI.

The fundamental output voltage of the 127-level MLI is 324.9 V and the fundamental voltages of the 15-level, 31-level and 63-level are 323 V, 323.9 V, and 324.6 V, respectively.

Figures 7–9 shows the circuit diagram of the 15-level, 31-level and 63-level multilevel inverter, using seven, eight and nine IGBT switches, respectively.

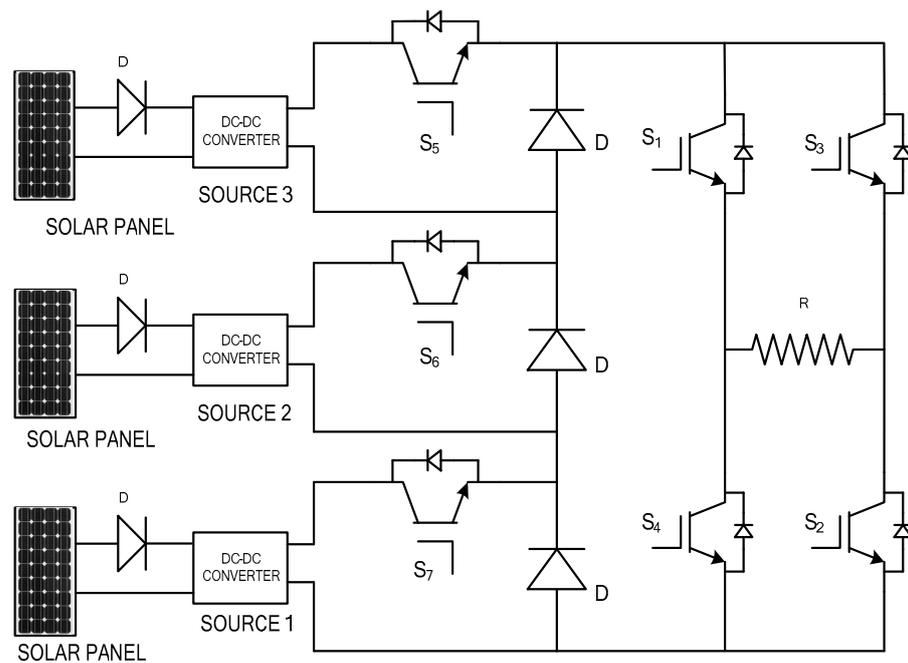


Figure 7. 15-level reduced switch multilevel inverter.

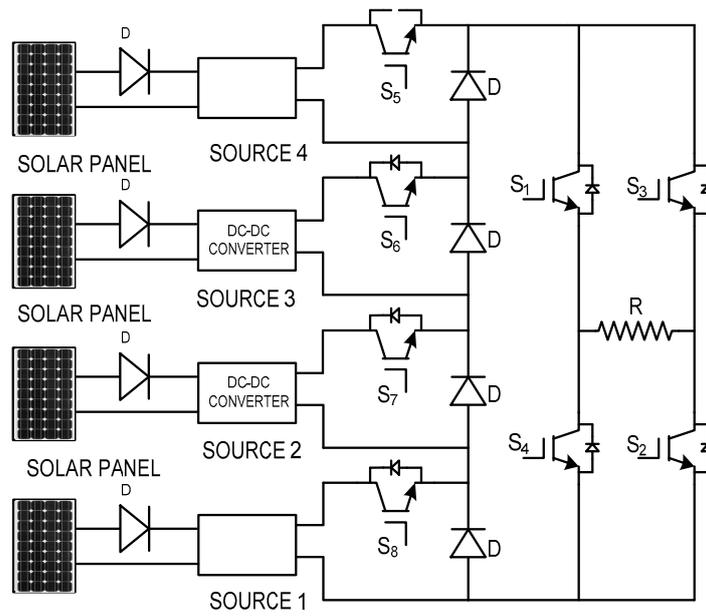


Figure 8. 31-level reduced switch multilevel inverter.

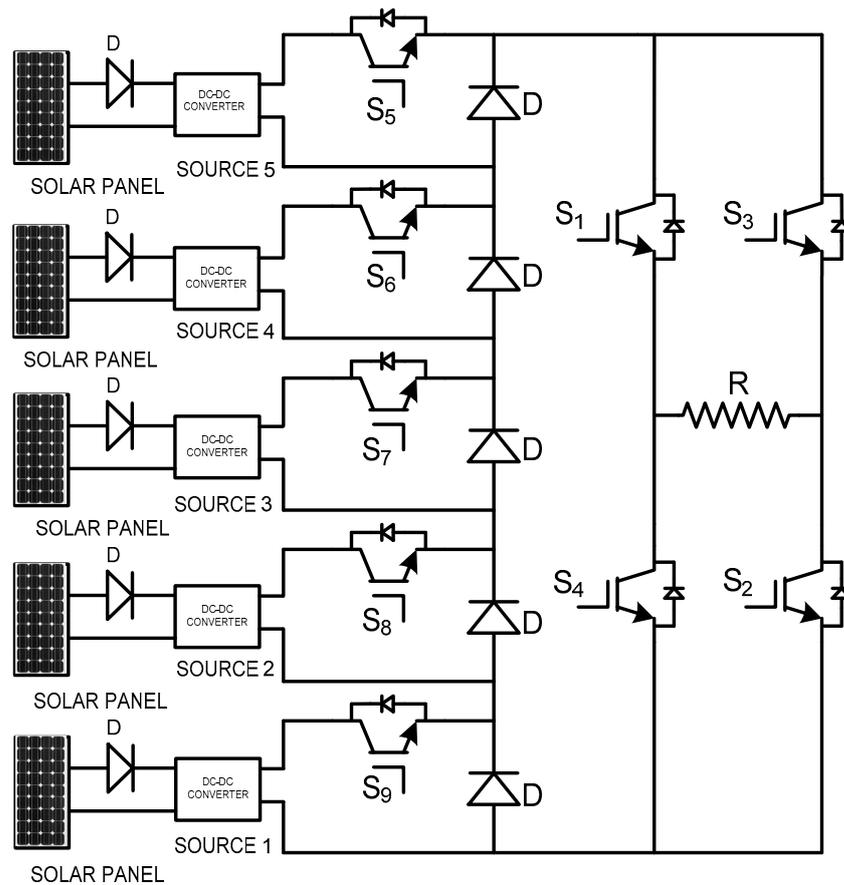


Figure 9. 63-level reduced switch multilevel inverter.

Figures 10–12 shows the harmonic spectra of the 15-level, 31-level, and 63-level MLI, respectively. The THDs of 15-level, 31-level and 63-level MLI are 5.72%, 3.84%, and 3.02%, respectively.

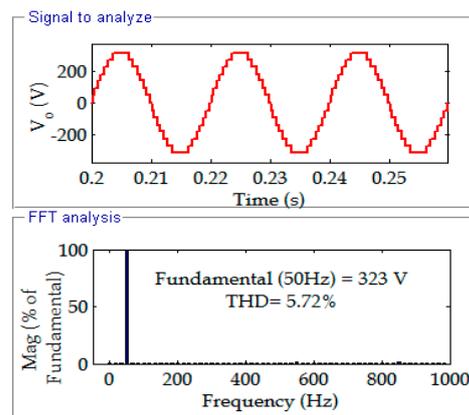


Figure 10. Harmonic spectra of 1-level MLI.

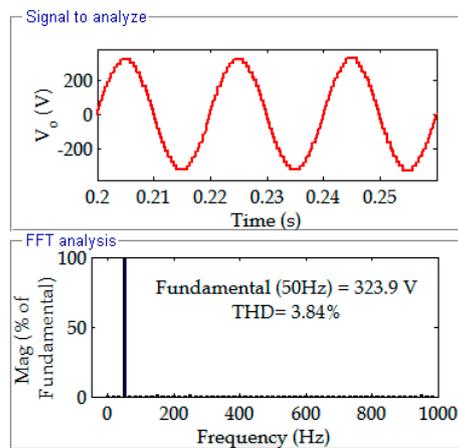


Figure 11. Harmonic spectra of 31-level MLI.

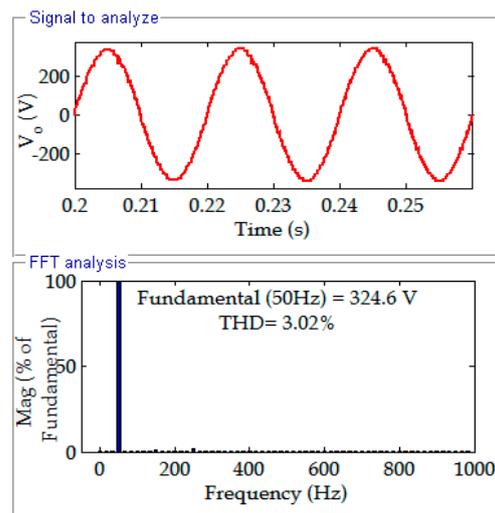


Figure 12. Harmonic spectra of 63-level MLI.

Comparison of the 127-level, 63-level, 31-level, and 15-level MLIs with regard to the number of IGBT Switches, number of diodes, number of voltage sources, fundamental voltage, % of THD and appended below in Table 2. Table 3 shows the comparison of convention MLIs to reduced switch MLIs.

Table 2. Comparison of various reduced switch MLIs.

No. of Levels	15	31	63	127	15
No. of IGBT Switches	07	08	09	10	07
No. of Diodes	03	04	05	06	03
No. of Voltage Sources	03	04	05	06	03
Fundamental Voltage	323 V	323.9 V	324.6 V	324.9 V	323 V
% of THD	5.72	3.84	3.02	2.33	5.72

Table 3. Comparison of conventional and reduced switch MLIs.

Topologies	NPC MLI	CHB MLI	FC MLI	SC MLI	Proposed Topology
Main switches	28	28	28	13	10
Main diodes	28	28	28	13	10
Clamping diodes	182	0	0	02	07
DC-sources	14	7	14	01	06
Flying capacitors	0	0	91	0	0
Gate driver circuits	28	28	28	13	10
Variety of DC sources	01	07	01	01	06 ($V_{dc1}, V_{dc2}, V_{dc3}, V_{dc4}, V_{dc5}, V_{dc6}$)
Maximum output voltage	V_{dc}	$7 \times V_{dc}$	V_{dc}	$6 \times V_{dc}$	$2 \times V_{dc6} - V_{dc1}$
Number of levels	15 Levels	15 Levels	15 Levels	13 Levels	127 Levels

5. Conclusions

The proposed configuration uses only ten switches to develop the reduced switch 127-level MLI. The proposed 127-level MLI is compared with the 15-level, 31-level, and 63-level MLI of similar configurations with regard to the number of IGBT switches, number of diodes, number of voltage sources, fundamental voltage, and percentage of THD. The proposed topology have been compared with the neutral point clamped (NPC) MLI, cascaded H bridge (CHB) MLI, flying capacitor (FC) MLI, switched capacitor (SC) MLI with the proposed topology with respect to the main switches, main diodes, clamping diodes, DC sources, flying capacitors, gate driver circuits, variety of DC sources, maximum output voltage, and number of levels. The proposed topology uses only ten switches to generate a near sine waveform with 127 levels. The harmonics are reduced very considerably, which reduces the distortion factor and total harmonic distortion (THD). The solar photovoltaic power generation with a DC-DC converter and battery acts as voltage sources for a reduced switch MLI and the proposed topology also reduces the voltage stress. The limitation of this topology is if one of the sources malfunctions, the effects the THD of output waveform is impacted. The configuration gives satisfactory results with the reduced number of switches when compared with a flying capacitor type MLI, cascaded H-bridge type MLI, diode clamped MLI and SC MLI. From the different types of MLIs discussed in this paper, it is clear that the 127-level MLI has less THD in the output waveform. Therefore, the output power quality is improved with reduced harmonics.

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