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Review

Heterogeneous Flight Management System (FMS) Design for Unmanned Aerial Vehicles (UAVs): Current Stages, Challenges, and Opportunities

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Abstract: In the Machine Learning (ML) era, faced with challenges, including exponential multi-sensor data, an increasing number of actuators, and data-intensive algorithms, the development of Unmanned Aerial Vehicles (UAVs) is standing on a new footing. In particular, the Flight Management System (FMS) plays an essential role in UAV design. However, the trade-offs between performance and SWaP-C (Size, Weight, Power, and Cost) and reliability–efficiency are challenging to determine for such a complex system. To address these issues, the identification of a successful approach to managing heterogeneity emerges as the critical question to be answered. This paper investigates Heterogeneous Computing (HC) integration in FMS in the UAV domain from academia to industry. The overview of cross-layer FMS design is firstly described from top–down in the abstraction layer to left–right in the figurative layer. In addition, the HC advantages from Light-ML, accelerated Federated Learning (FL), and hardware accelerators are highlighted. Accordingly, three distinct research focuses detailed with visual-guided landing, intelligent Fault Diagnosis and Detection (FDD), and controller-embeddable Power Electronics (PE) to distinctly illustrate advancements of the next-generation FMS design from sensing, and computing, to driving. Finally, recommendations for future research and opportunities are discussed. In summary, this article draws a road map that considers the heterogeneous advantages to conducting the Flight-Management-as-a-Service (FMaaS) platform for UAVs.

Keywords: heterogeneous computing; flight management system; UAV; SWaP-C

Citation: Wang, G.; Gu, C.; Li, J; Wang, J.; Chen, X.; Zhang, H. Heterogeneous Flight Management System (FMS) Design for Unmanned Aerial Vehicles (UAVs): Current Stages, Challenges, and Opportunities. *Drones* **2023**, *7*, 380. https://doi.org/10.3390/drones7060380

Academic Editor: Diego Gonzalez-Aguilera

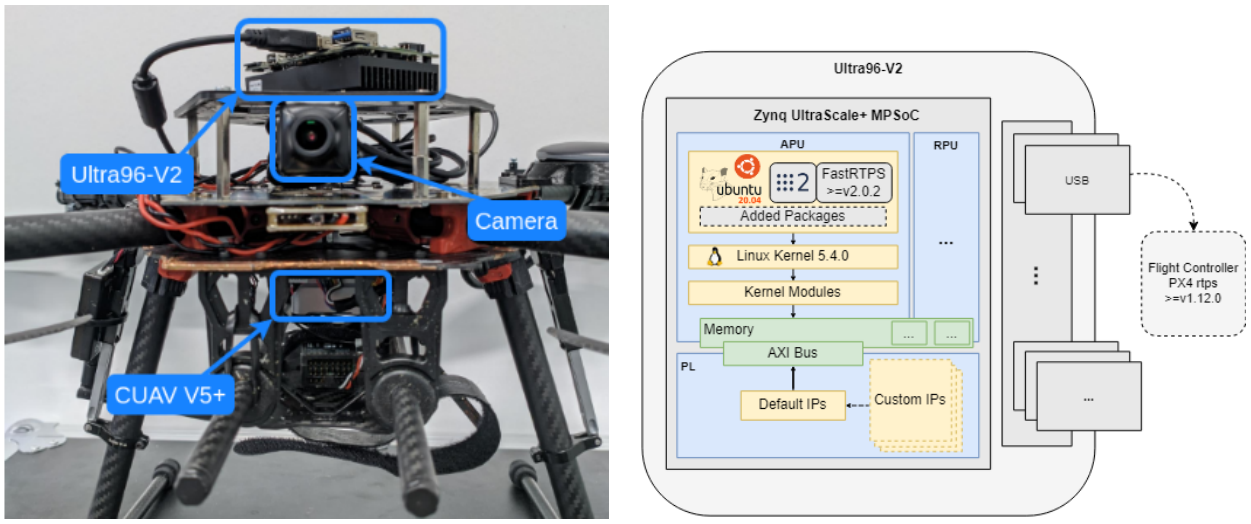
Received: 15 April 2023
Revised: 25 May 2023
Accepted: 2 June 2023
Published: 6 June 2023

1. Introduction

In recent years, the rapid development of data-driven ML and advances in information and communication technology (ICT) has brought more performance optimization possibilities to the modern computing platforms for UAVs [1,2]. Enabling the next generation of UAVs to process data from richer sensors and actuators and maximizing the performance with large-scale probabilistic ML models bears enormous potential [3]. However, the continuous proliferation of drones pose computing challenges, augmented by the higher performance necessities, big data-processing requirements, resource constraints, dynamic managing scenarios, and cyber-security concerns [4]. The greater the sophistication of the UAV, the greater the probability that a sub-system will fail [5]. Typically, the demand for higher computational speed [6], HC has attracted increasing attention from scholars to meet the real-time and power requirements and adaption of changing workloads of UAV [7]. The key technologies of heterogeneous computing can be categorized into architecture, programming languages, and the scheduling algorithm. In addition, as the

demand for computing power increases, many computing platforms are being accelerated by combining different computing units such as CPUs (Central Processing Units), GPUs (Graphics Processing Units), ASICs (Application-Specific Integrated Circuits), and FPGAs (Field Programmable Gate Arrays) [8].

To demonstrate how to meet the functional heterogeneous requirements of UAVs, the FMS architecture is considered as an example. FMS is the top-level architecture of the airborne subsystem among UAV avionic electronics [9]. The FMS of drones mainly includes flight plan management, integrated navigation, performance calculation, trajectory prediction, and flight guidance functions. In contrast to the Flight Control System (FCS), the FMS provides advances to improve flight safety and economy effectively. Figure 1 illustrates an exemplary comparison between FCS and FMS [10]. Generally, the FCS is deployed as the primary component for UAV control, such as CUAV V5+ in Figure 1a and Flight Controller PX4 in Figure 1b. Meanwhile, the FMS is implemented in Ultra96-V2 as an extra service.



(**a**) Drone platform (**b**) System diagram

Figure 1. Comparison between FCS and FMS [10].

Since the FCS is the basic platform for UAV, an in-depth study on isolated FMS rather than FCS could lead to lower research expenses, although prior experiments have failed to achieve this outcome. Nevertheless, the design of high-reliable heterogeneous FMS depends on many constraints, such as the requirements of being real-time, low-cost, low-power, high-performance, and minimal risk [11]. Another critical factor in the designing phase is the consideration of SWaP-C, which is an acronym for Size, Weight, Power, and Cost. Accomplishing even one or two criteria can be motivating enough to recommend or request a promising system design. However, it is always ideal to achieve progress in all four areas [12]. More specifically, as Figure 2 depicts, the trade-off between programmability and energy efficiency based on different hardware platforms is challenging to determine.

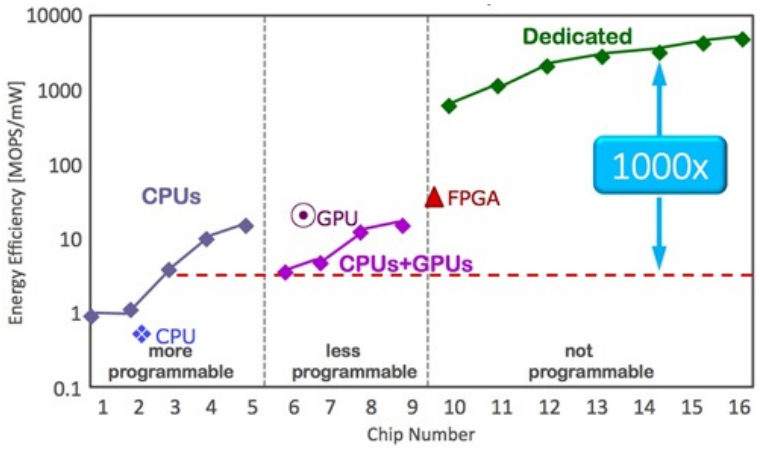


Figure 2. Programmability vs. Energy Efficiency [13].

A considerable amount of literature has been published on reliable computing platforms. Ahmed et al. [2] used a survey to assess the various computing platforms and the hardware reliability issues of UAVs. Bithas et al. [14] reviewed 5G and wireless communication integration in UAV-based networks for heterogeneous environments. Furthermore, the FPGA-based aerial robotic accelerators are surveyed in [15]. Moreover, the fault diagnosis and fault tolerant control for UAVs to avoid catastrophic Crazyflies are comprehensively discussed in [16]. Recently, power semiconductor devices have been expansively applied to enhance system robustness with the following constraints: fully controllable, higher switching speed, embedded capability, and low conduction loss [17,18]. In addition, to satisfy the safety-critical scenarios, the need for investigation via artificial intelligence solutions is of high significance to manage the increasing calculation resources [19]. Further, when focusing on deep learning, the parallel and optimization technologies of neural networks based on HC have attracted increasing attention [8]. Several scholars have shown promising results by combining hardware accelerators for ML applications [20].

To date, however, there needs to be more discussions held around a comprehensive overview of heterogeneous FMS design. Although Infrastructure-as-a-Service (IaaS) platforms could compactly provide valuable features, including hardware abstraction, resource allocation, and energy-aware workflow architecture to enable the remote management of applications, commercial UAVs, on the other hand, usually provide a limited software environment [21,22]. Therefore, by proposing a design road map of heterogeneous FMS for high-reliable UAVs in different levels and cross-layers, this article aims to replicate the specialized convenience and comfort of IaaS platforms by achieving the Flight-Management-as-a-Service (FMaaS) platform as a final product for drones. To sum up, the contributions of this article are as follows:

1. To the best of our knowledge, this represents the first time in the literature that the design road map of heterogeneous FMS for high-reliable UAVs is systematically proposed in different levels and cross-layers abstractly and figuratively.
2. The implications and novelties of acceleration possibilities in data-, model-, and hardware levels for pursuing heterogeneity management are comprehensively surveyed.
3. The advantages and limitations of the tools mentioned above are investigated. Several exemplary applications are provided, where the challenges and future trends are discussed in detail.

In this paper, we discuss the UAV FMS design's current status and future directions, focusing on heterogeneous computing. The structure of this survey is displayed in Figure 3. After the introduction, the cross-layer design stack of FMS for UAVs is described in Section 2. In Section 3, the essential and novel tools for the implication of heterogeneous FMS with ML and hardware accelerators are discussed. Section 4 provides three research hot-spot examples for FMS with comparisons and discussions: vision-based landing, fault

diagnosis, and embedded control system. In Section 5, challenges and open opportunities are proposed. Lastly, concluding remarks are provided in Section 6.

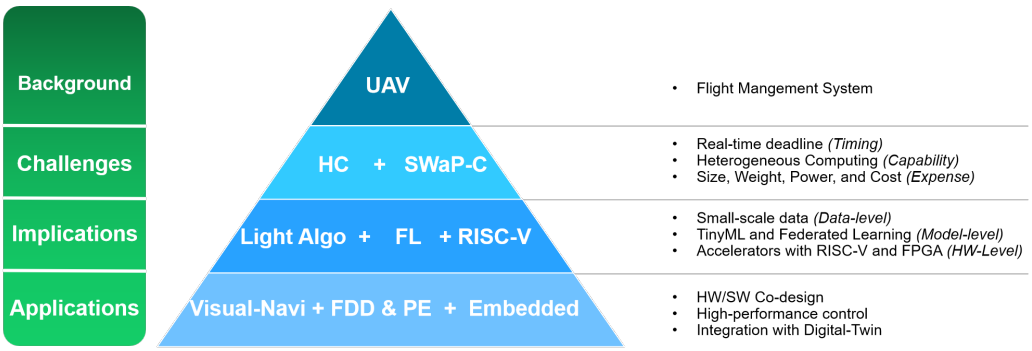


Figure 3. Structure of the survey.

2. Loop Cycle of UAV FMS Design

It is essential to explore how these different chips can be arranged differently to meet UAV domain requirements and increase the FMS's potential. Therefore, in order to identify the advances of heterogeneity for FMS, in this section, the loop cycle of UAV design is proposed from the abstract layer to the figurative layer.

2.1. Abstraction Layer

Wan et al. [4] reviewed the literature from the period and traversed down Figure 4 to explain robotic-specific computing. The general robot design algorithms can be divided into perception, localization and mapping, decision-making and control, Artificial Intelligence (AI), and cloud computing. At the system level, to match the entire operating system and reduce development effort, Xilinx [23] provides several tools for developers to accelerate cross-platform coding, especially for Robot Operating System (ROS), Linux, and Petalinux. Meanwhile, as for the heterogeneous System on Chips (SoC) layer, the different combinations of chips are highlighted with CPUs, GPUs, FPGAs, ASICs, and the recent hot-spot AI chip.

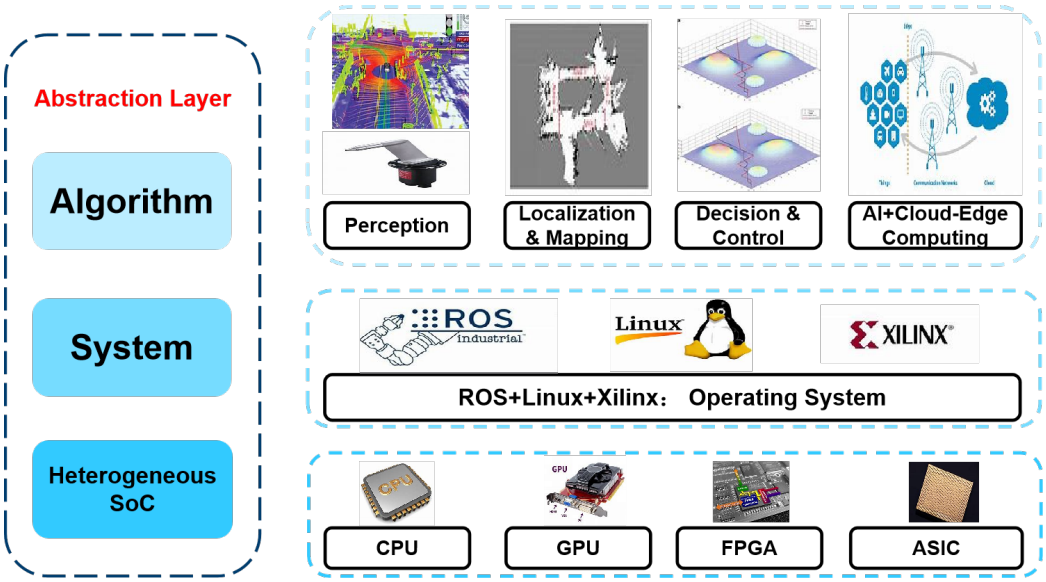


Figure 4. Abstraction layer of robotic computing systems (inspired by [4]).

2.2. Figurative Layer

Typically, three subsystems comprise the main components of a UAV system: actuators, primary structure, and sensors [16]. Moreover, when the SoC selection differences and

the arithmetic power increase, the high-performance possibility exists for a corresponding multi-sensor multi-actuator development UAV model. Figure 5 depicts the figurative layer design approach from the sensor side on the left to the actuator side on the right. Based on [24], the Multiple-Input Multiple-Output (MIMO) model at the top is a typical model for aerial robot design, where u represents the sensor input, $G(s)$ is the calculated and described model, and y represents the actuator output. However, with the increasing number of sensors such as cameras, Inertial Measurement Units (IMUs), and Global Position Systems (GPS) being supplied, decoupling $G(s)$ and deploying the model in a heterogeneous SoC has evolved into a new challenge. The diagram in the middle depicts a typical control model of how the control equation $K(s)$ can be developed so that the errors $e1$ and $e2$ are minimized to achieve accurate and robust control of multiple outputs y. Based on these, the block diagram of the figurative layer is described at the bottom.

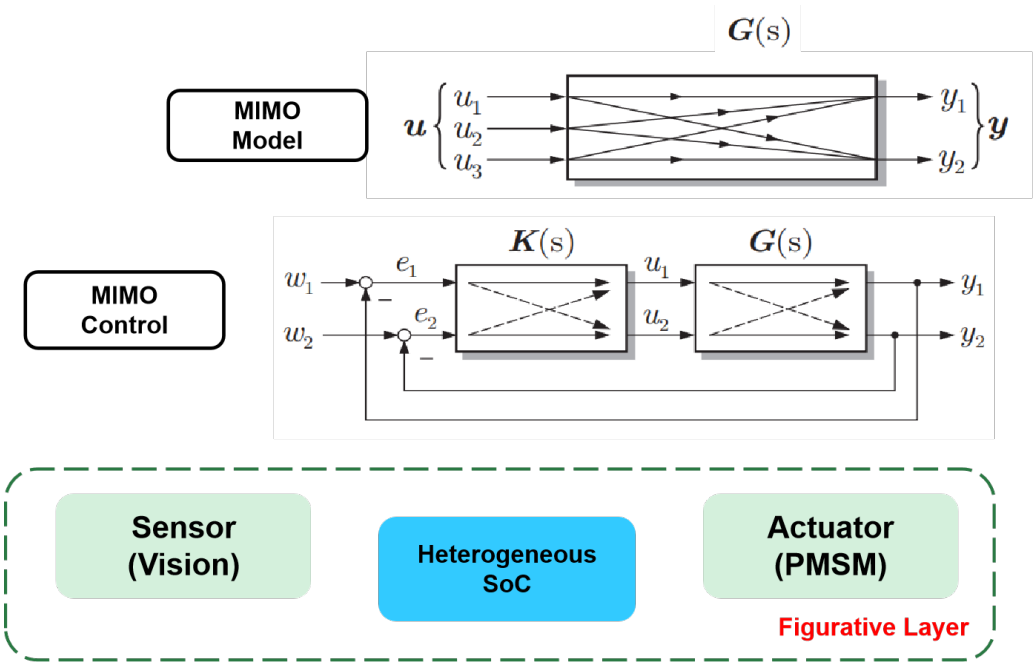


Figure 5. Figurative layer of MIMO system (inspired by [24]).

In complex control systems such as modern FMS, the versatility of implementing control laws has brought many opportunities [7], since place recognition is a crucial ability for real-time UAV tasks to perform long-term Simultaneous Localization. Furthermore, Mapping (SLAM) [25], vision sensors are treated as the instance of the sensor side. On the other side, the real-time implementation of the controller presents a challenging task [26]. To further illustrate the notion of heterogeneity, the synergistic development of Permanent-Magnet Synchronous Motor (PMSM) and heterogeneous SoCs as an example of the actuator side is focused on.

2.3. Cross Layer and Loop Cycle

To explore methods that ensure high efficiency, real-time security, reconfigurability, and predictability of heterogeneous SoCs at low cost, we have integrated the abstraction and figurative layers together, as shown in Figure 6. It builds a loop closure for the next generation of FMS. Firstly, as the number of sensors and actuators increases in this cycle, the required computational resources and control accuracy grow. Secondly, as computing power rises, the traditional development model is revolutionized. Thus, advanced sensors and actuators can be applied to assemble a positive cycle. Finally, the value of heterogeneous FMS can be demonstrated implicitly through its power consumption, throughput, and other metrics.

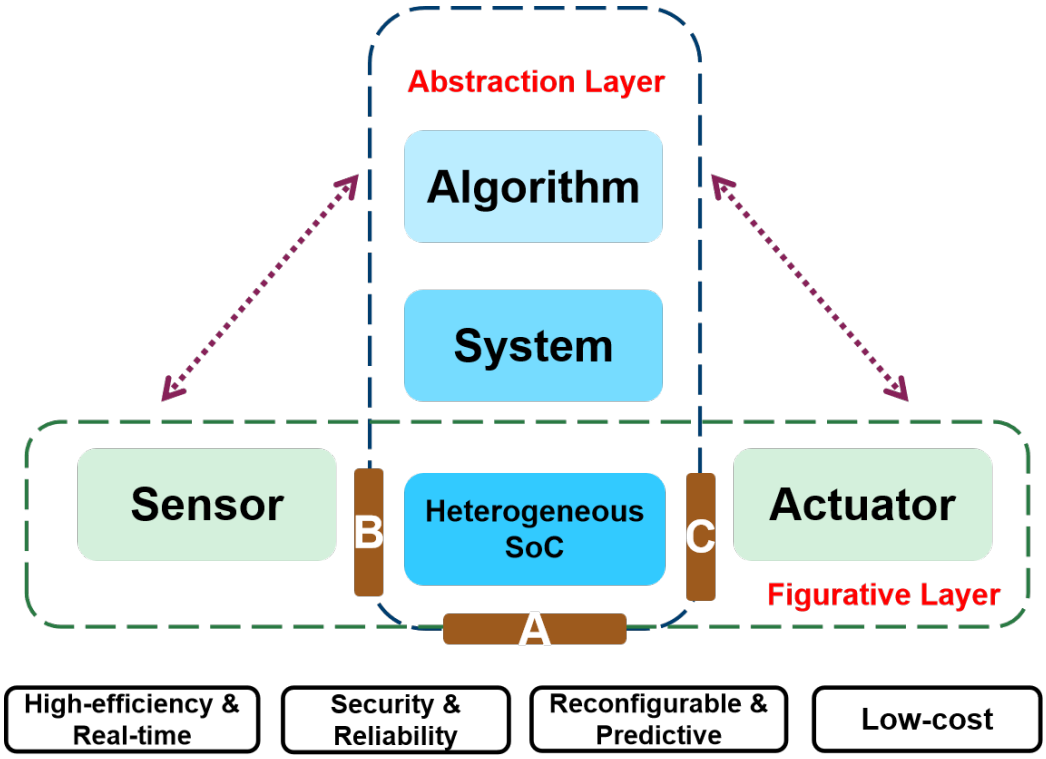


Figure 6. Cross layers as a loop-closure for heterogenous FMS design.

The following three directions and corresponding key technologies [27] are summarized in detail in Sections 3 and 4:

- Direction A: Challenges for heterogeneous SoC design for FMS with function "evaluation and decision."
- Direction B: Joint development of smart sensors and heterogeneous FMS with function "perception and monitoring."
- Direction C: Cooperated development of actuators and heterogeneous FMS with function "implementation and disposal."

3. Acceleration Methods

3.1. Light-Weight ML

Recent trends in ML have led to a proliferation of studies by integrating Deep Learning (DL) techniques with fault diagnosis and detection. Though ML has shown convincing performance in data-intensive applications [28], in practice, it is often hard and expensive to collect enough large-scale and independent and identically distributed (IDD) data [29]. Few-shot Learning (FSL) and Transfer Learning (TL) are of particular concern. FSL is utilized to address the issue of learning the underlying pattern in the data only from a few training samples [30]. Furthermore, in TL, the learner performs on target domains by transferring the knowledge obtained from different but related source domains [31]. By reusing the knowledge maintained from the source task, the performance of the target task could be significantly improved [32]. The task and mapping are the same in the related Domain Adaption (DA) case, while the input distribution is differs slightly [33]. The significant advantages of DA can be illustrated in Figure 7. Small-scale data training could decrease algorithm complexity and accelerate heterogeneous computing.

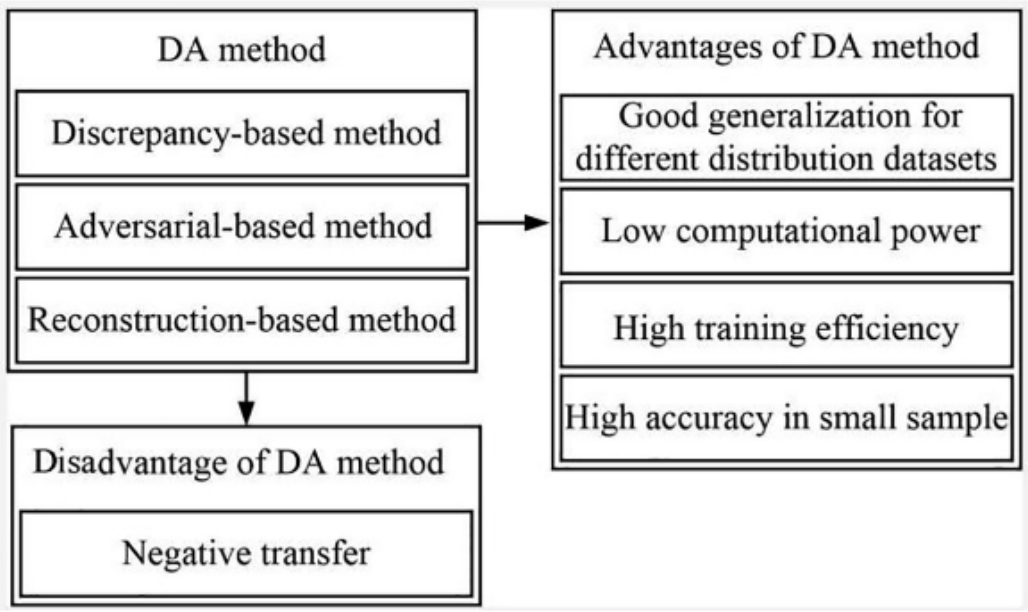


Figure 7. Advantages and disadvantages of DA [32].

Another essential tool for computational- and data-light ML on FMS is TinyML [34]. By enacting inference on-device or near-sensor, TinyML could enable remarkable responsiveness and revolutionize the real-time collection of data [35]. Liu et al. [36] proposed a TinyML framework for the Remaining Useful Life (RUL) to meet the real-time deadline efficiently. Islam et al. [37] envisioned a drone-based data processing framework with TinyML to secure a real-time heterogeneous management system. Furthermore, Liu et al. [38] presented a TinyML approach for hardware-efficient channel assessment and signal detection. The opportunity to locally execute the ML models on tiny devices has pushed research with more adaptable and configurable methodologies, as described in Table 1.

Table 1. Recent advanced integration possibilities with TinyML.

References	Challenges	Methods	Implications
[39]	TinyMLaaS	ML-as-a-Service	Energy saving
[40]	TinyOL	Online-Learning	On-device training
[41]	Tiny-MLOps	ML Operations	Extreme environments suitability
[42]	MCU	RISC-V	Computational cost optimization
[43]	TinyFedTL	FL and TL	Open-source

3.2. Federated Learning Acceleration

The end of Moore's Law is pushing ML to shift from cloud to edge [44], especially in the next-generation FMS system. Enabling ways to overcome the challenges of data silos and data sensibility, the collaboratively decentralized privacy-preserving paradigm known as Federated Learning (FL) has attracted particular concern among researchers for UAV-based authentication recently [45,46]. The core FL problem involves learning a single global statistical model from data stored on numerous devices. In addition to not only solving the privacy problem, the system and statistical heterogeneities are also a critical research direction for the FL technology to handle asynchronous communication and fault tolerance [47]. Typically, the goal of FL is to minimize the objective function by Equation (1):

$$\min_{w} F(w), \text{ where } F(w) := \sum_{k=1}^{m} p_k F_k(w). \tag{1}$$

Here, m is the total number of appliances, $p_k \geq 0$ and $\sum_k p_k = 1$, and F_k is the local objective function for the kth appliance [47]. Similar to the efforts to move toward the Internet of Things (IoT) with the Edge Computing (EC) environment [48], the next-generation of FMS could also benefit beyond the journey from centralized to distributed ML such as FL [49], especially for condition monitoring [50] and real-time updates for fault diagnosis [51].

However, when deploying FL on resource-constrained heterogeneous devices, the weak computation abilities may cause unexpected straggler problems [52]. Therefore, a considerable amount of literature has been published on FL acceleration [53]. These studies mainly focus on optimization by altering the steps or functions in the ML model. For example, Jin et al. [54] presented novel adaptive optimization methods for FL by considering the dynamics of Ordinary Differential Equations (ODEs). Liu et al. [55] accelerated the FL framework by considering Momentum Gradient Descent (MGD) in the local update part of the FL system, especially during the last iteration. Ozfatura et al. [56] proposed FedADC to accelerate the FL algorithm with drift control. In [57], the acceleration possibility with alleviated forgetting in local training is evaluated in-depth. Moreover, Wang et al. [58] have paid attention to considering cluster construction and hierarchical aggregation. Their efficient FL mechanism, referred to as FedCH, showed promising results by reducing the completion time and network traffic by more than 50%.

Similarly, Hanzely et al. [59] also focused on the local Stochastic Gradient Descent (SGD) methods by establishing the first lower bounds for optimization. On the other hand, Xu et al. [60] proposed a new paradigm, namely FL-PQSU, by addressing the issue with pruning, quantization, and selective updating. Furthermore, when pursuing the system-level solutions, Lee et al. [61] proposed a novel FL framework for resource allocation with multiple systems. They accelerated the learning speed by aggregating the policy at each system into a central policy. At the same time, by using the central policy, network adaptability is assured. Li et al. [62] presented SmartPC, a hierarchical online pace control framework for FL, which pursued meeting the balance between SWaP-C and real-time constraints with promising results.

In the fault diagnosis domain, Zhao et al. [63] first presented an application of FL on power electronics among scholars. They integrated the FL-based framework for detecting a series of different False Data Injection (FDI) attacks on dc/dc and dc/ac converters in photovoltaic (PV) systems. Their experimental results demonstrated significant efficiency and performance improvements over the standard ML paradigm in preserving data privacy. In addition, they identified possibilities for improvement and refinement via adopting the TinyML concept (mentioned in Section 3.1) on low-energy systems, which strongly supports our opinion. In [64], Lin et al. proposed an FL-channel attention-based Convolutional Neural Network (CA-CNN) to extrapolate the transformer fault type. It can extract hidden layers and weights from the Dissolved Gas Analysis (DGA) data and improve each client's performance against communication noises. In conclusion, exploiting FL on the FDD of modern FMS is a worthwhile pursuit. In summary, the research on resource-friendly combinations of TinyML and FL, such as TinyFedTL [43], ensures valuable data protection and security guarantees for the next generation of heterogeneous FMS.

3.3. Hardware Accelerators with FPGA and RISC-V

Why FPGA? Reconfigurable computing presents a potential paradigm that has been effectively performing primarily in developing devices with Field Programmable Gate Arrays (FPGAs). FPGA reconfigurable hardware is designed to handle latency-critical tasks while being energy efficient due to the ability to parallelize computations massively [65]. This places FPGAs as the next candidate for autonomous drone design. In addition, while GPUs excel at parallel processing, FPGAs perform integrated AI and provide several advantages with low latency, high throughput, excellent flexibility, affordable cost, and low-power consumption [66]. Furthermore, it is suitable for TinyML-based acceleration on FPGA in terms of Processing-in-Memory (PIM) architecture [67]. However, working

with FPGAs requires a deep understanding of hardware logic, creating a barrier to their adoption in aerial robotic communities [10].

Why RISC-V? Modern microprocessors are the fundamental component of providing solutions for the most complex systems applications. The instructions supported by a particular processor and their byte-level encodings are defined as Instruction Set Architecture (ISA) [68]. The RISC-V expresses a fallback solution for untreated corner cases [69]. Investigating Open-Source Hardware (OSH) and contributing to designing hardware-based accelerators with ML represent enduring concerns within such a high-reliable embedded ecosystem [70]. In addition, researchers have adopted the Reduced Instruction-Set Computer-five (RISC-V) open standard architecture worldwide. Recently, especially after the COVID-19 epidemic, the open RISC-V ISA has gained enormous popularity in the avionic power electronics and fault tolerance domain [71]. For achieving energy efficiency, open-source tools, such as the RISC-V ISA, have been introduced to optimize every internal stage of the system [72]. Figure 8 illustrates the similarity of the development cycle between RISC-V Vector operation and AI operation, which leads to the possibilities for ML acceleration.

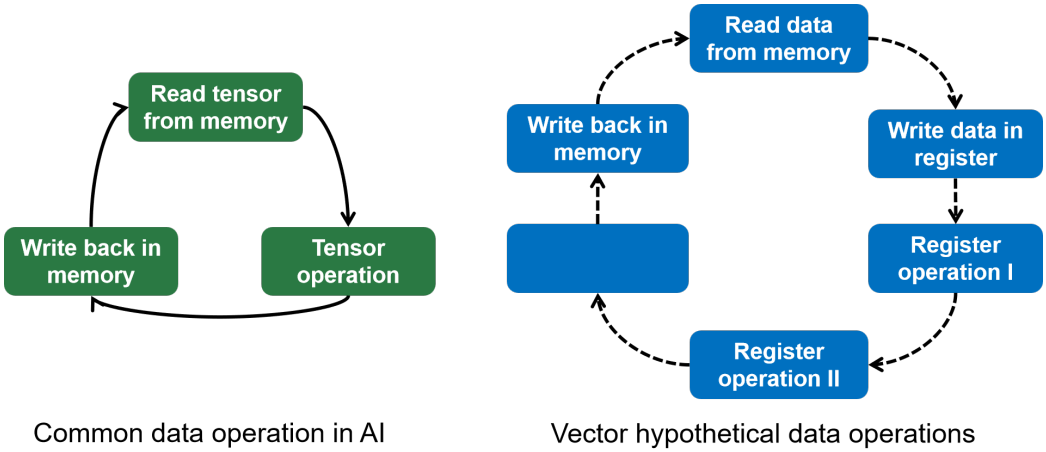


Figure 8. Similarity of the development cycle between RISC-V Vector operation and AI operation.

In China, the performance observed of the latest XT-910 chips convinced the RISC-V community that, *(I)* the RISC-V embedded MCUs satisfy low-cost, low-power, and high-performance computing requirements. *(II)* For AI- and data-centered applications, the RISC-V vector extension works well to meet acceleration expectations. *(III)* Academic and industry researchers could benefit significantly from the flexibility and customizability of RISC-V in the post-Moore's Law era [73]. In the U.S., lately, a full-stack open-source framework for TinyML acceleration on FPGAs and RISC-V was proposed by Prakash et al. [74] as a promising example. In Europe, the group led by Prof. Luca Benini presented a series of RISC-V-based accelerator tools from an open-source simulator (GVSoC) [75] for the Parallel Ultra-Low Power (PULP) architectures, an open hardware platform for always-on wearable smart skin [76], and in-network accelerator for flexible packet processing on streaming Processing in the Network (sPiN) [77].

4. Research Focuses

It has previously been observed that the heterogeneous capability to address complex and reliable performance has become a key enabler of further developments in FMS. Furthermore, the following cases from the theory and applications in [7] will demonstrate the results: the visual-guided landing of UAVs, intelligent Fault Detection and Diagnosis (FDD), and controller-embeddable PE. Furthermore, the exemplary applications correspond with the goal of typical system design, just as the motto of the Olympic Games: "Faster, Higher, Stronger" [78]. First, the visual-guided landing represents the "Faster" for real-time

responses. Second, the PE usage expresses the "Higher" for higher frequency in controlling. Third, the fault diagnosis symbolizes the "Stronger" for robust and stable system [79].

4.1. Visual-Guided Landing

With the rapid development of UAVs, the issue of visual-guided landing has received considerable critical attention [80], especially based on ML methodology such as Reinforcement Learning (RL) [81] and different neural network architectures [82,83]. In addition, in order to obtain the smooth flying progress of UAVs, SLAM technology has attracted plenty of attention among scholars [84]. However, the requirements for real-time massive information processing and limited onboard resources have brought difficulties for achieving high-performance [85]. When considering typical sensors, the Time-of-Flight (ToF) camera and Lidar (Light Detection and Ranging) are the most widely used modern sensors to obtain 3D information [86]. With a collection of data points maintaining depth images, the 3D point clouds could be generated to help the UAV understand the surroundings without sensor drift [87]. The typical approaches to maintain the visual-guided landing based on the ToF camera and Lidar are summarized in Table 2.

Table 2. ToF and Lidar utilization.

Sensor	References	Method	Application
ToF	[88]	Data fusion based on a ToF, IMU, and an optical flow sensor	Adaptive landing
	[89]	Hybrid combination of spread spectrum ultrasound and ToF	Indoor landing experiment
	[90]	A top-view ToF with adaptive matched filtering	GPS-denied environment
	[91]	Black-box and PID controller integration	Distinctive landing symbol detection
Lidar	[92]	Safe Landing Zone (SLZ) identification	Landing zone for helicopters
	[93]	Dual-channel with multi-pulse laser echo accumulation and the physical phenomenon with laser reflectivity	Landing system for ships at sea
	[94]	Point cloud progressing with Principal Component Analysis (PCA) and PROgressive SAmple Consensus (PROSAC) algorithms	Safe landing site selection
	[95]	On-board terrain hazard detection and avoidance (DAA)	Safety area identification

Integrating ML algorithms, in [96], Navardi et al. presented an approach named E2EdgeAI for energy-efficient Edge computing that harnesses the benefit of AI for tiny autonomous drones. This approach optimized the energy efficiency of DNNs by assessing the effects of memory access and core utilization on the power consumption of tiny UAVs. Their experiments showed promising results with a model size of up to 14.4×, improved energy per inference by 78%, and raised energy efficiency by 5.6×. Liu et al. [97] presented an integrated system for a UAV landing on a moving platform. The UAV could track the object dynamically in a complicated environment. In [98], Palossi et al. demonstrated a navigation engine for autonomous nano-drones endowed with end-to-end DNN-based visual navigation based on a novel parallel ultra-low-power computing platform. In [99], Albanese et al. presented a modular system with landing pad detection and facial recognition ML algorithms on a resource-constrained UAV in real-time.

In particular, to meet Real-Time (RT) deadlines, in [100], Delgado et al. achieved an RT control system based on Xenomai, an RT-embedded Linux, to overcome issues concerning the communication interface between RT and NRT (Non-Real-Time) tasks. In [101], the improved RT visual servo system is also combined with Xenomai. In [102], aiming at the requirements of multi-channel, low-power consumption, and small volume for receiver extension of ornaments of multichannel, low-power consumption of the system, a multi-channel signal acquisition and storage system based on FPGA and STM32 with a heterogeneous system of working channels and the sampling frequency is designed. In [25], their experiments were achieved on three large-scale data sets. They demonstrated an approach compared to the state-of-the-art methods concerning the recall rate of place recognition and pose estimation accuracy with significant advances.

In summary, though there are massive amounts of visual information and data required, the real-time landing could be realized with simpler algorithms and more powerful FMS.

4.2. Intelligent Fault Diagnosis and Detection

The concept of PMSM drive design is central to high-reliable FMS. In particular, it has attracted more attention from scholars in the aerospace domain for safety-critical applications [103]. The complicated control method requires high computational resources to avoid catastrophic performance during flight. One possibility is to utilize hardware accelerators such as Field Programmable Gate Array (FPGA) instead of Digital Signal Processors (DSP). Typically, several accelerators for CNN have been proposed based on FPGA owing to its high performance and reconfigurability [104].

To enable deep learning inference on RISC-V, Kong et al. [105] compared the performance of the DL interface on RISC-V and on $\times$86. For the vision of "AI on RISC-V", they implemented the ResNet-20 [106] deep neural network on three different platforms: Xilinx PYNQ Z2 FPGA based on RISC-V (50 MHz, one core), RISCV-QEMU, and an $\times$86 server. Furthermore, CIFAR-10 dataset [107] is utilized for modeling, which consists of 60,000 color images and corresponding labels. They contributed to reducing the development cycle of deep learning inference applications targeting RISC-V by cross-compilation. In [108], a configurable RVV-based (RISC-V Vector) Arrow accelerator architecture is proposed and evaluated for edge machine learning. Integrated with a subset of the RVV v0.9 ISA extension, a configurable vector co-processor known as Arrow was achieved. Their experiment demonstrated a faster (2–78$\times$ increase in speed) but lower-energy-consuming (20–99% less) benchmark result using a Xilinx board. Another RISC-V acceleration possibility of the ML algorithm is proposed in [109]. They exploited Data-Level Parallelism (DLP) to improve the controller's performance in two ways: execution of the same instruction and segmenting of large vectors. Their experiments were based on three platforms with 1.298 W at a maximum frequency of 50 MHz and 0.813 W, with a max frequency of 100 MHz. Similar to [105], ResNet-50 [106] serves as the ML benchmark. Their promising work gave significant improvements when the processor ran up to 100 MHz. In addition, the simultaneous-switching switched-capacitor dc/dc converters were also tightly integrated with an adaptive clock generator. An Adaptive Voltage Scaling (AVS) algorithm was proposed to track changes in the program phase, allowing for consistent energy consumption. Their prototype showed a bright future for energy-efficient mobile SoC design.

In [110], Richter et al. presented an RISC-V-based microprocessor for higher computational capability and efficient dc/dc converters. Their research modified the most critical features of the SoC to increase their reliability and error resilience. Benefiting from the RISC-V architecture instead of traditional Complex Instruction Set Computer (CISC), the processor was proposed to react to threshold violations on measurement inputs of 40 MHz. Their processor accomplished a benchmark score of 2.03 CoreMark per MHz. Towards safer features and characteristics, the coupling of heterogeneous SoC with multi-phase synchronization will be addressed in their future work. Such integration work based on RISC-V Vector processors and dc/dc converters has shown great potential in low-cost

devices [111]. An example of the SoC layout with the integration of RISC-V and PWM units is shown in Figure 9.

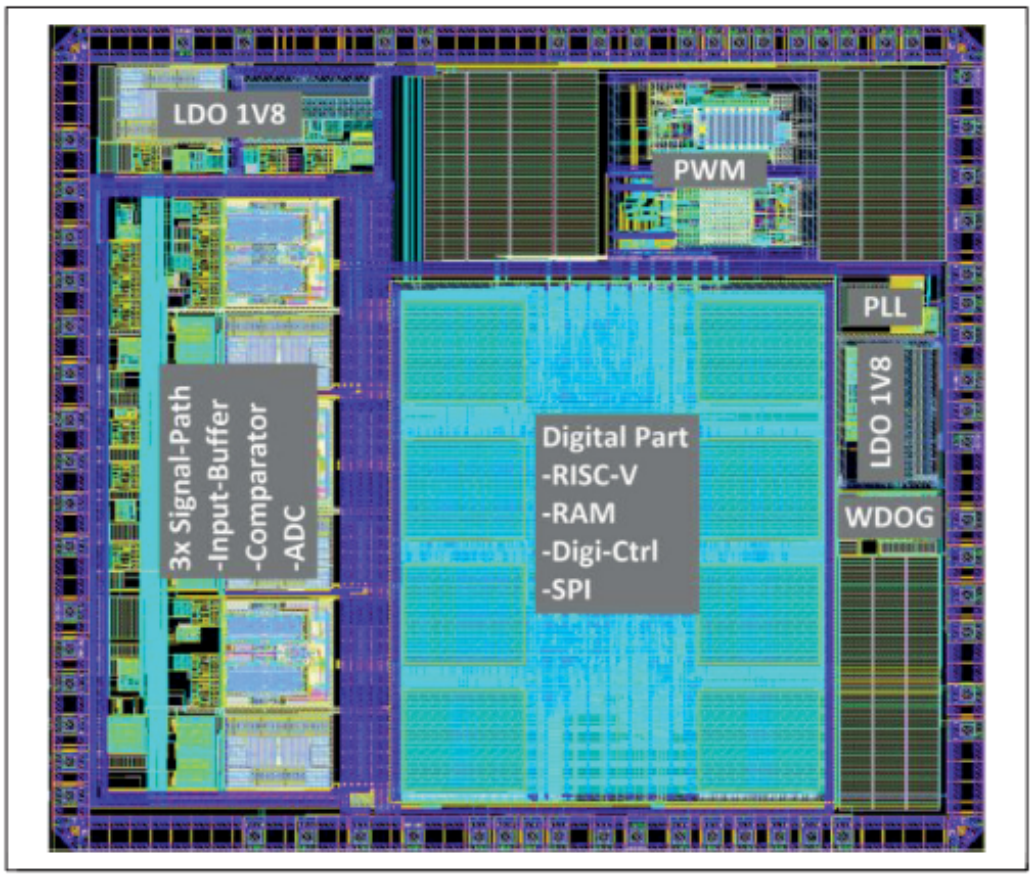


Figure 9. SoC layout with RSIC-V architecture [110].

To sum up, the main constraints for utilizing AI and hardware accelerators for rotating machinery fault detection and diagnosis are listed. Furthermore, parallel computing also plays an essential role by simultaneously carrying out many calculations or processes.

4.3. Controller-Embeddable Power Electronics

Embedded control and drive systems are faced with the exponential complexity of the algorithm. The utilization of FPGA for generating different types of PWM for power electronics applications has earned increased attention steadily over the last few years [112]. In [113], a codesign workflow and a runtime architecture for the heterogeneous deployment of multi-rate control algorithms were presented. Code migration toward the FPGA exploits high-level synthesis, while a Linux-Xenomai dual-kernel operating system manages the synchronization and parallel execution of tasks.

Motor Current Signature Analysis (MCSA) effectively builds the fault library and monitors conditions [114]. The method is achieved by observing the changes between the harmonic content of the motor line current under the fault occurrence [115]. However, the real-time deadline is hard to meet when implementing this technique on the controller. Thus, the acceleration for hardware implementation is highly demanded. Swakath et al. [116] presented an approach with an RISC-V microcontroller to avoid cyber-attacks. Schiavone et al. [117] proposed a novel fully programmable RISC-V microcontroller unit (MCU) called Arnold. Their proposed SoC delivers 3.4× better performance and 2.9× better energy efficiency than other same level heterogenous reconfigurable SoCs. As for low-power constraints, in [118], Keller et al. presented an RISC-V SoC with integrated voltage regulation and a power management system with the vector accelerator.

Regarding UAVs, Kuehne et al. [119] proposed an efficient parallelization strategy for optical flow computation by integrating low-power RISC-V-based microcontroller units. A parallel architecture meets the real-time deadline with a complex algorithm. In addition, they presented a paradigm that allows the execution of optimization and acceleration of data processing. Their experiments demonstrated that a commercial MCU's eight-core permitted cluster for a frame rate of 500 frames per second when running on a 50 MHz clock frequency. Based on their work, the FMS could be optimized, and the maximum flight speed could be increased with a 7.21× speedup with 500 frames per second on a 50 MHz clock frequency. In [3], a multi-GOPS fully programmable RISC-V IoT-edge computing engine featuring an 8-core cluster with a CNN accelerator is proposed, which is called GAP8. The power efficiency was maximized while the number of external components was minimized. Leveraging GAP-8 could lead to the low-cost and high-performance design of the flight management system according to work in [120]. Their results provided confidential evidence that combining the RISC-V accelerator and CNN enables better flight management applications with rich data-sensing capabilities. Overall, the heterogeneity level demands complex hardware and a full software stack to orchestrate the implementation and manipulate platform features [75].

Coming at the cost of harder controllability and more complex control circuits, a low-cost solution for easier and safer control power modules is expected [110]. However, few studies have been able to draw on any systematic research into RISC-V applications with power electronics and Pulse-Width-Modulation (PWM) controllers.

Overall, the heterogeneous integration for embedded control and drive system could be a promising technology for future integrated electrical drive and PE systems [121].

5. Discussion

Given the resource-constrained nature of the UAV, achieving high control and managing frequency presents a problematic task [122]. Furthermore, prior studies have shown that computing latency is essential for increasing the computing speed of UAV, which leads to low-power consumption during missing process [123]. In reviewing the literature, more data were needed on the association among AI, hardware accelerators, and FMS. Further studies on the current topic are therefore recommended. Furthermore, the following possibilities for the next generation of FMS will be analyzed in-depth and investigated.

HW/SW Co-design FMS: To improve the overall performance, FPGA-based SoC solutions for the FMS computing platform will be essential [124]. However, the computational cost of ML-based solutions leads to the software-only and hardware-only frameworks being inadequate for real-time monitoring on embedded devices [125]. Thus, the co-design of FMS is key to next-generation development. Nyboe et al. proposed an open framework of UAV development for ROS2, PX4, and FPGA integration [10]. In [122], Krishnan et al. showed the framework's effectiveness by orienting an obstacle avoidance algorithm for UAVs to navigate. Their framework develops various accelerator design possibilities for the best-performing algorithm with variable routine, area, and power consumption. However, changing workloads on reconfiguring robotic computing at run-time during flight could lead to non-real-time performance. In addition, suffering from diverse hardware components and inefficient ROS support, better mapping aerial robotic computing on heterogeneous platforms poses a difficult but worthwhile challenge to overcome [4]. Thus, the next important topic is investigating hardware/software (HW/SW) co-design in FMS characterized by heterogeneity. When integrating the popular RISC-V FPGA platform toward ROS-based UAV application [126], approaches to achieve the benchmark for the robust heterogeneous system are demanding. Overall, although there are differing thoughts on the implementation of hardware and software [127], the satisfied integration of heterogeneous HW/SW Co-design for FMS could decrease the development process from FPGA to ASIC [128], which is essential for the time-to-market factor in developing. Furthermore, as for the FL topic, Wang et al. [129] proposed an HW/SW co-designed FPGA accelerator.

Overall, a further step for integrating TinyML co-design application from HW-SW [130] to ML-HW [131] on FMS could provide immense potential.

High-performance control of electric machine drives: Compared to the traditional sensorless control of PMSM drives, such as state observers, Kalman filters, fuzzy logic, high-frequency signal injection, etc. [66,132], AI-based methods provide more high-performance solutions for inverter nonlinearities [133]. Figure 10 illustrates the ANN-based structure scheme for improving IPMSM sensorless control. Using a power converter system, the intelligent controller of the FMS with computation-light and data-light AI possesses immense potential [18].

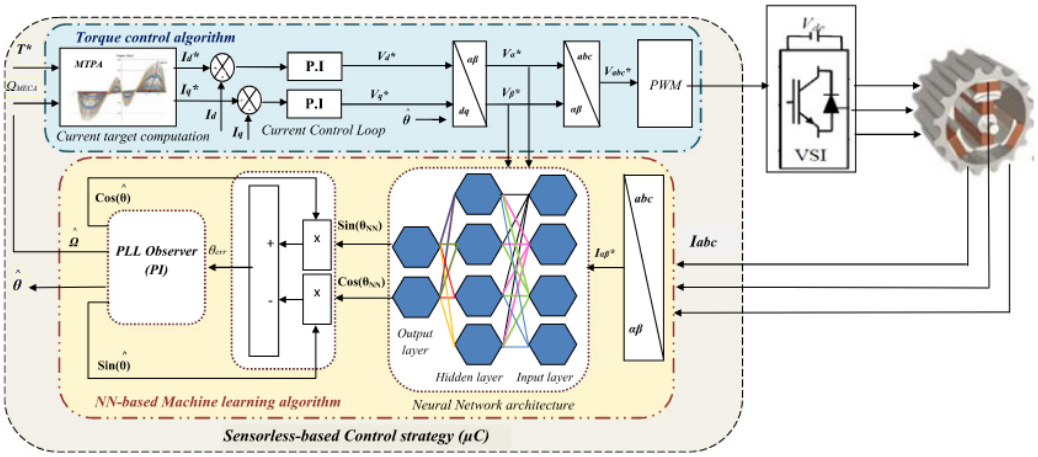


Figure 10. Structure of the IPMSM sensorless control based on AI [134].

Integration with Digital Twin: In the industry 4.0 era, the Digital Twin (DT) concept allows for rapid analysis and real-time decisions made through accurate analytics [135]. As Mandi et al. [136] defined digital twin in 2019, "A DT is a virtual instance of a physical system (twin) that is continually updated with the latter's performance, maintenance, and health status data throughout the physical system's life cycle'.' To accelerate the design of FMS, the DT technology could serve as a powerful tool. Kapteyn et al. [137,138] presented a series of probabilistic graphical models for enabling predictive digital twins at scale with a machine learning interface. In [139], a desktop electric machine emulator implementation method was proposed based on phase voltage reconstruction. In [140], the real-time FPGA-DT was applied to the health monitoring of the power electronic transformer. Furthermore, the advanced 5G technology empowered the FL and DT with superior effectiveness and efficiency to unravel heterogeneity, such as the work shown in [29]. In the PE area, Mulinka et al. [141] proposed a DT for fault diagnosis with limited data while Milton et al. [142,143] generated an FPGA-based with a controller-embeddable probabilistic DT Open Real-Time Simulation (ORTiS) framework with C++ for high performance and converter diagnostics of PE system. In summary, the integration and utilization of DT technology could reduce the life cycle of product development for UAVs.

Addressing FMS practical implementation: Alhough the advances in more electric power distribution systems [144], modern perception techniques [145], and intelligent fault tolerant control methods [146] have opened up new potentials for self-sufficient payload transportation from mini-UAV to heavy-load-UAV, the fusion of AI with FMS into practical implementation in defining future UAV is challenging [147]. Furthermore, incorporating as much modeling and data of the vehicle as possible into the considered heterogeneous FMS is also difficult. Thus, a suitable UAV platform is fundamental to bringing it into real-world application. According to the review by Ducard et al., [148], aerial platforms can normally be divided into two categories: *(I)* vertical take-off and landing (VTOL) or rotary-wing (RW), such as helicopter and multi-rotor platforms, and *(II)* fixed-wing (FW) aircraft. The work from Kuehne et al. [119] provided convincing results by integrating parallelizing optical flow estimation on an RISC-V Cluster for RW. As for the VTOL and

FW, advancements in the next-generation FMS could be conducted to provide significant performance with complex controlling allocation.

Furthermore, as AI-based FMS could be injected by cyber-attacks with manipulated signals to mislead the UAV flight path and decision-making process, causing disastrous consequences, the design of security solutions for preventing the attacks is pivotal. The integrated accelerated Federated Learning paradigm could well preserve privacy, data security, and communication confidentiality while enabling a collaborative model [149,150]. Zhao et al. [63] utilized unique characteristic measurements from voltage and current sensors at the point of common coupling to construct the ML model for detecting false data injection attacks. Mowla et al. [151] proposed a Flying Ad hoc Network (FANET) to serve as cognitive detection of the jamming attack. At the hardware level, since transient faults are increasingly posing threats to FMS, Wan et al. [152] proposed two cost-effective fault detection and recovery approaches with Federated reinforcement learning (FRL) to a more reliable navigation system.

Lastly, the limited battery life of UAVs could be affected when the FMS is in between deployments, especially implementing complex AI-based solutions. Furthermore, only some scholars have studied the influence of limited batteries on FL UAV systems [153]. To optimize energy efficiency and contribute to the next generation of UAV electrical systems [154], setting up optimization constraints based on energy consumption could be considerable [155]. At the path planning level, several approaches [156,157] are proposed to minimize the total energy consumption by UAVs for ML-added-well planned trajectory. At the task management level, Wan et al. [4] presented a runtime-reconfigurable compute platform to enable aerial robots to be adaptive in diverse environments so that the task of battery management is highly dynamic for different workloads. At the coding level, converting the AI model into edge-deployment-friendly types, such as TensorFlow Lite [158], ONNX [159], and NCNN [160] could help. Because only a few battery-relevant constraints have been identified and considered during the UAV design [161], it is worthwhile to invest in monitoring battery management during FMS practical implementation.

6. Conclusions

Heterogeneous UAV FMS design is a rising focal research point that demands reliable and efficient computing substrates. This paper illustrates the loop-closure of UAV FMS design and cross-layer stacks, which contributes systematically to the high-performance, high-reliable, and low-cost electrical UAV architecture. In addition, the computing acceleration possibilities with small-scale data ML, accelerated FL, and hardware accelerators are denoted. We also survey research of typical FMS application cases, including visual-guided landing, intelligent FDD, and controller-embeddable PE. The abovementioned issues represent the research that focuses on heterogeneous FMS design conducted decades ago in [7]. With the rapid advancement of tools at the data-, model-, and HW levels developed in recent years and summarized in this study, the next-generation FMS is expected to show more significant potential in new ways. Regarding this matter, the FMaaS platform is nearing the achievement of becoming a fully developed product for UAVs.

However, the incorporation of heterogeneous FMS into the real-world environment poses significant challenges. Consequently, the critical practical concerns are identified and discussed below. These issues will also serve as the basis for future work, highlighting the theoretical and practical importance of this study.

- HW/SW Co-design FMS: The HW/SW co-design process could accelerate implementation and provide more compact and satisfying solutions.
- High-performance control of electrical machine drives: The implementation of AI-based FMS can offer increased options for enhancing the performance of UAVs.
- Integration with DT: Integrating DT can potentially decrease the duration of the product development life cycle for UAVs.
- Determination of the suitable UAV platform: The appropriate choice of UAV platform is essential to harness the potential of FMS to the greatest extent.

- Security and battery concerns: Employing FL can address privacy concerns while considering battery-life constraints that can improve the reliability and performance of UAVs.

Author Contributions: Conceptualization, G.W. and C.G.; methodology, J.W.; validation, J.L.; writing—original draft preparation, G.W.; writing—review and editing, J.L.; supervision, H.Z. and X.C.; funding acquisition, H.Z. and X.C. All authors have read and agreed to the published version of the manuscript.

Funding: This research was funded by Ningbo Key Scientific and Technological Project under Grant 2022Z040, and Ningbo Science and Technology Bureau under Grant 2022Z019.

Data Availability Statement: Data sharing not applicable.

Conflicts of Interest: The authors declare no conflict of interest.

Abbreviations

The following abbreviations are used in this manuscript:

5G	5th Generation
AI	Artificial Intelligence
ANN	Artificial Neural Network
ASIC	Application-specific integrated circuit
AVS	Adaptive Voltage Scaling
CISC	Complex Instruction Set Computer
CNN	Convolutional Neural Network
CPU	Central Processing Unit
CV	Computer Vision
DA	Domain Adaption
DAA	Detection Furthermore, Avoidance
DC	Direct Current
DGA	Dissolved Gas Analysis
DL	Deep Learning
DLP	Data-Level Parallelism
DNN	Deep Neural Network
DSP	Digital Signal Processor
DT	Digital Twin
EC	Edge Computing
FANET	Flying Ad-hoc Network
FCS	Flight Control System
FDD	Fault Detection and Diagnosis
FDI	False Data Injection
FL	Federated Learning
FMaaS	Flight-Management-as-a-Service
FMS	Flight Management System
FPGA	Field Programmable Gate Array
FRL	Federated Reinforcement Learning
FSL	Few-shot Learning
FW	Fixed-Wing
GOPS	Giga Operations Per Second
GPS	Global Position System
GPU	Graphic Processing Unit

HC	Heterogeneous Computing
HW	Hardware
IaaS	Infrastructure-as-a-Service
IDD	Independent and Identically Distributed
IMUs	Inertial Measurement Unit
IoT	Internet of Things
IPMSM	Interior Permanent Magnet Synchronous Motor
ISA	Instruction Set Architecture
Lidar	Light detection and ranging
MCSA	Motor Current Signature Analysis
MCU	Micro Controller Unit
MGD	Momentum Gradient Descent
MIMO	Multi-Input Multi-Output
ML	Machine Learning
NRT	Non-Real-Time
ODEs	Ordinary Differential Equations
Ops	Operations
ORTiS	Open Real-Time Simulation
OSH	Open-Source Hardware
PCA	Principal component analysis
PE	Power Electronics
PID	Propotional-Integral-Derivative
PMSN	Permanent Magnet Synchronous Machine
PQSU	Pruning, Quantization, and Selective Updating
PROSAC	PROgressive SAmple Consensus
PULP	Parallel Ultra-Low Power
PV	Photovoltaic
PWM	Pulse-Width-Modulation
RISC-V	Reduced Instruction-Set Computer-Five
RL	Reinforcement Learning
ROS	Robot Operating System
RT	Real-Time
RUL	Remaining Useful Life
RW	Rotary Wing
SGD	Stochastic Gradient Descent
SLAM	Simultaneous Localization Furthermore, Mapping
SLZ	Safe Landing Zone
SoC	System on Chips
SW	Software
SWaP-C	Size, Weight, Power and Cost
TL	Transfer Learning
ToF	Time-of-Flight
UAVs	Unmanned Aerial Vehicles
VTOL	Vertical Take Off and Landing

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