

## Article

# Optimal Cascade Non-Integer Controller for Shunt Active Power Filter: Real-Time Implementation

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**Abstract:** Active power filters (APFs) are used to mitigate the harmonics generated by nonlinear loads in distribution networks. Therefore, due to the increase of nonlinear loads in power systems, it is necessary to reduce current harmonics. One typical method is utilizing Shunt Active Power Filters (SAPFs). This paper proposes an outstanding controller to improve the performance of the three-phase 25-kVA SAPF. This controller can reduce the current total harmonic distortion (THD), and is called fractional order PI-fractional order PD (FOPI-FOPD) cascade controller. In this study, another qualified controller was applied, called multistage fractional order PID controller, to show the superiority of the FOPI-FOPD cascade controller to the multistage FOPID controller. Both controllers were designed based on a non-dominated sorting genetic algorithm (NSGA-II). The obtained results demonstrate that the steady-state response and transient characteristics achieved by the FO (PI + PD) cascade controller are superior to the ones obtained by the multistage FOPID controller. The proposed controller was able to significantly reduce the source current THD to less than 2%, which is about a 52% reduction compared to the previous work in the introduction. Finally, the studied SAPF system with the proposed cascade controller was developed in the hardware-In-the Loop (HiL) simulation for real-time examinations.

**Keywords:** three-phase shunt active power filter; repetitive controller; fractional-order (PI + PD) cascade controller; multistage fractional-order PID Controller



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## 1. Introduction

At present, developments in power electronic technology have led to a major increase in the usage of power electronic converters in the power grid while also increasing the use of electrical energy. However, power electronic converters generate reactive power and harmonics, which pollute the power system [1]. Therefore, the optimal compensation of nonlinear loads' harmonics is an important issue in power networks. Current harmonics boost losses, destroy the quality of the voltage sine waveform, cause metering devices to malfunction, and may lead to resonances and interferences [2]. As a result, distortions in current and voltage sine waveforms are not only a source of technical problems, but also have economic effects [3]. There are several popular devices such as active power filters (APFs), which may be of a series, shunt or hybrid type [4–6], static compensator, and unified power quality controller. These utilities are widely used to decrease power quality problems [7] that affect the distribution side [8].

From the viewpoint of circuit topology, Reference [9] has a more comprehensive taxonomy of available APFs, which are divided into parallel/series/hybrid type and other types. The active power filter is an effective inhibition device of active compensation

harmonics that can efficiently omit harmonic contamination and improve the power factor compared with the classic passive filter [10]. Although series and/or shunt APFs are generally used to eliminate power quality problems, shunt APFs are used more often than series APFs due to their excellent performance [11,12]. SAPF is an especially efficient solution for power quality issues [13], and can reduce harmonic pollution [14–19] and compensate reactive power generated by linear/nonlinear loads in distribution networks. Therefore, SAPFs play an increasingly essential role in power distribution and delivery [20]. These filters are connected in parallel with the nonlinear loads to remove undesired current harmonics. A traditional PI controller or other control techniques, combined with the repetitive controller, can modify the dynamic response time of the repetitive controller [21].

In most cases, some characteristics should be complied with, such as low total harmonic distortion (THD) for the compensated currents and a fast transient response. To ensure an excellent design, it is believed that compromises must be found between some different necessities. Therefore, applying a multi-objective optimization approach to achieve a set of desirable objective functions based on the APFs' specifications is essential. SAPFs equipped with repetitive controllers promise an excellent compensation at steady-state with a slow, transient response [22]. In Reference [23], a traditional PI controller and FOPI controller were used to promote the performance of a 25-kVA parallel active filter based on the NSGA-II optimization approach. The optimization results proved that the obtained results using the FOPI controller were more acceptable than the achieved results by the traditional PI controller. The minimum obtained value of THD was about 3.8% in this article. In Reference [24], research was carried out looking at the superiority of FOPID controller compared to the integer-order PID controller. In fact, it is believed that the fractional-order PID/PI controller has a better performance than the integer-order PID/PI controller. In a different work, researchers presented the multistage PID controller for the automatic generation control of power systems. Hence, we were inspired by the multistage PID controller to devise a novel method, called a multistage fractional-order PID controller [25]. In the present research, a novel optimal fractional-order controller is proposed to achieve a better performance from the 25-kVA parallel active power filter, called a fractional-order (PI + PD) cascade controller, which was recently presented in Reference [26]. In addition, another fractional-order controller is designed for comparison with our proposed method. To the best of our knowledge, this controller was applied for the first time in this case study. It is called a multistage fractional-order PID controller.

As mentioned before, two different controllers were designed to optimize the performance of the shunt active power filter with the high-performance repetitive controller called the fractional order PI-fractional order PD cascade controller and multistage fractional-order PID controller. These controllers were designed based on the NSGA-II optimization method. This optimization approach is still a powerful multi-objective optimization technique to minimize the objective functions that the other researchers are using in several fields [27–39]. According to this optimization method, there are two result categories: one of them is related to the variables selected to design each controller, called the Pareto Optimal Set (POS), and another set of results is concerned with two objective functions, called the Pareto Optimal Front (POF). It is mandatory to choose an appropriate range for each variable in order to reach an excellent POF.

An acceptable performance means achieving both fast transient/settling time to obtain an appropriate transient response and a low THD to obtain a proper steady-state response [22,23]. It should be mentioned that transient time and THD are taken as two objective functions that must be simultaneously minimized, as well as settling time and THD. In fact, there is a compromise between two objective functions: the smaller the value of one, the higher the value of the other, and vice versa. In this research, first, the proposed controller is applied to acquire some transient/settling time and THDs, which are the same POF; therefore, the obtained results show the efficiency of this controller. Secondly, a multistage FOPID controller is used; different results are obtained for this, which include transient/settling time and THDs similar to the proposed controller. Eventually, the ob-

tained results from both controllers are compared to show the better performance of the proposed method for a three-phase shunt active power filter. The key contributions of the present study are summarized as follows:

1. Fractional controller is applied due to its having more tunable parameters, which allow for more flexibility to achieve a high accuracy.
2. The cascade controller is able to rapidly reject disturbance before it leaks to the other parts of the system.
3. Multi-objective NSGA-II algorithm offers optimal solutions to multidimensional objective functions, which minimize the THD.

The rest of this paper is structured as follows: Section 2 outlines the system under study, which is a three-phase shunt active power filter with a high-performance repetitive controller. In Section 3, the proposed controllers are implemented. Section 4 describes the NSGA-II optimization method, objective functions, case studies, and design parameters. The real-time results are discussed in Section 5, and, finally, Section 6 summarizes the conclusions.

### 2. Shunt Active Power Filter and Repetitive Controller

Some devices, such as passive, active, or hybrid power filters and operation strategies, have been developed for the local correction of power-quality problems [40–43]. Since the performance of SAPFs is more dependent on the current control method, many current-control schemes have been proposed in the research [44–46]. However, in this research, a 25-kVA parallel active power Filter (Figure 1) with a high-performance repetitive controller (Figure 2) is optimized [22].

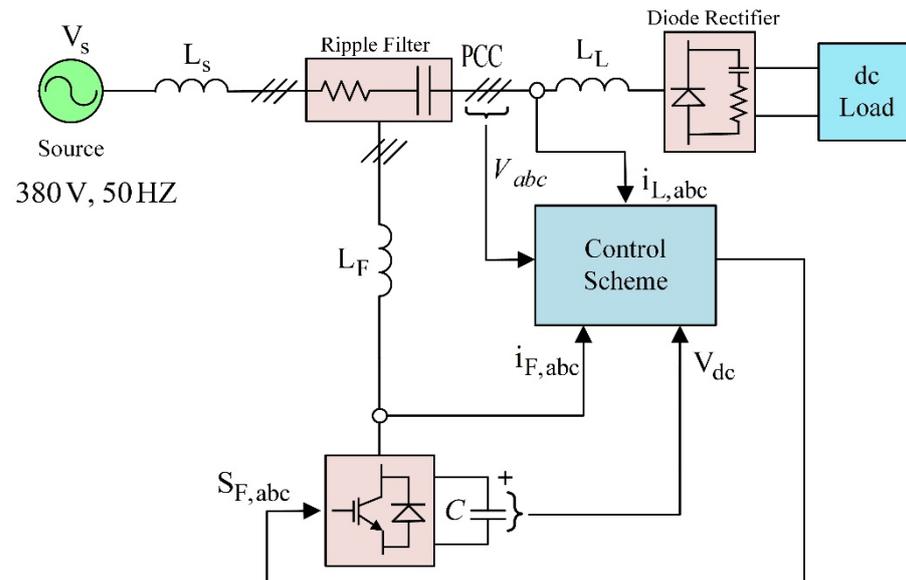


Figure 1. Structure of the 25-kVA SAPF [22,46].

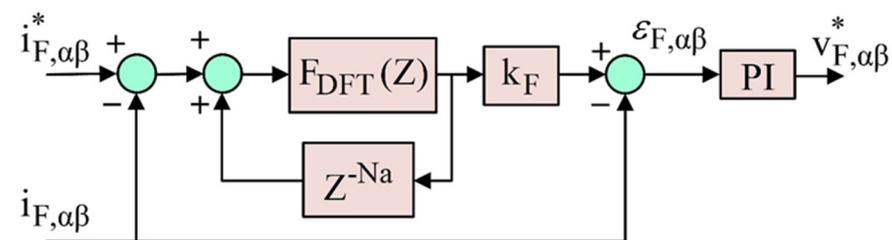


Figure 2. Structure of repetitive controller [22,46].

As seen in Figure 1, with these specifications  $V_s = 380$  v,  $f_s = 50$  Hz and  $I_s = 80$  A [22], the functioning idea is based upon the injection of a compensating current into the network, which provides the basic reactive component and the harmonic currents due to the distorting load operation. Hence, a reference waveform for the current to be injected in the alternative current (AC) network should be provided by the control unit, so that the inverter is required to produce a current that is as close as possible to the reference. In Figure 1,  $L_S$  is the equivalent supply inductance, as seen by the bus where the active filter and the distorting load are connected;  $L_L$  is the equivalent inductance of the line supplying the load, while  $L_F$  is the inductance of the series inductor filter [47]. In 1981, the repetitive control notion was initially developed [48–50]. The primary motivations and representative examples include the rejection of periodic disturbances in a power supply control application [48,50] and the tracking of periodic reference inputs in a motion control application [49,50]. The repetitive controller is mainly used in continuous processes to track or reject periodic exogenous signals [50]. Although this controller has a high tracking operation, its operation is inherently slow. This controller is inserted in series with a used controller, which is a PI controller in this figure, as shown in Figure 2, and a discrete Fourier transform (DFT) is used. This DFT has a frequency response that almost equals the frequency response used to track the harmonic reference (Figure 2) [51]. Equation (1) gives us the discrete transfer function of the mentioned DFT.

$$F_{DFT}(Z) = \frac{2}{N} \sum_{i=0}^{N-1} \left( \sum_{k \in N_h} \cos \left[ \frac{2\pi}{N} h(i + N_a) \right] \right) Z^{-i} \tag{1}$$

Here,  $N$  is the number of the coefficients;  $N_h$  is the set of selected harmonic frequencies, and  $N_a$  is the number of leading steps that are essential to guarantee the stability of the system. In fact, (1) can be considered a finite-impulse response (FIR) band pass filter of  $N$  taps with a unity gain at all selected harmonics  $h$ , and is also called a discrete cosine transform (DCT) filter [51].

### 3. Fractional Controllers

#### 3.1. Fractional-Order PID Controller (FOPID Controller)

The traditional PID controllers are basic, robust, impressive, and easily implementable control techniques [25]. The transfer function of the PID controller is as follows:

$$T_{PID}(s) = K_p + K_i s^{-1} + K_d s \tag{2}$$

In recent years, one of the best possibilities for improving the quality and robustness of PID controllers is to apply fractional-order controllers with non-integer derivation and integration parts [52,53]. The  $PI^\alpha D^\beta$  controller generalizes the PID controller including an integrator of order  $\alpha$  and a differentiator of order  $\beta$ .

The transfer function of the FOPID controller is acquired using the Laplace transformation, as given below:

$$T_{FOPID}(s) = K_p + K_i s^{-\alpha} + K_d s^\beta \tag{3}$$

To design a FOPID controller, three parameters ( $K_p$ ,  $K_i$ ,  $K_d$ ) and two non-integer orders ( $\alpha$ ,  $\beta$ ) should be optimally determined.

#### 3.2. Fractional-Order (PI + PD) Cascade Controller

As far as we know, it is difficult to achieve an excellent performance in terms of transient/steady-state response using a conventional PID controller. In this study, we applied a FOPI-FOPD cascade controller and a multistage FOPID controller instead of the traditional PI controller, as seen in Figure 2. Therefore, the FO (PI + PD) cascade controller is our proposed controller. It includes two controllers, which were connected in cascade, as shown in Figure 3. One of them is the FOPI controller and the other one is the FOPD controller. When the FOPI receives the ACE signal, the fractional-order PI controller

produces a signal, which also operates as the input of another controller. The output of the FO (PI + PD) cascade controller is the reference power setting or control input.

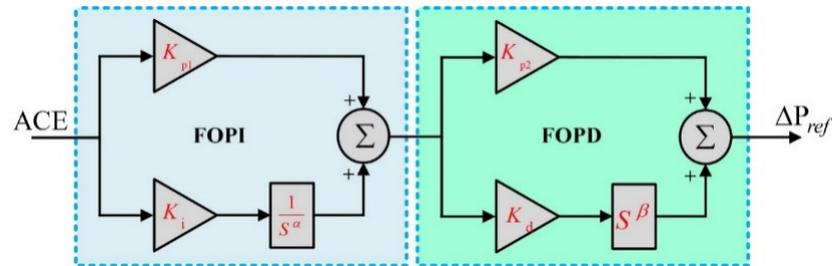


Figure 3. The structure of FO (PI + PD) controller.

$\Delta P_{ref}$  for the electric power systems to be controlled, as mathematically given by Equation (4):

$$\Delta P_{ref} = ACE \times (K_{p1} + K_i s^{-\alpha}) \times (K_{p2} + K_d s^\beta) \tag{4}$$

For  $\alpha = 1$  and  $\beta = 1$  the FOPI-FOPD cascade controller is transformed to a simpler form of conventional PI – PD cascade controller, i.e.,  $K_{p1}$ ,  $K_i$ ,  $K_{p2}$ ,  $K_d$ ,  $\alpha$ , and  $\beta$  are six variable parameters that must be optimized.

Three objectives contribute to the design of the FO (PI + PD) cascade controller. First of all, it should be economical, straightforward, and easy to apply and develop. As a result, its operation is comparable to that of a PID controller. Second, PI and PD controllers are cascaded, i.e., PI – PD, to combine the benefits of their distinct specifications and capabilities. On the other hand, a cascade controller has more adjustable parameters than a non-cascade controller, and it is obvious that if there are more adjustable parameters, the controller will provide a better system performance. Furthermore, the cascade controller is attractive because it can rapidly reject disturbances, before they reach the rest of the system. To comply with the third goal, a non-integer integrator/derivative order is considered, i.e., FOPI-FOPD, to enhance its freedom to design and promote PI – PD cascade controller performance [26].

### 3.3. Multistage Fractional-Order PID Controller

As stated before, it is difficult to obtain an excellent performance when applying a classic PID controller. According to Equation (2), increasing the integral gain to eliminate the steady-state error worsens the system’s transient response. The existence of integral gain affects the speed and stability of the system during transient conditions, which leads to decreases in these parameters. To improve the transient response, the integrator must be disabled during the transient part [25]. A two-stage FOPD-FOPI controller with a first-stage fractional-order PD controller and a second-stage fractional-order PI controller can accomplish this. Sensors generate noise in an automated control system. This noise usually has a high frequency. Sometimes, the tie-line telemetry system generates noise. Due to this noise, if the derivative term is used, the plant input becomes excessively big. As a result, it can be removed by applying a first-order derivative filter that reduces the high-frequency noise. Figure 4 depicts the structure of the presented multistage FOPID controller. The transfer function of the multistage FOPID controller is represented by:

$$T_{multistage-FOPID}(s) = \left[ K_p + K_d \left[ \frac{N}{N + S^\beta} \right] \right] \times \left[ 1 + K_{pp} + \frac{K_i}{S^\alpha} \right] \tag{5}$$

In the controller scheme shown in Figure 4,  $K_p$ ,  $K_d$ ,  $\beta$ ,  $K_i$ ,  $\alpha$ ,  $K_{pp}$  and  $N$  are proportional, derivative, non-integer derivative, integral, non-integer integral, proportional gain, and filter coefficient, respectively. The input of the controller is Area Control Error (ACE), as well as output of the controller is ( $\Delta F$ ), which produces a control signal through these

two stages. Afterward, this enters the power system. It is worth noting that the frequency deviation ( $\Delta F$ ) is the ACE in the case of a single-area system.

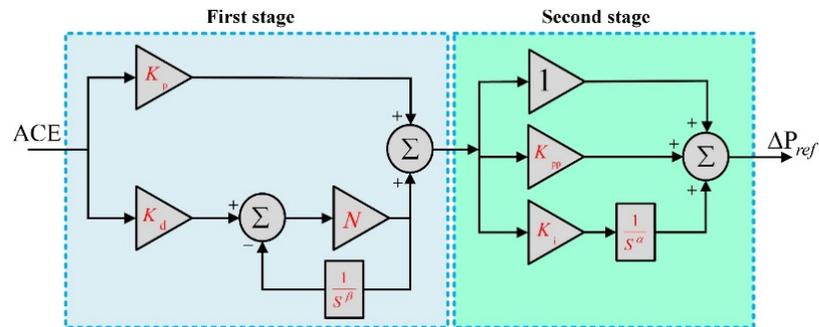


Figure 4. The structure of multi-stage FOPID controller.

#### 4. NSGA-II Optimization Method and Objective Functions

##### 4.1. NSGA-II: An Overview

NSGA-II is a popular multi-objective-optimization algorithm, which has three particular specifications: a speedy non-dominated sorting approach, prompt crowded distance estimate method and simple crowded comparison operator [54]. Typically, NSGA-II is described in detail as follows:

1. Population initialization:

The population must be initialized based upon the range of the problem and its limitations.

2. Non-dominated sorting process based upon non-domination criteria of the population that was initialized.

3. Crowding distance:

When the sorting is complete, the value of the crowding distance is determined in advance. The individuals in the population are chosen based on crowding distance and rating.

4. Selection:

Individuals are selected by applying a binary contest election with a crowded-comparison operator.

5. Genetic Operators:

Actual coded GA is achieved by applying simulated polynomial mutation and binary crossover.

6. Recombination and selection:

Population of children and population of the current generation are combined. The next generation is set by election. The new generation is filled by each front until the size of the population exceeds the current population size [55]. Figure 5 shows the NSGA-II procedure.

##### 4.2. Objective Functions

The purpose of this work is to minimize the transient/steady-state response as two objective functions by the proposed controller based on the NSGA-II optimization technique. It offers optimal solutions to multidimensional objective functions [23]. Three objective functions have been chosen, which must be minimized in two case studies, as follows:

1. Steady-State Response (THD (up to the 50th harmonic) of the source current)

Steady-State Response: In electronics, steady-state is an equilibrium condition of a circuit that occurs when the effects of transients are no longer important. Steady-State

determination is an important issue because many design features of electronic systems are given in terms of their steady-state characteristics. The periodic steady-state solution is also a prerequisite for small-signal dynamic modeling. The steady-state analysis is, therefore, an essential component of the design process.

Total harmonic distortion (THD) is a widely occupied concept when defining the level of harmonic content in alternating signals, which is measured in percentages.

2. Transient Response (Transient/Settling Time): In electrical engineering, transient response is the response of a system to changes from the equilibrium. The impulse response and step response are transient responses to a specific input (an impulse and a step, respectively).

Rise time or transient time ( $t_r$ ) refers to the time required for a signal to alter from a specified low value to a specified high value. Usually, these values are 10% and 90% of the step height. Settling time ( $t_s$ ) is the time needed for a response to become steady. This is defined as the time needed by the response to reach and remain within the determined range of from 2% to 5% of its final value. Therefore, the following two case studies were considered to be synchronously minimized:

Case study 1: THD (up to the 50th harmonic) and Transient (Rise) Time must be synchronously minimized.

Case study 2: THD (up to the 50th harmonic) and Settling Time must be synchronously minimized.

The set of designing parameters used to minimize the objective functions is presented in the next section.

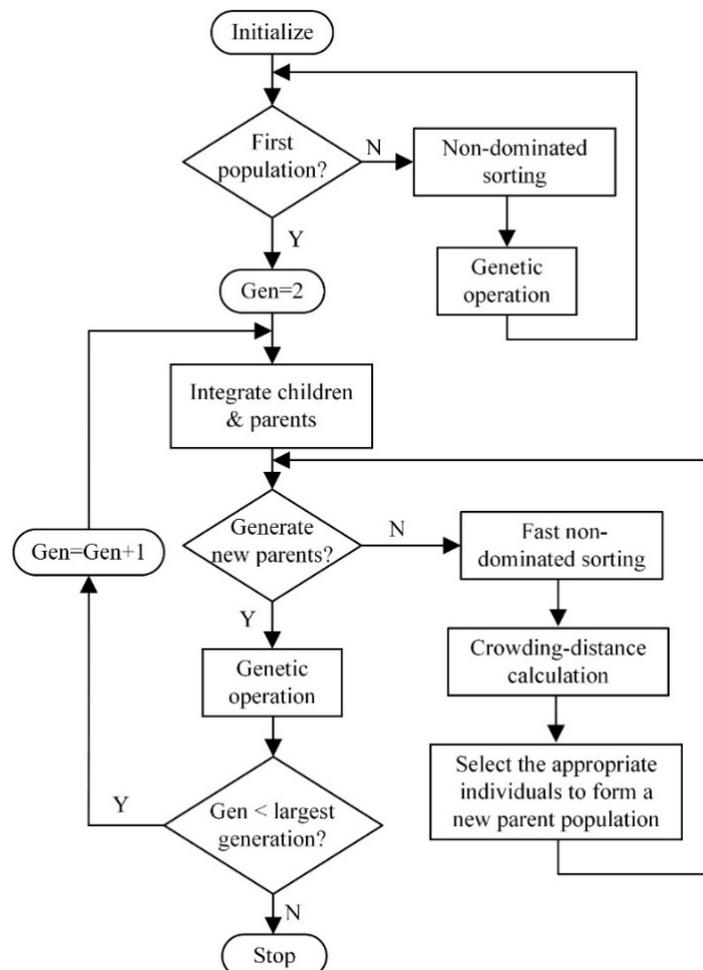


Figure 5. Flowchart of non-dominated sorting genetic algorithm (NSGA-II) [56].

### 4.3. Design Parameters

DC bus voltage ( $V_{dc}$ ) and the FO (PI + PD) cascade controller parameters, which are  $K_{p1}, K_i, K_{p2}, K_d, \alpha$  and  $\beta$ , in Figure 3, as well as  $V_{dc}$  and multistage FOPID controller parameters, which are  $K_p, K_d, \beta, K_i, \alpha, K_{pp}$  and  $N$  in Figure 4, are determined based on the NSGA-II optimization technique.  $V_{dc}$  affects the transient response and the steady-state response in the shunt active power filter. In fact, it acts an important role to decrease current harmonics, i.e., THD. Hence, it was chosen as a design variable. In this optimization approach, the mentioned parameters are experimentally limited. These limitations dramatically reduce the computational time [41]. Therefore, it is said that  $K_{p1}, K_i, K_{p2}, K_d, \alpha, \beta, V_{dc}$  are POS members for the FO (PI + PD) controller, and the POS for multistage FOPID controller has the following parameters:

$K_p, K_i, K_{pp}, N, K_d, \alpha, \beta, V_{dc}$ . As mentioned before, the different obtained values from POS members are called POF, and concern the values of the objective functions.

The general multi-objective optimization problem is considered as the following, with  $x$  as the design:

$$\begin{aligned} & \text{Minimize} \\ & g = f(x) = (f_1(x), \dots, f_i(x), \dots, f_k(x)) \\ & \text{Subject To :} \\ & x = (x_1, x_2, \dots, x_n) \in X \end{aligned} \tag{6}$$

where  $k$  is the number of objective functions,  $n$  is the number of inequality constraints,  $x$  is a vector of design variables, and  $f(x)$  is a vector of the objective functions to be minimized. Figure 6 depicts a Pareto front block diagram.

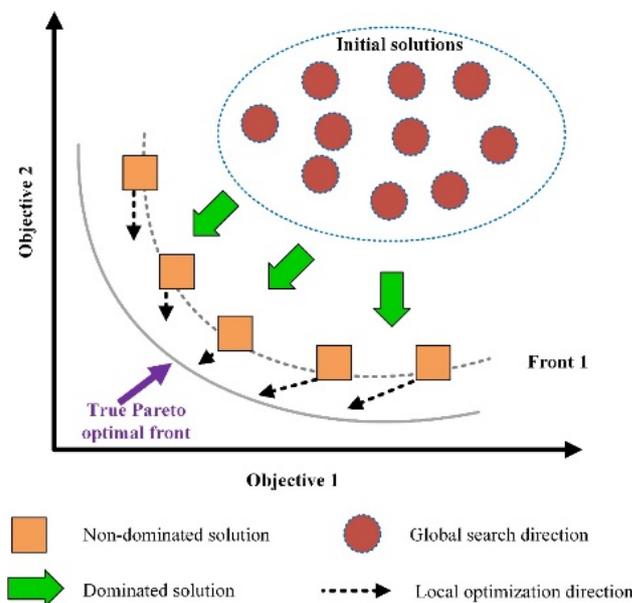


Figure 6. A Pareto front of the multi-objective problem.

Therefore, in this research, for the first case study, the goal is as follows:

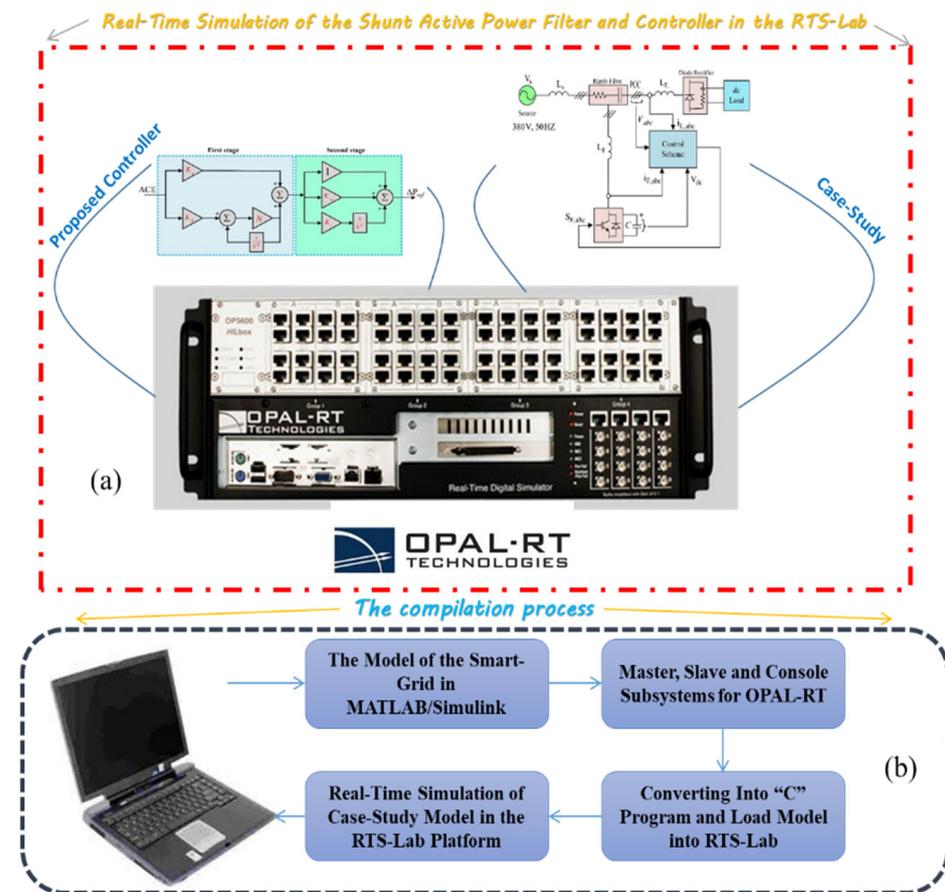
$$\begin{aligned} & \text{Minimize} \\ & g = f(x) = (\text{THD}(\text{up to the 50th harmonic}), t_r) \\ & \text{Subject To :} \\ & x = (K_{p1}, K_i, K_{p2}, K_d, \alpha, \beta, V_{dc}) \in X \text{ for FO (PI + PD) controller,} \\ & x = (K_p, K_i, K_{pp}, N, K_d, \alpha, \beta, V_{dc}) \in X \text{ for multistage FOPID controller} \end{aligned} \tag{7}$$

For the second case study, the goal is as follows:

$$\begin{aligned}
 & \text{Minimize} \\
 & g = f(x) = (\text{THD}(\text{up to the 50th harmonic}), t_s) \\
 & \text{Subject To :} \\
 & x = (K_{p1}, K_i, K_{p2}, K_d, \alpha, \beta, V_{dc}) \in X \text{ for FO (PI + PD) controller,} \\
 & x = (K_p, K_i, K_{pp}, N, K_d, \alpha, \beta, V_{dc}) \in X \text{ for multistage FOPID controller}
 \end{aligned}
 \tag{8}$$

**5. Real-Time Simulation Results**

In this research, the 25-kVA parallel APF in Figure was developed in the hardware-In-the Loop (HiL) to verify the efficiency of the proposed control scheme in the real-time framework. The HiL set-up based on the OPAL-RT simulator was adopted to consider the effects of the control errors and computation delays on the SAPF system (see Figure 7) [57]. The compensator was a three-phase PWM inverter with a switching frequency of 10 kHz. A 3.3 us dead time was also considered for the inverter’s switches [22]. The NSGA-II algorithm in the aforementioned case studies was implemented for 20 generations. Each generation includes 30 individuals. For all the sections of the case studies, the remaining parameters for the repetitive controller were:  $N = 200$ ,  $N_a = 3$ , and  $k_f = 1$  [51]. For the FO (PI + PD) cascade controller and multistage FOPID controller, the Crone approximation with order 5 and frequency range equals [0.01; 1000] rad/s has been considered. According to the above description, all tables and figures related to POF show the optimization results after 20 generations based on the NSGA-II multi-objective optimization method.



**Figure 7.** Process of HiL setup based on OPAL-RT (a) illustration of real-time simulation, (b) compilation process.

5.1. Case Study 1: THD (up to the 50th Harmonic) and Transient (Rise) Time Must Synchronously Be Minimized

Transient time and settling time can determine the transient response. In this case optimization, the rise time is the quantity that must be optimized with the THD. This time is defined as the time gap between the beginning of the compensation and the time when the THD starts to be lower than 5% [22]. Here, THD (up to the 50th harmonic) of the source current and rise time were synchronously minimized. The system outcomes achieved using an FO (PI + PD) cascade controller and multistage FOPID controller are as follows.

5.1.1. First Section of the First Case Study: Applying FO (PI + PD) Cascade Controller

In this work, the POS for FO (PI + PD) cascade controller included ( $K_{p1}$ ,  $K_i$ ,  $K_{p2}$ ,  $K_d$ ,  $\alpha$ ,  $\beta$ ) and  $V_{dc}$ . The obtained results from POS members are known as POF; the POF is related to THD values and rise time. All obtained results are optimal, but the designer can pick one of them based on any other issues posed by the technical, economical, or managerial benefits requirements. The THD range and transient time for the FO (PI + PD) cascade controller are important from the technical viewpoint. According to Table 1, the lowest THD and the highest rise time are related to row no. 6; row no. 9 is concerned with the highest THD and the lowest rise time, as shown in Figure 8:

Table 1. POS and POF for FO (PI + PD) cascade controller.

No	$K_{p1}$	$K_i$	$V_{dc}$	$K_{p2}$	$K_d$	$\alpha$	$\beta$	THD (%)	$t_r$ (s)
1	2.4154	10.4602	815.0000	3.0000	0.4257	0.7481	0.3224	1.9673	0.0369
2	2.0321	10.4680	815.0000	2.5807	0.4287	0.7496	0.3224	1.9048	0.0387
3	1.9759	12.4680	815.0000	3.0000	0.4257	0.7481	0.3224	2.0416	0.0368
4	2.2689	12.4055	815.0000	3.0000	0.4287	0.7481	0.3224	2.0654	0.0367
5	1.9759	12.4680	815.0000	2.5807	0.4287	0.7481	0.3216	1.8360	0.0388
6	2.0321	12.4679	814.9904	2.5807	0.4287	0.7481	0.3224	1.8068	0.0388
7	2.2689	12.4055	814.9904	2.5807	0.4287	0.7481	0.3224	1.9122	0.0387
8	2.4154	10.4602	815.0000	2.9902	0.4703	0.7481	0.3302	2.1114	0.0366
9	2.2970	12.4680	814.6924	3.0000	0.4257	0.7481	0.3224	2.1513	0.0366
10	2.4154	10.4602	814.9994	2.9902	0.4257	0.7481	0.3224	2.1024	0.0366
11	2.4154	10.4602	815.0000	2.9207	0.4287	0.7481	0.3224	1.9616	0.0370
12	2.4154	10.4602	815.0000	2.5807	0.4287	0.7480	0.3212	1.9345	0.0385

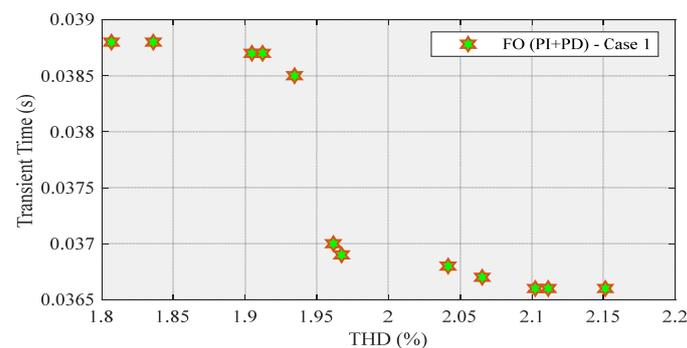
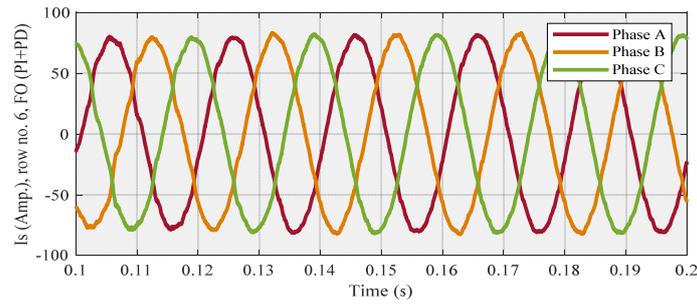
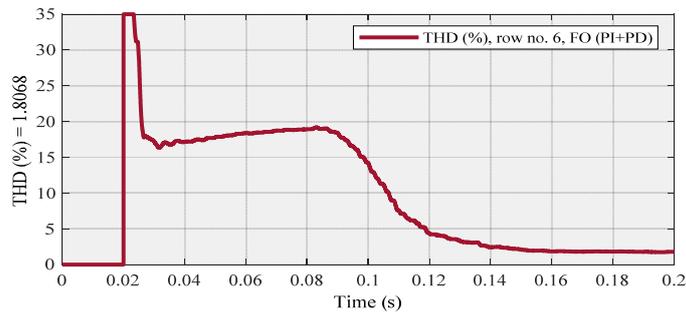


Figure 8. POF for FO (PI + PD) cascade controller.

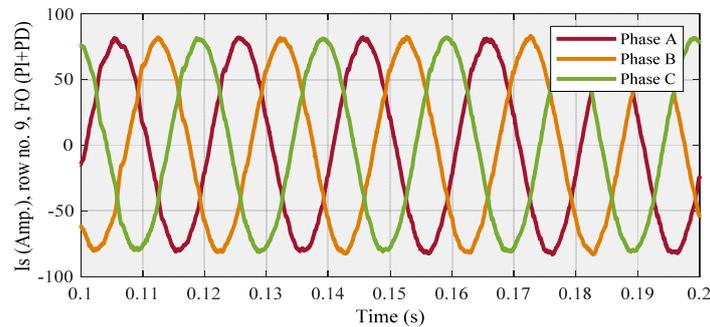
The compensated source current (Figure 9) and THD (Figure 10) diagrams are related to row no. 6, also  $I_s$  (Figure 11) and THD (Figure 12) diagrams are associated with row no. 9 as below:



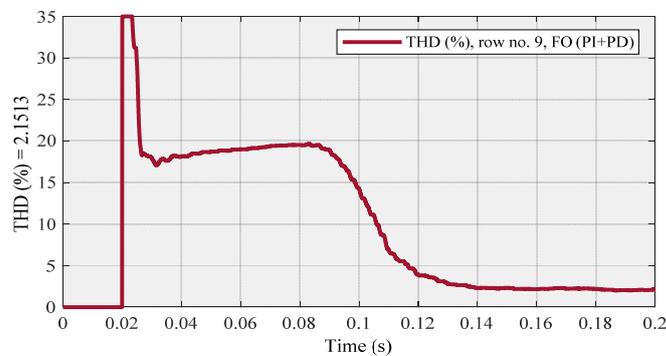
**Figure 9.** Compensated source current for row no. 6 (Lowest THD) using FO (PI + PD) cascade controller.



**Figure 10.** Row no. 6 (with the lowest THD at steady-state) using FO (PI + PD) cascade controller.



**Figure 11.** Compensated source current for row no. 9 (Highest THD) using FO (PI + PD) cascade controller.



**Figure 12.** Row no. 9 (with the highest THD at steady-state) using FO (PI + PD) cascade controller.

Figure 10 (row no. 6) and Figure 12 (row no. 9) show the variations in THD using the FO (PI + PD) cascade controller. By looking at these two figures, we can see that the value of THD in Figure 10 is lower than the THD value in Figure 12. Additionally, this claim is valid for subsequent sections with similar conditions.

5.1.2. Second Section of the First Case Study: Applying Multistage FOPID Controller

According to Table 2, ( $K_p, K_i, V_{dc}, K_{pp}, N, K_d, \alpha, \beta$ ) are members of POS. THD and  $t_r$  are concerned with POF. In the case of variables for the multistage FOPID controller and  $V_{dc}$  has already been discussed. This table shows that row no. 2 is related to the lowest THD and the highest rise time; row no. 7 is associated with the highest THD and the lowest rise time, as shown in Figure 13.

Table 2. POS and POF for multistage FOPID controller.

No	$K_p$	$K_i$	$V_{dc}$	$K_{pp}$	$N$	$K_d$	$\alpha$	$\beta$	THD (%)	$t_r$ (s)
1	2.5400	12.4261	719.0607	11.2424	1.7693	0.9098	0.9000	0.0287	2.0274	0.0386
2	1.8393	10.7355	573.2281	11.7506	1.6734	0.1000	0.9408	0.0904	1.9219	0.0393
3	2.6000	13.2472	601.7378	11.7506	1.6734	0.6063	0.9041	0.0287	2.0992	0.0370
4	2.6000	10.0000	812.8484	11.7428	1.0054	0.2728	0.9683	0.0760	2.0621	0.0386
5	2.5315	13.8570	812.8484	11.7424	1.7693	0.2728	0.9683	0.0535	1.9946	0.0388
6	2.4969	13.8570	812.8484	11.6879	1.7547	0.9098	0.9683	0.0287	1.9299	0.0389
7	2.5764	11.1837	529.0360	11.3453	1.6186	0.4805	0.9335	0.0801	2.8242	0.0369
8	2.5764	11.5726	686.4316	11.9324	1.5213	0.6709	0.9335	0.0960	2.2386	0.0369
9	2.5764	11.5745	686.4515	11.9324	1.5213	0.6709	0.9336	0.0967	2.1409	0.0369
10	2.5764	11.5764	686.4515	11.9324	1.5213	0.6709	0.9336	0.0967	2.2158	0.0369

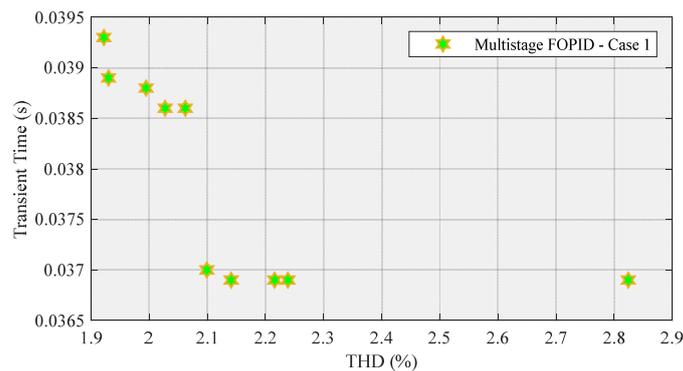


Figure 13. POF for multistage FOPID.

Is (Figure 14) and THD (Figure 15) diagrams are concerned with row no. 2, also the compensated source current (Figure 16) and THD (Figure 17) diagrams are related to row no. 7 as follows:

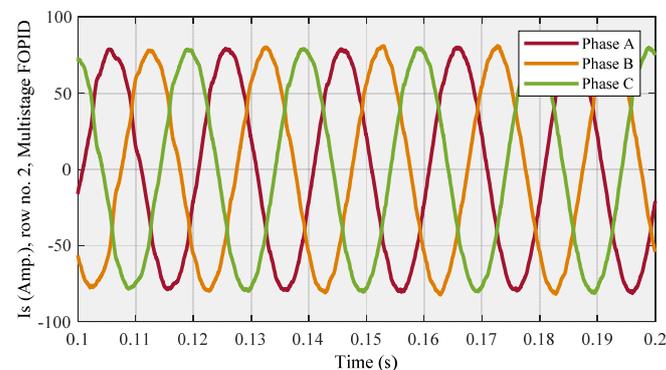


Figure 14. Compensated source current for row no. 2 (lowest THD) using the multistage FOPID controller.

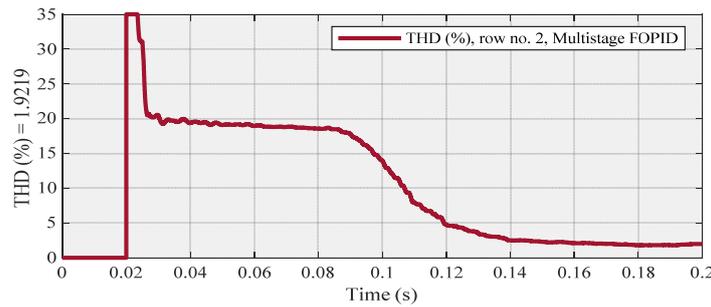


Figure 15. Row no. 2 (with the lowest THD at steady-state) using a multistage FOPID controller.

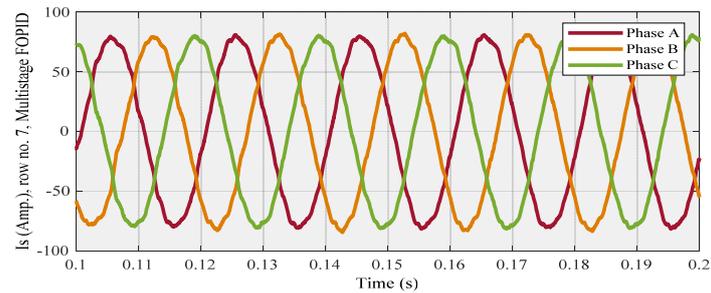


Figure 16. Compensated source current for row no. 7 (highest THD) using a multistage FOPID controller.

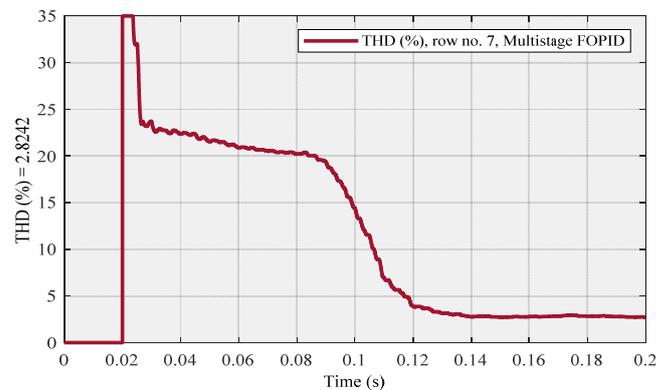


Figure 17. Row no. 7 (with the highest THD at steady-state) using a multistage FOPID controller.

Figure 15 (row no. 2) and Figure 17 (row no. 7) illustrate the changes in source current THD using a multistage FOPID controller. Therefore, by comparing Figures 15 and 17, it is obvious that the THD value in Figure 17 is higher than the THD value in Figure 15.

### 5.1.3. Third Section of the First Case Study: Comparison between FO (PI + PD) Cascade Controller and Multistage FOPID Controller

In this section, the real-time results of two controllers are compared with each other. Figure 18 depicts a comparison between the obtained POF values of FO (PI + PD) cascade controller and the acquired POF values of a multistage FOPID controller. This figure proves that the values obtained by the FO (PI + PD) cascade controller dominate all the values using a multistage FOPID controller. Figure 19, which has two parts, shows a comparison between the values of current THD that were obtained using these two controllers. The magnified part precisely demonstrates that the FO (PI + PD) cascade controller has better behavior than the multistage FOPID controller. Additionally, this figure shows that the THD (around 1.8068%) related to our proposed controller reached steady-state earlier than the THD (around 1.9219%), which is related to the other controller.

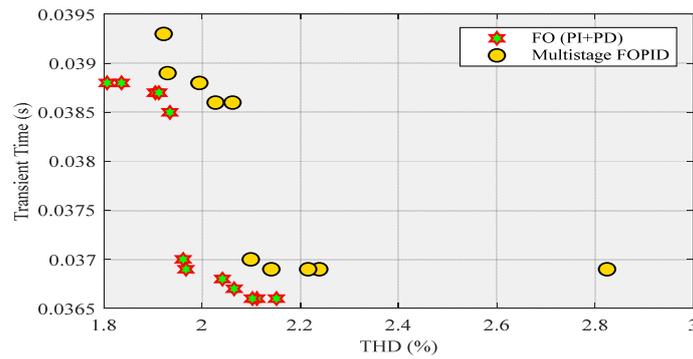


Figure 18. POF of FO (PI + PD) cascade and multistage FOPID controller—a comparison.

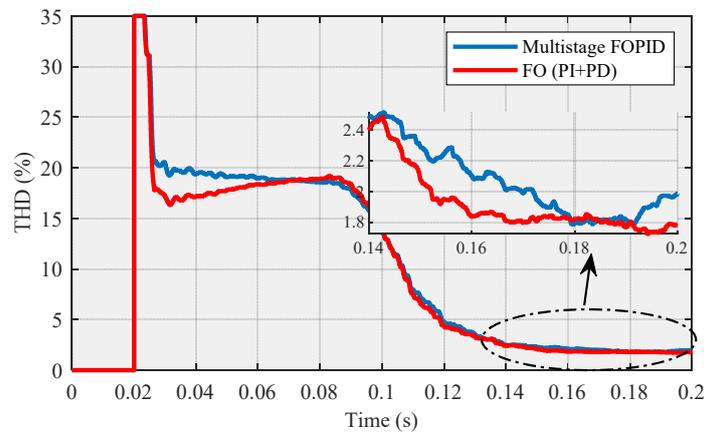


Figure 19. THD of “row no. 6 in Table 1” and “row no. 2 in Table 2”—a comparison.

In the following, it is worth noting that Figure 20 shows that the THD (around 2.1513%), which is related to row no. 9 in Table 1, is much lower than the THD (around 2.8242%), which is seen in row no. 7 in Table 2. As a result, this figure also confirms the superiority of the FO (PI +PD) cascade controller compared to the multistage FOPID controller in this research.

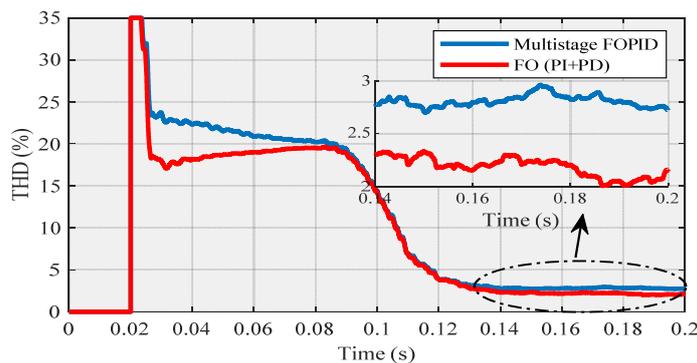


Figure 20. THD of “row no. 9 in Table 1” and “row no. 7 in Table 2”—a comparison.

### 5.2. Case Study 2: THD (up to the 50th Harmonic) and Settling Time Must Synchronously Be Minimized

In the second case study, the THD (up to the 50<sup>th</sup> harmonic) of the source current and settling time were chosen to be minimized at the same time. Therefore, a low THD is necessary, and the transient response of the compensator is momentous, especially when quick and frequent variations occur in the load [22]. In this part, the settling time was computed based on the time needed for the source current THD to reach and stay inside

a  $\pm 2\%$  error band near its steady-state value. The system results that were obtained by means of FO (PI + PD) cascade controller and multistage FOPID controller are as follows.

5.2.1. First Section of the Second Case Study: Applying FO (PI + PD) Cascade Controller

According to Table 3, as stated, ( $K_{p1}, K_i, K_{p2}, K_d, \alpha, \beta$ ) and  $V_{dc}$  are related to POS. THD and  $t_s$  are associated with POF. This table indicates that the lowest THD and the highest settling time are related to row no. 3. Row no. 7 is concerned with the highest THD and the lowest settling time, as shown in Figure 21.

Table 3. POS and POF for FO (PI + PD) cascade controller.

NO	$K_{p1}$	$K_i$	$V_{dc}$	$K_{p2}$	$K_d$	$\alpha$	$\beta$	THD (%)	$t_s$ (s)
1	1.2000	13.9922	816.6667	2.1886	1.2999	0.8416	0.3667	1.8429	0.1130
2	1.2000	13.9922	816.6667	2.1618	0.0100	0.7333	0.6349	1.8836	0.1013
3	2.4667	13.4800	816.6667	2.2449	1.2999	0.8416	0.3667	1.7717	0.1197
4	3.0667	14.2904	552.2070	3.0000	1.3000	0.6000	0.3667	2.7445	0.0643
5	2.6000	10.0000	616.6667	2.1667	0.8700	0.6000	0.1000	2.0936	0.0720
6	2.6000	10.0000	616.6667	2.1618	0.8700	0.9999	0.1000	2.0609	0.0763
7	2.6000	10.0000	500.0000	2.1618	1.3000	0.6002	0.1000	2.7926	0.0590

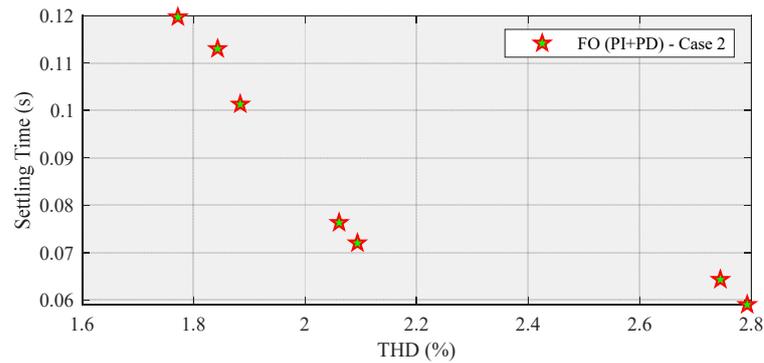


Figure 21. POF for FO (PI + PD) cascade controller.

For a fair comparison in the third section, “row no. 1” should be selected as an example, instead of “row no. 3”, because the POF values related to the first row can thoroughly dominate the values of the corresponding POF in the next table. Therefore, the compensated source current (Figure 22) and THD (Figure 23) diagrams are associated with row no. 1, also  $I_s$  (Figure 24) and THD (Figure 25) diagrams are concerned with row no. 7, as shown below:

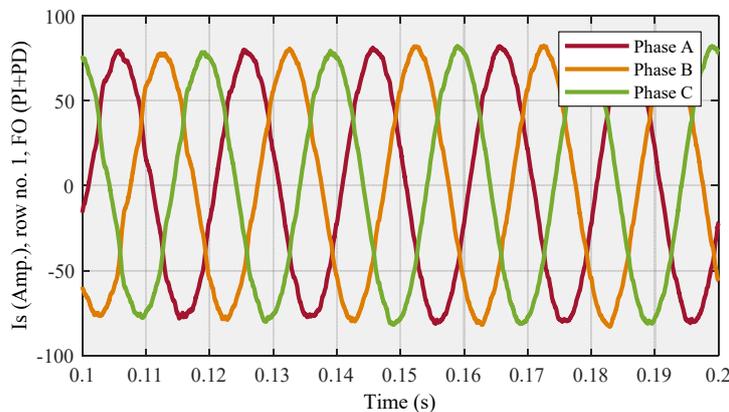


Figure 22. Compensated source current for row no. 1 (THD = 1.8429) using FO (PI + PD) cascade controller.

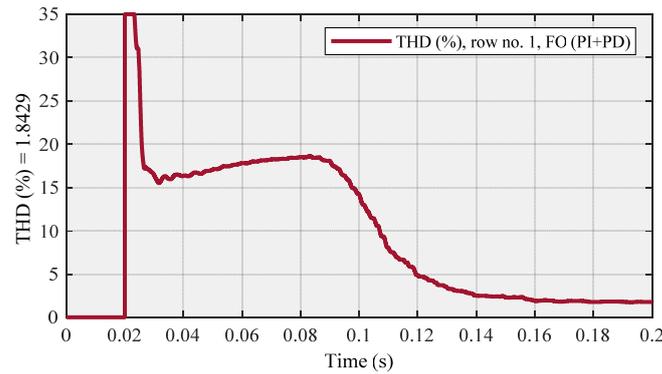


Figure 23. Row no. 1 (with THD = 1.8429 at steady-state) using FO (PI + PD) cascade controller.

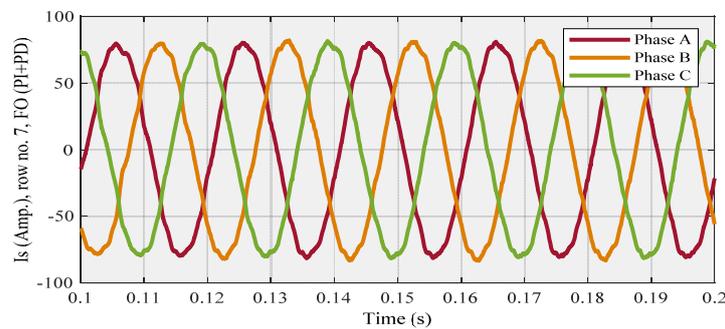


Figure 24. Compensated source current for row no. 7 (highest THD) using FO (PI + PD) cascade controller.

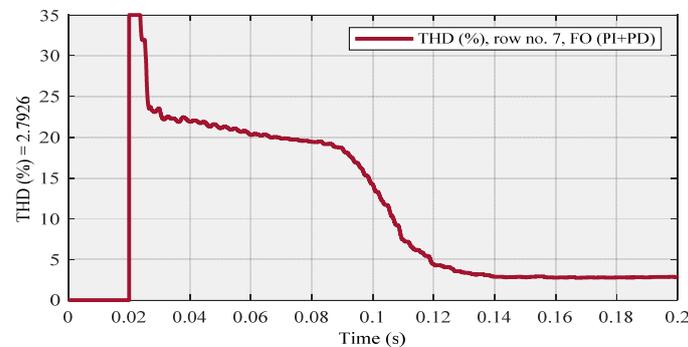


Figure 25. Row no. 7 (with the highest THD at steady-state) using FO (PI + PD) cascade controller.

Figure 23 (row no. 1) and Figure 25 (row no. 7) show the changes in THD using the FO (PI + PD) cascade controller.

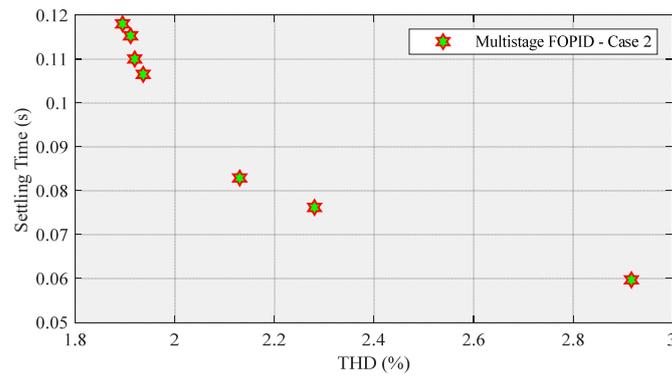
Based on the above-mentioned results, we can recognize that Figure 25, which has a higher THD value, reached steady-state earlier than Figure 23. In other words, Figure 25 has a lower settling time than Figure 23.

### 5.2.2. Second Section of the Second Case Study: Applying Multistage FOPID Controller

According to Table 4, as previously mentioned,  $(K_p, K_i, V_{dc}, K_{pp}, N, K_d, \alpha, \beta)$  are members of POS. THD and  $t_s$  are related to POF. This table shows that the lowest THD and the highest settling time are shown in row no. 1. The highest THD and the lowest settling time are shown in row no. 3, as seen in Figure 26:

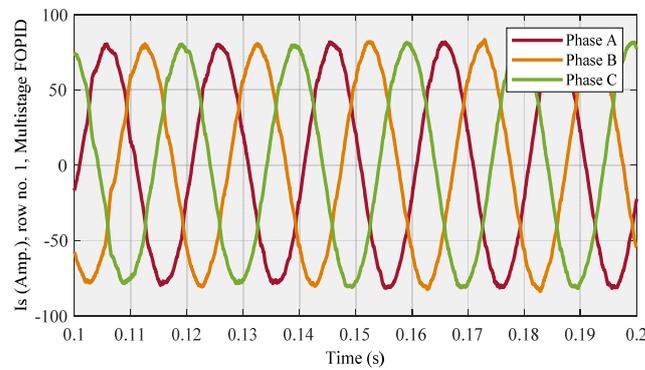
**Table 4.** POS and POF for multistage FOPID controller.

NO	$K_p$	$K_i$	$V_{dc}$	$K_{pp}$	$N$	$K_d$	$\alpha$	$\beta$	THD (%)	$t_s$ (s)
1	2.5434	11.0508	794.7464	11.6264	1.3662	0.8016	0.9822	0.0984	1.8948	0.1180
2	2.5432	11.8920	763.7147	11.9952	1.2958	0.8016	0.9399	0.0321	2.1301	0.0829
3	2.4183	11.7547	490.0000	11.9461	0.1583	1.0000	0.9169	0.0886	2.9171	0.0597
4	2.1557	11.8764	763.7147	11.2523	0.2918	0.4703	0.9822	0.0984	1.9191	0.1100
5	2.1426	11.8998	763.7147	11.2523	0.2754	0.4703	0.9688	0.0984	1.9363	0.1065
6	2.1426	11.8920	763.7147	11.2523	0.2918	0.8016	0.9688	0.0666	1.9108	0.1153
7	2.3213	10.6331	547.4531	11.0189	1.2924	0.2266	0.9267	0.0921	2.2803	0.0762

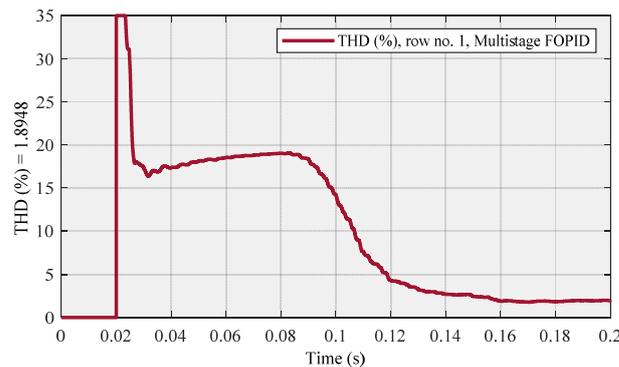


**Figure 26.** POF for multistage FOPID controller.

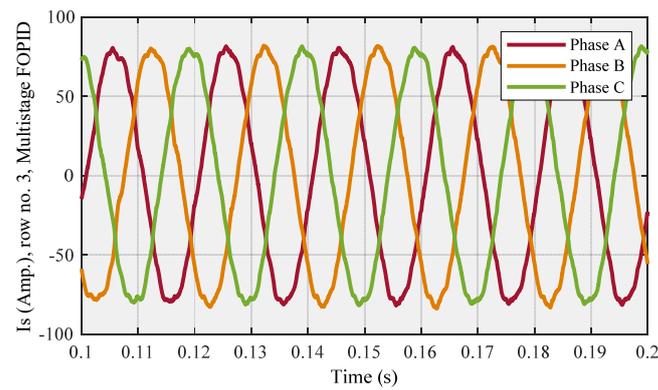
Is (Figure 27) and THD (Figure 28) diagrams are related to row no. 1, also Is (Figure 29) and THD (Figure 30) diagrams are associated with row no. 3, as follows:



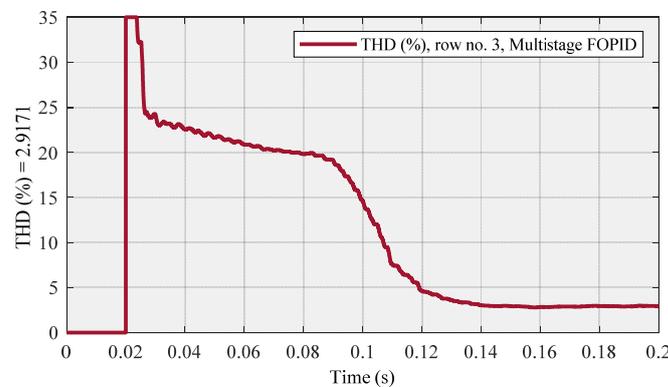
**Figure 27.** Compensated source current for row no. 1 (lowest THD) using multistage FOPID controller.



**Figure 28.** Row no. 1 (with the lowest THD at steady-state) using multistage FOPID controller.



**Figure 29.** Compensated source current for row no. 3 (highest THD) using multistage FOPID controller.



**Figure 30.** Row no. 3 (with the highest THD at steady-state) using multistage FOPID controller.

Figure 28 (row no. 1) and Figure 30 (row no. 3) indicate the variations in THD using a multistage FOPID controller. As in the two aforementioned figures, the difference between the values of THD and settling time is quite explicit.

### 5.2.3. Third Section of the Second Case Study: Comparison between FO (PI + PD) Cascade Controller and Multistage FOPID Controller

In this section, Figure 31 shows a comparison between Figures 21 and 26. As discussed earlier, Figure 21 is related to POF values, which were obtained using FO (PI + PD) cascade controller, and Figure 26 is concerned with POF that was achieved using the multistage FOPID controller. This figure confirms that the values acquired using the FO (PI + PD) cascade controller dominate the values by means of the multistage FOPID controller. Figure 32 shows a comparison between the THD values obtained by the mentioned controllers. The magnified part of this figure affirms that the multistage FOPID controller was dominated by the proposed controller. Moreover, this figure demonstrates that the THD (around 1.8429%), which is associated with the FO (PI + PD) controller, reached steady-state sooner than the THD (around 1.8948%) related to the multistage FOPID controller.

Finally, Figure 33 demonstrates that the THD (around 2.7926%), which is related to row no. 7 in Table 3, is lower than the THD (around 2.9171%), which is seen in row no. 3 in Table 4. Hence, this figure also affirms that the performance of the proposed controller is better than the multistage FOPID controller in this research.

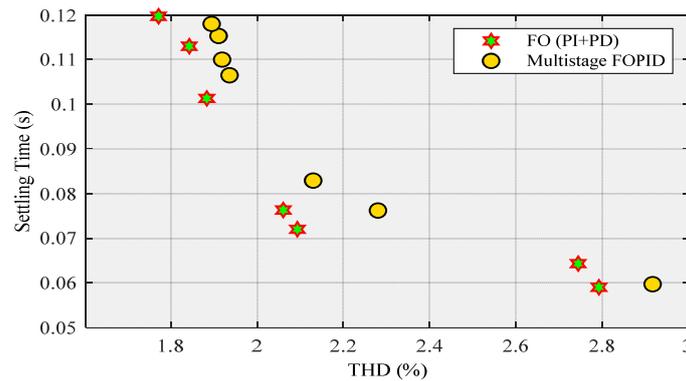


Figure 31. POF of FO (PI + PD) cascade and multistage FOPID controller—a comparison.

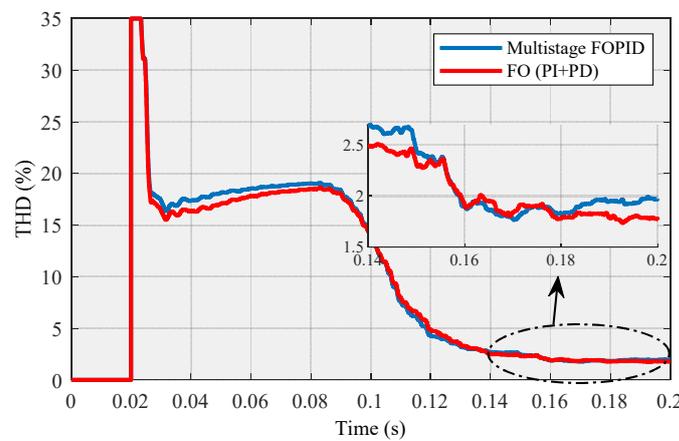


Figure 32. THD of “row no. 1 in Table 3” and “row no. 1 in Table 4”—a comparison.

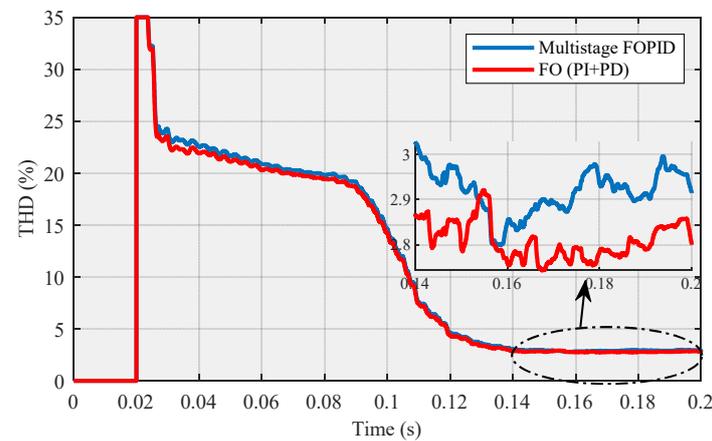


Figure 33. THD of “row no. 7 in Table 3” and “row no. 3 in Table 4”—A comparison.

### 5.3. Summary

In this section, this work and the obtained results are stated. The steps were as follows:

- We designed two different controllers to improve the performance of a shunt active power filter based on the NSGA-II optimization approach.
- The mentioned controllers were the FO (PI + PD) cascade controller and multistage FOPID controller.
- For the first time, we devised a multistage FOPID controller using the inspired multistage PID.
- FO (PI + PD) cascade controller was our proposed controller, which was compared with the other controller.

- The obtained results demonstrate that the first controller is superior to the other one. Table 5 shows the compared THDs with their corresponding  $t_r$  and  $t_s$ .

**Table 5.** POF for FO (PI + PD) cascade/ Multistage FOPID controller—a comparison.

NO	Controller	THD (%)	$t_r$ (s)	THD (%)	$t_s$ (s)
1	FO (PI + PD) cascade	1.8068	0.0388	1.8429	0.1130
2	Multistage FOPID	1.9219	0.0393	1.8948	0.1180
3	FO (PI + PD) cascade	2.1513	0.0366	2.7926	0.0590
4	Multistage FOPID	2.8242	0.0369	2.9171	0.0597

Row no. 1/2 and row no. 3/4 show the lowest/highest THD for each controller, respectively. The obtained POF demonstrates that the lowest values belong to the FO (PI + PD) cascade controller.

## 6. Conclusions

In this paper, two new controllers, called the FO (PI + PD) cascade and multistage FOPID controller, were employed to promote the performance of a 25-kVA parallel active power filter with a repetitive controller. They were devised based on the NSGA-II optimization method, and each controller was applied instead of the classic PI controller in the repetitive controller. Although both are powerful and practical, the FO (PI + PD) cascade controller was the proposed compensator in this study. It should be mentioned that the cascade controller can rapidly reject disturbance before it leaks to the other parts of the system. Eventually, real-time results based on the HiL setup proved that the intended controller has better behavior than the multistage FOPID controller in terms of its steady-state/transient response. Despite the successful performance of the proposed scheme, it suffers from a lack of adaptivity, because the control gains are adjusted in an offline manner. Therefore, the future work can be directed towards the development of robust control design using the training ability of neural networks.

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**Informed Consent Statement:** Not applicable.

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