

Supplementary Information

Enhanced Synaptic Behaviors in Chitosan Electrolyte-Based Electric-Double-Layer Transistors with Poly-Si Nanowire Channel Structures

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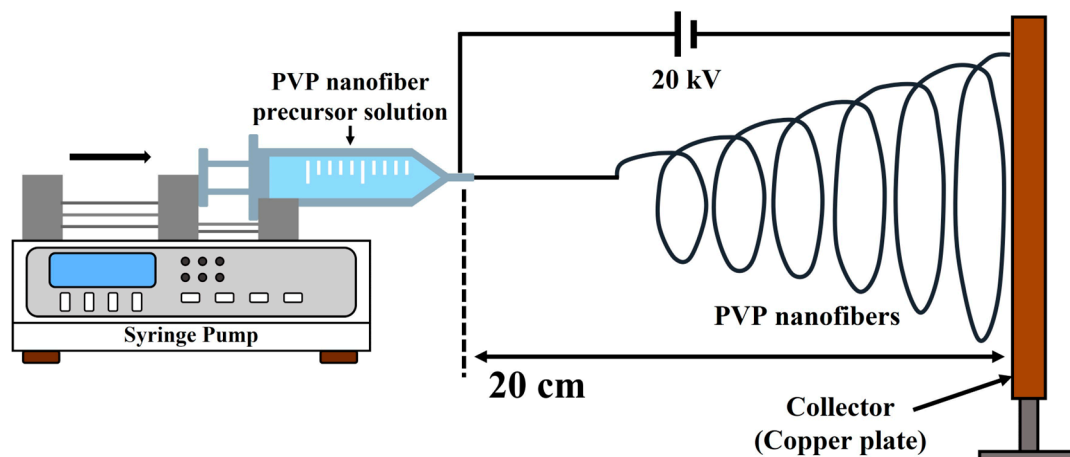


Figure S1. Schematic illustration of electrospinning equipment.

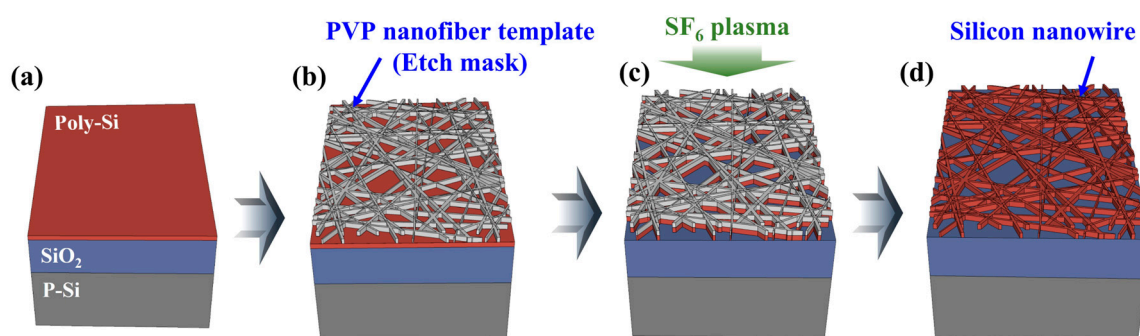


Figure S2. Schematic diagram of the process sequence for poly-Si nanowire channel.

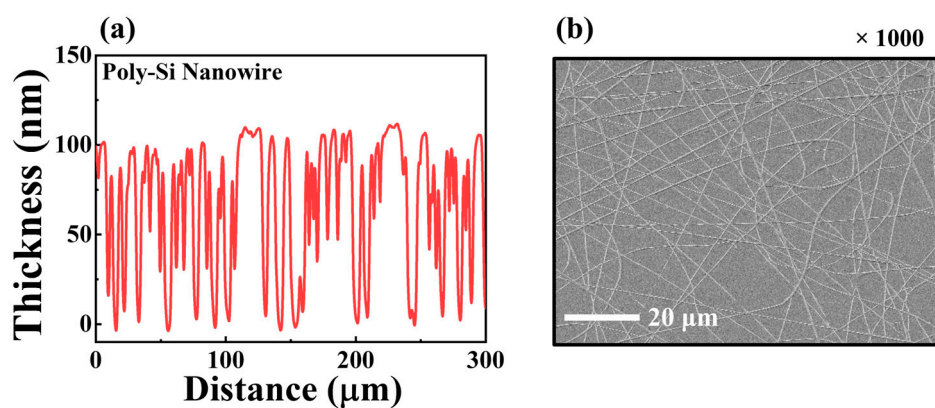


Figure S3. (a) Roughness profile and (b) scanning electron microscopy (SEM) image of the

poly-Si nanowire (NW) channel.

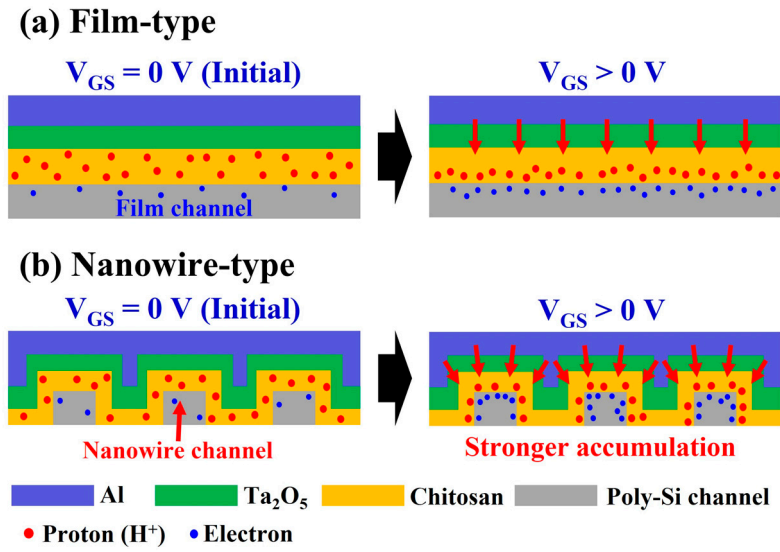


Figure S4. Schematic diagram of proton migration upon applying positive gate voltage in (a) film-type channel and (b) NW-type channel.

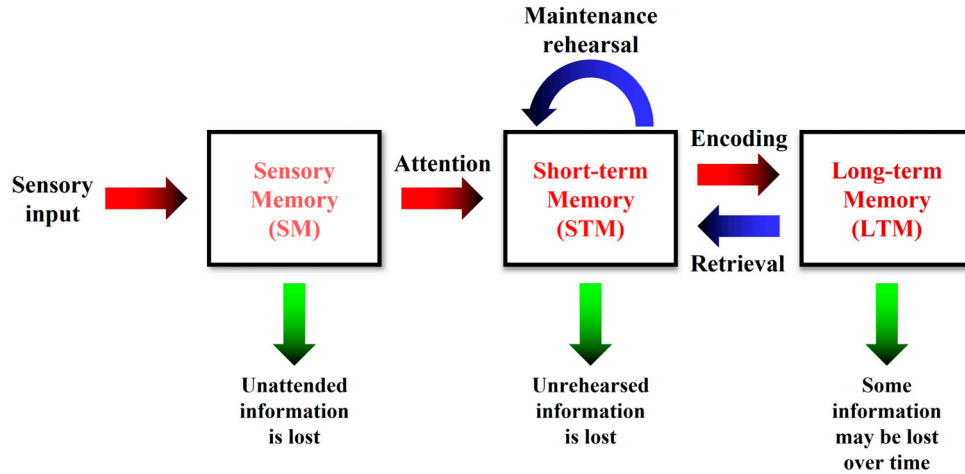


Figure S5. Schematic illustration of the typical model for transitioning from STM to LTM.

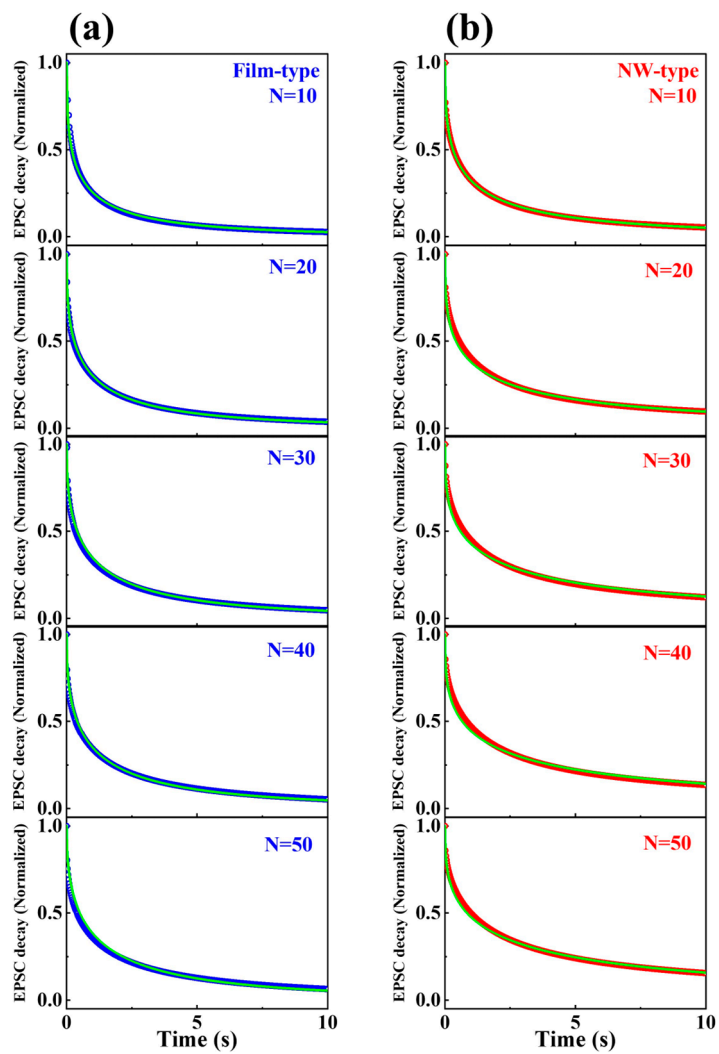


Figure S6. Fitting of synaptic weight decay in (a) film-type and (b) NW-type synaptic transistors.