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Novel Bidirectional Isolated DC/DC Converter with High Gain Ratio and Wide Input Voltage for Electric Vehicle Storage Systems

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Abstract: This study proposes a novel bidirectional isolated DC/DC converter with a high gain ratio and wide input voltage for electric vehicle (EV) storage systems. The DC bus of an EV can be used to charge its battery, and the battery pack can discharge energy to the DC bus through the bidirectional converter when the DC bus lacks power. The input voltage range of the proposed converter is 24 to 58 V on the low-voltage side, which meets the voltage specifications of most servers and batteries on the market. The proposed topology is verified through design, simulation, and implementation, and voltage gain, voltage stress, and current stress are investigated. The control bidirectional converter is simple. Only one set of complementary signals is required for step-up and step-down modes, which greatly reduces costs. The converter also features a continuous current at the low-voltage side, a leakage inductance function for energy recovery, and zero-voltage switching (ZVS) on certain switches, which can prevent voltage spikes on the switches and increase the efficiency of the proposed converter. A bidirectional converter with a total power of 1 kW is used to verify the topology's feasibility and practicability. The power at the low-voltage side was 24–58 V, and the maximum efficiency in step-up mode was 94.5%, 96.5%, and 94.8%, respectively; the maximum efficiency in step-down mode was 94.4%, 95.4%, and 93.7%, respectively.

Keywords: bidirectional DC/DC converter; wide voltage range; zero voltage switching; high voltage conversion ratio

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1. Introduction

The public's awareness of environmental problems is increasing. In response to global warming, renewable energy is gradually replacing power derived from fossil fuels. The burning of fossil fuels causes substantial pollution, such as that from CO_2, SO_2, and particulate matter [1]. These pollutants are detrimental to health and influence climatic conditions. The price of lithium-ion battery pack was around $1100/kWh in 2010, but now it is only $157/kWh in 2021 [2]. Further, MOSFETs, which deliver high current reliably, have been the backbone of converters in recent years [3]. As mentioned above, the development of converters will get better and better.

The application of diverse converters can be divided into three types: AC/DC, DC/DC, and DC/AC converters, as shown in Figure 1. Basic DC/DC converters are broadly divided into two categories: nonisolated converters and isolated converters. Boost converters have been widely applied for maximum power point tracking (MPPT) in solar power systems [4–6]. Buck converters, which step down a voltage from its input to its output, are extensively used in consumer electronics such as laptops [7–9]. Forward and flyback converters are commonly used in industry settings. The flyback converter is the most popular option for isolated DC/DC converters because of its cost effectiveness and high efficiency. However, leakage inductance energy cannot be released when the converter switch is turned off; the high spike on the switch is also a serious problem [10–12].

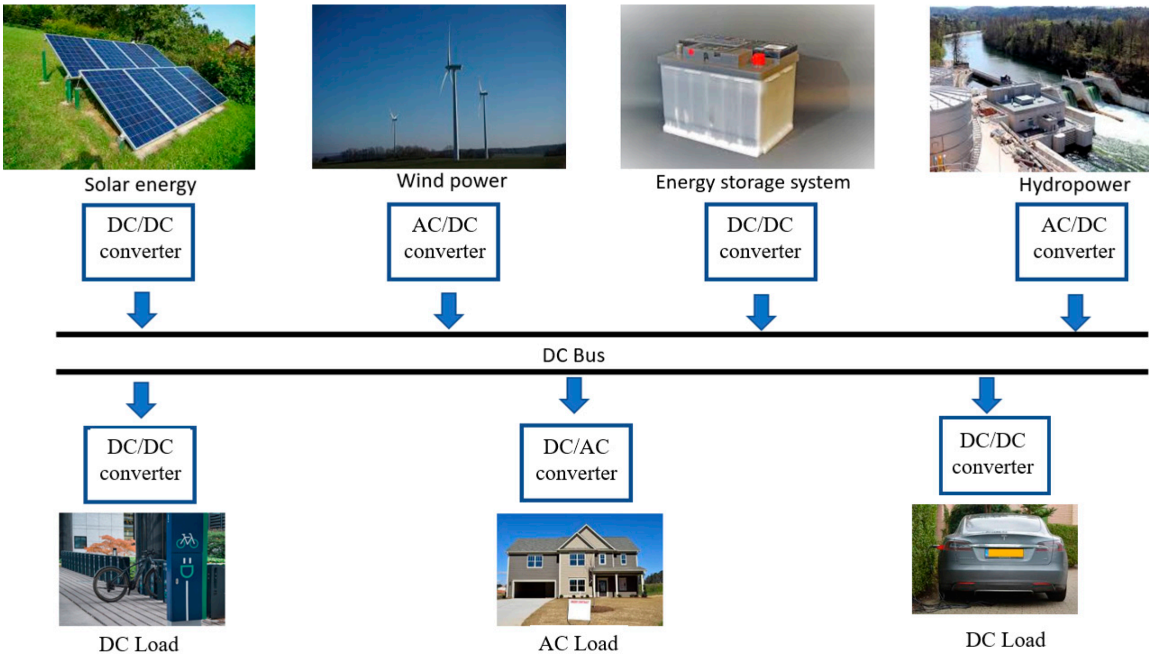

Figure 1. Application of diverse converters with DC buses.

Rapid advancements have been made in bidirectional DC/DC converter technology. The reliability and efficiency of DC/DC converters must be increased for an improvement in power supply. For cost reductions, fewer components used to obtain increased power output is a main research direction. Ref. [13] presents a nonisolated bidirectional DC/DC converter with ZVS technology; its advantages include achieving ZVS and a clamping circuit, but the converter does not apply galvanic isolation. Ref. [14] presents a switched quasi-Z-source nonisolated bidirectional DC/DC converter; it has a wide voltage gain range in step-up and step-down modes. However, it possesses high switching loss and noise because all switches of this converter are operated with hard switching. Ref. [15] presents an isolated bidirectional converter with Cuk topology; it is suitable for photovoltaic (PV) applications because of the wide input voltage range for supporting a wide variety of DC supply equipment. However, high-voltage stress and high-current stress across switches can damage the circuit. Voltage gain bidirectional LLCL resonant DC/DC converters [16] are among the most popular converters and can be adapted for high-power fields, but their control method is complicated. Bidirectional full-bridge converters [17–19] are widely used in EVs, energy storage systems, and uninterruptible power supply (UPS) systems. Such converters contain many components, and their complicated control leads to increased converter costs. An improved current-fed bidirectional DC/DC converter for EVs was developed [20] to achieve ZVS turn-on and ZCS (zero-current switching) turn-off for all power switches, but it only provides 250 W of output power for step-up and step-down modes. This output power is insufficient for EV batteries. Researchers have developed an isolated two-stage bidirectional DC/DC converter for residential energy storage systems [21] and a reactive power elimination bidirectional converter with ripple-free current [22]; these converters have a low output ripple and high voltage gain, but they have two crucial disadvantages: too many components are required and the PWM control signals are complex.

To solve these problems, this study designed a converter to provide flexible power conversion. It can be installed in EVs to supply energy to servers or batteries. A common voltage of servers and batteries for cloud systems is 48 V, and the voltage of a DC bus is 400 V. Therefore, in the proposed converter, low-side voltage V_L is 48 V, and high-side voltage V_H is 400 V. The proposed converter can convert a battery's voltage (24–58 V) to that of a DC bus (400 V) to balance grid energy, as shown in Figure 2.

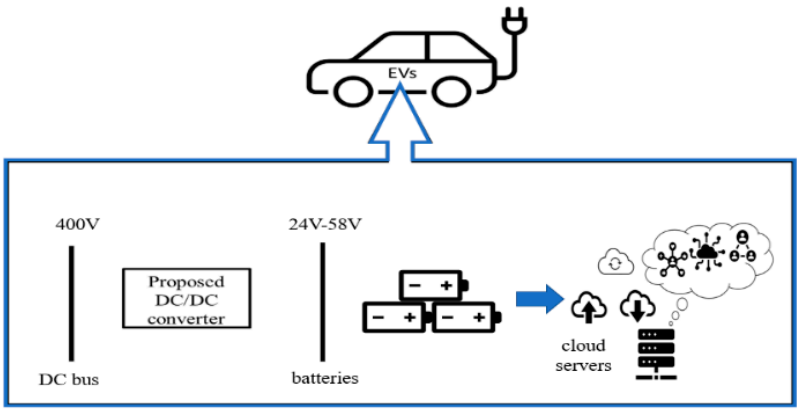

Figure 2. Application of proposed bidirectional isolated DC/DC converter.

2. Circuit Architecture and Operation Principle

Figure 3 presents the circuit architecture of the proposed bidirectional converter. V_H and V_L are the high-voltage side and low-voltage side power ports, respectively. The transformer consists of leakage inductance L_{lk1} and L_{lk2}, as well as magnetizing inductance L_{m1}, for which the turn ratio is N_2:N_1. The proposed converter features six switches (S_1 to S_6). Body diodes D_{S1} to D_{S6} and parasitic capacitances C_{S1} to C_{S6} are the parasitic elements of switches S_1 to S_6. Capacitors C_1 to C_4 and inductor L_1 are components of the proposed converter.

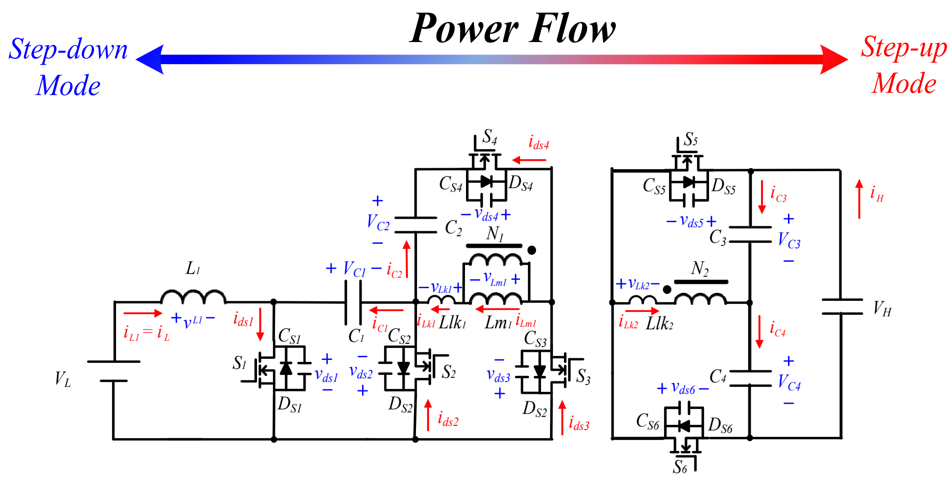

Figure 3. Voltage polarity and current direction of components.

The operating principles and operation mode of the proposed topology in step-up and step-down modes were analyzed. This section details the operating principles of the proposed topology in step-up and step-down modes. The voltage polarity and current direction of components in the topology are presented in Figure 3. To simplify our analysis of the operating principles, several assumptions were made:

(1) All internal resistance and parasitic effects were ignored.
(2) The voltages of the capacitors and the currents of inductors increase and decrease linearly.
(3) The capacitance values of C1, C2, C3, and C4 are infinite.
(4) All magnetic components are operated in CCM.
(5) The turns of N_1 are less than those of N_2, and N_2/N_1 are defined as N.

2.1. Step-Up Mode (Batteries Discharging Mode)

In step-up mode, the complementary PWM signal is composed of two sets of signals, namely, (v_{gs1}, v_{gs3}) and (v_{gs2}, v_{gs4}). The gate signals of S_1 and S_3 are the complementary waveforms of S_2 and S_4. The signals of S_5 and S_6 are in the OFF state. The theoretical waveforms of the proposed topology in step-up mode are presented in Figure 4. One operating cycle features five operation modes, as shown in Figure 5a–e.

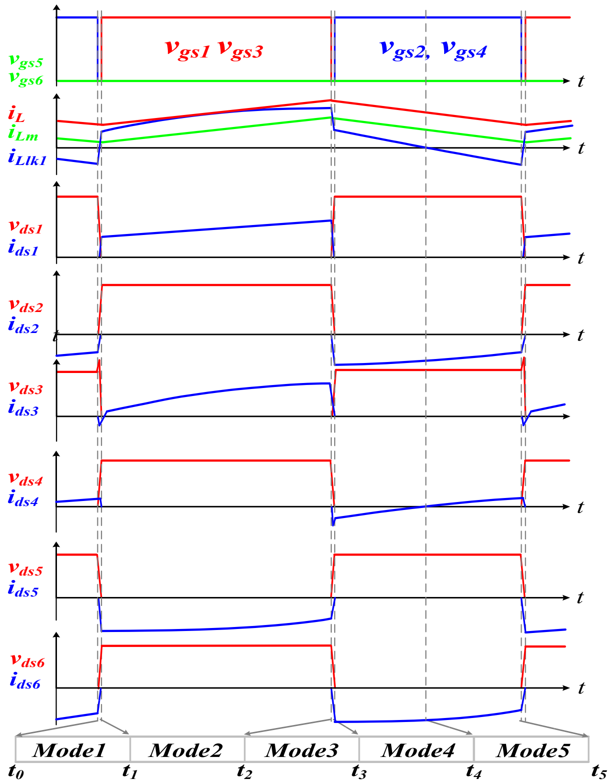

Figure 4. Key waveform of proposed topology in step-up mode.

(1) Mode 1 [t_0–t_1]

The equivalent circuit of Mode 1 is presented in Figure 5a. This mode is operated in a deadtime period. All switch signals are in the OFF state. At the beginning of this mode at time t = t_0, the magnetizing currents of inductor L_1 and coupled inductor Lm_1 start rising. The operation of Mode 1 is followed by that of Mode 5. The energy of the inductor L_1 charges C_1, and C_2 recycles energy from leakage inductance L_{lk1} at the primary side of coupled inductor. To achieve ZVS, the energy of the parasitic capacitance of S_3 is released to ground, and then the parasitic diode of S_3 is turned on. On the high-voltage side, coupled inductor Lm_1 and capacitor C_3 supply energy to capacitor C_4 and V_H through body diode D_{S6} of S_6. Mode 1 ends when S_1 and S_3 turned on.

(2) Mode 2 [t_1–t_2]

The equivalent circuit of Mode 2 is presented in Figure 5b. When S_1 and S_3 are completely turned on at time t = t_1, the low-voltage side V_L supplies energy to inductor $L_{1,}$ and the capacitor C_1 releases energy to magnetizing inductance L_{m1} and leakage inductance L_{lk1}. The magnetizing currents of inductor L_1 and coupled inductor Lm_1 continue rising. A coupled inductor Lm_1 transmits energy from the primary N_1 to the secondary N_2. Subsequently, the energy of capacitor C_4 and coupled inductor Lm_1 charge V_H and C_3 through the body diode D_{S5} of S_5.

(3) Mode 3 [t_2–t_3]

The equivalent circuit of Mode 3 is indicated in Figure 5c. This mode is operated in a deadtime period. All switch signals are in the OFF state. At the start of this mode's operation, at time t = t_2, the magnetizing currents of inductor L_1 and coupled inductor Lm_1 start falling. The energy of the inductor L_1 charges the capacitor C_1. To achieve ZVS, the energy of the S_4 parasitic capacitance is absorbed into leakage inductance L_{lk1}, and then the parasitic diode S_4 is turned on. Capacitor C_2 transmits energy to the coupled inductor

Lm_1 through the parasitic diode S_4. On the high-voltage side, Mode 3 operates in the same manner as Mode 2. Mode 3 ends when S_2 and S_4 are completely turned on.

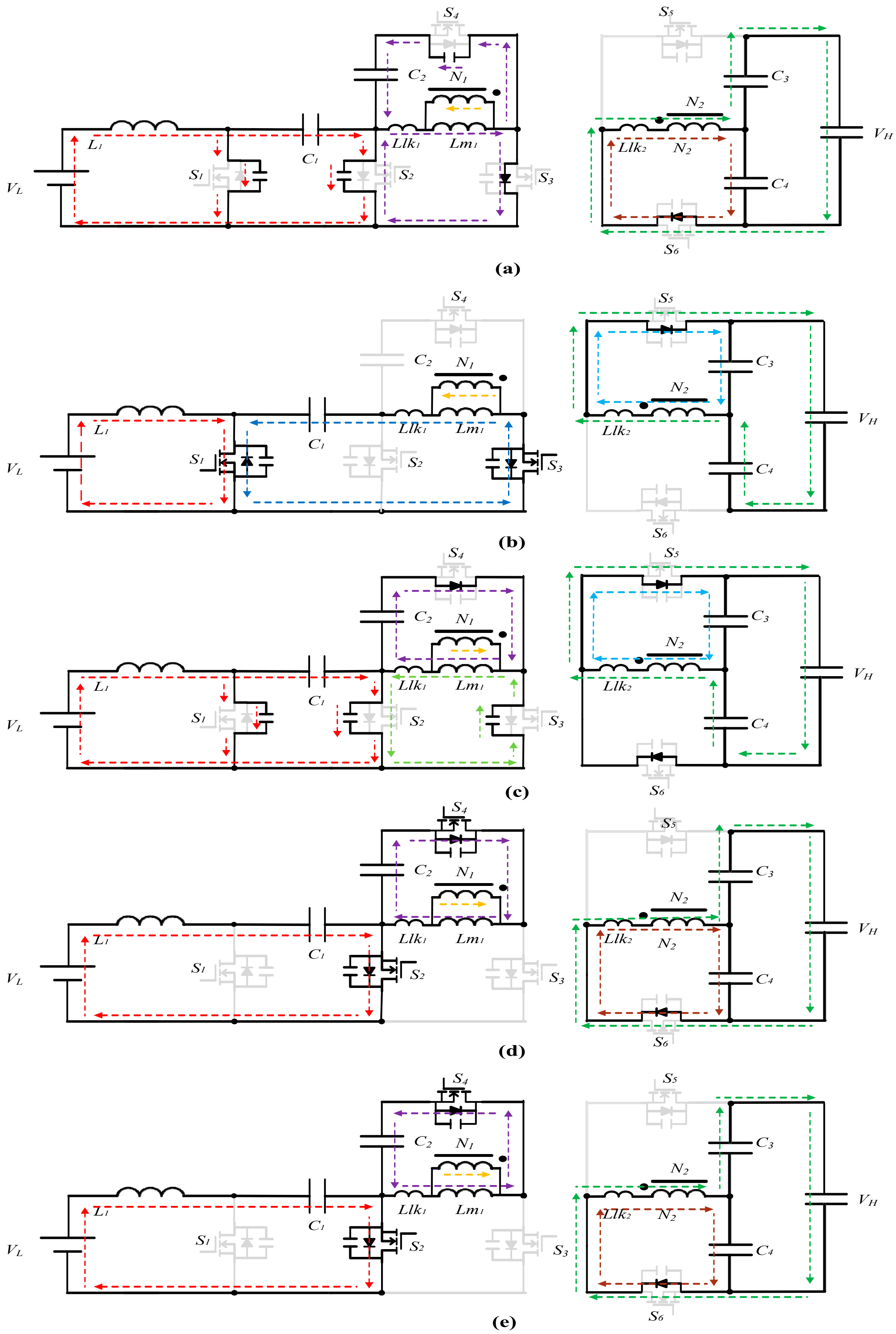

Figure 5. Equivalent circuit in step-up mode. (**a**) Mode 1, (**b**) Mode 2, (**c**) Mode 3, (**d**) Mode 4, and (**e**) Mode 5.

(4) Mode 4 [t_3–t_4]

The equivalent circuit of Mode 4 is presented in Figure 5d. When S_2 and S_4 are completely turned on at time $t = t_3$, inductor L_1 supplies energy to capacitor C_1, and capacitor C_2 recycles the energy of leakage inductance L_{lk1} on the low-voltage side. The magnetizing currents of inductor L_1 and coupled inductor Lm_1 continue falling. On the high-voltage side, Mode 4 operates in the same manner as Mode 5 and Mode 1. Mode 4 ends when inductance i_{Llk1} drops to zero.

(5) Mode 5 [t_4–t_5]

The equivalent circuit of Mode 5 is presented in Figure 5e. At time $t = t_4$, the switch signals are the same as those in the previous mode during this time interval. Mode 5 operates in a similar manner to Mode 4, but in this mode, capacitor C_2 releases energy to magnetizing inductance L_{m1} and leakage inductance L_{lk1}. Coupled inductor Lm_1 transmits energy from the primary N_1 to the secondary N_2.

2.2. Step-Down Mode (Batteries Charging Mode)

In step-down mode, the complementary PWM signal is composed of two sets of signals: (1) v_{gs1}, v_{gs3}, and v_{gs5} and (2) v_{gs2}, v_{gs4}, and v_{gs6}. The gate signals of S_1, S_3, and S_5 are complementary waveforms of S_2, S_4, and S_6. The theoretical waveforms of the proposed topology in step-up mode are detailed in Figure 6. One operating cycle features five operation modes, as shown in Figure 7a–e.

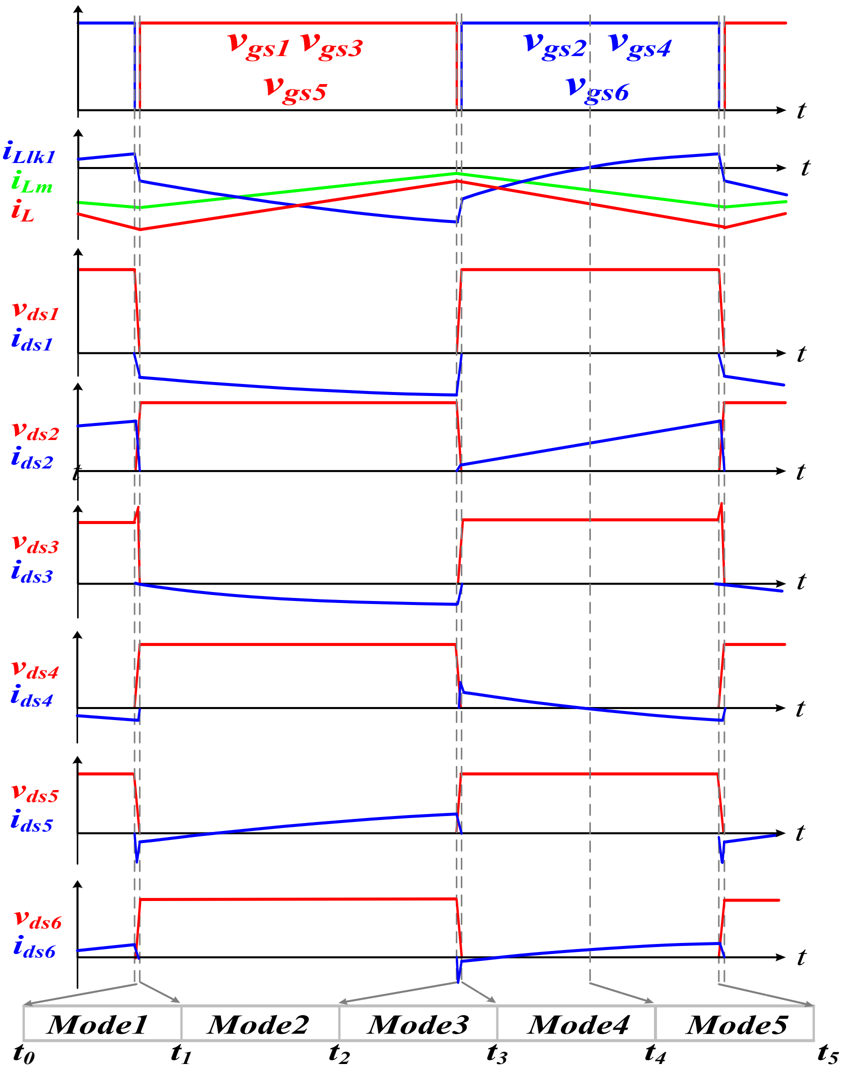

Figure 6. Key waveforms of the proposed topology in step-down mode.

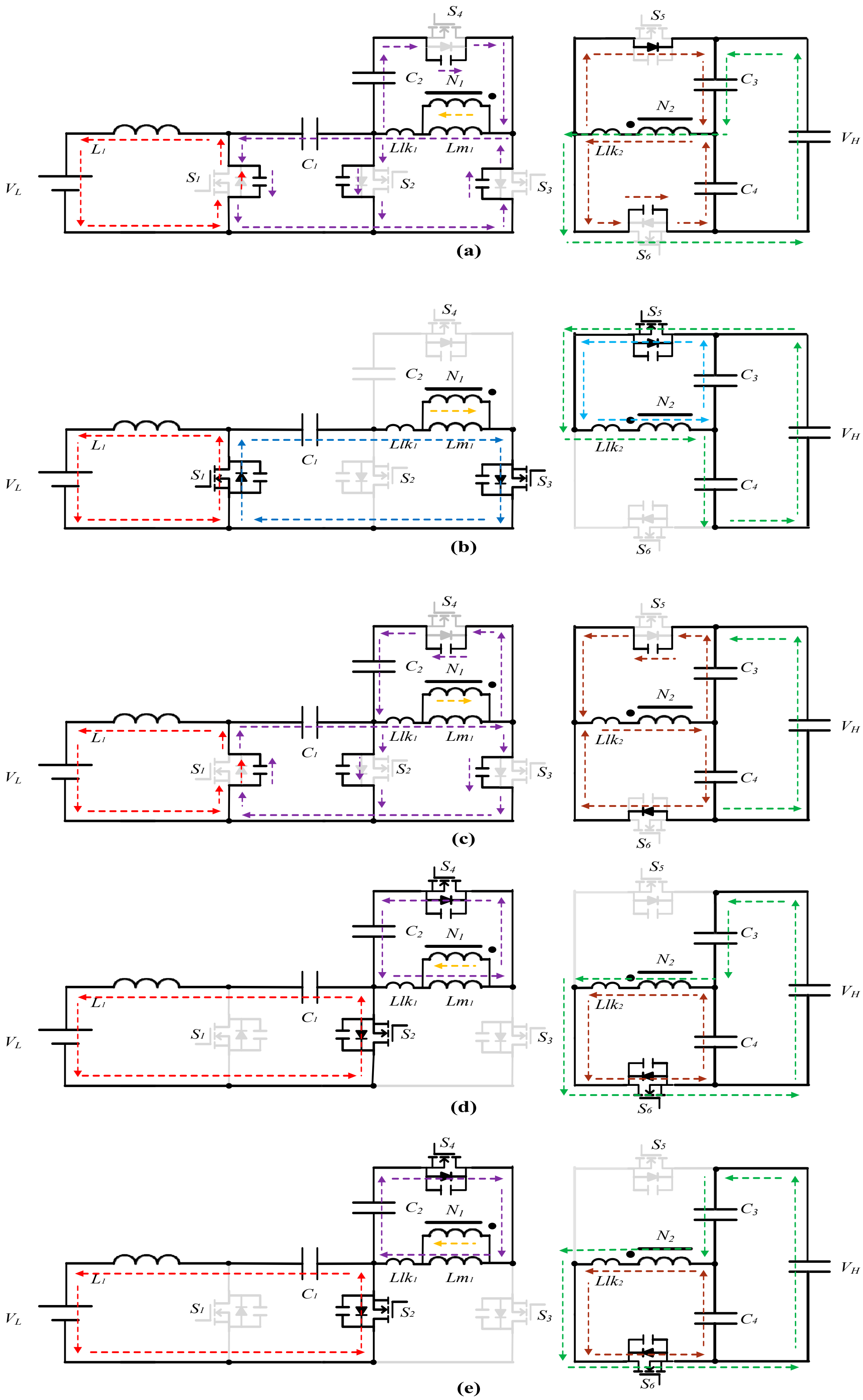

Figure 7. Equivalent circuit in step-down mode. (**a**) Mode 1, (**b**) Mode 2, (**c**) Mode 3, (**d**) Mode 4, and (**e**) Mode 5.

(1) Mode 1 [t0–t1]

The equivalent circuit of Mode 1 is illustrated in Figure 7a. This mode operates in a deadtime period. All switch signals are in the OFF state. On the high-voltage side, V_H charges the capacitor C_3. To achieve ZVS, the energy of parasitic capacitance S_5 is absorbed into capacitor C_3, and then the parasitic diode S_5 is turned on. Capacitor C_4 charges the coupled inductor L_{m1} until the end of this mode's operation at time t = t0. Mode 1 is followed by Mode 5. C_1 continuously charges inductor L_1, and C_2 recycles the energy of leakage inductance L_{lk1}. Mode 1 ends when S_1, S_3, and S_5 are completely turned on.

(2) Mode 2 [t_1–t_2]

The equivalent circuit of Mode 2 is presented in Figure 7b. When S_1, S_3, and S_5 are completely turned on at time $t = t_1$, V_H and C_3 charge capacitor C_4 via N2 at the high-voltage side. The magnetizing currents of inductor L_1 and coupled inductor Lm1 continue falling. Coupled inductor L_{m1} transmits energy to C_2. Inductor L_1 supplies energy to V_L on the low-voltage side.

(3) Mode 3 [t_2–t_3]

The equivalent circuit of Mode 3 is presented in Figure 7c. This mode operates during a deadtime period. All switch signals are in the OFF state. At the beginning of this mode's operation at time $t = t_2$, on the high-voltage side, V_H and C_3 charge C_4 and L_{m1}. The magnetizing currents of L_1 and L_{m1} start rising. To achieve ZVS, the energy of parasitic capacitance S_6 is absorbed into leakage inductance L_{lk2}, and then parasitic diode S_6 is turned on. C_3 charges L_{m1} until the end of this mode at time $t = t_{3.}$ L_1 continuously supplies energy to V_L. C_2 charges L_{m1} on the low-voltage side. Mode 3 ends when S_2, S_4, and S_6 are completely turned on.

(4) Mode 4 [t_3–t_4]

The equivalent circuit of Mode 4 is illustrated in Figure 7d. When S_1, S_3, and S_5 are completely turned on at time $t = t_3$, V_H charges C_3. Capacitor C_4 supplies energy to Lm_1 on the high-voltage side. The magnetizing currents of L_1 and L_{m1} continue rising. C_2 continuously charges coupled inductor L_{m1}, and C_1 releases energy to L_1 on the low-voltage side. Mode 4 ends when current of leakage inductance i_{Llk1} drops to zero.

(5) Mode 5 [t_4–t_5]

The equivalent circuit of Mode 5 is presented in Figure 7e. At time $t = t_4$, the switch signals are the same as those in the previous mode. Mode 5 operates in a similar manner to Mode 4, but in this mode, C_2 recycles the energy of leakage inductance L_{lk1}.

3. Steady-State Analysis

In step-up mode, the complementary PWM signal is composed of two sets of signals. The switching period is D_1T_S. v_{gs1} and v_{gs3} are turned ON, and v_{gs2} and v_{gs4} are turned ON for time (1-D_1)T_S.

In step-down mode, the complementary PWM signal is composed of two sets of signals. v_{gs1}, v_{gs3}, and v_{gs5} are turned ON for time D_6T_S, and v_{gs2}, v_{gs4}, and v_{gs6} are turned OFF for time (1-D_6)T_S. Our steady-state analysis of the proposed topology is based on the following assumptions:

(1) All internal resistance and parasitic effects are ignored.
(2) The currents of the inductors and voltages of the capacitors increase and decrease linearly.
(3) N_2/N_1 are defined as N.
(4) All magnetic components are operated in CCM.
(5) The capacitance values of C_1, C_2, C_3, and C_4 are infinite.

3.1. Step-Up Mode (Batteries Discharging Mode)

(1) Voltage Gain Analysis

On the basis of the voltage–second balance for an inductor, the relationship between V_{C1}, V_{C2}, V_{C3}, V_{C4}, and V_L can be expressed as follows:

$$V_{C1} = \frac{1}{1-D_1}V_L \tag{1}$$

$$V_{C3} = NV_{C1} \tag{2}$$

These equations are solved simultaneously, where V_{C3} is given by

$$V_{C3} = \frac{N}{1-D_1}V_L \tag{3}$$

Equation (1) is substituted into (4)

$$V_{C4} = \frac{ND_1}{1-D_1}V_{C1} \tag{4}$$

where V_{C4} is given by

$$V_{C4} = \frac{ND_1}{(1-D_1)^2}V_L \tag{5}$$

Equation (1) is substituted into (6)

$$V_{C4} = NV_{C2} \tag{6}$$

where V_{C2} is given by

$$V_{C2} = \frac{D_1}{(1-D_1)^2}V_L \tag{7}$$

In accordance with the Mode 2 of step-up mode, the relationships between V_H, V_{C1}, and V_{C3} can be expressed as follows:

$$V_H = NV_{C1} + V_{C4} \tag{8}$$

By substituting (1) and (7) into (8), we can obtain the voltage gain in step-up mode $G_{step\text{-}up}$ as follows:

$$G_{step-up} = \frac{V_H}{V_L} = \frac{N}{(1-D_1)^2} \tag{9}$$

Figure 8 presents the relationship between voltage gain and duty cycle in step-up mode.

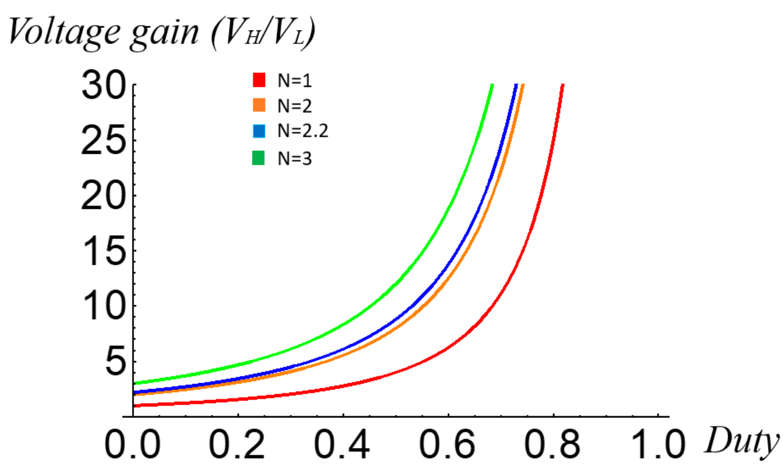

Figure 8. Relationship between voltage gain and duty cycle in step-up mode.

(2) Voltage Stress Analysis of Components

On the basis of the equivalent circuit during D_1T_S, the voltage across S_2 is V_{C1}, and the voltage across S_4 is the sum of V_{C1} and V_{Lm1}. The voltage stress on S_6 is V_H. The voltage stresses on the switch are as follows:

$$V_{S2,stress} = V_{C1} = \frac{1-D_1}{N}V_H = \frac{1}{1-D_1}V_L \tag{10}$$

$$V_{S4,stress} = V_{C1} + V_{C2} = \frac{1}{N}V_H = \frac{1}{(1-D_1)^2}V_L \tag{11}$$

$$V_{S6,stress} = V_H = \frac{N}{(1-D_1)^2}V_L \tag{12}$$

On the basis of the equivalent circuit during $(1-D_1)T_S$, the voltage stress on S_1 is V_{C1}. The voltage across S_3 is V_{C2}, and the voltage across S_5 is V_H. The voltage stresses on the switches are as follows:

$$V_{S1,stress} = V_{C1} = \frac{1-D_1}{N}V_H = \frac{1}{1-D_1}V_L \tag{13}$$

$$V_{S3,stress} = V_{C2} = \frac{D_1}{N}V_H = \frac{D_1}{(1-D_1)^2}V_L \tag{14}$$

$$V_{S5,stress} = V_H = \frac{N}{(1-D_1)^2}V_L \tag{15}$$

The voltage stresses of the capacitor are as follows:

$$V_{C1,stress} = \frac{(1-D_1)}{N}V_H = \frac{1}{(1-D_1)}V_L \tag{16}$$

$$V_{C2,stress} = \frac{D_1}{N}V_H = \frac{D_1}{(1-D_1)^2}V_L \tag{17}$$

$$V_{C3,stress} = (1-D_1)V_H = \frac{N}{(1-D_1)}V_L \tag{18}$$

$$V_{C4,stress} = D_1V_H = \frac{ND_1}{(1-D_1)^2}V_L \tag{19}$$

(3) Current Stress Analysis of Components

On the basis of the equivalent circuit during D_1T_S, the induced current of the coupled inductor Lm_1 and i_{C4} flows through the parasitic diode of S_5 to release energy to C_3 and i_H. On the low-voltage side, no current flows to C_2. C_1 releases energy to Lm_1. According to Kirchhoff's current law, the currents of i_{C3}, i_{C4}, i_{C2}, and i_{C1} can be expressed as follows:

$$i_{C3} = i_{ds5} + i_H \tag{20}$$

$$i_{C4} = -i_H \tag{21}$$

$$i_{C2} = 0 \tag{22}$$

$$i_{C1} = i_{Lm1} + Ni_{ds5} \tag{23}$$

According to the equivalent circuit during $(1-D_1)T_S$, the induced current of the coupled inductor iLm_1 and i_{C3} flows through the parasitic diode of S_6 to release energy to C_4 and i_H. On the low-voltage side, no current flows to C_2 and S_4 because leakage inductance is neglected. L_1 releases energy to C_1.

$$i_{C3} = -i_H \tag{24}$$

$$i_{C4} = i_{ds6} + i_H \tag{25}$$

$$i_{C2} = 0 = i_{ds4} \tag{26}$$

$$i_{C1} = i_{L1} \tag{27}$$

According to the ampere–second balance of a capacitor, the average current through a capacitor for steady-state operation is zero. The relationships between i_{ds4}, i_{ds5}, i_{ds6} and i_H can be expressed as follows:

$$i_{ds4} = 0 \tag{28}$$

$$i_{ds5} = \frac{i_H}{D_5} \tag{29}$$

$$i_{ds6} = \frac{i_H}{1 - D_5} \tag{30}$$

On the basis of the Mode 2 of step-up mode, the relationship between i_{ds1} and i_{ds3} can be expressed as follows:

$$i_{ds1} = \frac{N}{D_1(1 - D_1)^2} i_H \tag{31}$$

$$i_{ds3} = \frac{N}{D_1(1 - D_1)} i_H \tag{32}$$

On the basis of the Mode 4 of step-up mode, the i_{ds2} can be expressed as follows:

$$i_{ds1} = -\frac{N}{D_1(1 - D_1)^2} i_H \tag{33}$$

3.2. *Step-down Mode (Batteries Charging Mode)*

(1) Voltage GainAnalysis

On the basis of the voltage–second balance of an inductor, the relationships between V_{C1}, V_{C2}, V_{C3}, V_{C4}, and V_H can be expressed as follows:

$$V_{C1} = \frac{1 - D_5}{ND_5} V_{C4} \tag{34}$$

$$V_{C4} = D_5 V_H \tag{35}$$

where V_{C1} is given by

$$V_{C1} = \frac{1 - D_5}{N} V_H \tag{36}$$

Substituting (35) into (37) provides the following equation:

$$V_{C2} = \frac{1}{N} V_{C4} \tag{37}$$

where V_{C2} is given by

$$V_{C2} = \frac{D_5}{N} V_H \tag{38}$$

where V_{C3} is given by

$$V_{C3} = (1 - D_5) V_H \tag{39}$$

On the basis of the voltage–second balance of an inductor, the relationship between V_{C1} and V_L can be expressed as follows:

$$V_{C1} = \frac{1}{1 - D_5} V_L \tag{40}$$

By substituting (1) into (2), we can obtain the voltage gain in step-up mode $G_{step\text{-}down}$ as follows:

$$G_{step-down} = \frac{V_L}{V_H} = \frac{(1-D_5)^2}{N} \tag{41}$$

Figure 9 presents the relationship between voltage gain and duty cycle operated in step-down mode.

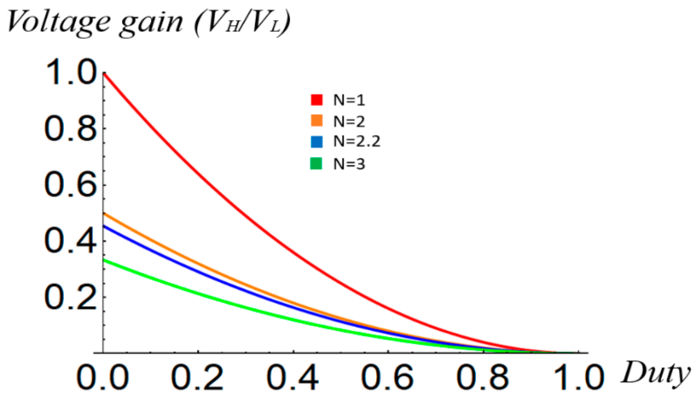

Figure 9. Voltage gain versus duty cycle in step-down mode.

(2) Voltage Stress Analysis of Components

On the basis of the equivalent circuit during D_5T_S, the voltage across S_2 is V_{C1}, and the voltage across S_4 is V_{C2}. The voltage stress on S_6 is V_H. The voltage stresses on the switches are as follows:

$$V_{S2,stress} = V_{C1} = \frac{1-D_5}{N}V_H = \frac{1}{1-D_5}V_L \tag{42}$$

$$V_{S4,stress} = V_{C1} + V_{C2} = \frac{1}{N}V_H = \frac{1}{(1-D_5)^2}V_L \tag{43}$$

$$V_{S6,stress} = V_H = \frac{N}{(1-D_5)^2}V_L \tag{44}$$

On the basis of the equivalent circuit during $(1-D_5)T_S$, the voltage across S_1 is V_{C1}. The voltage across S_3 is V_{C2}. The voltage stress on S_5 is V_H. The voltage stresses of the switches are as follows:

$$V_{S1,stress} = V_{C1} = \frac{1-D_5}{N}V_H = \frac{1}{1-D_5}V_L \tag{45}$$

$$V_{S3,stress} = V_{C2} = \frac{D_5}{N}V_H = \frac{D_5}{(1-D_5)^2}V_L \tag{46}$$

$$V_{S5,stress} = V_H = \frac{N}{(1-D_5)^2}V_L \tag{47}$$

The voltage stresses of the capacitor are as follows:

$$V_{C1,stress} = \frac{1-D_5}{N}V_H = \frac{1}{1-D_5}V_L \tag{48}$$

$$V_{C2,stress} = \frac{D_5}{N}V_H = \frac{D_5}{(1-D_5)^2}V_L \tag{49}$$

$$V_{C3,stress} = D_1V_H = \frac{ND_1}{(1-D_1)^2}V_L \tag{50}$$

$$V_{C4,stress} = (1 - D_1)V_H = \frac{N}{(1 - D_1)}V_L \quad (51)$$

(3) Current Stress Analysis of Components

On the basis of the equivalent circuit during D_5T_S, V_H charges C_4. C_3 transmits energy to C_1 through Lm_1, S_1, and S_3. C_2 has no current. The inductor L_1 releases energy to V_L. According to Kirchhoff's current law, the currents flowing to C_1-C_4 can be represented as follows:

$$i_{C1} = -i_{ds1} + i_{L1} = -i_{ds3} \quad (52)$$

$$i_{C2} = 0 \quad (53)$$

$$i_{C3} = i_H - i_{ds5} \quad (54)$$

$$i_{C4} = i_H \quad (55)$$

On the basis of the equivalent circuit during $(1-D_5)T_S$, V_H charges capacitor C_3. C_4 transmits energy to Lm_1. C_2 and S_4 still have no current at this time because leakage inductance is neglected. C_1 releases energy to L_1 through S_2. According to Kirchhoff's current law, the currents of i_{C1}, i_{C2}, i_{C3}, and i_{C4} can be expressed as follows:

$$i_{C1} = i_{L1} = -i_{ds2} \quad (56)$$

$$i_{C2} = 0 = i_{ds4} \quad (57)$$

$$i_{C3} = i_H \quad (58)$$

$$i_{C4} = i_H - i_{ds6} \quad (59)$$

On the basis of the ampere–second balance of a capacitor, the average current through a capacitor for steady-state operation is zero. The relationships between i_{ds4}, i_{ds5}, i_{ds6} and i_H can be expressed as follows:

$$i_{ds1} = i_{L1} \quad (60)$$

$$i_{ds2} = -(1 - D_5)i_{L1} \quad (61)$$

$$i_{ds3} = (1 - D_5)i_{L1} \quad (62)$$

$$i_{ds4} = 0 \quad (63)$$

$$i_{ds5} = -\frac{(1 - D_5)^2}{ND_5}i_{L1} \quad (64)$$

$$i_{ds6} = -\frac{1 - D_5}{N}i_{L1} \quad (65)$$

3.3. Magnetic Component Design

The magnetic components of the proposed converter are designed in CCM, and the maximum currents of L_1 and L_{m1} are determined as follows:

$$i_{L1,max} = I_{L1,avg} + \frac{\Delta i_{L1}}{2} \quad (66)$$

$$i_{Lm1,max} = I_{Lm1,avg} + \frac{\Delta i_{Lm1}}{2} \quad (67)$$

The minimum currents of L_1 and L_{m1} are as follows:

$$i_{L1,min} = I_{L1,avg} - \frac{\Delta i_{L1}}{2} \quad (68)$$

$$i_{Lm1,min} = i_{Lm1,avg} - \frac{\Delta i_{Lm1}}{2} \quad (69)$$

When the switch S_1 is turned off, the current Δi_{L1} and Δi_{Lm1} are as follows:

$$\Delta i_{L1} = \frac{V_{L1}}{L_1} D_1 T_S \tag{70}$$

$$\Delta i_{Lm1} = \frac{V_{Lm1}}{L_{m1}} D_1 T_S \tag{71}$$

While the magnetic components are operated in the boundary conduction mode (BCM; Figures 10 and 11), currents $i_{L1,\ min}$ and $i_{Lm1,\ min}$ are equal to zero. The $i_{L1,\ min}$ current can be expressed as follows:

$$i_{L1,min} = 0 = \frac{N}{(1-D_1)^2} i_H - \frac{(1-D_1)^2 D_1 T_s}{2L_1 N} V_H \tag{72}$$

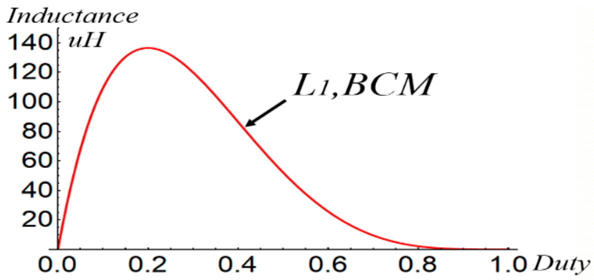

Figure 10. $L_{1,\ BCM}$ in step-up mode.

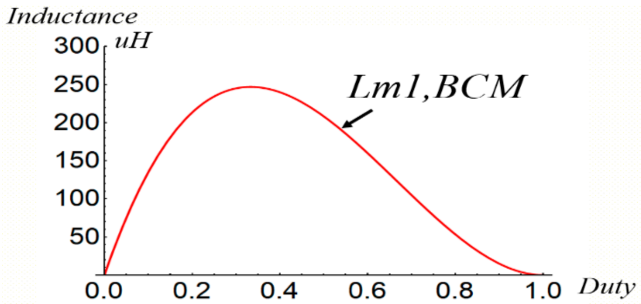

Figure 11. $Lm_{1,\ BCM}$ in step-up mode.

Similarly, the $i_{Lm1,\ min}$ currents can be expressed as follows:

$$i_{Lm1,min} = 0 = \frac{N}{1-D_1} i_H - \frac{(1-D_1)D_1}{2L_{m1} f_s N} V_H \tag{73}$$

After (24) and (25) are simplified, $L_{1,BCM}$ and $L_{m1,BCM}$ can be obtained as follows:

$$L_{L1,BCM} = \frac{(1-D_1)^4 D_1}{2 f_s N^2} \frac{V_H}{i_{H,BCM}} \tag{74}$$

$$L_{m1,BCM} = \frac{(1-D_1)^2 D_1}{2 f_s N^2} \frac{V_H}{i_{H,BCM}} \tag{75}$$

4. Experimental Results

The measured waveforms were used to verify the correctness and feasibility of the proposed topology. The key waveforms in step-up and step-down modes were measured separately and compared with the simulated waveforms. Finally, the conversion efficiency levels of step-up and step-down modes were measured. Table 1 shows the electrical specifications and component parameters of proposed topology. A photograph of the proposed bidirectional isolated DC/DC converter with a microcontroller (MCU) is presented in Figure 12.

Table 1. Electrical specifications of proposed topology.

Parameter	Specification
High-side power P_H	1000 W
Low-side power P_L	1000 W
High-side voltage V_H	400 V
Low-side voltage V_L	24–58 V
Switching frequency fs	40 kHz
Power switches S_1, S_2, and S_3	IRFP4568PbF
Power switch S_4	IRFP4768PbF
Power switches S_5 and S_6	IXFH50N50P3
Inductor L_1	47 µH
Magnetizing inductance L_{m1}	190 µH
Leakage inductance L_{lk1}	2.4 µH
Capacitor C_1	100 µF
Capacitor C_2	70 µF
Capacitor C_3 and C_4	220 µF
Turns ratio N	2.2

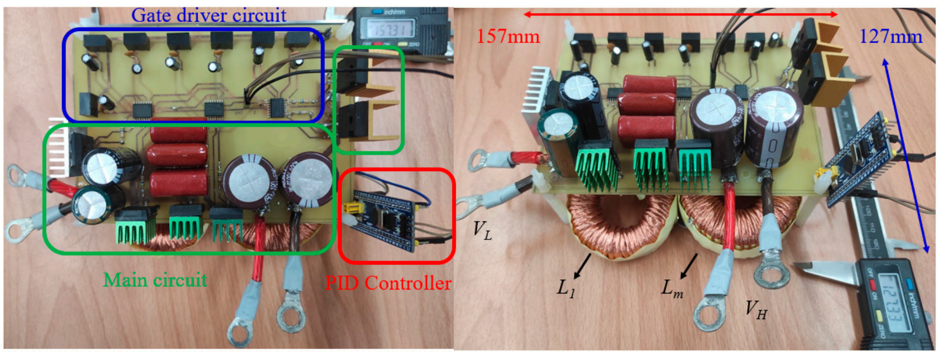

Figure 12. Photograph of the proposed converter.

A proportional–integral–derivative (PID) controller is used to control the proposed converter and presented in Figure 13. The overall control function is:

$$K_{\mathrm{p}}e(t) + K_{\mathrm{i}}\int_0^t e(\tau)\mathrm{d}\tau + K_{\mathrm{d}}\frac{\mathrm{d}e(t)}{\mathrm{d}t} \tag{76}$$

In both modes, by receiving voltage feedback from a voltage divider circuit at the other voltage side, the MCU generates PWM signals to control the duty cycle of switches to achieve stable output voltage. The PID parameters are Kp = 0.3, Ki = 0.04, and Kd = 0.001, respectively. In step-down mode, to alter the input voltage (24–58 V), the MCU generates PWM signals to control the duty of switches to achieve stable output voltages. The PID parameters are Kp = −0.275, Ki = −0.1, and Kd = −0.01, respectively.

During measurement, V_L was maintained at 24–58 V, and the high-voltage side V_H was maintained at 400 V. Figures 14–16 present the measured waveforms of the low-voltage side at 24, 48, and 58 V at full load in step-up mode.

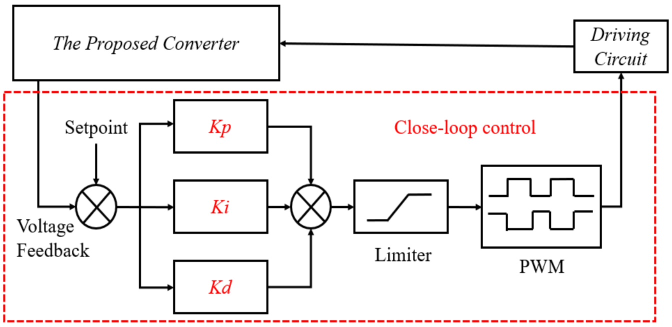

Figure 13. Closed-loop control scheme of the proposed converter.

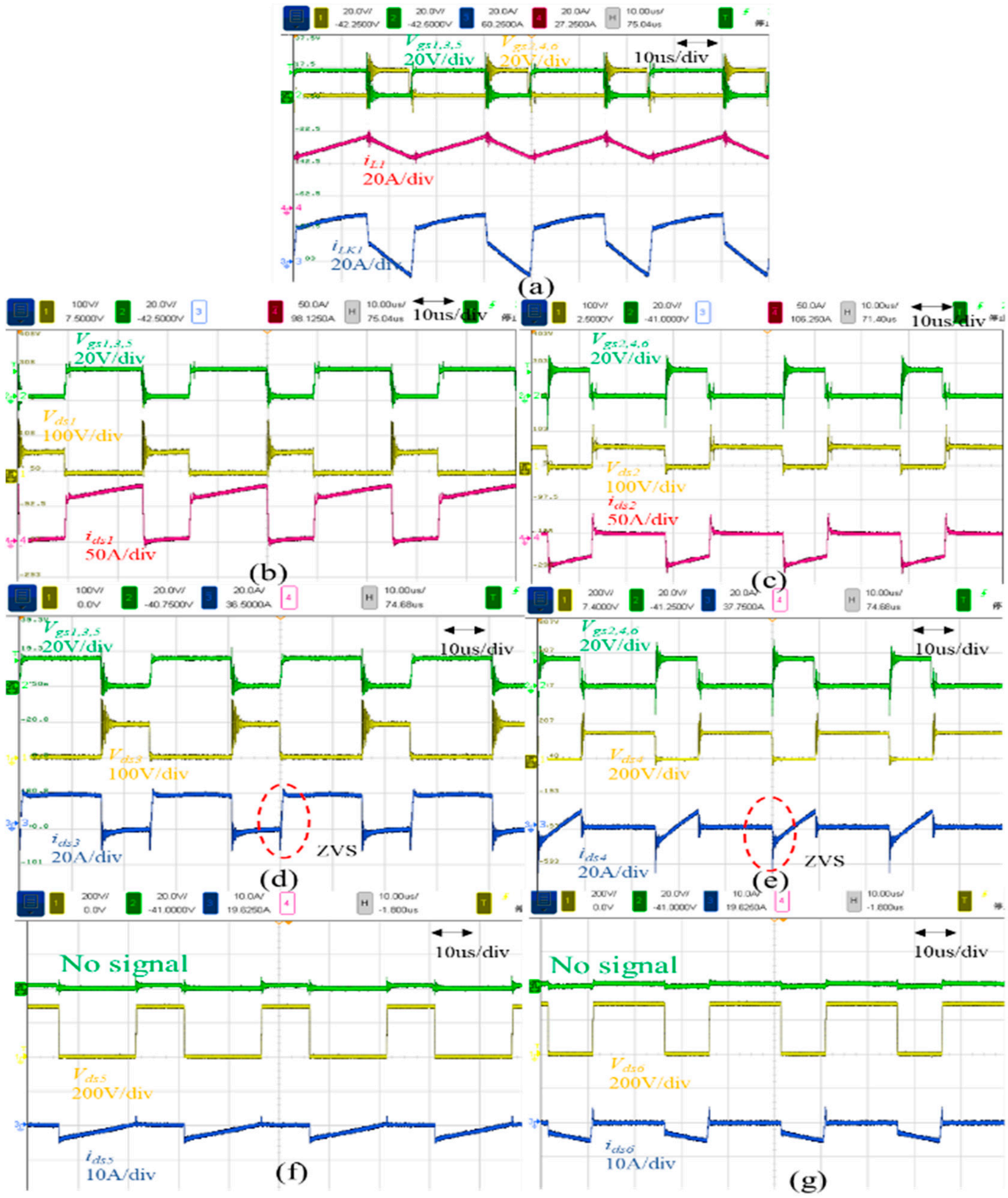

Figure 14. Experimental results for operation of the proposed converter at full load and at V_L = 24 V in step-up mode. (**a**) Waveforms of $v_{gs1,3,5}$, $v_{gs2,4,6}$, i_{L1}, and i_{lk1}. (**b**) Waveforms of $v_{gs1,3,5}$, v_{ds1}, and i_{ds1} of S_1. (**c**) Waveforms of $v_{gs2,4,6}$, v_{ds2}, and i_{ds2} of S_2. (**d**) Waveforms of $v_{gs1,3,5}$, v_{ds3}, and i_{ds3} of S_3. (**e**) Waveforms of $v_{gs2,4,6}$, v_{ds4}, and i_{ds4} of S_4. (**f**) Waveforms of v_{ds5} and i_{ds5} of S_5. (**g**) Waveforms of v_{ds6} and i_{ds6} of S_6.

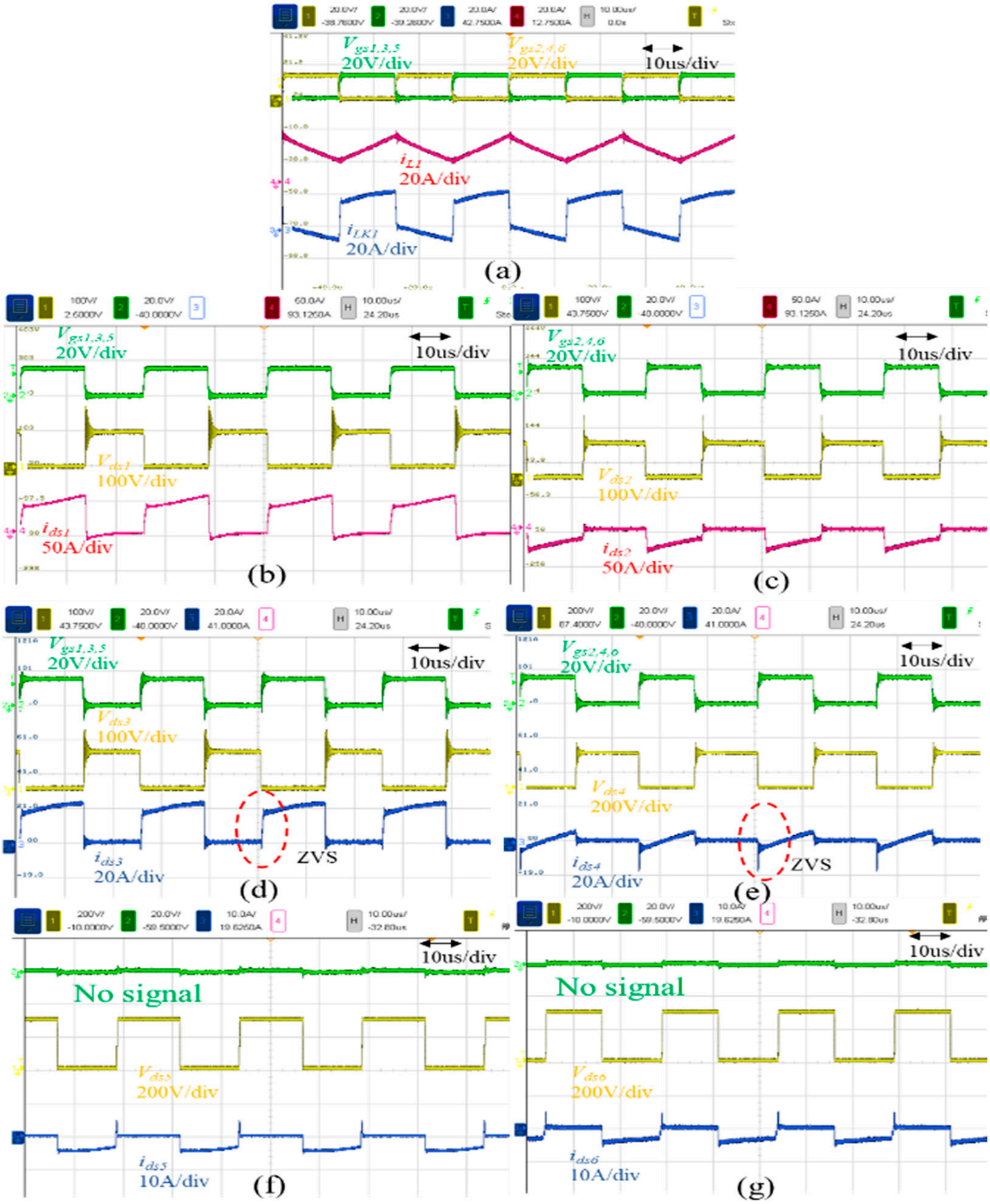

Figure 15. Experimental results from operating the proposed converter at full load and at V_L = 48 V in step-up mode. (**a**) Waveforms of $v_{gs1,3,5}$, $v_{gs2,4,6}$, i_{L1}, and i_{lk1}. (**b**) Waveforms of $v_{gs1,3,5}$, v_{ds1}, and i_{ds1} of S_1. (**c**) Waveforms of $v_{gs2,4,6}$, v_{ds2}, and i_{ds2} of S_2. (**d**) Waveforms of $v_{gs1,3,5}$, v_{ds3}, and i_{ds3} of S_3. (**e**) Waveforms of $v_{gs2,4,6}$, v_{ds4}, and i_{ds4} of S_4. (**f**) Waveforms of v_{ds5} and i_{ds5} of S_5. (**g**) Waveforms of v_{ds6} and i_{ds6} of S_6.

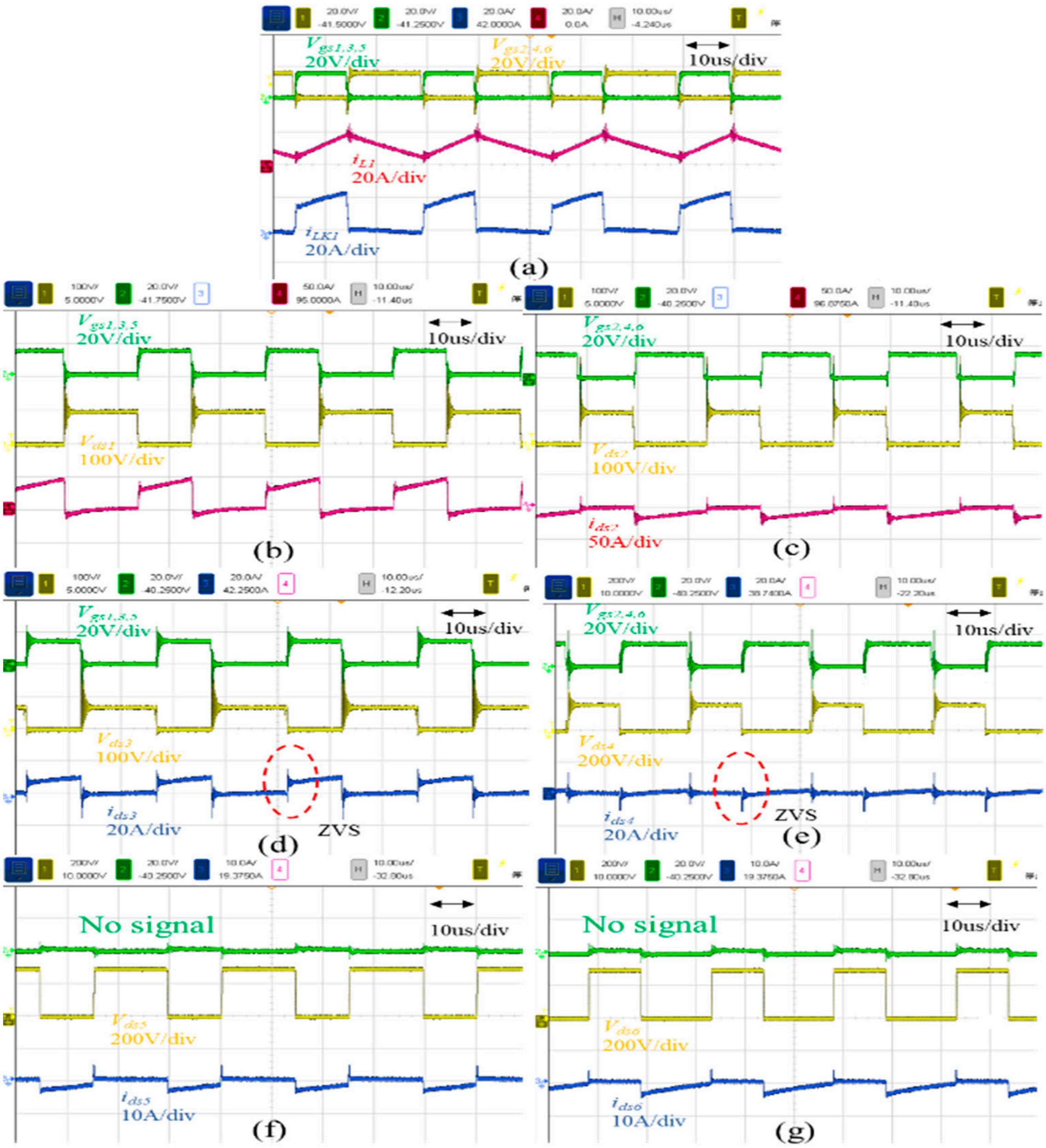

Figure 16. Experimental results from operating the proposed converter at full load and at V_L = 58 V in step-up mode. (**a**) Waveforms of $v_{gs1,3,5}$, $v_{gs2,4,6}$, i_{L1}, and i_{lk1}. (**b**) Waveforms of $v_{gs1,3,5}$, v_{ds1}, and i_{ds1} of S_1. (**c**) Waveforms of $v_{gs2,4,6}$, v_{ds2}, and i_{ds2} of S_2. (**d**) Waveforms of $v_{gs1,3,5}$, v_{ds3}, and i_{ds3} of S_3. (**e**) Waveforms of $v_{gs2,4,6}$, v_{ds4}, and i_{ds4} of S_4. (**f**) Waveforms of v_{ds5} and i_{ds5} of S_5. (**g**) Waveforms of v_{ds6} and i_{ds6} of S_6.

The images of waveforms are magnified to reveal the ZVS performance. Before ZVS turn-on, the v_{ds} of S_3 and S_4 dropped to zero, as shown in Figure 17.

Figure 18 presents an analysis of the losses of the proposed converter at V_L = 24 V in step-up mode and under full load. The switching loss and conduction loss of all power switches account for a large proportion of the overall loss.

During measurement, V_L was maintained at 24–58 V, and the high-voltage side V_H was maintained at 400 V. Figures 19–21 present the measured waveforms of the low-voltage side at 24, 48, and 58 V at full load in step-down mode.

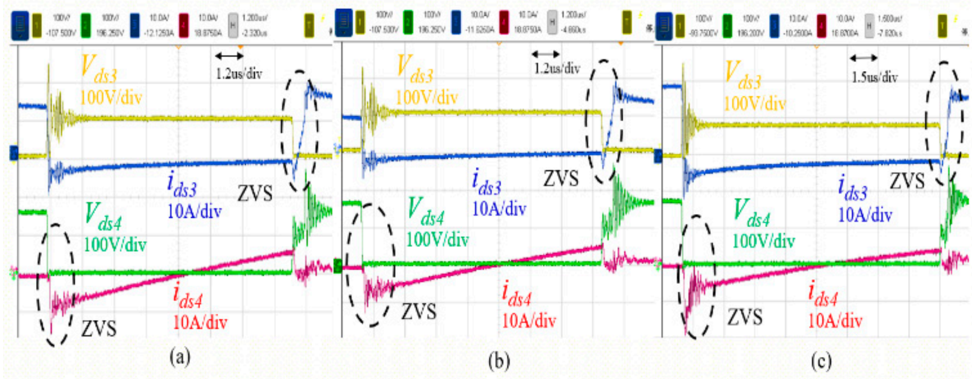

Figure 17. Experimental results related to ZVS for one cycle at full load (1000 W) in step-up mode. (**a**) v_{ds} and i_{ds} of S_3 and S_4 at V_L = 24 V. (**b**) v_{ds} and i_{ds} of S_3 and S_4 at V_L = 48 V. (**c**) v_{ds} and i_{ds} of S_3 and S_4 at V_L = 58 V.

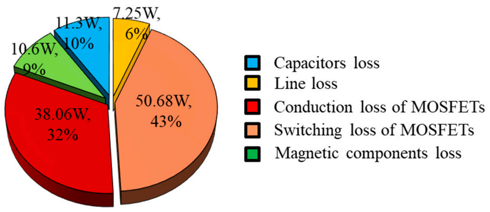

Figure 18. Loss distribution for experiment under V_L = 24 V, V_H = 400 V, and P = 1000 W in step-up mode.

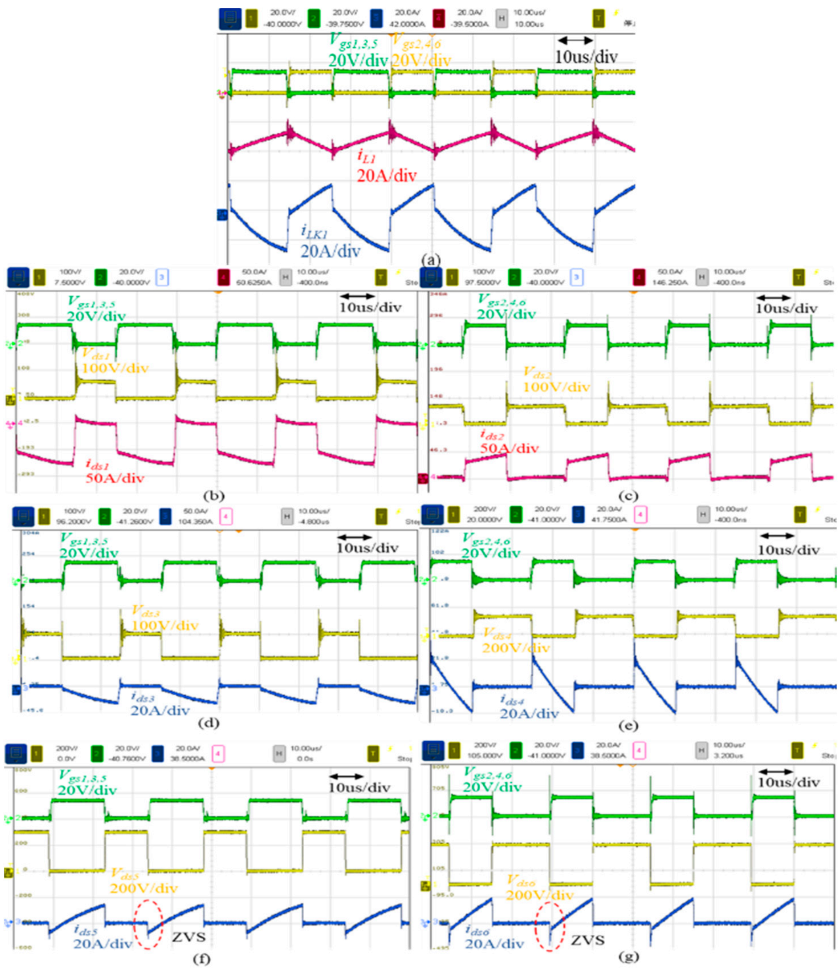

Figure 19. Experimental results from operating the proposed converter at full load (1000 W) and at

V_L = 24 V in step-down mode. (**a**) Waveforms of $v_{gs1,3,5}$, $v_{gs2,4,6}$, i_{L1}, and i_{lk1}. (**b**) Waveforms of $v_{gs1,3,5}$, v_{ds1}, and i_{ds1} of S_1. (**c**) Waveforms of $v_{gs2,4,6}$, v_{ds2}, and i_{ds2} of S_2. (**d**) Waveforms of $v_{gs1,3,5}$, v_{ds3}, and i_{ds3} of S_3. (**e**) Waveforms of $v_{gs2,4,6}$, v_{ds4}, and i_{ds4} of S_4. (**f**) Waveforms of $v_{gs1,3,5}$, v_{ds5}, and i_{ds5} of S_5. (**g**) Waveforms of $v_{gs2,4,6}$, v_{ds6}, and i_{ds6} of S_6.

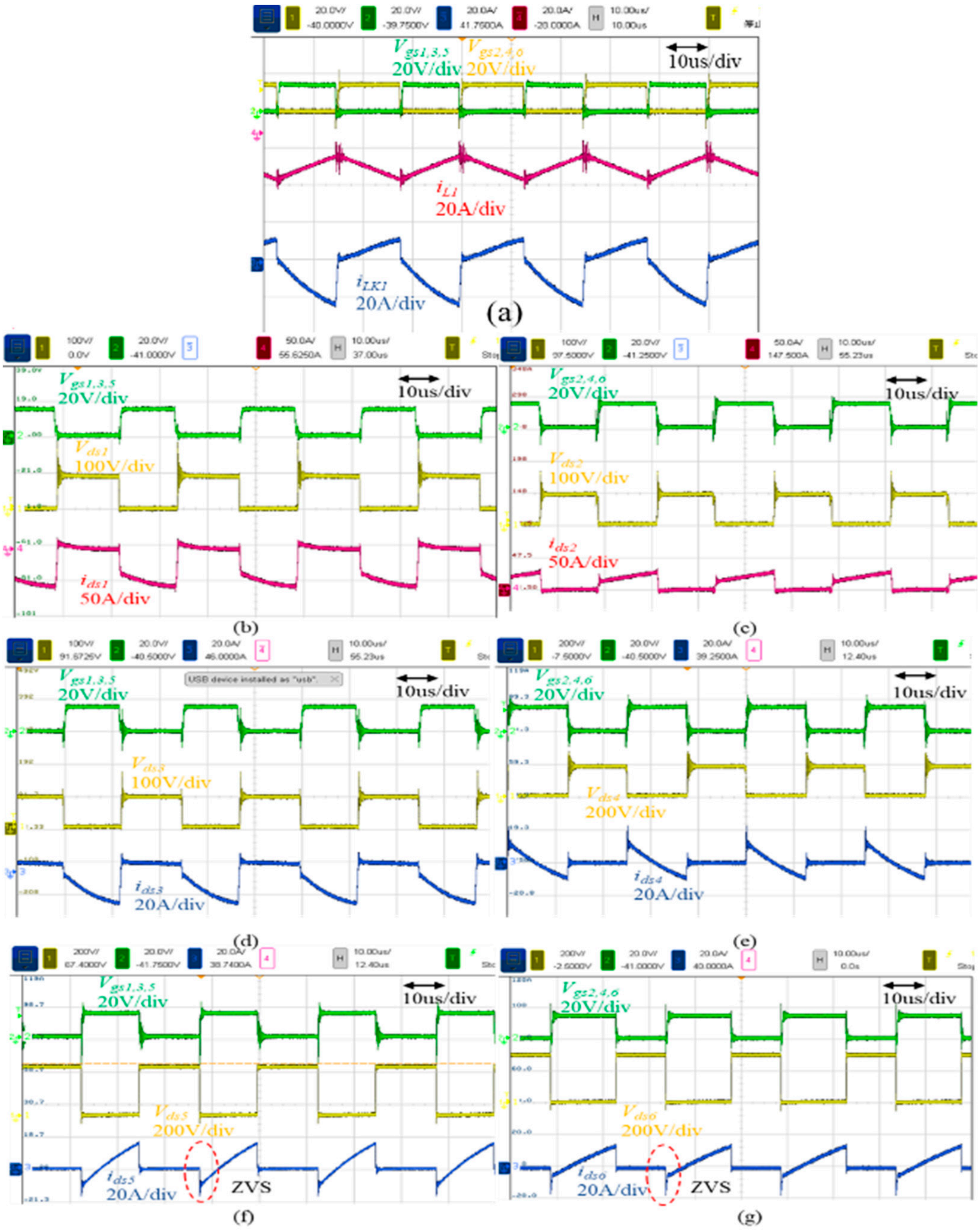

Figure 20. Experimental results from operating the proposed converter at full load (1000 W) and at V_L = 48 V in step-down mode. (**a**) Waveforms of $v_{gs1,3,5}$, $v_{gs2,4,6}$, i_{L1}, and i_{lk1}. (**b**) Waveforms of $v_{gs1,3,5}$, v_{ds1}, and i_{ds1} of S_1. (**c**) Waveforms of $v_{gs2,4,6}$, v_{ds2}, and i_{ds2} of S_2. (**d**) Waveforms of $v_{gs1,3,5}$, v_{ds3}, and i_{ds3} of S_3. (**e**) Waveforms of $v_{gs2,4,6}$, v_{ds4}, and i_{ds4} of S_4. (**f**) Waveforms of $v_{gs1,3,5}$, v_{ds5}, and i_{ds5} of S_5. (**g**) Waveforms of $v_{gs2,4,6}$, v_{ds6}, and i_{ds6} of S_6.

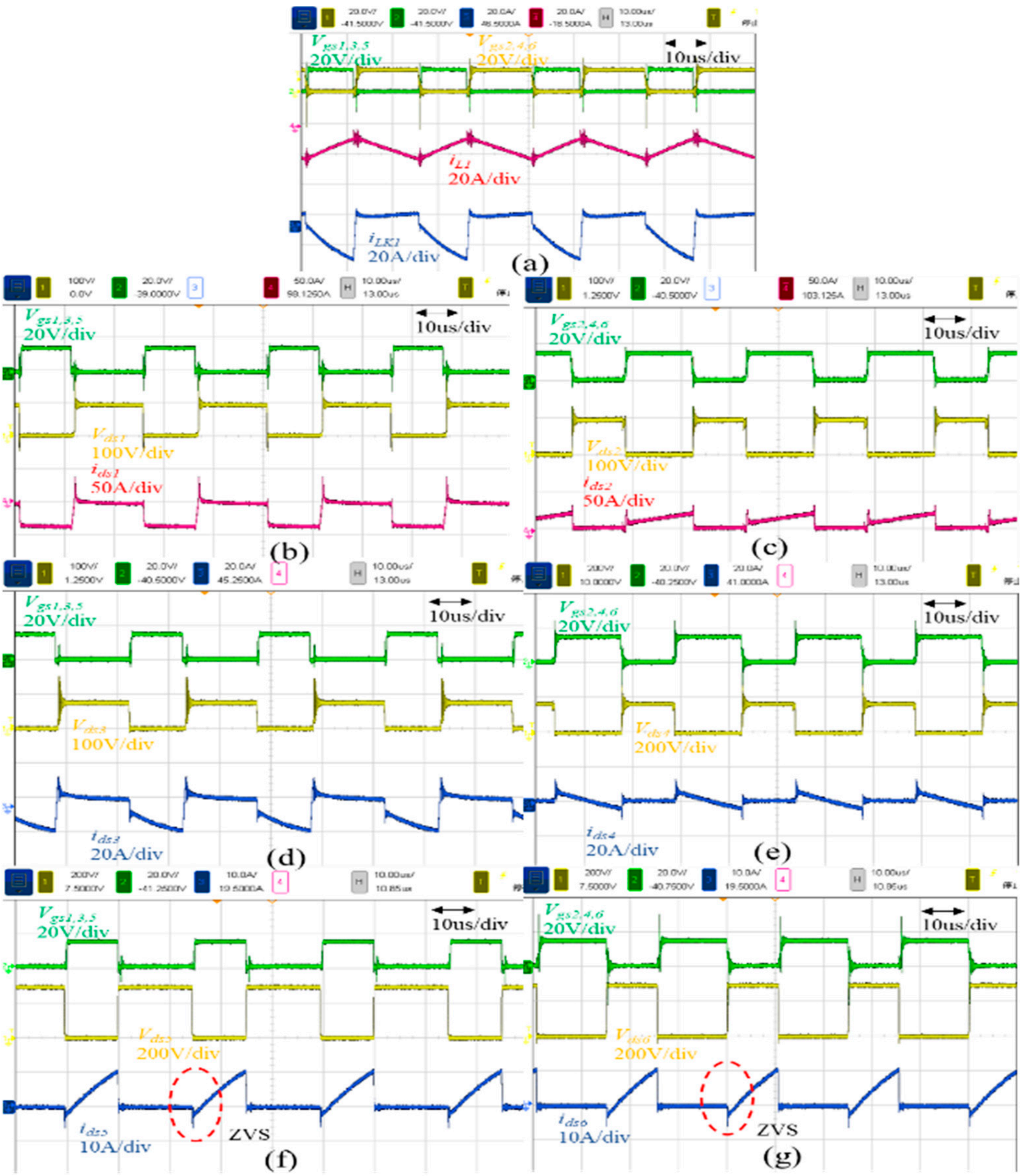

Figure 21. Experimental results from operating the proposed converter at full load (1000 W) and at V_L = 58 V in step-down mode. (**a**) Waveforms of $v_{gs1,3,5}$, $v_{gs2,4,6}$, i_{L1}, and i_{lk1}. (**b**) Waveforms of $v_{gs1,3,5}$, v_{ds1}, and i_{ds1} of S_1. (**c**) Waveforms of $v_{gs2,4,6}$, v_{ds2}, and i_{ds2} of S_2. (**d**) Waveforms of $v_{gs1,3,5}$, v_{ds3}, and i_{ds3} of S_3. (**e**) Waveforms of $v_{gs2,4,6}$, v_{ds4}, and i_{ds4} of S_4. (**f**) Waveforms of $v_{gs1,3,5}$, $v_{\mathrm{ds}5}$, and $i_{\mathrm{ds}5}$ of S_5. (**g**) Waveforms of $\mathrm{v}_{\mathrm{gs}2,4,6}$, $\mathrm{v}_{\mathrm{ds}6}$, and $\mathrm{i}_{\mathrm{ds}6}$ of S_6.

The magnified images of waveforms are presented to reveal the ZVS performance. Before ZVS turn-on, the v_{ds} of S_5 and S_6 dropped to zero, as shown in Figure 22.

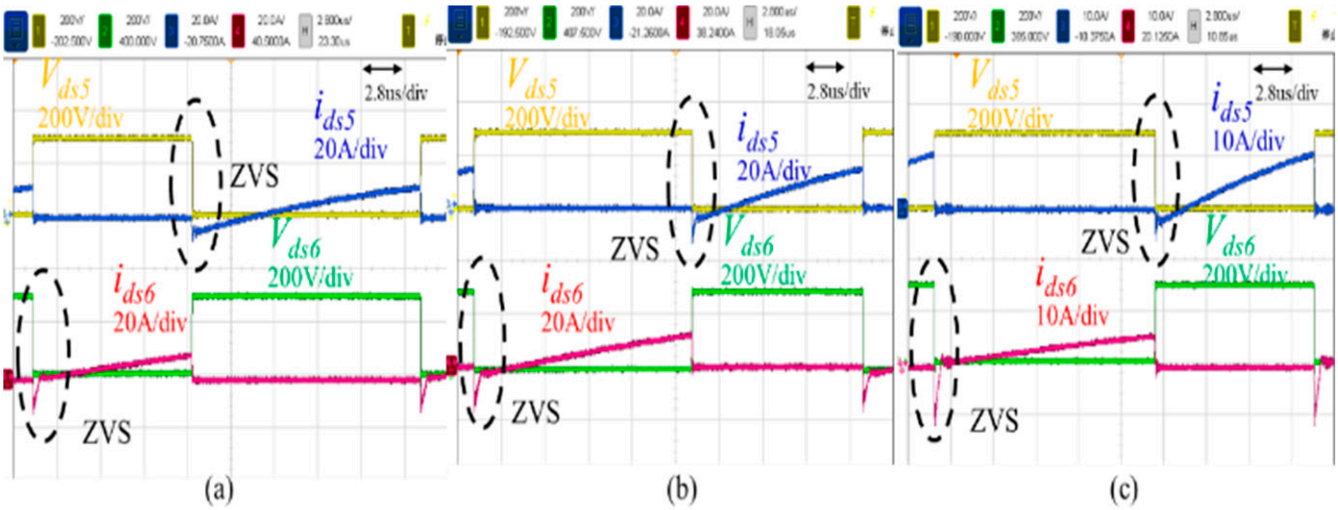

Figure 22. Experimental results related to ZVS for one cycle at full load (1000 W) in step-down mode. (**a**) v_{ds} and i_{ds} of S_5 and S_6 at V_L = 24 V. (**b**) v_{ds} and i_{ds} of S_5 and S_6 at V_L = 48 V. (**c**) v_{ds} and i_{ds} of S_5 and S_6 at V_L = 58 V.

Figure 23 presents the results from analyzing the losses of the proposed topology at V_L = 48 V in step-down mode at full load. The switching loss and conduction loss of all switches account for a large proportion of the overall loss.

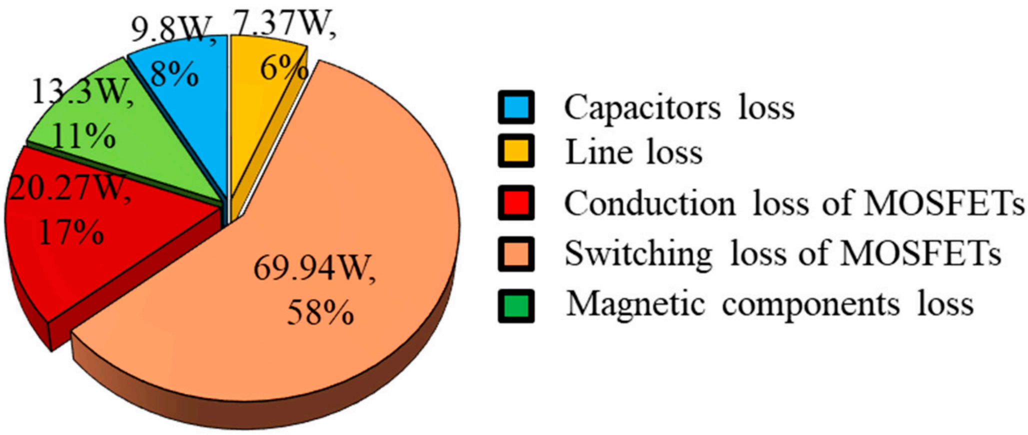

Figure 23. Calculated loss distribution from experimentation under V_L = 48 V, V_H = 400 V, and P = 1000 W in step-down mode.

Figure 24 shows the conversion efficiency of the proposed converter in step-up mode. When V_L is 24 V, the highest efficiency is 95.1% at 200 W, and the full-load conversion efficiency is 88%. When V_L is 48 V, the maximum efficiency is moved to 300 W, which is 96.55%, and the full-load conversion efficiency is 92.9%. When V_L is 58 V, the highest efficiency is also 94.8% at 300 W, and the full-load conversion efficiency is 93.3%.

Figure 25 shows the conversion efficiency of the proposed converter in step-down mode. When V_L is 24 V, the highest efficiency is 94.4% at 400 W, and the full-load conversion efficiency is 88.2%. When V_L is 48 V, the highest efficiency is 95.48% at 400 W, and the full-load conversion efficiency is 92.1%. When V_L is 58 V, the highest efficiency point is moved to 500 W, which is 93.7%, and the conversion efficiency at full load is 92.4%.

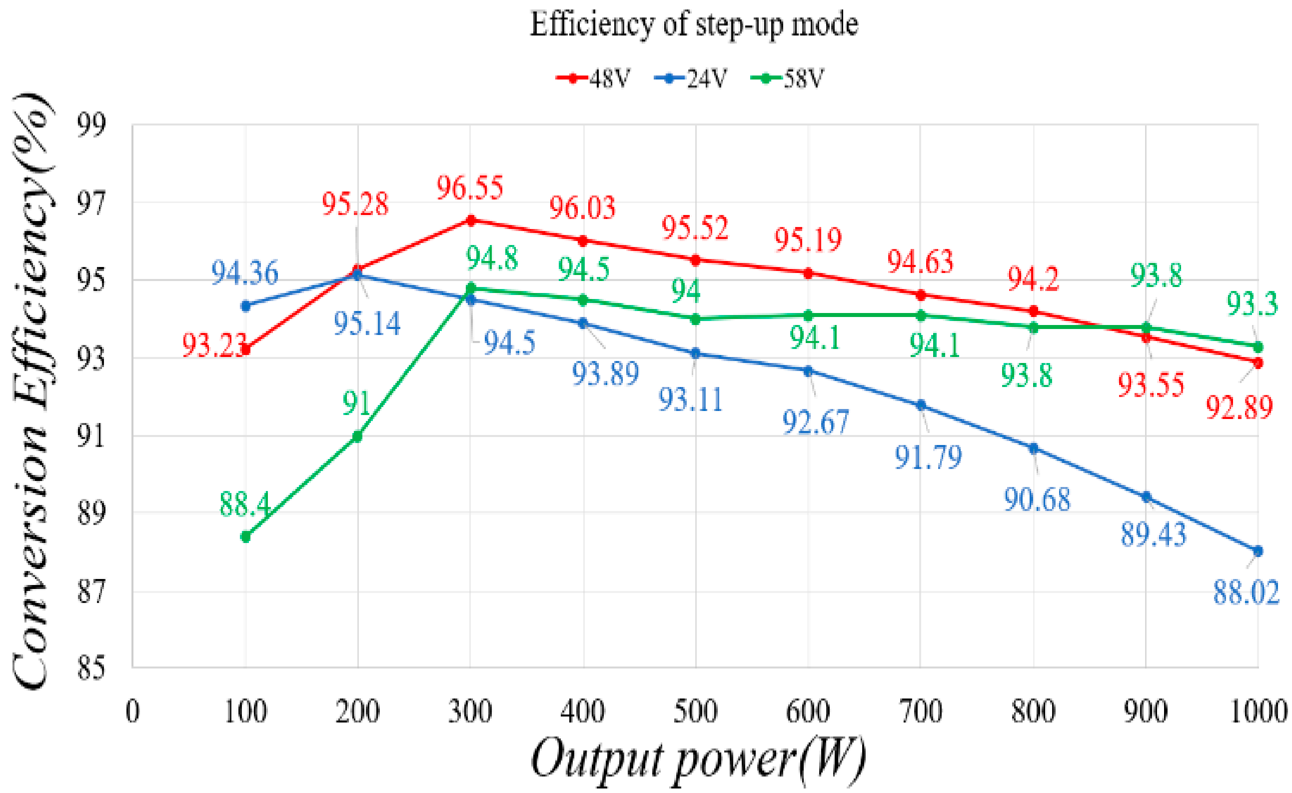

Figure 24. Efficiency of proposed converter in step-up mode.

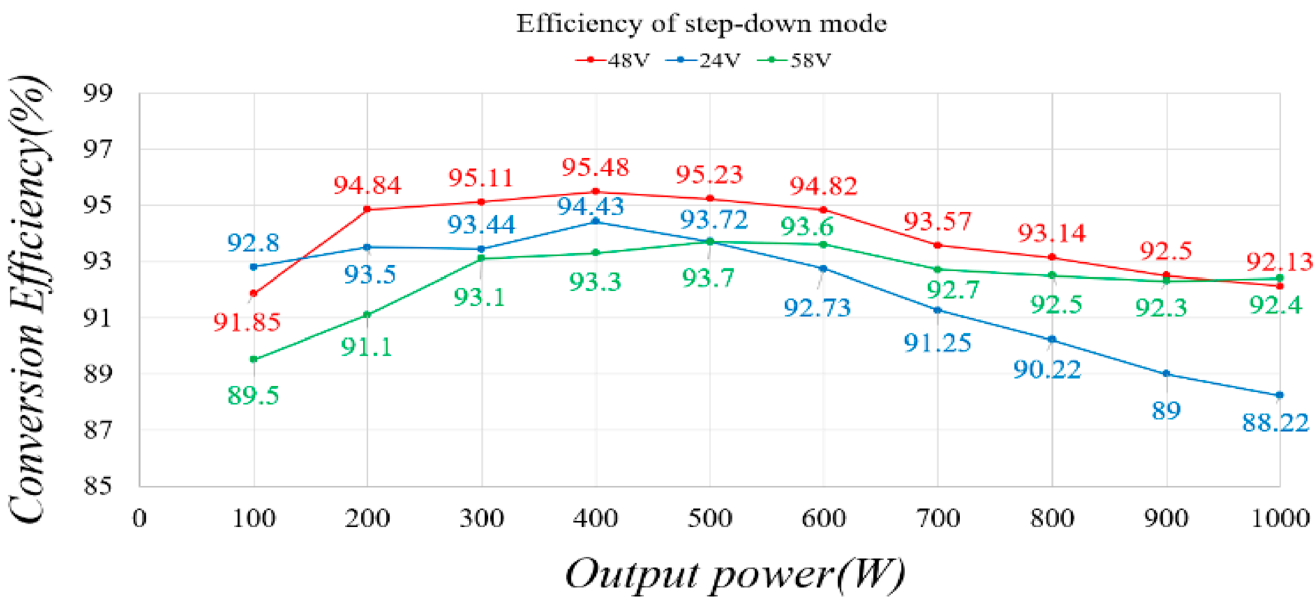

Figure 25. Efficiency curve of the proposed converter in step-down mode.

Figure 26 presents the measured waveforms for step variations in output load. When the output power was changed from half load to full load, the transient voltage fluctuation in the proposed converter was sufficiently small so as to be neglected, output voltage V_H was stable at 400 V in step-up mode, and output voltage V_L was stable at 24 V in step-down mode.

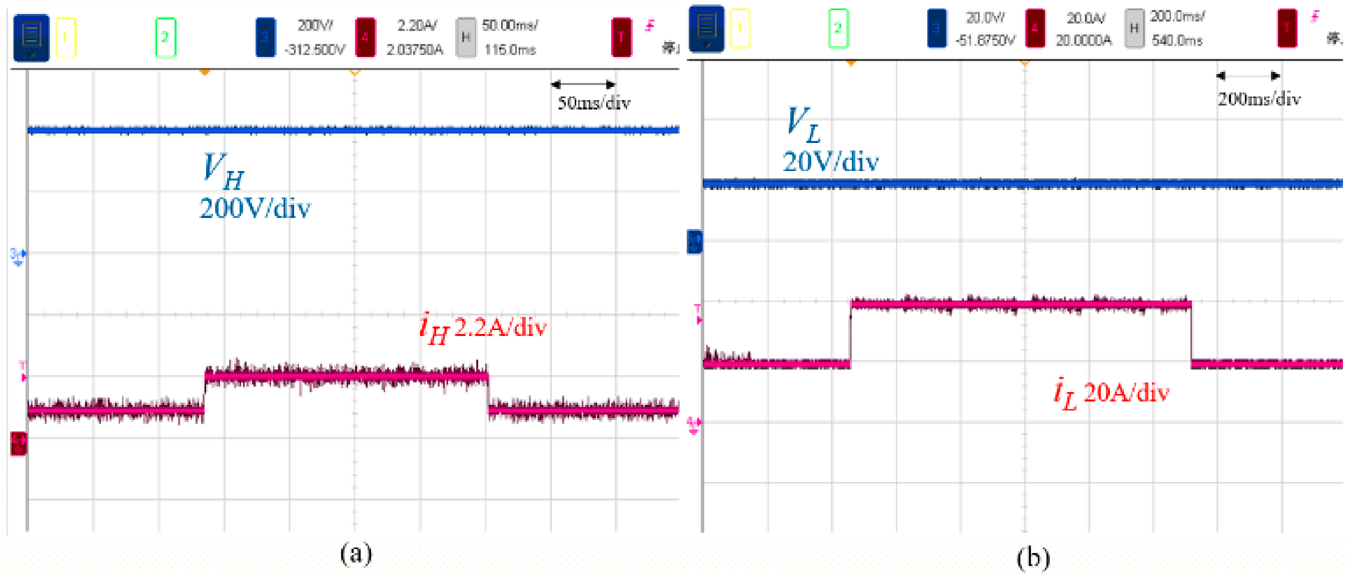

Figure 26. Step variation in output load in (**a**) step-up mode and (**b**) step-down mode.

Table 2 presents a comparison of the proposed converter with those in [20,21] and [23–27]. The proposed converter has larger power output, higher efficiency, and higher voltage gain, meaning that it can be widely used in numerous industries. In addition, related equipment can be operated safely under galvanic isolation. Comparisons of the voltage gain in step-up and step-down modes are presented in Figures 27 and 28, respectively. The duty variation influences the voltage gain of the converter, and the proposed converter possesses a wider voltage gain than do other bidirectional converters through duty cycle control. When the duty ratio exceeds 0.6, the proposed converter has the highest voltage gain.

Table 2. Comparison between the proposed converter and related bidirectional converters.

	Converter in [20]	**Converter in [21]**	**Converter in [23]**	**Converter in [24]**	**Converter in [25]**	**Converter in [26]**	**Converter in [27]**	**Proposed Converter**
Voltage gain in step-up mode $\frac{V_H}{V_L}$	$\frac{1}{(1-D)} \cdot 2N$	$\frac{N}{D_1 \cdot D_2 \cdot D_3}$	$\frac{N+1}{1-D}$	$\frac{N}{(1-D)^2}$	$\frac{1+D(N+Na)}{1-D}$	$\frac{2N+2}{1-D}$	$\frac{2(N+1)}{1-D}$	$\frac{N}{(1-D)^2}$
Voltage gain in step-down mode $\frac{V_L}{V_H}$	$\frac{D}{2N}$	$\frac{D_1 \cdot D_2 \cdot D_3}{N}$	$\frac{D}{N+1}$	$\frac{(1-D)^2}{N}$	$\frac{D}{1+(1-D)(N+Na)}$	$\frac{D}{2N+2}$	$\frac{D}{2(N+1)}$	$\frac{(1-D)^2}{N}$
Vin	24–48 V	35–50 V	40 V	24–55 V	48 V	48 V	48 V	24–58 V
Vo	360 V	400 V	400 V	400 V	380 V	384 V	400 V	400 V
Switches	4	10	4	6	3	6	4	6
Inductors	1	2	0	1	0	0	0	1
Coupled inductor	1	1	1	1	1	1	2	1
Capacitors	6	3	2	3	1	4	3	4
Diodes	0	0	0	0	0	0	3	0
Output power	250 W	1000 W	300 W	500 W	300 W	250 W	400 W	1000 W
Efficiency of step-up mode	94%	94%	94%	96%	94%	96%	95%	96%
Efficiency of step-down mode	93%	94%	94%	94%	95%	96%	95%	95%
PWM Control Signals	Normal	Complex	Normal	Normal	Normal	Normal	complex	Normal
Isolated	Yes	Yes	No	Yes	No	No	No	Yes

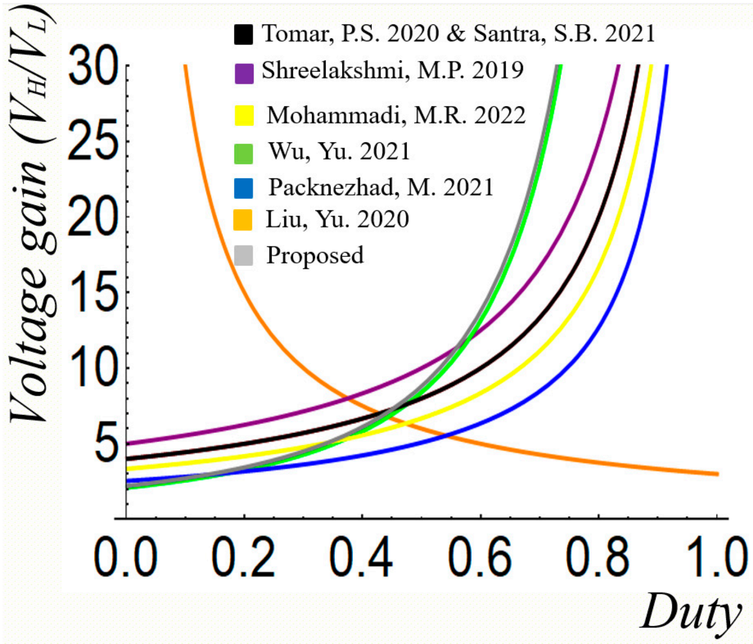

Figure 27. Comparison of voltage gain in step-up mode. In colorful order the references are [20], [26], [23], [27], [24], [25], and [21].

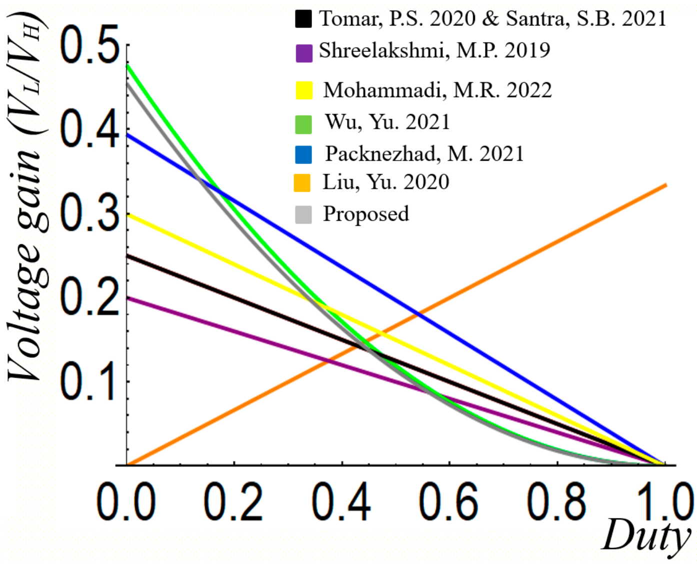

Figure 28. Comparison of voltage gain in step-down mode. In colorful order the references are [20], [26], [23], [27], [24], [25], and [21].

Figures 29 and 30 present conversion efficiency comparisons between the proposed converter and the converters proposed in [20,21] and [23–27] operated in step-up and step-down modes, respectively. In the converter described in [20], the conversion efficiency was not high, and the output power of the converter was insufficient. Of all the converters, the converter in [21] has the highest switching frequency; this can greatly reduce converter size, but too many components lead to increased costs. In the converter described in [25], all switches have ZVS, but the efficiency is mediocre. The overall conversion efficiency is the highest in the converter described in [26], but the output power of this converter is insufficient for storage systems. In the converter described in [27], the PWM control signals are too complex.

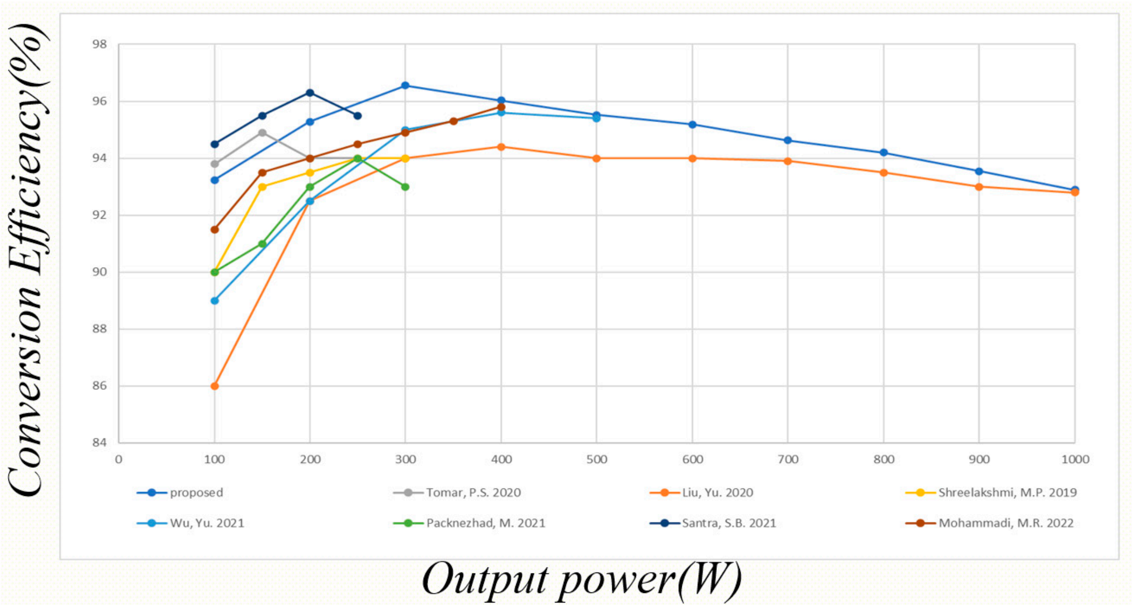

Figure 29. Efficiency comparison in step-up mode. In colorful order [20], [21], [23], [24], [25], [26], and [27].

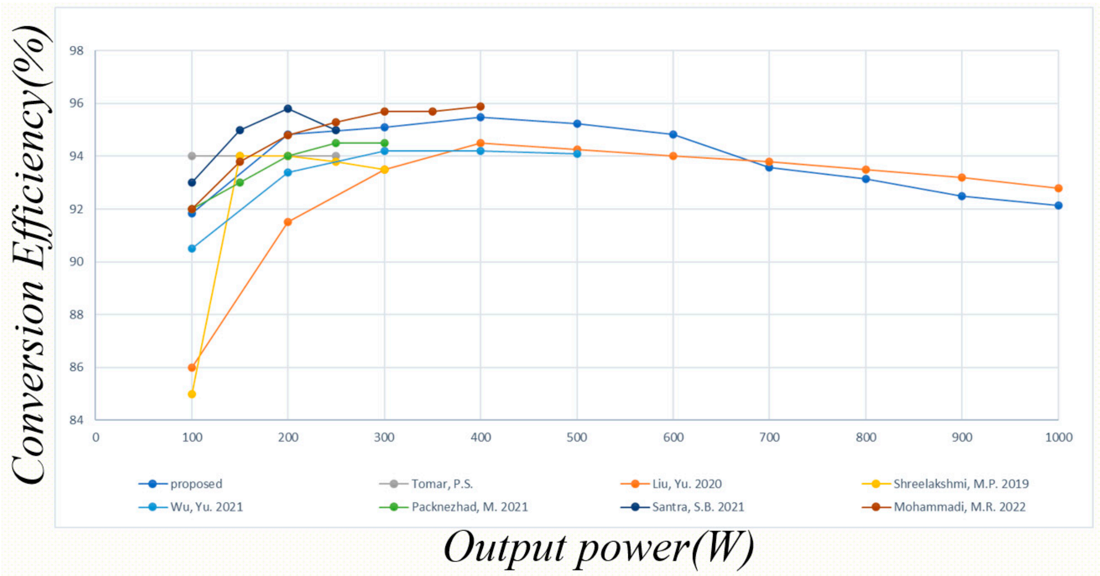

Figure 30. Efficiency comparison in step-down mode. In colorful order [20], [21], [23], [24], [25], [26], and [27].

In summary, the overall conversion efficiency of the proposed converter is high, and the converter has substantial power in both step-up and step-down modes. In addition, this converter has the widest input range of all the converters.

5. Conclusions

This study proposed a novel bidirectional isolated DC/DC converter with a high gain ratio and wide input voltage for EV storage systems. This converter only requires one complementary PWM output to control step-up and step-down modes. Partial switches achieve ZVS, which can increase efficiency. The topology proposed in this paper was demonstrated to be feasible through theoretical analysis and experimentation. When the power on the low-voltage side was 24, 48, and 58 V, the maximum efficiency in step-up mode was 95.1%, 96.5%, and 94.8%, respectively, and the maximum efficiency in step-down mode was 94.4%, 95.4%, and 93.6%, respectively.

The advantages of the proposed converter are as follows: (1) The circuit structure is simple. (2) The converter only requires one complementary PWM output. (3) The converter achieves a wide voltage gain and high voltage gain. (4) Galvanic isolation separates the input and output power supplies. (5) The current of the low-voltage side is continuous in CCM. (6) ZVS technology is used in specific switches to reduce switching loss.

Future research directions include: (1) The proposed topology can be designed for three-stage charging, which are bulk charge, absorption, and float charge to extend battery life effectively by adding current sensor. (2) Modularize the proposed topology to achieve multiple groups of bidirectional energy transmission in parallel to deal with the application of greater power. (3) Implement greater practical power.

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