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Analysis of a PWM Converter with Less Current Ripple, Wide Voltage Operation and Zero-Voltage Switching

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Abstract: This paper studies and implements a power converter to have less current ripple output and wide voltage input operation. A three-leg converter with different primary turns is presented on its high-voltage side to extend the input voltage range. The current doubler rectification circuit is adopted on the output side to have low current ripple capability. From the switching states of the three-leg converter, the presented circuit has two equivalent sub-circuits under different input voltage ranges (V_{in} = 120–270 V or 270–600 V). The general phase-shift pulse-width modulation is employed to control the presented converter so that power devices can be turned on at zero voltage in order to reduce switching loss. Compared to two-stage circuit topologies with a wide voltage input operation, the presented converter has the benefits of simple circuit structure, easy control algorithm using a general integrated circuit or digital controller, and less components. The performance of the presented circuit is confirmed and validated by an 800 W laboratory prototype.

Keywords: PWM converter; soft switching; less current ripple

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1. Introduction

For the past decade, clean energy sources have brought attention to the depletion of fossil fuel demand due to the rising demand for electric power. Fuel cell stacks, wind energy, and photovoltaic (PV) are the most attractive renewable energy sources [1–6]. However, the output voltage of dc wind power and PV panels is unstable and widely varies. High-frequency dc-link converters can convert an unstable dc voltage to a constant dc voltage by using duty cycle control [7–9] or pulse frequency modulation (PFM) [10–12]. In duty cycle control, the turn-on time of the power switch is related to input voltage under the constantly switching frequency. Therefore, the load terminal is regulated at the command voltage. In the PFM approach, the switching frequency is variable and related to input voltage. Thus, the input impedance of the resonant tank is variable to change voltage gain and regulate load voltage. For dc wind energy and PV power, the solar intensity and wind speed have a wide deviation. Therefore, the output voltage of PV panels and wind generators is variable in a wide voltage range. In conventional isolated dc converters, the maximum and minimum effective duty cycles are related to input voltage, $d_{eff,max}/d_{eff,min} = V_{in,max}/V_{in,min}$. In phase-shift pulse-width modulation (PWM) converters, the maximum (or minimum) effective duty cycle or duty ratio is normally less (or greater) than 0.45 (or 0.15). Then, the available input voltage variation range $V_{in,max}/V_{in,min}$ is less than 3. However, the output voltage variation of some dc wind power and PV panels may be greater than 4. To overcome this problem, dc converters with a cascaded structure [13–15] have been studied which have a wide input voltage variation. The problem with the cascaded structure converters is low efficiency. The dc converters with duty cycle control were studied in [16–18] to achieve wide voltage operation and low switching loss. However, the control algorithm is too complicated for using a general-purpose integrated circuit. Full-bridge converters with wide input voltage range that have PWM or PFM schemes have been presented in [19,20]. The input voltage variation range in [20] with two transformers

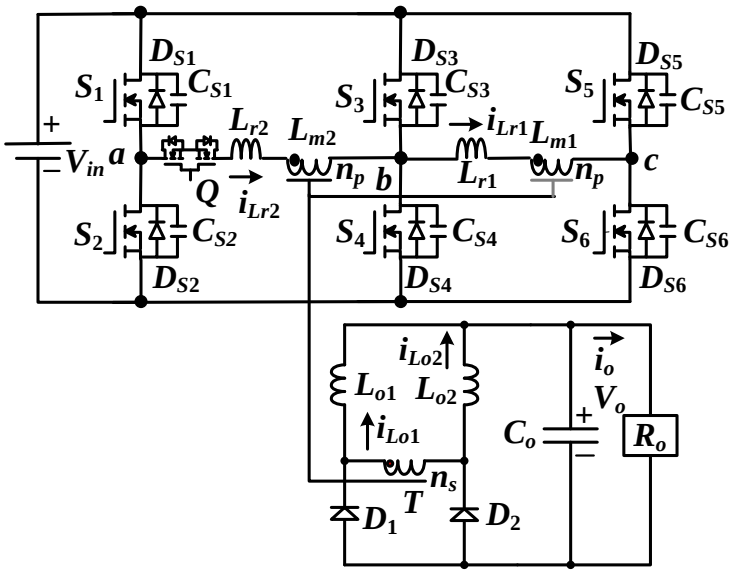
and one ac switch structure could achieve $V_{in,max}/V_{in,min}$ = 4. Four equivalent circuits could be operated in [14] to realize wide voltage operation. However, the control scheme is more complicated when using a general-purpose integrated circuit. In [21], a hybrid dc–dc converter is presented to have wide voltage operation between V_{in} = 120 V and 600 V. However, this converter has more ripple current on the output inductor and more passive components on the secondary side. In [22], a wide voltage resonant converter was discussed and implemented to be operated between V_{in} = 10 V and 160 V for low-power applications. However, the circuit topology was still a cascaded dc–dc converter.

In the present work, a three-leg structure phase-shift PWM converter is studied and implemented to have a wide voltage input operation and a wide load range of zero-voltage turn-on operation. Two sub-circuits with different voltage gains can be operated in the presented converter according to input voltage ranges. Hence, the presented converter can accomplish wide input voltage operation. The phase-shift PWM approach is used to control the gating signals of power devices. Then, the zero-voltage switching (ZVS) operation for the three-leg converter can be easily achieved. The current doubler rectification circuit is operated on the load terminal. Therefore, the current ripple on the output terminal is decreased. A Schmitt voltage comparator is used in the control circuit to select the proper sub-circuit, having a high voltage gain under a low voltage input range or a low voltage gain under ahigh voltage input range. The reference voltage of the voltage comparator is equal to 270 V. The presented circuit is designed to be operated under V_{in} = 120~600 V. Compared to the conventional cascaded structure converter in [13–18], the studied converter has an easy control algorithm and a simple circuit structure. Compared to conventional converters with a wide voltage operation [19–22], the proposed converter has fewer active switches and a wider voltage deviation region. The effectiveness and benefits of the presented circuit are verified by theoretical analysis and experimental verifications with an 800 W prototype.

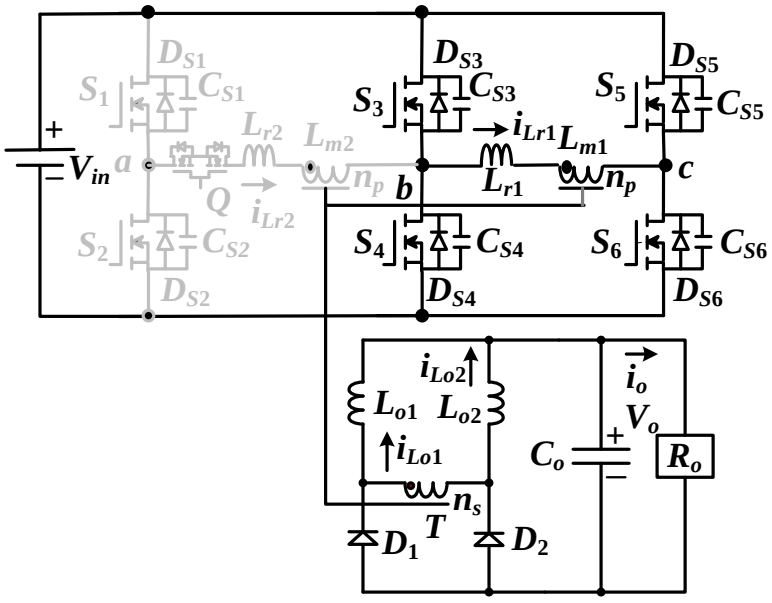
2. Proposed Converter

Figure 1a gives the circuit schematic of the presented converter. It can be observed that the three-leg circuit structure is operated on the primary side and a current doubler rectification structure is adopted on the secondary side. An isolation transformer with two sets of primary-turn n_p and one set of secondary-turn n_s is selected in the converter. The ac switch Q is realized by two power MOSFETs (Metal-Oxide-Semiconductor Field-Effect Transistors) with a back-to-back connection. According to low voltage or high voltage input conditions, Q is controlled to be OFF or ON. Therefore, two equivalent sub-circuits are worked in the presented converter. For a low voltage input region (e.g., $V_{in,L} = V_{in,min}$~$2.3V_{in,min}$), Q, S_1, and S_2 are OFF, and the two-leg PWM converter shown in Figure 1b with active switches S_3–S_6 is operated to regulate the load voltage. The duty cycle control is selected to generate the necessary gate signals of active switches S_3–S_6. Thus, the ZVS operation of S_3–S_6 is achieved. The output voltage can be estimated as $V_o = n_s V_{in,L} d_{eff}/n_p - V_D$, where d_{eff} is an effective duty cycle and V_D is the voltage drop on D_1 or D_2. The output voltage can be kept stable and constant by the regulation of the effective duty ratio d_{eff}. The minimum effective duty ratio $d_{min,min}$ happens at the maximum input voltage case $V_{in,L,max}$ under the low voltage input range. On the other hand, the minimum input voltage $V_{in,L,min}$ will result in the maximum effective duty ratio $d_{eff,max}$ when the converter is operated in the low voltage input range. The voltage gain of the converter in the low voltage input range is $G_{dc\text{-}L} = V_o/V_{in,L} \approx d_{eff}/N_L$, where $N_L = n_p/n_s$. For the high voltage input region (e.g., $V_{in,H} = 2.3V_{in,min}$~$5V_{in,min}$), Q is ON and S_3 and S_4 are OFF. The two-leg PWM converter shown in Figure 1c with active switches S_1, S_2, S_5, and S_6 is operated to regulate the output voltage. S_1 and S_2 (S_5 and S_6) are active devices on the leading leg (lagging leg) of the phase-shift PWM converter. As can be noted in Figure 1c, the transformer turns ratio is $N_H = 2n_p/n_s$ instead of n_p/n_s. Under the high voltage input condition, the output voltage is expressed as $V_o = n_s V_{in,H} d_{eff}/(2n_p) - V_D$ and the voltage gain becomes $G_{dc\text{-}H} = V_o/V_{in,H} \approx d_{eff}/N_H$. From the circuit operation

in the previous statements, the presented circuit can achieve ZVS operation and a wide voltage input operation with about $V_{in,min} - 5V_{in,min}$ input voltage variation by the proper switching of Q and S_1–S_6.

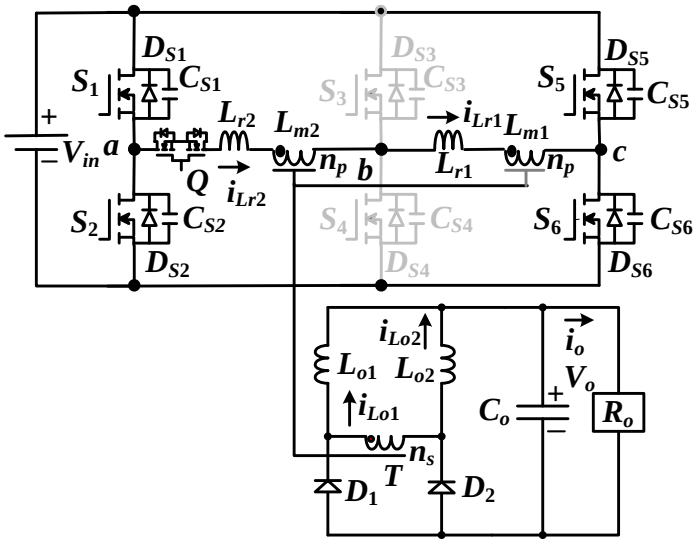


(**a**)



(**b**)

Figure 1. *Cont.*



(**c**)

Figure 1. Proposed converter (**a**); circuit schematic (**b**); equivalent sub-circuit under low voltage input range (**c**); equivalent sub-circuit under high voltage input range.

3. Principle of Operation

The converter has two sub-circuits shown in Figure 1b,c for low voltage input $V_{in,L}$ and high voltage input $V_{in,H}$ operations. For the low voltage input region ($V_{in,min} \leq V_{in,L} < 2.3V_{in,min}$) in Figure 1b, Q, S_2 and S_1 are turned OFF and S_3–S_6 are active with duty cycle control. The transformer turns ratio is $N_L = n_p/n_s$. The corresponding PWM waveforms are provided in Figure 2a. For the high voltage input region ($2.3V_{in,min} \leq V_{in,H} < 5V_{in,min}$) in Figure 1c, Q is ON and S_3 and S_4 are OFF. S_1, S_2, S_5, and S_6 are active with duty cycle control. The transformer turns ratio is $N_H = 2n_p/n_s$. It is assumed the magnetizing inductances $L_{m1} = L_{m2} = L_m >> L_{r1} = L_{r2} = L_r$ and the output capacitances $C_{S1} = ... = C_{S6} = C_{oss}$. The PWM waveforms under the high voltage input condition are given in Figure 2b.

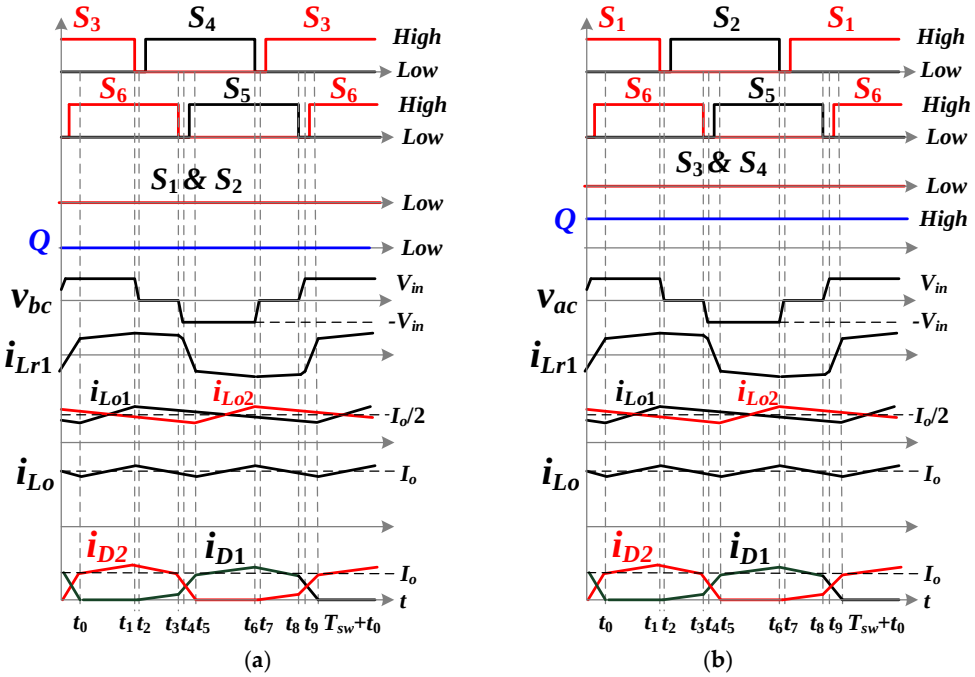


Figure 2. Pulse-width modulation (PWM) singles in the (**a**) low voltage input range; (**b**) high voltage input range.

According to the PWM waveforms of S_3–S_6 and the conducting states of D_1 and D_2, ten operating steps can be observed in Figure 2a under the low voltage input case. As can be observed, the PWM waveforms are symmetric for each half cycle. Thus, only the first five operating steps are explained briefly, and the corresponding step circuits are given in Figure 3.

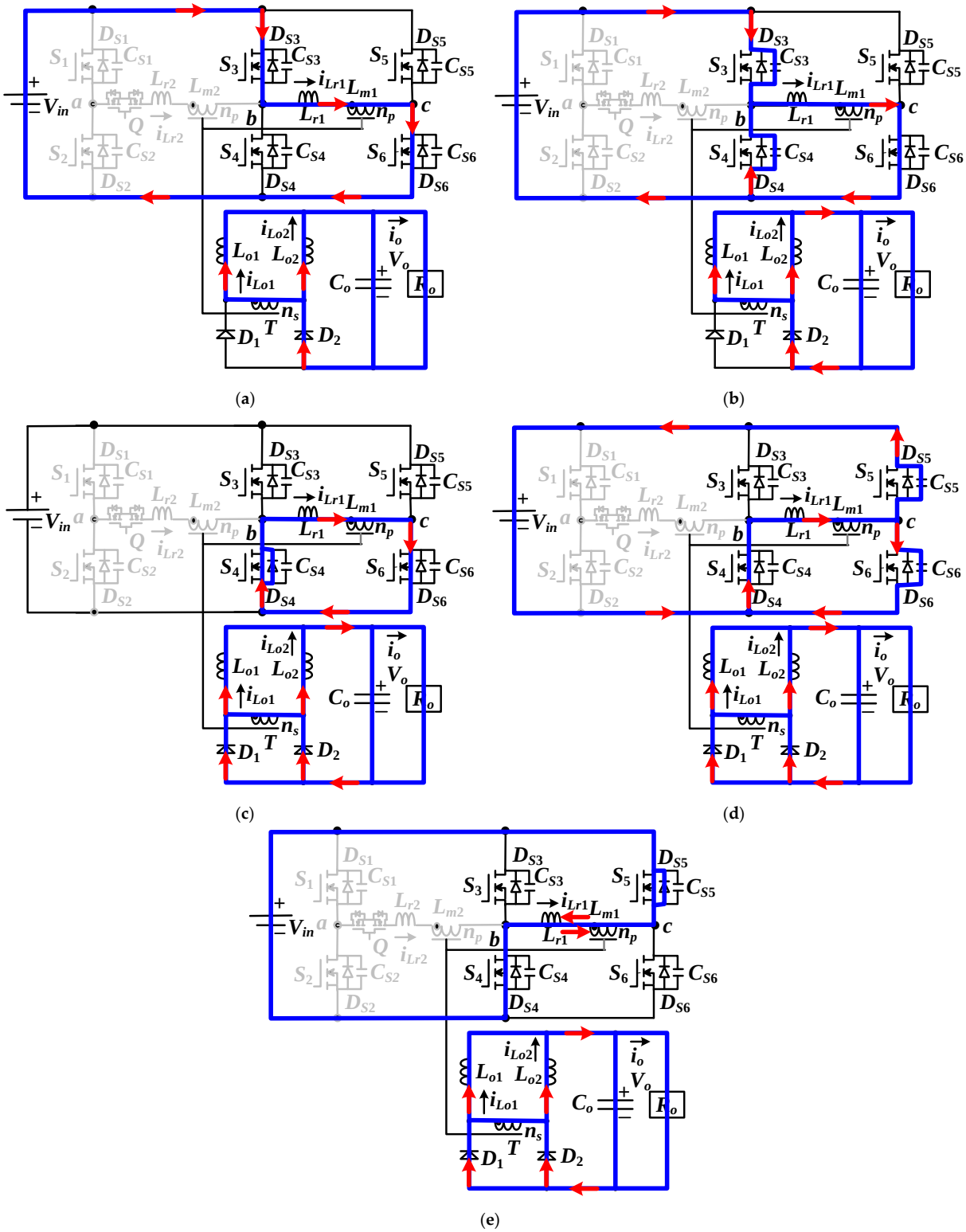


Figure 3. Equivalent circuits under low voltage input condition during the first half switching period: (**a**) step 1 circuit; (**b**) step 2 circuit; (**c**) step 3 circuit; (**d**) step 4 circuit; (**e**) step 5 circuit.

Step 1 [t_0, t_1]: At t_0, $i_{D1} = 0$. S_3 and S_6 are active in this step. The leg voltage is $v_{bc} = V_{in}$, $v_{Lo1} = V_{in}/N_L - V_o$, and $v_{Lo2} = -V_o$. Therefore, i_{Lo1} will increase and i_{Lo2} will decrease in this step. The primary and secondary inductor currents are given in Equations (1)–(3).

$$i_{Lr1}(t) \approx i_{Lr1}(t_0) + \frac{V_{in} - N_L V_o}{N_L^2 L_{o1}}(t - t_0) \tag{1}$$

$$i_{Lo1}(t) \approx i_{Lo1}(t_0) + \frac{V_{in}/N_L - V_o}{L_{o1}}(t - t_0) \tag{2}$$

$$i_{Lo2}(t) \approx i_{Lo2}(t_0) - \frac{V_o}{L_{o2}}(t - t_0) \tag{3}$$

Step 2 [t_1, t_2]: S_3 turns OFF at time t_1. $i_{Lr1}(t_1)$ is positive and C_{S4} is discharged. C_{S4} can be discharged to zero at t_2 if Equation (4) is satisfied. Therefore, the ZVS operation of S_4 is achieved.

$$(L_r + N_L^2 L_o) i_{Lr1}^2(t_1) \geq 2C_{oss} V_{in}^2 \tag{4}$$

The time Δt_{12} in this step is expressed in Equation (5).

$$\Delta t_{12} \approx 2V_{in} C_{oss} N_L / i_{Lo1}(t_1) \tag{5}$$

where $i_{Lo1}(t_1) \approx i_{Lo1}(t_0) + (V_{in}/N_L - V_o) d_{eff} T_{sw}/L_{o1}$.

Step 3 [t_2, t_3]: At t_2, $v_{CS4} = 0$ and D_{S4} is conducting due to $i_{Lr1} > 0$. Thus, the ZVS turn-on operation of S_4 can be naturally realized. Due to leg voltage $v_{bc} = 0$, D_1 and D_2 are both conducting. It can be observed that $v_{Lo1} = v_{Lo2} = -V_o$ and $v_{Lr1} = -v_{S4,dp} - v_{S6,dp}$, where $v_{S4,dp}$ and $v_{S6,dp}$ are voltage drops on S_4 and S_6. In step 3, i_{Lo1}, i_{Lo2} and i_{Lr1} all decrease, i_{D1} increases and i_{D2} decreases.

Step 4 [t_3, t_4]: At t_3, S_6 is turned off. i_{Lr1} will charge C_{S6} and discharge C_{S5}. The ZVS turn-on condition of S_5 is given in Equation (6).

$$L_r i_{Lr1}^2(t_3) \geq 2C_{oss} V_{in}^2 \tag{6}$$

Step 4 ends at t_4 when $v_{CS5} = 0$. The time Δt_{34} in this step can be obtained in Equation (7).

$$\Delta t_{34} \approx 2V_{in} C_{oss} / i_{Lr1}(t_3) \tag{7}$$

Step 5 [t_4, t_5]: At t_4, $v_{CS5} = 0$. Then D_{S5} is conducting due to $i_{Lr1}(t_4) > 0$. The ZVS operation of S_5 is naturally realized. In step 5, the leg voltage $v_{bc} = -V_{in}$ and D_1 and D_2 are still conducting. The inductor voltage $v_{Lr1} = -V_{in}$. The output filter inductor voltages $v_{Lo1} = v_{Lo2} = -V_o$. Therefore, inductor currents i_{Lo1}, i_{Lo2}, and i_{Lr1} all decrease. Step 5 ends at t_5 when $i_{D2} = 0$. The time duration Δt_{45} is derived as Equation (8):

$$\Delta t_{45} \approx (I_o L_r)/(V_{in} N_L) \tag{8}$$

The duty loss in this step can be derived in Equation (9).

$$d_5 \approx (I_o L_r f_{sw})/(V_{in} N_L) \tag{9}$$

where f_{sw} is the switching frequency. Then, the circuit operation will go to next half switching cycle at time t_5.

For high voltage input operation ($2.3V_{in,min} \leq V_{in,H} < 5V_{in,min}$), ac switch Q is ON and active devices S_4 and S_3 are OFF. Then, the full-bridge converter with switches S_1, S_2, S_5, and S_6, as shown in Figure 1c, is operated with duty cycle control. The transformer turns ratio on this equivalent circuit becomes $N_H = 2n_p/n_s$. The dc gain can be expressed as $V_o/V_{in,H} \approx d_{eff}/N_H$. This can be observed in Figure 2b. The converter has five steps in one-half of the switching period. The corresponding step circuits are given in Figure 4, and the circuit operations are explained briefly in the following discussions.

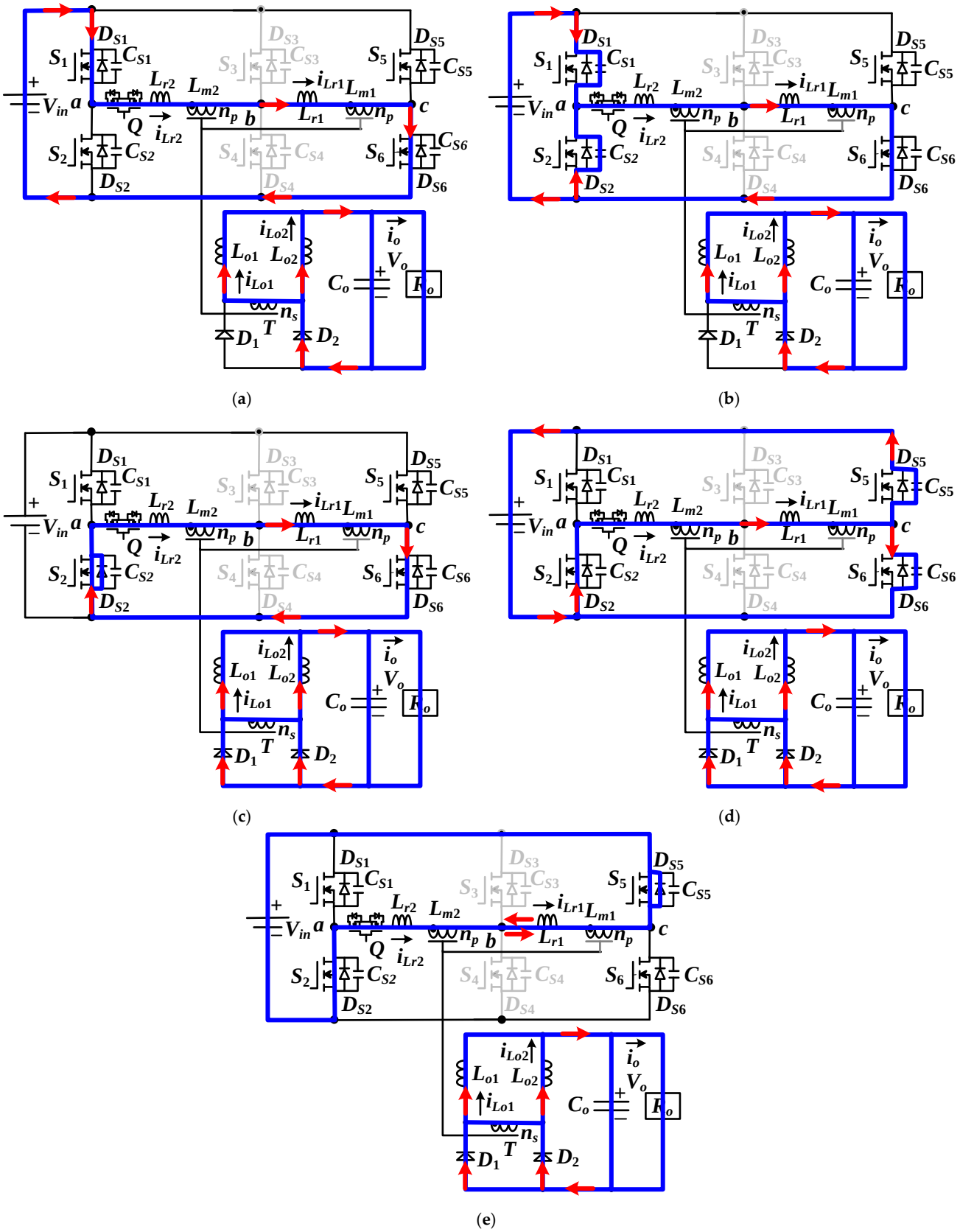


Figure 4. Equivalent circuits under high voltage input condition during the first half switching period: (**a**) step 1 circuit; (**b**) step 2 circuit; (**c**) step 3 circuit; (**d**) step 4 circuit;(**e**) step 5 circuit.

Step 1 [t_0, t_1]: The current $i_{D1} = 0$ at t_0. Thus, D_1 is OFF. In step 1, S_1 and S_6 are conducting, $v_{ac} = V_{in}$, $v_{Lo1} = V_{in}/N_H - V_o$, and $v_{Lo2} = -V_o$. The currents i_{Lr1} and i_{Lo1} increase and i_{Lo2} decreases. Step 1 ends at t_1 when S_1 turns off.

Step 2 [t_1, t_2]: S_1 is turned off at t_1. $i_{Lr1} = i_{Lr2} > 0$ and C_{S2} (C_{S1}) is discharged (charged) by i_{Lr2}. The ZVS turn-on operation of S_2 is expressed as Equation (10):

$$(2L_r + N_H^2 L_o) i_{Lr2}^2(t_1) \geq 2C_{oss} V_{in}^2 \tag{10}$$

Step 3 [t_2, t_3]: $v_{CS2}(t_2) = 0$. $i_{Lr2} > 0$ and D_{S2} is forward biased. At this moment, S_2 is turned ON under zero voltage. The leg voltage $v_{ac} = 0$ and both diodes D_1 and D_2 conducting. Therefore, $v_{Lo1} = v_{Lo2} = -V_o$ and $v_{Lr1} + v_{Lr2} = -v_{S2,drop} - v_{S6,drop} - v_{Q,drop}$. The currents i_{Lo1}, i_{Lo2}, i_{Lr1}, and i_{D2} decrease and i_{D1} increases.

Step 4 [t_3, t_4]: S_6 turns OFF at t_3. i_{Lr1} charges (discharges) C_{S6} (C_{S5}). The ZVS turn-on condition of S_5 is obtained as Equation (11):

$$2L_r i_{Lr2}^2(t_3) \geq 2C_{oss} V_{in}^2 \tag{11}$$

This step ends at t_4 when C_{S5} is discharged to zero voltage.

Step 5 [t_4, t_5]: $v_{CS5}(t_4) = 0$. Since $i_{Lr1}(t_4)$ is positive, D_{S5} becomes forward biased. In this step, $v_{ac} = -V_{in}$ and D_2 and D_1 are ON. It can be obtained that $v_{Lr1} + v_{Lr2} = -V_{in}$, and $v_{Lo2} = v_{Lo1} = -V_o$. i_{Lo2}, i_{Lo1}, and i_{Lr1} all decrease. This step ends at t_5 when $i_{D2} = 0$. The time Δt_{45} is obtained as Equation (12):

$$\Delta t_{45} \approx (2I_o L_r)/(V_{in} N_H) \tag{12}$$

The duty loss can be calculated in Equation (13).

$$d_5 \approx (2I_o L_r f_{sw})/(V_{in} N_H) \tag{13}$$

At t_5, the circuit operation will go to the next half switching period.

4. Steady State Analysis

In relation to the ON/OFF status of Q and S_1–S_6, two equivalent sub-circuits shown in Figure 1 are operated to have a wide voltage input operation and a ZVS turn-on operation. According to the voltage-second balance on L_{o1} or L_{o2}, the load voltage V_o can be expressed as Equation (14):

$$V_o = \begin{cases} \frac{n_s V_{in,L}}{n_p}(d - \frac{n_s I_o L_r f_{sw}}{n_p V_{in,L}}) - V_D, \; V_{in,\min} \leq V_{in,L} < 2.3V_{in,\min} \\ \frac{n_s V_{in,H}}{2n_p}(d - \frac{n_s I_o L_r f_{sw}}{n_p V_{in,H}}) - V_D, \; 2.3V_{in,\min} < V_{in,L} \leq 5V_{in,\min} \end{cases} \tag{14}$$

where d is the duty cycle on voltage v_{ac} or v_{bc}. For the low voltage input condition, $N_L = n_p/n_s$ is obtained as Equation (15):

$$N_L = \frac{V_{in,L}}{(V_o + V_D)}(d - \frac{I_o L_r f_{sw}}{N_L V_{in,L}}) \tag{15}$$

The winding turns of transformer T are expressed as $n_p \geq (V_{in,\min} d_{\max} T_{sw})/(\Delta B A_e)$ and $n_s = n_p/N_L$. If the duty loss in (9) is defined, L_{r1} and L_{r2} can be approximated as Equation (16):

$$L_r = L_{r1} = L_{r2} = \frac{N_L d_5 V_{in}}{f_{sw} I_o} \tag{16}$$

In the presented circuit, the load current is equally distributed on inductors L_{o1} and $L_{o2,}$ and $I_{Lo1} = I_{Lo2} = I_o/2$. If the ripple currents of L_{o1} and L_{o2} are identical (i.e., $\Delta i_{Lo1} = \Delta i_{Lo1} = \Delta i_{Lo}$), then $L_{o1} = L_{o2} = L_o$ can be calculated in Equation (17).

$$L_o = \frac{(V_o + V_D)}{\Delta i_{Lo} f_{sw}}\left(1 - d + \frac{n_s I_o L_r f_{sw}}{n_p V_{in,L}}\right) \tag{17}$$

Then, the winding turns of L_{o1} and L_{o2} are obtained as $n_{Lo} \geq [L_o(I_o + \Delta i_{Lo})/2]/(B_{\max} A_e)$. The peak switch currents are approximated as Equation (18):

$$i_{Sx,paek} \approx \frac{(I_o + \Delta i_{Lo})/2}{N_L} + \frac{\Delta i_{Lm}}{2} = \frac{(I_o + \Delta i_{Lo})/2}{N_L} + \frac{dV_{in,L}T_{sw}}{2L_m} - \frac{L_r I_o}{2N_L L_m} \tag{18}$$

where x = 1~6. From the ZVS conditions in (4) and (6), the ZVS operation of leading-leg switches are easier to achieve than lagging-leg switches under the given inductance L_{r1}. The necessary inductances $L_{r1} = L_{r2} = L_{r2}$ are derived as $L_r \geq 2C_{oss}V_{in}^2/i_{Lr1}^2(t_3)$ to achieve the ZVS operation of lagging-leg switches S_5 and S_6. The voltage stress of S_1–S_6 and Q is $V_{in,max}$. The voltage stress and dc currents of D_2 and D_1 are obtained as $V_{in,max}/N_L$ and $I_o/2$, respectively.

5. Experimental Results

The performance of the converter is confirmed from a laboratory circuit with 800 W rated power. The electric specifications of the test circuit are V_{in} = 120–600 V, the output voltage V_o = 48 V, the maximum power P_o = 800 W, and f_{sw} = 140 kHz. The presented converter operates in the low voltage input condition if 120 V $\leq V_{in} <$ 270 V. Then, Q, S_1, and S_2 are OFF. Likewise, the presented converter operates in the high voltage condition if 270 V $< V_{in} \leq$ 600 V. For the high voltage input operation, S_3 and S_4 are OFF and Q is ON. A Schmitt trigger circuit with ±20 V voltage tolerance is selected to avoid control signal oscillation at the transition voltage 270 V. Therefore, the actual low and high voltage input ranges are $V_{in,L}$ = 120–290 V and $V_{in,H}$ = 250–600 V. Figure 5a gives the circuit parameters of a prototype circuit. The phase-shift PWM integrated circuit UCC3895 is selected to produce the gating waveforms of S_5 and S_6. The gating waveforms of S_1–S_4 are generated by the logic gates and PWM output of UCC3895. Figure 5b gives the picture of the prototype circuit in the laboratory test.

The experimental waveforms of the proposed converter at a low voltage input range (V_{in} = 120~290 V) are given in Figures 6–9. The measured results under a high voltage input range (V_{in} = 250~600 V) are given in Figures 10–13. Figure 6 provides the experimental primary-side (Figure 6a) and secondary-side (Figure 6b) waveforms at V_{in} = 120 V and P_o = 800 W. Note that the duty cycle on voltage v_{bc} is close to 0.5, the ripple current on $i_{Lo1} + i_{Lo2}$ is reduced compared to the ripple current on i_{Lo1} or i_{Lo2}, and the resultant current $i_{Lo1} + i_{Lo2}$ has twice the switching frequency of currents i_{Lo1} and i_{Lo2}. Figure 7a,b gives the PWM signal of S_3 at 20% power and 100% power with the V_{in} = 120 V input case. In the same way, the PWM waveform of S_5 (lagging-leg switch) at 50% and 100% loads are illustrated in Figure 7c,d. Figures 8 and 9 provide the measured results of the presented converter operated at V_{in} = 290 V in the low voltage input region. Since the higher input voltage will result in a lower duty cycle, it is clear that the voltage v_{bc} at V_{in} = 290 V input has less duty ratio than in the V_{in} = 120 V input condition. It can also be noted in Figures 6b and 8b that $i_{Lo1} + i_{Lo2}$ has more ripple current at V_{in} = 290 V than V_{in} = 120 V. Figure 9 gives the experimental waveforms of S_3 in leading leg and S_5 in lagging leg in the 290 V input condition. It can be observed from Figures 7 and 9 that the ZVS turn-on operation of S_3 is realized from 20% power for both 120 V and 290 V input conditions. Likewise, the ZVS turn-on operation of S_5 is accomplished from 50% power under 120 V and 290 V input cases. For a high voltage input range (Q is ON and S_3 and S_4 are OFF), the test results are shown in Figures 10–13. For V_{in} = 250 V, the experimental results at 100% power are given in Figure 10. The PWM signals of S_1 and S_5 are given in Figure 11. In the same way,

the experimental waveforms for V_{in} = 600 V input are given in Figures 12 and 13. From the experimental results in Figures 7, 9, 11 and 13, it can be observed that the leading-leg switch, such as S_1 and S_3, can achieve ZVS operation from 20% load, and the ZVS operation of S_5 in the lagging leg is from 50% power. The measured results of V_{in}, $v_{Q,g}$, $v_{S1,g}$, and $v_{S3,g}$ between 120V and 600 V input are shown in Figure 14. When V_{in} is increased from 120 V to 290 V, the presented circuit is controlled in the low voltage input range. Q, S_1, and S_2 are OFF and S_3 and S_4 are controlled with the phase-shift PWM approach. When V_{in} > 290 V, Q is ON and S_3 and S_4 are OFF. S_1 and S_2 are operated with duty cycle control. When V_{in} is decreased from 600 V to 250 V, the converter is controlled in the high voltage input range. The switch Q is ON and S_3 and S_4 are OFF. The test results in Figure 14 are in agreement with the theoretical analysis. The test efficiencies of the proposed converter are 89.3% and 91.2% for 120 V and 600 V input cases under a full load. The synchronous rectifiers can be further used on the secondary side to reduce the conduction losses on D_1 and D_2 and improve the converter efficiency.

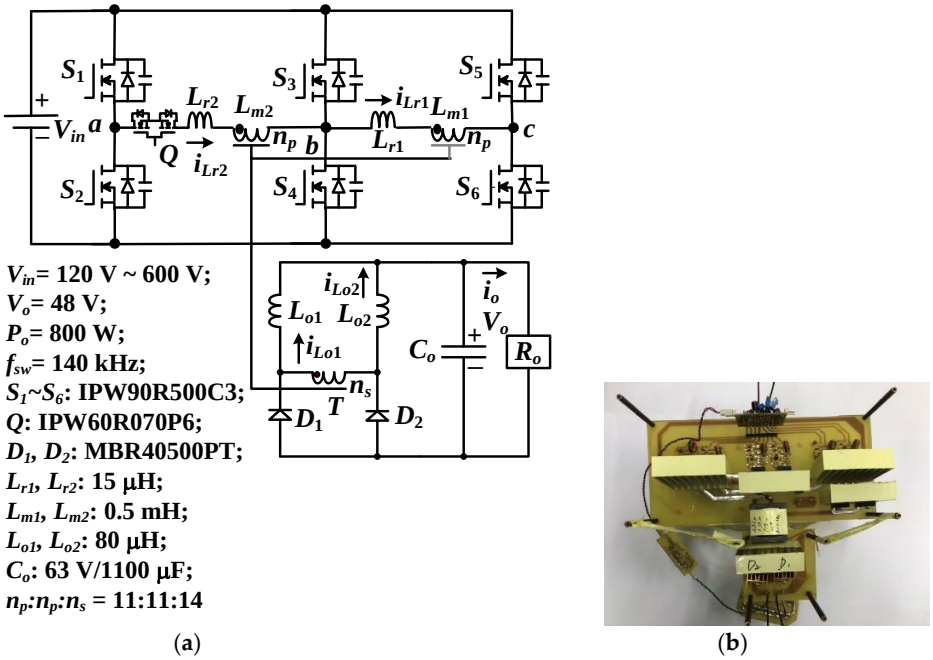


Figure 5. Laboratory prototype: (**a**) circuit diagram; (**b**) picture of prototype circuit.

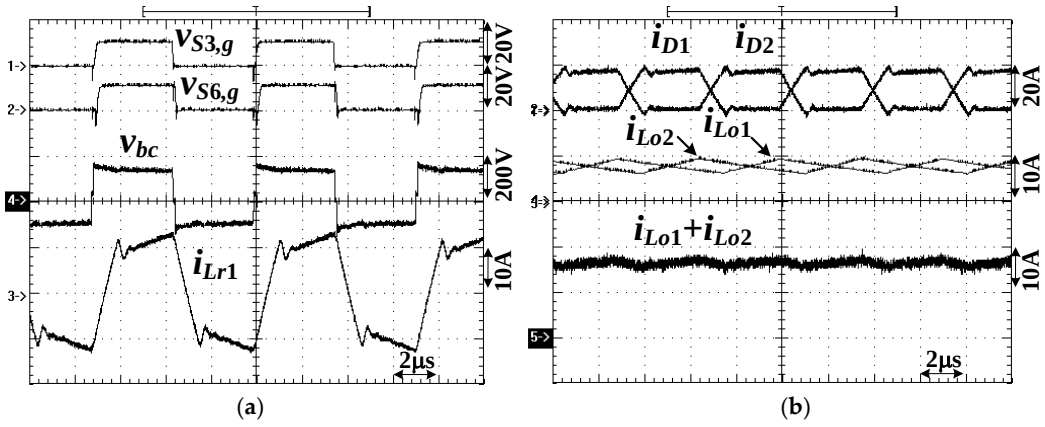


Figure 6. Test waveforms at V_{in} = 120 V (low voltage input range) and P_o = 800 W: (**a**) primary-side waveforms $v_{S3,g}$, $v_{S5,g}$, v_{bc}, and i_{Lr1}; (**b**) secondary-side waveforms i_{D1}, i_{D2}, i_{Lo1}, i_{Lo2}, and i_{Lo1} + i_{Lo2}.

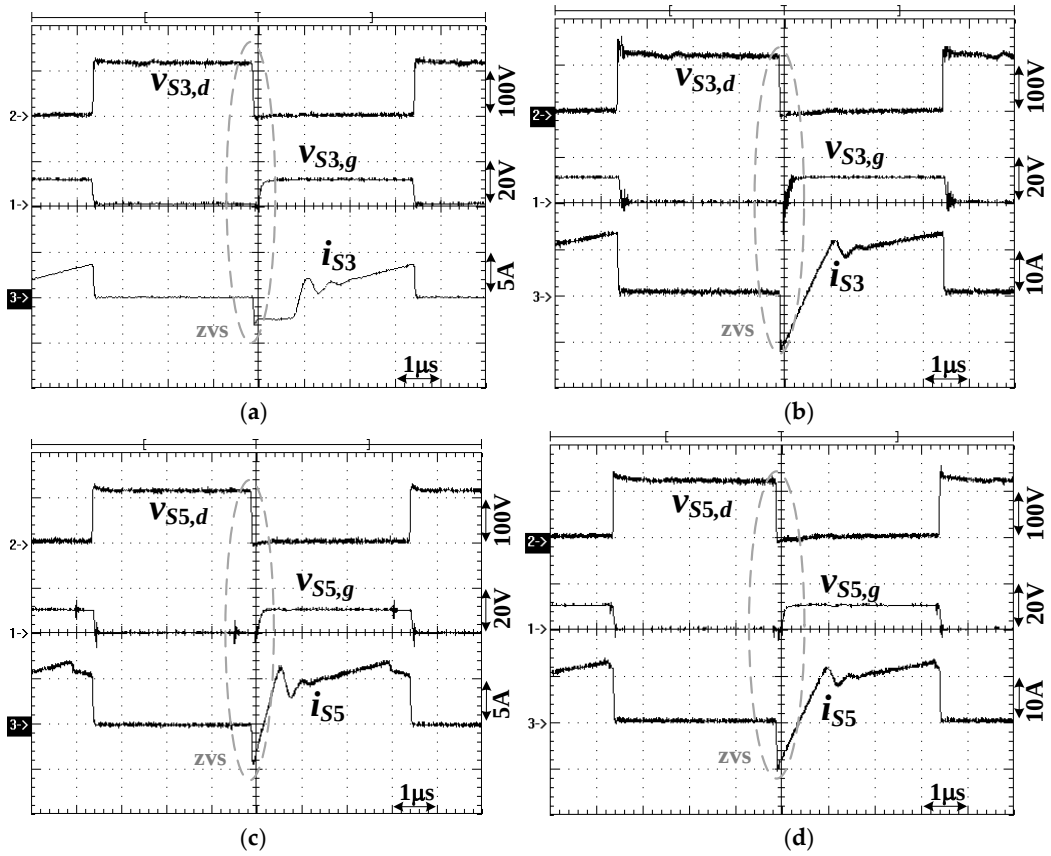


Figure 7. Test waveforms of S_3 and S_5 at V_{in} = 120 V (low voltage input range): (**a**) S_3 under 20% load; (**b**) S_3 under 100% load; (**c**) S_5 under 20% load; (**d**) S_5 under 100% load.

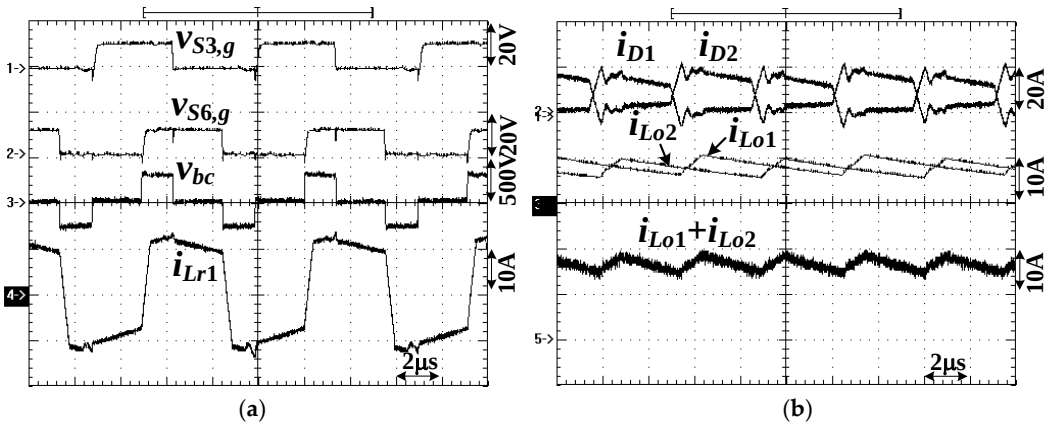


Figure 8. Test waveforms at V_{in} = 290 V (low voltage input range) and P_o = 800 W: (**a**) primary-side waveforms $v_{S3,g}$, $v_{S5,g}$, v_{bc}, and i_{Lr1}; (**b**) secondary-side waveforms i_{D1}, i_{D2}, i_{Lo1}, i_{Lo2}, and i_{Lo1} + i_{Lo2}.

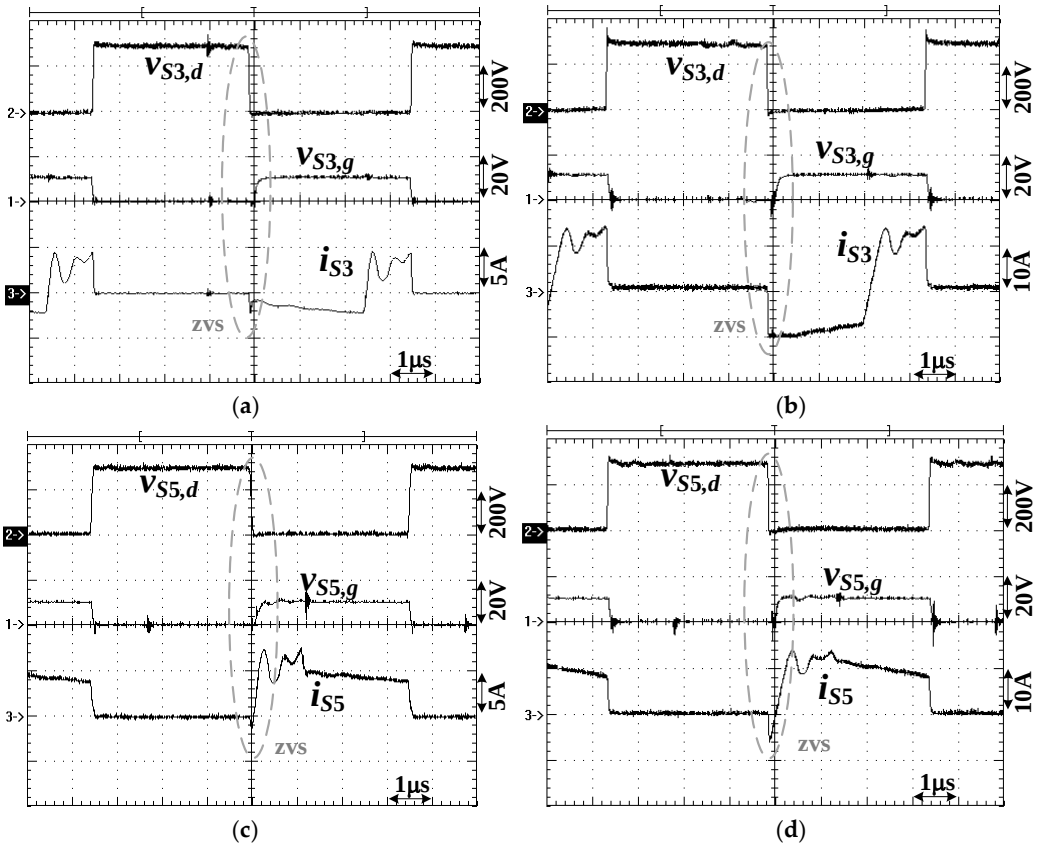


Figure 9. Test waveforms of S_3 and S_5 at V_{in} = 290 V (low voltage input range): (**a**) S_3 under 20% load; (**b**) S_3 under 100% load; (**c**) S_5 under 20% load; (**d**) S_5 under 100% load.

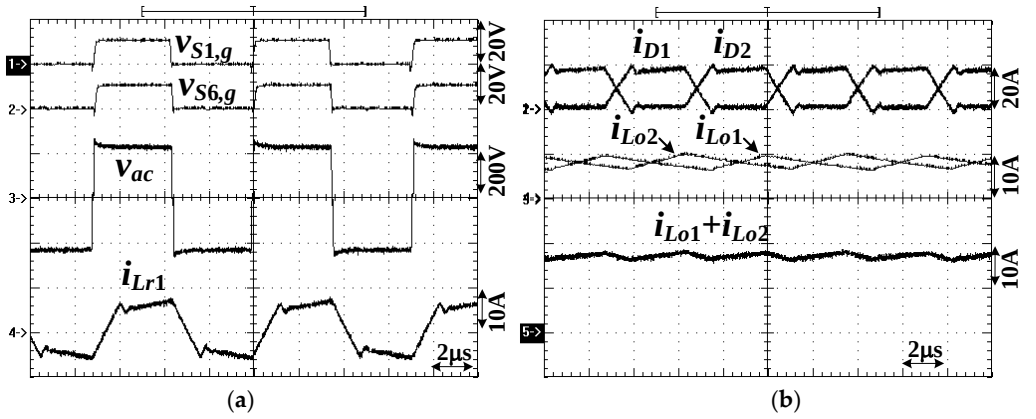


Figure 10. Test waveforms at V_{in} = 250 V and P_o = 800 W: (**a**) primary-side waveforms $v_{S1,g}$, $v_{S5,g}$, v_{ac}, and i_{Lr1}; (**b**) secondary-side waveforms i_{D1}, i_{D2}, i_{Lo1}, i_{Lo2}, and i_{Lo1} + i_{Lo2}.

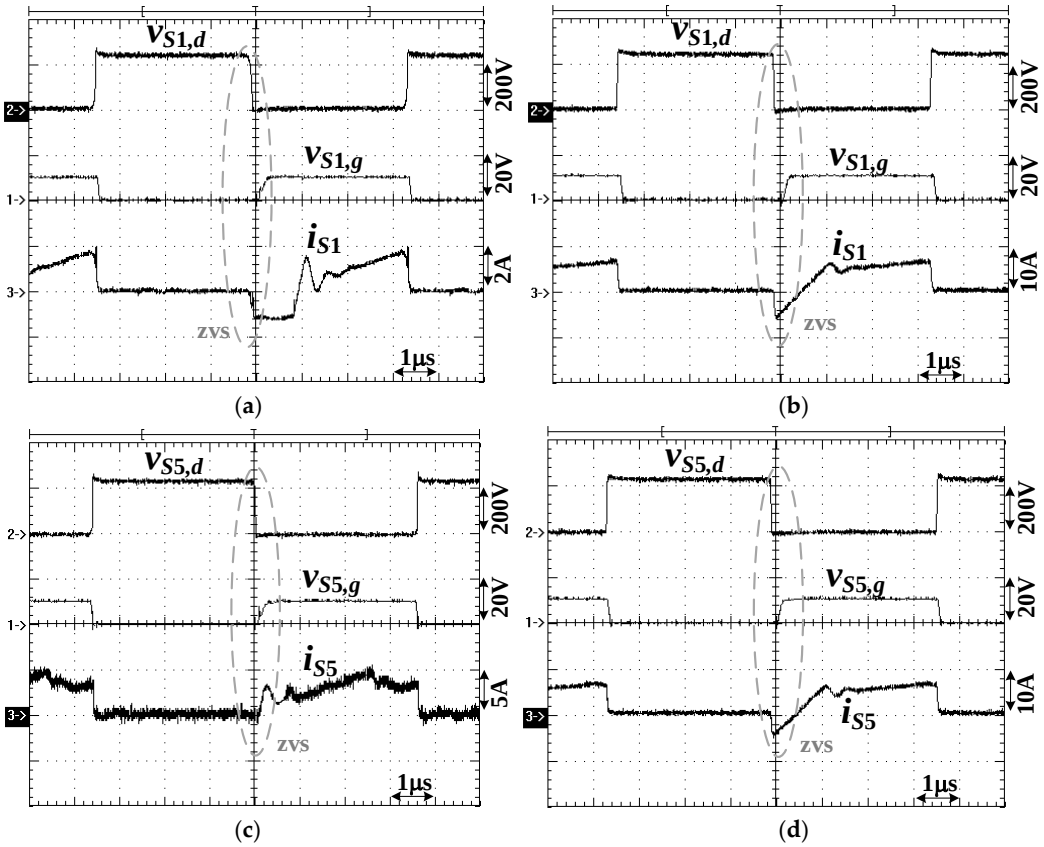


Figure 11. Test waveforms of S_1 and S_5 at V_{in} = 250 V: (**a**) S_1 under 20% load; (**b**) S_1 under 100% load; (**c**) S_5 under 20% load; (**d**) S_5 under 100% load.

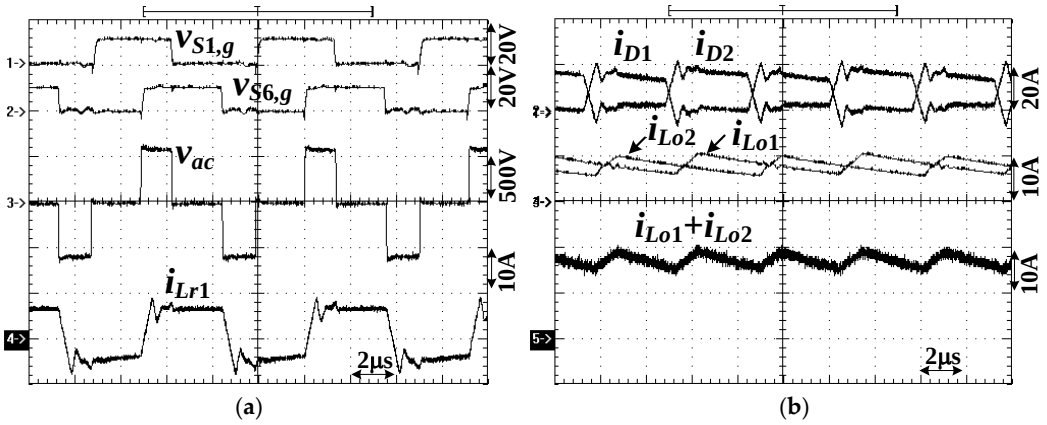


Figure 12. Test waveforms at V_{in} = 600 V and P_o = 800 W: (**a**) primary-side waveforms $v_{S1,g}$, $v_{S5,g}$, v_{ac}, and i_{Lr1}; (**b**) secondary-side waveforms i_{D1}, i_{D2}, i_{Lo1}, i_{Lo2}, and i_{Lo1} + i_{Lo2}.

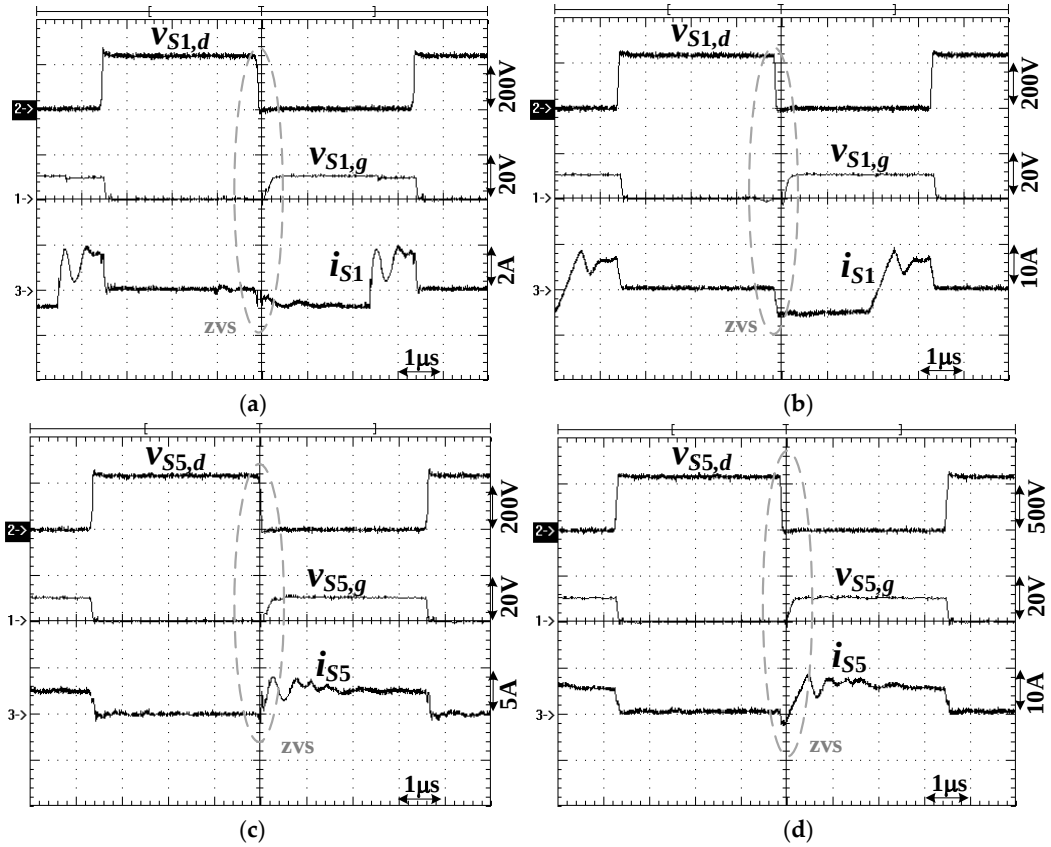


Figure 13. Test waveforms of S_1 and S_5 at V_{in} = 600 V: (**a**) S_1 under 20% load; (**b**) S_1 under 100% load; (**c**) S_5 under 20% load; (**d**) S_5 under 100% load.

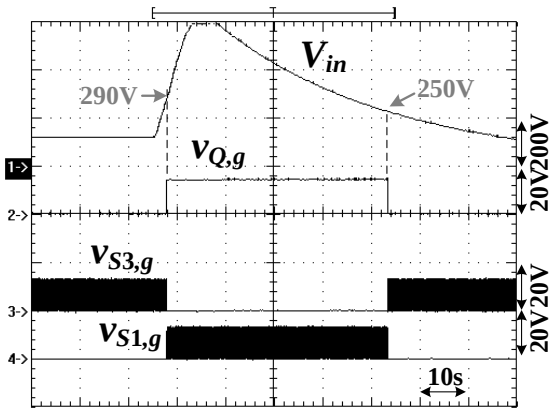


Figure 14. Test waveforms of V_{in}, $v_{Q,g}$, $v_{S1,g}$, and $v_{S3,d}$ under V_{in} = 120–600 V variation.

6. Conclusions

A ZVS converter with three-leg circuit topology is presented and discussed, and an 800 W prototype is constructed and measured to achieve ZVS operation and a wide voltage input operation. The presented converter is expected to be used for dc converters with wide input-voltage or output-voltage demand such as dc wind power applications, battery charger systems with wide voltage operation, and solar PV panel power units with variable input voltage. The proposed converter with a phase-shift PWM scheme can be operated at two equivalent circuits. Therefore, active devices in the leading leg are easily turned on under zero voltage. The current doubler rectification circuit is operated on the low-voltage side in order to have less output ripple current. Compared to conventional phase-shift PWM converters, the studied circuit topology has a wider voltage input capability with

the drawback of using an extra three switches in the presented converter. Finally, test results with an 800 W prototype are provided to demonstrate circuit characteristics and the validity of the operating principle.

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