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Review

Flip-Chip (FC) and Fine-Pitch-Ball-Grid-Array (FPBGA) Underfills for Application in Aerospace Electronics—Brief Review

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Abstract: In this review, some major aspects of the current underfill technologies for flip-chip (FC) and fine-pitch-ball-grid-array (FPBGA), including chip-size packaging (CSP), are addressed, with an emphasis on applications, such as aerospace electronics, for which high reliability level is imperative. The following aspects of the FC and FPGGA technologies are considered: attributes of the FC and FPBGA structures and technologies; underfill-induced stresses; the roles of the glass transition temperature (T_g) of the underfill materials; some major attributes of the lead-free solder systems with underfill; reliability-related issues; thermal fatigue of the underfilled solder joints; warpage-related issues; attributes of accelerated life testing of solder joint interconnections with underfills; and predictive modeling, both finite-element-analysis (FEA)-based and analytical ("mathematical"). It is concluded particularly that the application of the quantitative assessments of the effect of the fabrication techniques on the reliability of solder materials, when high reliability is imperative, is critical and that all the three types of research tools that an aerospace reliability engineer has at his/her disposal, should be pursued, when appropriate and possible: experimental/testing, finite-element-analysis(FEA) simulations, and the "old-fashioned" analytical ("mathematical") modeling. These two modeling techniques are based on different assumptions, and if the computed data obtained using these techniques result in the close output information, then there is a good reason to believe that this information is both accurate and trustworthy. This effort is particularly important for high-reliability FC and FPBGA applications, such as aerospace electronics, as the aerospace IC packages become more complex, and the requirements for their failure-free operations become more stringent.

Keywords: aerospace electronics; flip-chip; FC and FPBGA, underfill; predictive modeling; reliability

1. Introduction

The drive for higher performance and smaller size of FC and FPBGA packages is attractive for numerous applications. These applications include:

(1) commercial products, operated in relatively mild conditions and for which highly reliable performance is usually not as important as, say, cost-effectiveness and time-to-market;
(2) automotive electronics, experiencing during operation and testing extreme environmental conditions (such as temperatures ranging from −40 °C to +125 °C, high humidity of, say, 85% RH,

and extensive vibrations); although the requirements for its failure-free performance are more stringent than for commercial electronics, these requirements are still rather moderate; and

(3) aerospace, military, long-haul communication, and medical electronics, whose high-level reliability is always imperative, no matter how severe and uncertain the operation conditions might be.

The emphasis of this review is on the third type of IC products.

Recent and numerous experiments have demonstrated that, for the same FC and the solder ball size and count, reduced ball pitch, package size, and increased ball density resulted, for the right design-for-reliability (DfR) solution in higher reliability of the solder system. This suggests that package miniaturization by employing FC and FPBGA technologies is a feasible low-cost and high-reliability packaging technologies of choice. These technologies are currently used in different IC packaging designs including chip-scale packaging (CSP), in which the die is directly attached to the printed circuit board (PCB). There are, nonetheless, numerous situations when the appropriate reliability level cannot be achieved without bringing in "surrogate" materials, known as underfills, under the chip to assure the short- and long-term reliability of the product. The review that follows provides a brief literature survey of the state-of-the-art in the field of FC and FPBGA IC packages with underfills. Their key role is to improve reliability by redistributing the stress, and moving the high stresses away from the vulnerable solder interconnects without introducing other unwanted failures. Solder joint fatigue failures and delaminations (usually at the chip-solder interface) were found as the most typical failure modes in FC and FPBGA structures with underfills. The appropriate underfills are expected to eliminate these failure modes.

Underfill processes and materials introduced about 60 years ago is a continuously evolving effort. First of all, one should answer, of course, the fundamental question: "to underfill or not to underfill?" the FC package of interest, i.e., whether it would be possible to get away with an un-encapsulated FC or FPBGA design and still meet the reliability requirements for the given product and application. If an "underfill" decision is made, because otherwise the product's reliability will be most likely compromised, one should look at the type of the adequate encapsulation process and underfill material(s) he/she is going to use, considering time-to-market (completion), cost, manufacturability, testability, etc.

A non-appropriate underfill material or process can easily result in more harm than good, i.e., it can make the situation worse, not better. Because of that reliability-physics based, quantifiable, and trustworthy ways should be used to predict, at the design stage, the product's reliability without and with an underfill. Alternate approaches could and should be also considered and developed, such as, e.g., using layer(s) of constraining materials (carbon fiber-reinforced polymers, aluminum and copper, etc.) to reduce the Coefficient of Thermal Expansion (CTE) of the PCB to achieve better thermal stress match with silicon (Si) and for lower thermally induced stresses.

2. FC and FPBGA Technologies in IC Packaging

Developed by IBM in the 1960s, FC interconnection technology addresses IC packaging design problems by distributing input/outputs (I/Os) and power connections across the FC active surface area. The solder bump array allows, in a FC design, for high interconnect densities and provides both electrical connections and mechanical support for the chip. In addition, short interconnect lengths minimize signal inductance, thereby resulting in considerable speed improvements over wire-bonded chip designs. With the exception of 3D packaging, the FC technology provides the ultimate in size reduction and has become, therefore, a popular packaging method for ultimate density and performance.

FCs may be attached directly to a circuit board. These are CSP designs. In such designs, FCs are overmolded by an encapsulant. Another option is to attach a FC to its own substrate and to place the thereby-obtained package onto a PCB using BGA or column-grid-array (CGA) interconnections. This option is known as the second level of interconnection. Yet another possible option is to juxtapose

a FC package onto another FC package. This structure is known as a package-on-package (PoP) design, or a stack-package-design (SPD). In addition to real estate savings, FCs and FPBGAs are appreciably less expensive in high-volume production than wire-bonded chips. This makes them ideal for high-volume electronics applications in devices like cell phones (CPs) and personal digital assistants (PDAs)—handheld information electronic devices.

The reliability of FC and FPBGA technologies is, however, often insufficient for particular products and applications, especially when high operational reliability is required. This is mostly because FC and FPBGA solder joint interconnections are stiff and firmly sandwiched between the chip and the substrate, or between the chip and the PCB. Unlike wire-bonds, FC bumps are not free to flex, and, because of that, FC and FPBGA assemblies experience high thermal stresses during temperature excursions. Accordingly, epoxy encapsulants, "underfills", are widely employed to fill in the gap between the FC and the substrate. This results in thermal stress relief in the solder material and is aimed at preventing the fatigue damage of the solder joints and their delamination from the chip.

The underfill mechanically couples the chip and the substrate. As has been indicated, the attributes of the underfill materials and technologies are critically important: a poorly selected encapsulant can easily worsen the package reliability. The design and testing of a suitable underfill should consider, in addition to thermal loading, also mechanical (mostly drop and/or vibration induced) loading. In combination with thermally induced stresses, mechanical (mostly dynamic) stresses are also of concern. Furthermore, the employment of FC and FPBGA technologies could be limited also by the requirements for testability, standardization, PCB routability, rework, as well as by the various technological requirements for the underfilling process. Considered underfill material (whether flowable, no-flow, or reworkable), encapsulation technique, curing methods, fillers and filler particles, the role of viscosity during the product's fabrication and operation, and the attributes of the manufacturing process, as well as short- and long-term reliability of this material, should always be carefully evaluated and decided upon in every FC or FPGGA effort.

Although several possible FC encapsulants and several ways of applying them were initially considered (about three decades ago) [1], it was the underfill encapsulation that became the today's technology of choice [2–8]. Because the main reason for introducing FC and FPBGA technologies was insufficient reliability of FC and FPBGA technologies, the overwhelming majority of publications were and still are dedicated to the reliability issues and challenges (see, e.g., [9,10]), as well as to the selection of the appropriate FC or FPBGA technology and encapsulant [11–15].Ceramic packages are, as is known, more reliable than plastic packages, both because a better thermal match of ceramic materials with Si and because of high reliability of these materials The early investigations of FC technologies were geared therefore to ceramic packages (see, e.g., [16]).

A comprehensive review of the state-of-the-art in the field in question was carried out by Ghaffarian [17]. He addressed the following major aspects of the today's FC and FPBGA technologies: adhesives in electronics, curing methods, underfill encapsulants and encapsulation techniques, application of flowable and no-flow underfills, fillers and filler particles, reworkable underfills, and the role of the underfill viscosity. Because of that, these important properties of the underfill materials and technologies are only cursorily mentioned in the current review.

3. Underfill-Induced Stresses, and the Roles of the Glass-Transition-Temperature (*Tg*)

Thermally induced stresses in the chip, in the substrate, and in the underfill itself depend on the CTE of all the assembly materials and components, their size and thickness, and their mechanical ("physical") characteristics. Typically, because of the larger CTE of the substrate and the underfill relative to the Si, the chip is subjected to compression as a result of cooling down from the cure/fabrication temperature. The package is considered stress free at this temperature. The composite solder-underfill layer and the substrate are under tension.

The bonding layer in a FC or a FPBGA assembly is characterized, unlike in adhesively bonded joints, by a relatively high effective Young's modulus: this layer is comprised of high-modulus

solder and low-modulus epoxy encapsulant (underfill), even when the underfill epoxy is loaded with fillers. Tri- and bi-material analytical stress models were considered [18,19] for the evaluation of the thermally induced interfacial shearing stresses, as well as normal stresses acting in the cross-sections of the assembly components, in the application to a typical FC or a FPBGA design. While in a tri-material model all the three materials (the chip, the substrate, and the bonding layer) are treated as "equal partners", i.e., all experience thermally induced forces acting in their cross-sections, in a bi-material model a significant simplification is made, assuming that the bonding layer is much thinner than the bonded components and its Young's modulus is significantly lower than the moduli of the chip and the substrate materials. In the carried out numerical example [18] based on the application of the tri-material model, the highest shearing stress occurred, as it has been expected, at the chip-bond interface and was significantly, by a factor of about 2.45, higher than the shearing stress at the substrate-bond interface. However, even the latter stress was about twice as high as the maximum shearing stress predicted using the bi-material model. As to the normal stresses in the cross-sections of the assembly components, the tri-material model predicted that the highest (compressive) stress occurred in the chip; the lowest (tensile)—in the substrate; and that the stresses in the underfill-containing bond, also tensile, are rather high, comprising about 59% of the stresses in the compressed chip. The bi-material model simply assumes, as has been indicated above, that the longitudinal normal stresses in the bonding layer are zero, while the interfacial shearing and peeling stresses in it are not. The normal stresses in the chip predicted on the basis of this model are only about 78% of the stress predicted by the tri-material model. The normal stresses in the substrate evaluated on the basis of the bi-material model are almost twice as high as the tri-material model predicts, but these stresses are low anyway: it is the stress in the chip and in the bonding layer, and, even more importantly, the interfacial stress at the chip-bond interface that should be of major concern to the device designer and reliability engineer. It is concluded that while a simple bi-material model can be successfully used for adhesively bonded assemblies, a tri-material model should be employed for FC and FPBGA assemblies, especially when high-modulus solders and high enough modulus underfills, and particularly those loaded with fillers, are used. As to the interfacial shearing stresses, the highest predicted shearing stress occurred in the carried out example at the chip/solder interface and was as high as about 62% of the normal stress in the chip. It is this stress that determines the strength of the solder joints in a FC and FPBGA designs.

Epoxy underfills often undergo during the curing process a phase transition when crossing the glass transition temperature (T_g) [20]. Below this temperature the epoxy is in a hard, glassy state. Above the T_g, the encapulant transitions to a rubbery state, and its molecules become less orderly and have more freedom to move freely. Most epoxies are characterized above the T_g by a significantly lower strength; by a considerably, by an order of magnitude, lower modulus; and by a substantially higher, by a factor, of about 3 or so, CTE. If these properties were to change drastically during thermal cycling, solder fatigue or delamination could occur. Because of this, epoxies considered as underfills are typically formulated with T_g of 150 °C or higher, i.e., well above the maximum test, not to mention service conditions for most electronic materials. Underfills with high T_g usually show better performance during temperature cycling tests. It is noteworthy that while for adhesively bonded assemblies (a bi-material thermal stress model can be used in such a case), there is an incentive to employ adhesives with low T_g, because such adhesives have low Young's moduli and, as a result of that, low shear moduli and high interfacial compliance, thereby leading to significant stress relief, it might be not the case for FP and FPBGA designs

Experiments show that packages with high-T_g underfills are less sensitive to the 85 °C/85% RH temperature-humidity bias, while those with low-T_g underfills are somewhat sensitive to such a bias. It has also been found that higher T_g underfills result in somewhat higher induced curvatures than low T_g underfills; that packages with low-T_g underfills exhibit during cooling processes appreciable stress relaxation; and that the final deformations of the packages (at low temperature conditions) depend on the cooling rate. The latte phenomenon has not been observed though for packages with high-T_g

underfills. Lead-free solders (discussed in greater detail in the next section) are more brittle than tin-lead solders and, because of that, might have less fatigue resistance when subjected to temperature excursions and mechanical loading. Because of that, a higher T_g underfill might be recommended for better fracture toughness of lead-free solders.

The literature of the visco-elastic properties of underfills and particularly their manufacturing and viscous flow-related properties is enormous (see, e.g., [21–27] as suitable examples) and is beyond the scope of this review.

4. Lead-Free Solders

Since lead-free alloys require higher reflow temperatures for assembly than tin–lead eutectic alloys, the use of such solders places higher demands on package materials. On the other hand, lead-free solders are characterized by higher yield stress, and therefore are less prone to low-cycle fatigue condition. The use of lead-free solders is addressed during the last decade by numerous investigators (see, e.g., [28]). The attributes of lead-free solders in connection with the use of underfills were also evaluated in a number of investigations (see, e.g., [29–32]) and are beyond the scope of this review.

5. Some Reliability-Related Issues

As has been indicated, underfills have been introduced to improve the fatigue strength of the encapsulated solder material [32–48]. The predominant type of failure in underfilled FCs and FPBGA designs is often, however, not solder fatigue, but possible delaminations, especially when FC and FPBGA assemblies are subjected, during temperature cycling testing, to high temperatures and high humidity. When moisture penetrates the underfill encapsulant, the excessive heat applied during reflow soldering may produce enough vapor pressure to stress the joints. If the resulting "popcorning" stress exceeds the adhesive strength of the underfill, delamination between the underfill and the die, or, less likely, between the underfill and the substrate, may occur. Consequently, underfills should be formulated to resist moisture and to have enough adhesive strength to overcome vapor pressure built up in the underfill during solder processing. Note that not only the adhesive and cohesive strength of the underfill, but even its CTE and elastic constants, needed for reliability modeling evaluations, both analytical and FEA-based, can be determined from more or less routine shear-off tests [49]. The corresponding predictive model should be re-considered, however, and the tri-material model should be employed in the analysis of such tests.

To achieve higher reliability and proper use of underfills, it is critical to establish correlation between FC or FPBGA reliability and the mechanical properties of the underfill material [50–53]. This includes the role of voids [54].To what extent is it crucial to prevent their formation? Voids at the base of the solder joint due to flux residue from the no-clean solder paste are thought to have a negative effect on the thermal cycle performance of the underfilled FC and FPBGA products. It is equally important to understand the role of any environment exposure from the standpoint of the fatigue behavior of the solder and the underfill materials.

6. Thermal Fatigue of the Underfilled Solder Joints

Pioneering publications [54–57] addressed materials, mechanics, and reliability of solder joints for surface mount electronics. Analytical thermal stress modeling [58–73] was applied to predict the magnitude and the distribution of thermal stresses and provide recommendations for preventing thermal stress failures in IC packages, including those with solder joints. It was shown particularly [60–63] that by employing solder joints with elevated stand-off heights, one could provide considerable stress relief in the solder material. As has been mentioned above, solder joint failures are often delaminations and not material's fatigue failures. A simple experimental technique has been suggested [65] to evaluate the propensity of solder material to delamination. The technique is based on analytical interfacial compliance models [74,75]. It was shown [64] that the stress analysis for the

actual inhomogeneous solder joint system employed in the today's FC and FPBGA designs could be based on the models initially developed for homogeneous adhesively bonded or soldered assemblies, provided, of course, that the "effective" modulus and the "effective" CTE is used, i.e., the modulus and the CTE of the composite underfill system evaluated with consideration of the moduli and CTEs of both the solder material and the encapsulant. It was shown also [66–68,76–80] that substantial thermal stress relief can be achieved by employing inhomogeneous solder systems, in which the peripheral portions of the bonding layer are characterized by substantially lower moduli and/or by lower soldering temperatures. Such an optimized system is characterized by two stress maxima: one—at the boundaries between the high-modulus mid-portion and the low-modulus peripheral portions of the solder system, and the other—at the ends of the assembly. The appropriate lengths of the peripheral portions of the soldered assembly could be selected, for the given materials properties, in such a way that the above two maxima become equal. It has been shown that if this is done, then each of these stress maxima will be considerably lower than the interfacial stress at the ends of a homogeneously bonded assembly, even if the low modulus attachment is employed for the entire homogeneously bonded assembly

A parametric study of FC solder fatigue was carried out, using FEA modeling, by Popelar [81]. He determined that harsh accelerated conditions, such as −40 °C to125 °C, could lead to significant reductions in solder joint fatigue life. Popelar investigated also the impact of the lid and different underfills on package warpage and solder ball fatigue, and indicated that "the die stresses can be directly determined by Suhir's die stress solution associated with the curvature data from the experiments".

Co-planarity of the packages with and without fillets has been addressed by the FEA combined with experiments [81,82]. It has been found particularly that "the fillet effect on the package warpage is negligible for the tested FC packages" and that "Suhir's 2-D axi-symmetrical model can be used for the approximate assessment of the global warpage".

The effectiveness of corner stacking was investigated by Ghaffarian [83] who addressed the problem of thermal cycle reliability and possible failure mechanisms in BGA assemblies with and without corner stacking. Note that an opportunity to get away with bonding such assemblies only at their peripheral portions, including corners, was indicated back in 2002 [84]. Kwak and Chung have investigated the effects of underfill on the thermal fatigue of solder joints in a novel FC design [85].

7. Warpage Related Issues

Excessive warpage is highly undesirable. First of all, it might prevent successful and reliable manufacturing of IC packages [86,87]. Warpage after curing and subsequent steps may be used sometime as a convenient, but not necessarily trustworthy, indicator of the level of the residual thermal stress. One should have in mind, however, that "low warpage" does not mean "low stress" at all. It could be just the opposite: bow-free assemblies are characterized by elevated thermal stresses [88]. In many applications, however, especially in optics, there is often a need for a warpage-free and temperature-change-independent assembly. It is possible to design one [88], provided that the induced stresses are and remain elastic during the entire time of the operation of the assembly, otherwise the bow-free condition will be compromised

Viscoelastic behavior of the underfill material can have a significant impact on the package warpage [89–91]. Application of the elevated stand-off heights of the solder joints could lead to significant relief in both the thermally induced stresses and in the warpage [92]. This is because amore compliant (in both the longitudinal and through-thickness directions) interface acts as an effective strain buffer between the two thermally mismatched adherends.

A comprehensive warpage analysis of FC and FPBGA packages subjected to thermal loading was carried out by Tsai, Chang, and Pecht [90]. The objective of their paper was to measure and simulate the warpage of FPBGA packages under thermal loading. The loading was from room temperature to as high as 260 °C. A full-field shadow moiré was used to measure out-of-plane deformations (warpages)

on the substrate and chip surfaces under thermal excursion conditions. It has been indicated that "a FEM and Suhir's die-assembly theory, together with the measured material data (elastic moduli and CTEs) for organic substrates, were used to analyze the deformations of the packages". Chiu et al. [91] employed FEM to simulate warpage of an overmolded FC surface mount package during the solder reflow process. The calculated data was compared with the experimental shadow moiré measurements and satisfactory agreement has been found between the calculated and the measured data.

8. Accelerated Testing

Accelerated tests in electronics reliability engineering include product development tests (PDT), highly accelerated life tests (HALT), qualification tests (QT), burn-in tests (BiT), and FOAT [93–95]. FOAT for Si-on-Si FC Bell Labs technology addressed in [93] included all the major components of the PDfR concept: analytical and FEA modeling, FOAT, and development of design recommendations. Accelerated tests of the underfill material and underfilled solder joints include, depending on the electronic product and application, tests aimed at evaluating the degradation of the underfill material, drop tests, bend/flex tests, temperature cycling tests, mechanical shock tests, board level drop tests, and thermal shock tests.

Ability to predict long-term material response to high humidity and high temperatures is critical. FC and FPBGA package underfills are subjected to temperature and humidity conditions during manufacturing and operation. Elevated temperature and moisture affect the behavior, performance, and aging of the polymeric underfills. Moisture can affect the cross-linking between the polymers chains in the underfill and accelerate their chemical aging. The research [46] was aimed at quantifying the effects of time, temperature, and moisture on the degradation of FC underfill. The rates of corner fillet cracking and the delamination of the underfills from the chip passivation and individual solder joints in subsequent cycling tests were used as appropriate measures of the material's degradation. Model FC assemblies were built in [46] using three different underfills: one snap cure with non-anhydride chemistry and two normal cure with anhydride chemistry.

Ibe et al. [96] conducted drop, bend, and temperature cycling tests of BGA packages with and without underfill. The drop block was dropped in their tests from a height of 1.4 m along two guided rods onto a surface covered with a layer of felt. During bend tests, the board with components facing down was placed on two supports with a span of 105 mm, and a cycling load applied to the board center produced downward displacement of 0.4 mm. Thermal cycling was carried out in the range of temperatures between −40 °C and +125 °C at 40 min per cycle. It has been concluded that "the use of a properly designed underfill" can improve the results of all the test categories. Both predictive modeling and highly-focused and highly-cost-effective FOAT are certainly a must to come up with a "properly designed underfill". In lieu of full underfilling, partial underfilling or corner/edge-bonding may be recommended for some applications. At the board level, key parameters that influence thermal cycle and mechanical reliability of underfill are edge-bond and corner bonds (see also [97]).

FPBGAs and CSPs also allow rework to replace defective devices. Thermal cycle reliability has been shown to meet many consumer application requirements. However, FPBGAs and CSPs have difficulty meeting mechanical shock and substrate flexing tests for portable electronics applications.

Drop tests could be of FOAT type [93–95], i.e., conducted until all the components fail, or half of the tested population fails, or to the maximum number of decided-upon drops (say, 250 drops). Mechanical shock and flexing requirements, and not the thermal stresses, are often the primary reasons why industry is considering underfills for FC, FPBGA, and CSP packages. It has been demonstrated that significant improvement in the mechanical performance of such packages can be achieved with both reworkable and non-reworkable underfills. Experiments, however, indicate that underfills did not significantly alter the thermal shock performance.

Here are some more or less general recommendations based on accelerated test data and considerations of the use of underfills to improve FC and FPBGA solder joint reliability:

- Use well established technologies for applying underfill;

- Prudent selection of underfill is particularly critical when employing advanced technologies with low fatigue resistance to thermal and mechanical loading;
- Use underfills with low shrinkage, low volatile condensation, and low total mass loss;
- Reduce cure-related stresses by moderating the cure conditions: step cure or lower temperature cure are advisable;
- Select underfills with CTE that closely matches CTE of adherends; this is really imperative, since the magnitude and the distribution of thermal stresses are caused, first of all, by the thermal mismatch of the adherend materials: the package (or the chip) and the substrate (PCB);
- Establish the appropriate effective modulus of elasticity for the intended underfill: low modulus might lead to lower thermal stresses, but high modulus results in higher cohesive and adhesive strength of the underfill bond, i.e., to better resistance to delamination;
- Control disruption in the induced stresses during operation or testing by selecting T_g of the underfill either well below or well above the expected operational temperature ranges; the latter choice is usually more preferable;
- Employ, wherever possible, corner and edge-bonding rather than full underfilling, unless full underfilling might be needed for better thermal performance of the interface;
- Consider FPBGAs and CSPs designs that allow rework to replace defective devices;
- Take into account that temperature cycling has been shown to meet many consumer application requirements, but still has many shortcomings and could be replaced by, say, a combination of low temperatures and random vibrations;
- Reliability engineers should always define the appropriate test matrix, using highly reliable underfill materials and their application and, when appropriate, their reworkable versions, to determine the key parameters of the test vehicles.

9. Predictive Modeling

Some studies on predictive modeling have been indicated in the above sections. Predictive modeling is the core of the recently suggested PDfR concept. This concept is based on (1) the recognition that nothing is perfect, i.e., the probability of failure is never zero, on (2) the understanding that the difference between a highly reliable and an insufficiently reliable device is "merely" in the level of their never zero probability of failure, and that the device's reliability should be quantified and, if appropriate and possible, its the never-zero probability of failure should be predicted and, if possible and appropriate, even specified to assure failure free performance of the product. The following principles are critical for the application of the PDfR concept [46,84,98–101]:

1. The best engineering product is the best compromise between the requirements for its reliability, cost-effectiveness, and time-to-market (completion);
2. The reliability of the product cannot be low, but need not be higher than necessary either: it has to be adequate for a particular device, application, and expected stressors, and should consider the consequences of the most likely and never impossible failures;
3. When adequate, predictable, and assured reliability of the product are critical, ability to quantify this probability is imperative;
4. One cannot design a product with quantified and assured reliability by just conducting HALT that does not quantify reliability, and/or just by following the existing practices, especially for new products and new applications, when best practices do not yet exist;
5. Reliability evaluations and assurances cannot be delayed until the product is made and shipped to the customer, i.e., cannot be left to the highly popular today prognostics and health monitoring (PHM) effort;
6. Design, fabrication, qualification, and other reliability related efforts should consider and be specific for the given product and its most likely anticipated application(s);

7. Highly focused and highly cost effective FOAT is the "reliable" experimental basis of the PDfR concept; it is aimed at understanding of the physics of failure, should be conducted for the most vulnerable material or the weakest structural element of the device (such as, e.g., solder), and should be geared to a physically meaningful, flexible, and trustworthy predictive model, such as, e.g., the multi-parametric BAZ equation [101].

Let us indicate several pertinent modeling-related publications that were either aimed at underfill FC materials or can be used to better understand the mechanical or rheological behavior and performance of these materials: Schwarz and Staverman [102] addressed time-dependent behavior of viscoelastic polymers; Williams, Landel, and Ferry [103] evaluated temperature dependence of relaxation mechanisms in amorphous polymers; Suhir's publications on the predictive analytical modeling of thermal stresses in bi-material adhesively bonded or soldered assemblies [75,76] have addressed the problem in question and are in good agreement with FEA predictions. These publications have attracted hundreds of citations, because the obtained simple and easy-to-use closed form solutions suggested in these publications enable one to predict the magnitude and the distribution of the stresses acting in bi-material assembly components. Two years later, an analytical predictive model was developed for a tri-material assembly [104].

Last year it was shown [18] that because of the attributes of a FC design it is this, tri-material, model that should be used to evaluate the stresses in the FC design, while the results based on the bi-material model might be misleading. The bi-material model can be still used for the evaluation of thermal stresses in adhesively bonded assemblies, when the bonding layer is thin and Young's modulus of the bonding material is significantly lower than the moduli of the adherends—the chip and its substrate. In the Bell-Labs Si-on-Si technology the FC solder joints were placed between two identical materials, and the thermal stresses were caused during temperature cycling by the CTE mismatch of the low expansion Si with high expansion solder. This situation was addressed using an analytical model [105], and the solder joint configurations were approximated by short cylinders. The solution was obtained in modified Bessel functions, assuming elastic behavior of the solder material. It was shown particularly that although the external loading on the end planes of the joint are radial shearing stresses, the maximum interfacial stresses are directed in the axial directions (these stresses are analogous to the peeling stresses in adhesively bonded or soldered assemblies) and exceed substantially the maximum shearing stresses. Both categories of stresses are the highest at the joint circumference. The predictions based on this model were in good agreement with the FEA data. In this connection, it should be emphasized that the analytical and FEA solutions are based, as a rule, on different assumptions, and if these solutions are in good agreement, then there is reason to believe that the obtained results are accurate and trustworthy.

The stress relief in solder joints due to the underfill, possible failure mechanisms, and the role and attributes of the visco-elastic behavior of the underfill material were assessed by Suryanarayana et al. [106], Gilleo and Blumel [107], Semmens and Adams [108], Guo et al. [109], Fan et al. [110], Hirohata et al. [111], Chai et al. [112], and Erickson et al. [113]. No modeling is possible, of course, if the mechanical/physical characteristics of the material are not available. Qu and Wong [114] suggested a methodology, based on the Mori-Tanaka method, for the estimation of the elastic modulus of the underfill material from the known filler content and the properties of the matrix and the fillers. Predictions of the modulus from their theory were compared with experimentally measured moduli, and excellent agreement has been observed. Xu et al. [115] employed fracture mechanics J-Integral method for the evaluation of the possible underfill delamination from the FC; Caruthers et al. [116] suggested a rigorous approach for modeling the behavior of glassy polymers used as encapsulants; Adolf et al. [117] suggested a nonlinear viscoelastic model for glassy polymers; Zhai et al. [118] analyzed possible underfill delamination in FC packages and suggested a way to minimize its possibility; Wan et al. [119,120] reviewed advances in modeling the underfill process and have indicated the critical clearance (space) between the adjacent solder bumps as an important feature of a FC design; Zhang et al. [121] carried out a 3D fracture mechanics based analysis of

underfill delamination; Adolf et al. [122] suggested a simplified potential energy clock model for the behavior of glassy polymers; Suhir et al. [123] suggested a simple formula for the evaluation of the size of the inelastic zone at the peripheral portions of a soldered assembly; Celina et al. [124] (Sandia) analyzed Zymet underfill epoxy material, and Wyatt and Chambers [125] (also Sandia) reported on a comprehensive materials analysis and modeling of underfill materials. The thermal-mechanical properties of three potential underfill candidate materials for FPBGA applications were characterized. Two of the materials are formulations developed at Sandia for underfill applications, while the third is a commercial product that utilizes a snap-cure chemistry to drastically reduce cure time. Viscoelastic models were calibrated and fitted using the property data collected for one of the Sandia formulated materials. Along with the thermal-mechanical analyses performed, a series of simple bi-material strip tests were conducted to comparatively analyze the relative effects of cure and thermal shrinkage amongst the materials under consideration. Finally, current knowledge gaps, as well as questions arising from the present study, were identified, and a path forward was suggested

Choubey et al. [126] and Paulus [127] reported on a novel underfill material—non-conductive film (NCF) underfill for highly reliable FC assembly. NCF is a potential technology that can speed up FC assembly process, as compared with, say, capillary underfill. In this approach, the underfill adhesive is applied to wafers prior to chip preparation and thermo-compression bonding. To model/simulate an NCF undergoing thermo-compression bonding, a multiphysics model has been developed that involves multiphase flow, heat transfer, and surface wetting. In the developed COMSOL Multiphysics® software, the heat transfer interface is used to track heating and cooling in the model. In addition, a two-phase flow, moving mesh interface accounts for the compression of the die into the substrate and tracks the boundary of the underfill and air.

Suhir and Ghaffarian [128] have recently published a review of the current work on predictive modeling of the dynamic response of electronic systems to impact loading. Suhir et al. [50] suggested that not only the interfacial strength of the underfilled FC design, but also the effective elastic constants of the composite bond, can be evaluated from the shear-off data. This could be done on the basis of the previously developed model considering interfacial compliance of the assembly. Suhir [19] suggested also an analytical model for thermal stresses in a typical FC design.

10. Conclusions and Future Work

The following major conclusions could be drawn from the above review:

- FC and FPBGA technologies are highly effective and highly promising, and solder joint interconnections is the bottle-neck of the today's electronics reliability. No wonder that these technologies are widely used and their attributes, with an emphasis on their short- and long-term reliability, are extensively investigated by numerous authors;
- One should have in mind that as the FC and FPBGA packages become more complex, the application of a non-appropriate underfill material or a process can easily result in more harm than good, as far as its reliability is concerned. That is why quantitative assessments of the effect of a particular FC and FPBGA technology and technique on the operational reliability of the design of interest are critical;
- An important new dimension of the today's underfill technologies, as far as the DfR is concerned, is therefore the application of the quantitative evaluations, and, especially, when appropriate and possible, since "nothing is perfect", PDfR assessments of the effect of a particular technological technique and improvements in the operational reliability of the product of importance, considering its time in operation and the most likely loading and environmental conditions;
- The best engineering product is, as is known, the best compromise between its cost-effectiveness, operational reliability, and time-to-market (completion); such a compromise (optimization) cannot be achieved if these aspects of the underfill technology are not quantified;

- Such a quantification should be based, of course, on a clear understanding of the underlying reliability physics, and therefore conducting highly-focused and highly cost-effective FOAT, geared to a relevant physically meaningful model, such as, e.g., the recently suggested BAZ constitutive equation, is imperative;
- The ability of bridging the gap between the accelerated test data and the field (operational) performance of the electronic product is certainly critical, in order to establish the right balance between the various technological techniques aimed at the improvement of the performance of the device/product of interest;
- Electronic and optical materials, devices, and systems have a lot in common, as far as their reliability is concerned, and therefore the possibility of the application of a particular electronic packaging technology in photonics engineering should be considered, whenever appropriate and possible;
- There is a necessity for using all the three research tools that a reliability engineer has at his/her disposal: experiment, FEA-based and other computer-aided simulations techniques, and, whenever possible and appropriate, also analytical modeling. This is particularly important for high-reliability applications, such as aerospace, military, long-haul communication, and medical electronics. If simulation and analytical ("mathematical") data are in good agreement then there is good reason to believe that the obtained results are both accurate and trustworthy. In this connection it should be emphasized that, in connection with a modeling effort, there is an obvious incentive for the development of a simple and practically useful ways to evaluate the mechanical/physical properties) of the composite solder-underfill layer.
- There is an incentive for the development a physically substantiated, strain-energy-based modeling technique for the evaluation of the life-time of an underfilled solder joints subjected to inelastic strains. This could be done particularly based on the idea of the (now classical) Pete Hall's hysteresis concept [55–57].

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References

1. Suhir, E.; Segelken, J.M. Mechanical behavior of flip-chip encapsulants. *J. Electr. Packag.* **1990**, *112*, 327–332. [CrossRef]
2. Tsukada, Y. Surface laminar circuit and flip-chip attach packaging. In Proceedings of the 42nd Electronic Components & Technology Conference, San Diego, CA, USA, 18–20 May 1992.
3. Suryanarayana, D.; Wu, T.Y.; Varcoe, J.A. Encapsulants used in flip-chip packages. In Proceedings of the 43rd Electronic Components and Technology Conference (ECTC'93), Orlando, FL, USA, 1–4 June 1993.
4. Lau, J.H. *Flip Chip Technologies*; McGraw-Hill: New York, NY, USA, 1995.
5. Lau, J.H.; Chang, C. How to select underfill materials for solder bumped flip chips on low cost substrates? *Int. J. Microcircuits Electron. Packag.* **1999**, *22*, 20–28.
6. Wong, C.P.; Lou, S.; Zhang, Z. Flip the chip. *Science* **2000**, *290*, 2269–2270. [CrossRef] [PubMed]
7. Nazuka, K. Underfill agent for BGA/CSP mounting. In *Three Bond Technical News*; Three Bond International: West Chester, OH, USA, 2000.
8. Braun, T.; Becker, T.F.; Koch, M.; Bader, V.; Aschenbrenner, R.; Reichl, H. Flip chip molding—Recent progress in flip chip encapsulation. In Proceedings of the 8th International Advanced Packaging Materials Symposium, Stone Mountain, GA, USA, 3–6 March 2002.
9. Chen, T.; Wang, J.; Lu, D. Emerging challenges of underfill for flip chip applications. In Proceedings of the 54th Electronic Components and Technology Conference, Las Vegas, NV, USA, 4 June 2004.

10. Lau, J.; Powers, L.; Baker, J.; Rice, D.; Shaw, B. Solder joint reliability of fine pitch surface mount technology assemblies. In Proceedings of the Seventh IEEE/CHMT International Electronic Manufacturing Technology Symposium, San Francisco, CA, USA, 25–27 September 1989.
11. Brenner, W. *Use Underfill Encapsulants to Enhance Flip-Chip Assembly Reliability*; Informa PLC: London, UK, 2012.
12. Johnson, R.W.; Capote, M.A.; Chu, S.; Zhou, L.; Gao, B. Reflow-curable polymer fluxes for flip-chip encapsulation. In Proceedings of the International Conference on Multichip Modules and High Density Packaging, Denver, CO, USA, 17 April 1998.
13. Weber, P.O. Chip Package with Molded Underfill. U.S. Patent 6,038,136, March 2000.
14. Peng, H.; Johnson, R.W.; Flowers, G.; Ricketts, A.; Yeager, E.; Konarski, M. Underfilling Fine Pitch BGAs. *IEEE Trans. Electron. Packag. Manuf.* **2001**, *24*, 293–299. [CrossRef]
15. Zhang, Z.; Wong, C.P. Novel filled no-flow underfill materials and process. In Proceedings of the 8th International Advanced Packaging Materials Symposium, Stone Mountain, GA, USA, 3–6 March 2002.
16. Clementi, J.; McCreary, J.; Niu, T.M.; Palomaki, J.; Varcoe, J.; Hill, G. Flip chip encapsulation on ceramic substrates. In Proceedings of the IEEE 43rd Electronic Components and Technology Conference, Orlando, FL, USA, 1–4 June 1993.
17. Ghaffarian, R. *BOK–Underfill Optimization for FPGA Package/Assembly*; Jet Propulsion Laboratory: Pasadena, CA, USA, 2012.
18. Suhir, E. Flip-chip assembly: Is a bi-material model acceptable? *J. Mater. Sci.* **2017**, *28*, 15775–15781. [CrossRef]
19. Suhir, E. Analytical thermal stress model for a typical flip-chip package design. *J. Mater. Sci.* **2018**, *29*, 2676–2688. [CrossRef]
20. Tsai, M.Y.; Lin, Y.C.; Huang, C.Y.; Wu, J.D. Thermal deformations and stresses of flip-chip BGA packages with low- and high-T_g underfills. *IEEE Trans. Electron. Packag. Manuf.* **2005**, *28*, 328–337. [CrossRef]
21. Kim, Y.K.; Park, S.; Choi, J. Warpage mechanism analyses of strip panel type PBGA chip packaging. *Microelectron. Reliab.* **2010**, *50*, 398–406. [CrossRef]
22. Schwiebert, M.K.; Leong, W.H. Underfill flow as viscous flow between parallel plates driven by capillary action. *IEEE CPMT Trans. Part C* **1996**, *19*, 133–137. [CrossRef]
23. Han, S.; Wang, K.K. Analysis of the flow of encapsulant during underfill encapsulation of flip-chips. *IEEE CPMT Trans. Part B* **1997**, *20*, 424–433.
24. Young, W.B.; Yang, W.L. Underfill of flip-chip: The effect of contact angle and solder bump arrangement. *IEEE Trans. Adv. Packag.* **2006**, *29*, 647–653. [CrossRef]
25. Wan, J.W.; Zhang, W.J.; Bergstrom, D.J. Numerical modeling for the underfill flow in flip-chip packaging. *IEEE Trans. Compon. Packag. Technol.* **2009**, *32*, 227–234. [CrossRef]
26. Yao, X.J.; Fang, J.J.; Zhang, W. A further study on the analytical model for the permeability in flip-chip packaging. *J. Electron. Packag.* **2018**, *140*, 011001. [CrossRef]
27. Yao, X.J.; Wang, Z.D.; Zhang, W.J.; Zhou, X.Y. A new model for permeability of porous medium in the case of flip-chip packaging. *IEEE Trans. Compon. Packag. Manuf. Technol.* **2014**, *4*, 1265–1275.
28. Yao, X.J.; Wang, Z.D.; Zhang, W.J. A new analysis of the capillary driving pressure for underfill flow in flip-chip packaging. *IEEE Trans. Compon. Packag. Manuf. Technol.* **2014**, *4*, 1534–1544.
29. Cheng, S.; Huang, C.M.; Pecht, M. A review of lead-free solders for electronics applications. *Microelectron. Reliab.* **2017**, *75*, 77–95. [CrossRef]
30. Mahalingam, S.; Goray, K.; Joshi, A. Design of underfill materials for lead free flip chip application. In Proceedings of the 9th Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems, Las Vegas, NV, USA, 1–4 June 2004.
31. Ji, Q.; Zhao, R.; Huang, Q.; Zhu, P. Underfills for lead-free and low-k flip-chip packages. In Proceedings of the 59th Electronic Components and Technology Conference, San Diego, CA, USA, 26–29 May 2009.
32. Shi, B.H.; Ueda, T. Mitigation of thermal fatigue failure in fully underfilled lead-free array-based package assemblies using partial underfills. In Proceedings of the 13th Electronics Packaging Technology Conference, Singapore, 7–9 December 2011.
33. Chan, Y.; Song, F.; Lee, S.W. Investigation on Lead-free Solder Joint Reliability of Edge-Bonded CBGA under Temperature Cycling. In Proceedings of the 12th International Conference on Electronic Packaging Technology and High Density Packaging, Shanghai, China, 8–11 August 2011.

34. Shamash, M.B. *Development of Highly Reliable Soldered Joints for Printed Circuit Boards*; NASA: Washington, DC, USA, 1968.
35. Lall, P.; Panchagade, D.R.; Liu, Y.; Johnson, R.W.; Suhling, J.C. Models for Reliability Prediction of Fine-Pitch BGAs and CSPs in Shock and Drop-Impact. *IEEE Trans. Compon. Packag. Technol.* **2006**, *29*, 464–474. [CrossRef]
36. Bressers, H.; Beris, P.; Caers, J.; Wondergermi, J. Influence of chemistry and processing of flip-chip underfills on reliability. In Proceedings of the 2nd International Conference on Adhesive Joining and Coating Technology in Electronic Manufacturing, Stockgolm, Sweden, 2–6 June 1996.
37. Nysaether, J.B.; Lundstrom, P.; Liu, J. Measurements of solder bumps lifetime as a function of the underfill material properties. In Proceedings of the First IEEE International Symposium on Polymeric Electronics Packaging, PEP '97, Norrkoping, Sweden, 30 October 1997.
38. Young, S.J. Under filling of BGA and CSP for harsh environment deployment. In Proceedings of the International Conference on High Density Packaging and MCM, Denver, CO, USA, 7–9 April 1999.
39. Ghaffarian, R. Area array technology for high reliability applications. In *Micro-and Opto-Electronic Materials and Structures: Physics, Mechanics, Design, Reliability, Packaging*; Suhir, E., Ed.; Springer: Berlin, German, 2006; Chapter 16.
40. Mercado, L.; Sarihan, V. Evaluation of the die attach cracking in flip-chip PBGA packages. *IEEE Trans. Compon. Packag. Technol.* **2003**, *26*, 719–723. [CrossRef]
41. Dudek, R.; Schubert, A.; Michel, B. Analysis of flip chip attach reliability. In Proceedings of the 4th International Conference on Adhesive Joining and Coating Technology in Electronics Manufacturing, Espoo, Finland, 18–21 June 2000.
42. Ghaffarian, R. BGA assembly reliability. In *Area Array Packaging Handbook*; Gilleo, K., Ed.; McGraw-Hill: New York, NY, USA, 2004; Chapter 20.
43. Tian, G.; Liu, Y.; Johnson, W.; Lall, P.; Palmer, M.; Islam, M.; Crane, L.; Yeager, E.; Konarski, M.; Torres, A. Corner bonding of CSPs: Processing and reliability. *IEEE Trans. Electron. Packag. Manuf.* **2005**, *28*, 231–240. [CrossRef]
44. Ghaffarian, R. CCGA Packages for Space Applications. *Microelectron. Reliabil.* **2006**, *46*, 2006–2024. [CrossRef]
45. Ghaffarian, R. Reliability of column/board CCGA attachment. In Proceedings of the 13th InterSociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems, San Diego, CA, USA, 30 May–1 June 2012.
46. Suhir, E. *Failure-Oriented-Accelerated-Testing (FOAT) and Its Role in Making a Viable IC Package into a Reliable Product*; Circuits Assembly: Smyrna, GA, USA, 2013.
47. Suhir, E.; Bechou, L.; Ghaffarian, R.; Nicolics, J. Column-Grid-Array (CGA) technology could lead to a highly reliable package design. In Proceedings of the IEEE Aerospace Conference, Big Sky, MT, USA, 5–12 March 2016.
48. Suhir, E. What could and should be done differently: Failure-Oriented-Accelerated-Testing (FOAT) and its role in making an aerospace electronics device into a product. *J. Mater. Sci.* **2018**, *29*, 2939–2948. [CrossRef]
49. Ghaffarian, R. Assembly and reliability of 1704 I/O FCBGA and FPBGA. In Proceedings of the IPC/APEX, San Diego, CA, USA, 28 February–1 March 2012.
50. Suhir, E.; Ghaffarian, R.; Yi, S.; Nicolics, J. Assessed interfacial strength and elastic moduli of the bonding material from shear-off test data. *J. Mater. Sci.* **2017**, *28*, 6794–6799. [CrossRef]
51. Shi, S.H.; Yao, Q.; Qu, J.; Wong, C.P. Study on the correlation of flip-chip reliability with mechanical properties of no-flow underfill materials. In Proceedings of the 6th International Symposium on Advanced Packaging Materials Processes, Properties and Interfaces, Braselton, GA, USA, 6–8 August 2000.
52. Hannan, N.; Viswanadham, P.; Crane, L.; Yaeger, E.; Torres, A.; Johnson, R.W. Reworkable underfill materials for improved manufacturability and reliability of CSP assemblies. In Proceedings of the APEX Conference, San Diego, CA, USA, 14–18 January 2001.
53. Wang, T.; Chew, T.H.; Chew, Y.X.; Foo, L. Reliability studies of flip-chip package with reflowable underfill. In Proceedings of the Pan Pacific Microelectronics Symposium, Kauai, Hawaii, HI, USA, 13–16 February 2001.
54. Liu, J.; Johnson, R.W.; Yaeger, E.; Konarski, M.; Crane, L. CSP underfill, processing and reliability. In Proceedings of the APEX Technical Conference, San Jose, CA, USA, 22–24 January 2002.
55. Loh, K.; Ibe, I. *Preventing Voids in CSP and BGA Underfill Encapsulants*; Circuit Assembly magazine: Canton, GA, USA, 2004.

56. Hall, P.M.; Dudderar, T.D.; Argyle, J.F. Thermal deformations observed in leadless ceramic chip carriers surface mounted to printed wiring boards. *IEEE Trans. Compon. Hybrids Manuf. Technol.* **1983**, *6*, 544–552. [CrossRef]
57. Hall, P.M. Forces, moments and displacements during thermal chamber cycling of leadless ceramic chip carriers soldered to printed boards. *IEEE Trans. Compon. Hybrids Manuf. Technol.* **1984**, *7*, 314–327. [CrossRef]
58. Sherry, W.M.; Hall, P.M. Materials, structures and mechanics of solder joints for surface mount microelectronics technology. In Proceedings of the Conference on Interconnection Technology in Electronics, Fellbach, Germany, 18–20 February 1986.
59. Suhir, E. Thermal stress failures in microelectronics and photonics: Prediction and prevention, future circuits international. *J. Therm. Stress.* **2013**, *36*, 537–563. [CrossRef]
60. Suhir, E. Thermal stress failures in electronics and photonics: Physics, modeling, Prevention. *J. Therm. Stress.* **2013**, *36*, 537–563. [CrossRef]
61. Suhir, E. Predicted stresses in a Ball-Grid-Array (BGA)/Column-Grid-Array (CGA) assembly with a low modulus solder at its ends. *J. Mater. Sci.* **2015**, *26*, 9680–9688. [CrossRef]
62. Suhir, E. Analysis of a short beam with application to solder joints: Could larger stand-off heights relieve stress? *Eur. J. Appl. Phys.* **2015**, *71*. [CrossRef]
63. Suhir, E.; Ghaffarian, R.; Nicolics, J. Could application of Column-Grid-Array technology result in inelastic-strain-free state-of-stress in solder material? *J. Mater. Sci.* **2015**, *26*, 10062–10067. [CrossRef]
64. Suhir, E.; Ghaffarian, R.; Nicolics, J. Predicted stresses in Ball-Grid-Array (BGA) and Column-Grid-Array (CGA) interconnections in a mirror-like package design. *J. Mater. Sci.* **2016**, *27*, 2430–2441. [CrossRef]
65. Suhir, E.; Ghaffarian, R.; Nicolics, J. Could thermal stresses in an inhomogeneous BGA/CGA system be predicted using a model for a homogeneously bonded assembly? *J. Mater. Sci.* **2016**, *27*, 570–579.
66. Suhir, E. Bi-material assembly subjected to thermal stress: Propensity to delamination assessed using interfacial compliance model. *J. Mater. Sci.* **2016**, *27*, 6779–6785. [CrossRef]
67. Suhir, E. Expected stress relief in a bi-material inhomogeneously bonded assembly with a low-modulus-and/or-low-fabrication-temperature bonding material at the ends. *J. Mater. Sci.* **2016**, *27*, 5563–5574. [CrossRef]
68. Suhir, E. Bi-material assembly with a low-modulus-and/or-low-fabrication-temperature bonding material at its ends: Optimized stress relief. *J. Mater. Sci.* **2016**, *27*, 4816–4825. [CrossRef]
69. Suhir, E.; Ghaffarian, R. Predicted stresses in a Ball-Grid-Array (BGA)/Column-Grid-Array (CGA) assembly with epoxy adhesive at its ends. *J. Mater. Sci.* **2016**, *27*, 4399–4409. [CrossRef]
70. Suhir, E. *Avoiding Low-Cycle Fatigue in Solder Material Using Inhomogeneous Column-Grid-Array (CGA) Design*; Chip Scale Review: Campbell, CA, USA, 2016.
71. Suhir, E. *Relieving Stress in Flip-Chip Solder Joints*; Chip Scale Review: Campbell, CA, USA, 2017.
72. Suhir, E.; Yi, S.; Ghaffarian, R. How many peripheral solder joints in a surface mounted design experience inelastic strains? *J. Electron. Mater.* **2017**, *46*, 1747–1753. [CrossRef]
73. Suhir, E.; Ghaffarian, R. Solder material experiencing low temperature inelastic thermal stress and random vibration loading: Predicted remaining useful lifetime. *J. Mater. Sci.* **2017**, *28*, 3585–3597.
74. Suhir, E.; Ghaffarian, R. Probabilistic Palmgren-Miner rule with application to solder materials experiencing elastic deformations. *J. Mater. Sci.* **2017**, *28*, 2680–2685. [CrossRef]
75. Suhir, E. Stresses in bi-metal thermostats. *J. Appl. Mech.* **1986**, *53*, 657–660. [CrossRef]
76. Suhir, E. Interfacial stresses in bi-metal thermostats. *J. Appl. Mech.* **1989**, *53*, 595–600. [CrossRef]
77. Suhir, E. Thermal stress in an adhesively bonded joint with a low modulus adhesive layer at the ends. *J. Appl. Phys.* **2003**, *55*, 3657–3661. [CrossRef]
78. Suhir, E. Interfacial thermal stresses in a bi-material assembly with a low-yield-stress bonding layer. *Model. Simul. Mater. Sci. Eng.* **2006**, *14*, 1421. [CrossRef]
79. Suhir, E. Predictive Analytical Thermal Stress Modeling in Electronics and Photonics. *Appl. Mech. Rev.* **2009**, *62*, 040801. [CrossRef]
80. Suhir, E. On a paradoxical situation related to bonded joints: Could stiffer mid-portions of a compliant attachment result in lower thermal stress? *J. Solid Mech. Mater. Eng.* **2009**, *3*, 990–997. [CrossRef]
81. Popelar, S.F. A parametric study of flip chip reliability based on solder fatigue modeling. In Proceedings of the Twenty First IEEE/CPMT International Electronics Manufacturing Technology Symposium, Austin, TX, USA, 13–15 October 1997.

82. Shi, X.Q.; Pang, H.L.J.; Zhou, W.; Wang, Z.P. Low cycle fatigue analysis of temperature and frequency effects in eutectic solder alloy. *Int. J. Fatigue* **2000**, *22*, 217–228. [CrossRef]
83. Ghaffarian, R. Thermal cycle reliability and failure mechanisms of CCGA and PBGA assemblies with and without corner staking. *IEEE Trans. Compon. Packag. Technol.* **2008**, *31*, 285–296. [CrossRef]
84. Suhir, E. Bi-Material Assembly Adhesively Bonded at the Ends and Fabrication Method. U.S. Patent 6,460,753, 8 October 2002.
85. Kwak, J.B.; Chung, S. The effects of underfill on the thermal fatigue reliability of solder joints in newly developed flip chip on module. In Proceedings of the 13th InterSociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems, San Diego, CA, USA, 30 May–1 June 2012.
86. Suhir, E. Predicted bow of plastic packages of integrated circuit devices. In *Thermal Stress and Strain in Microelectronic Packaging*; Lau, J.H., Ed.; Van Nostrand Reinhold: New York, NY, USA, 1993.
87. *High Temperature Package Warpage Measurement Methodology*; JEDEC: Arlington, VA, USA, 2009.
88. Suhir, E. Device and Method of Controlling the Bowing of a Soldered or Adhesively Bonded Assembly. U.S. Patent 6,239,382, 29 May 2001.
89. Lin, W.; Lee, M.W. PoP/CSP warpage evaluation and viscoelastic modeling. In Proceedings of the 58th Electronic Components and Technology Conference, Lake Buena Vista, FL, USA, 27–30 May 2008.
90. Tsai, M.Y.; Chang, H.Y.; Pecht, M. Warpage analysis of flip-chip PBGA packages subject to thermal loading. *IEEE Trans. Dev. Mater. Reliabil.* **2009**, *9*, 419–424. [CrossRef]
91. Chiu, T.C.; Huang, D.Y.; Lee, B.S.; Chen, D.L.; Yang, P.F.; Kao, C.L. Development of a consistent multiaxial viscoelastic model for package warpage simulation. In Proceedings of the IEEE 65th Electronic Components and Technology Conference, San Diego, CA, USA, 26–29 May 2015.
92. Suhir, E. Solder joints in surface mounted IC assemblies: Relief in stress and warpage owing to the application of elevated stand-off heights. *J. Mod. Appl. Phys.* **2018**, *2*, 4–9.
93. Suhir, E. Mechanical behavior and reliability of solder joint interconnections in thermally matched assemblies. In Proceedings of the 42nd Electronic Components & Technology Conference, San Diego, CA, USA, 18–20 May 1992.
94. Suhir, E. Accelerated Life Testing (ALT) in microelectronics and photonics: Its role, attributes, challenges, pitfalls, and interaction with qualification tests. *ASME J. Electr. Packag.* **2002**, *124*, 281–291. [CrossRef]
95. Chaware, R. Accelerated testing of flip-chip underfills and the effect of moisture and temperature on the aging of underfills. In Proceedings of the SMTA International Conference, Orlando, FL, USA 8–10 December 2004.
96. Ibe, E.; Loh, K.; Luan, J.-E.; Tee, T.Y. Underfill effects on BGA drop, bend and thermal cycle tests. *Adv. Packag.* **2005**, *14*, 28–30.
97. Suhir, E. *Probabilistic Design for Reliability*; Chip Scale Review: Campbell, CA, USA, 2010.
98. Suhir, E.; Yi, S. Probabilistic design for reliability of medical electronic devices: Role, significance, attributes, challenges. In Proceedings of the IEEE Medical Electronic Symposium, Portland, OR, USA, 14–15 September 2016.
99. Zhurkov, S.N. Kinetic concept of the strength of solids. *Int. J. Fract. Mech.* **1984**, *26*, 295–307. [CrossRef]
100. Suhir, E.; Kang, S. Boltzmann-Arrhenius-Zhurkov (BAZ) model in physics-of-materials problems. *Mod. Phys. Lett. B* **2013**, *27*. [CrossRef]
101. Suhir, E.; Mahajan, R.; Lucero, A.; Bechou, L. Probabilistic design-for-reliability concept and novel approach to qualification testing of aerospace electronic products. In Proceedings of the IEEE Aerospace Conference, Big Sky, MT, USA, 3–10 March 2012.
102. Schwarz, F.; Staverman, A.J. Time-temperature dependence of linear viscoelastic behavior. *J. Appl. Mech.* **1952**, *23*, 838. [CrossRef]
103. Williams, M.L.; Landel, R.F.; Ferry, J.D. The temperature dependence of relaxation mechanisms in amorphous polymers and other glass-forming liquids. *J. Am. Chem. Soc.* **1955**, *77*, 3701–3707. [CrossRef]
104. Suhir, E. Analysis of interfacial thermal stresses in a trimaterial assembly. *J. Appl. Phys.* **2001**, *89*, 3685. [CrossRef]
105. Suhir, E. Axisymmetric elastic deformations of a finite circular cylinder with application to low temperature strains and stresses in solder joints. *J. Appl. Mech.* **1989**, *56*, 328–333. [CrossRef]
106. Suryanarayana, D.; Hsiao, R.; Gall, T.P.; McCreary, J.M. Enhancement of flip-chip fatigue life by encapsulation. *IEEE Trans. Compon. Hybrids Manuf. Technol.* **1991**, *14*, 218–223. [CrossRef]

107. Gilleo, K.; Blumel, D. New generation underfills power the 2nd flip chip revolution. In Proceedings of the Pan Pacific Microelectronics Symposium, Surface Mount Technology Association, Edina, MN, USA, 10–13 February 1998.
108. Semmens, J.E.; Adams, T. Flip chip package failure mechanism. *Solid State Technol.* **1998**, *41*, 59–64.
109. Guo, Y.; Lehmann, G.L.; Driscoll, T.; Cotts, E.J. A model of the underfill flow process: particle distribution effects. In Proceedings of the 49th Electronic Components and Technology Conference, San Diego, CA, USA, 1–4 June 1999.
110. Fan, X.J.; Wang, H.B.; Lim, T.B. Investigation of the underfill delamination and cracking in flip-chip modules under temperature cyclic loading. *IEEE Trans. Compon. Packag. Technol.* **2001**, *24*, 84–91. [CrossRef]
111. Hirohata, K.; Kawamura, N.; Mukai, M.; Kawakami, T.; Aoki, H.; Takahashi, K. Mechanical fatigue test method for chip/underfill delamination in flip-chip packages. *IEEE Trans. Electron. Packag. Manuf.* **2002**, *25*, 217–222. [CrossRef]
112. Chai, K.; Wu, E.; Hsieh, R.; Tong, J.Y. Challenge of flip chip encapsulation technologies. In Proceedings of the SPIE, Denver, CO, USA, 15 July 2002.
113. Erickson, D.; Li, D.; Park, C.B. Numerical simulations of capillary-driven flows in non-uniform cross-sectional capillaries. *J. Colloid Interface Sci.* **2002**, *250*, 422–430. [CrossRef] [PubMed]
114. Qu, J.; Wong, C.P. Effective elastic modulus of underfill material for flip-chip applications. *IEEE Trans. Compon. Packag. Technol.* **2002**, *25*, 53–55.
115. Xu, B.; Cai, X.; Huang, W.; Cheng, Z. Research of underfill delamination in flip chip by the J-integral method. *ASME J. Electron. Packag.* **2004**, *126*, 94–99. [CrossRef]
116. Caruthers, J.M.; Adolf, D.B.; Chambers, R.S.; Shrikhande, P.A. A thermodynamically consistent, nonlinear viscoelastic approach for modeling glassy polymers. *Polymer* **2004**, *456*, 4577–4597. [CrossRef]
117. Adolf, D.B.; Chambers, R.S.; Caruthers, J.M. Extensive validation of a thermodynamically consistent: Nonlinear viscoelastic model for glassy polymers. *Polymer* **2004**, *45*, 4599–4621. [CrossRef]
118. Zhai, C.J.; Sidharth; Blish, R.C.; Master, R.N. Investigation and minimization of underfill delamination in flip chip packages. *IEEE Trans. Dev. Mater. Reliabil.* **2004**, *4*, 86–91. [CrossRef]
119. Wan, J.W.; Zhang, W.J.; Bergstrom, D.J. An analytical model for predicting the underfill flow characteristics in flip-chip encapsulation. *IEEE Trans. Adv. Packag.* **2005**, *28*, 481–487. [CrossRef]
120. Wan, J.W.; Zhang, W.J.; Bergstrom, D.J. Recent advances in modeling the underfill process in flip-chip packaging. *Microelectron. J.* **2007**, *38*, 67–75. [CrossRef]
121. Zhang, Z.; Zhai, C.J.; Master, R.N. *3D Fracture Mechanics Analysis of Underfill Delamination for FC Packages*; I-THERM: Waltham, MA, USA, 2008.
122. Adolf, D.B.; Chambers, R.S.; Neidigk, M.A. A simplified potential energy clock model for glassy polymers. *Polymer* **2009**, *50*, 4257–4269. [CrossRef]
123. Suhir, E.; Bechou, L.; Levrier, B. Predicted size of an inelastic zone in a ball-grid-array assembly. *J. Appl. Mech.* **2013**, *80*, 021007. [CrossRef]
124. Celina, M.C.; Giron, N.H.; Alam, T.M.; Mowry, C.D.; Pimentel, A.S. *Analysis and Characterization of Zymet Underfill Epoxy Material*; SAND2015-4686; Sandia National Laboratories: Albuquerque, NM, USA, 2015.
125. Wyatt, N.B.; Chambers, R.S. Materials analysis and modeling of underfill materials. In *SANDIA Report*; SAND2015-7070; Sandia National Laboratories: Albuquerque, NW, USA, 2015.
126. Choubey, A.; Anzures, E.; Fleming, D.; Dhoble, A.; Herong, L.; Barr, R.; Calvert, J.; Oh, J.S. *Non-Conductive Film (NCF) Underfill for Flip Chip Assembly and High Reliability*; Dow Chemical: Midland, MI, USA, 2014.
127. Paulus, B. *Simulating the Thermo-Compression Bonding of an Underfill Adhesive*; Veryst Engineering LLC: Needham Heights, MA, USA, 2017.
128. Suhir, E.; Ghaffarian, R. Predictive modeling of the dynamic response of electronic systems to impact loading: Review. In *Zeitschrift fur AngewandteMathematik und Mechanik (ZAMM)*; Wiley: Hoboken, NJ, USA, 2017.