

Article

# Ultra-Low-Voltage Inverter-Based Operational Transconductance Amplifiers with Voltage Gain Enhancement by Improved Composite Transistors

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**Abstract:** This paper proposes topological enhancements to increase voltage gain of ultra-low-voltage (ULV) inverter-based OTAs. The two proposed improvements rely on adoption of composite transistors and forward-body-biasing. The impact of the proposed techniques on performance figures is demonstrated through simulations of two OTAs. The first OTA achieves a 39 dB voltage gain, with a power consumption of 600 pW and an active area of 447  $\mu\text{m}^2$ . The latter allies the forward-body-bias approach with the benefit of the independently biased composite transistors. By combining both solutions, voltage gain is raised to 51 dB, consuming less power (500 pW) at the cost of an increased area of 727  $\mu\text{m}^2$ . The validation has been performed through post-layout simulations with the Cadence Analog Design Environment and the TSMC 180 nm design kit, with the supply voltage ranging from 0.3 V to 0.6 V.

**Keywords:** operational transconductance amplifier (OTA); inverter-based OTA; push-pull based OTA; improved forward-body-bias; composite transistors; ultra-low-voltage (ULV); ultra-low-power (ULP)

## 1. Introduction

The increasing demand for electronic devices supplied by energy-harvesting power sources bring about the need for integrated circuits (ICs) able to properly operate at ultra-low-voltage supply and with ultra-low-power consumption [1–6].

In this context, the Operational Transconductance Amplifiers (OTAs) are the building blocks of any front-end and signal processing chain that are traditionally unsuitable to operate at very low voltage fulfilling performance like a rail-to-rail input/output voltage swing and high transconductance-gain that are also independent by process, supply voltage, and temperature variations [7]. To face such challenges, several OTAs have been proposed targeting ultra-low-voltage (ULV) supply and Ultra-Low-Power consumption. The input and output voltage swings of such OTAs are severely limited because of their conventional gate-driven differential pair (DP). On the other hand, bulk-driven input DPs OTAs [8–11] exhibit increased input range linearity at the cost of bandwidth, power efficiency, and finite DC input impedance [12].

As an alternative, push-pull inverter-based OTA topologies [13,14] and their respective ULV variations [15,16] have been proposed, including push-pull based bulk-driven OTAs [17,18], offering a higher power-efficiency, linearity, and voltage gain with low output voltage swing degradation.

In this framework, the composite transistors [19], such as rectangular arrays [20] and trapezoidal arrays [21], can be used to increase the voltage gain of inverter-based OTAs at the cost of area.

Moreover, improved composite transistors with forward-body-bias offer additional features to increase the voltage gain [22].

This paper describes how inverter-based OTAs can benefit from forward-body-biasing to implement common-mode input voltage rejection [21] in single-ended OTAs, balance the charge mobility asymmetry of PMOS and NMOS transistors with parallel and series transistor arrays [19] to save area, and adapt improved composite transistors [22] to enhance voltage-gain.

In Section 2, an elementary composite transistor made of two N-type MOS is considered and how the gain can benefit from an independent bias of their bulk terminals is discussed. Then, in Section 3, two inverter-based OTAs with common-mode rejection forward-body-bias circuits are described. The first is made of with parallel PMOS transistors arrays and NMOS series arrays for the pull-up and the pull-down networks, targeting the lowest area for the described approach. The second is a version of the first OTA which uses adapted improved composite transistors to achieve a greater voltage-gain. In Section 4, the characteristics of such two OTAs are verified and compared through post-layout simulations with the 180 nm technology process. Finally, in Section 5, conclusions are drawn.

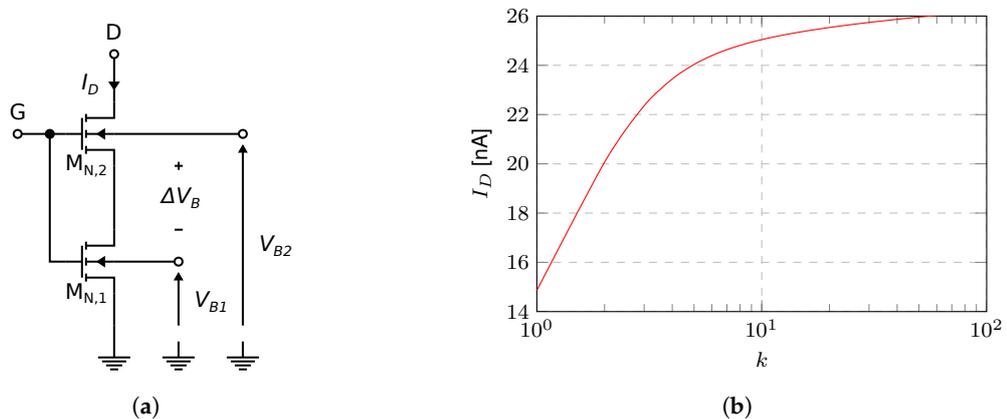
## 2. Composite Transistor with an Improved Forward-Body-Bias

Implementing inverter-based OTAs with composite transistors allows designers to exploit the gain-area trade-off. Figure 1a represents an elementary composite N-type transistor  $M_N$  made of two series transistors  $M_{N,2}$  and  $M_{N,1}$ . Considering that  $M_{N,1}$  and  $M_{N,2}$  have the same length, the equivalent transistor aspect ratio  $S_{eq}$  is defined by (1) [19]:

$$S_{eq} = \frac{W_{eq}}{L_{eq}} = \frac{S_{N,1} \cdot S_{N,2}}{S_{N,1} + S_{N,2}} = \frac{k}{k + 1} \cdot S_{N,1} \tag{1}$$

where

$$k = \frac{S_{N,2}}{S_{N,1}} = \frac{W_{N,2}}{W_{N,1}} \tag{2}$$



**Figure 1.** N-MOS composite transistor: (a) schematic; (b) drain current  $I_D$  versus the aspect ratio  $k$  variation of the transistors  $M_{N,2}$  and  $M_{N,1}$  for  $V_G = V_D = V_{B1} = V_{B2} = 0.25$  V ( $\Delta V_B = V_{B2} - V_{B1} = 0$ ).

Such use of composite transistors improves voltage gain by increasing the  $k$  factor [21], which is the ratio of the transistors  $M_{N,2}$  and  $M_{N,1}$  aspect ratios  $S_{N,2}$  and  $S_{N,1}$ . The equivalent transistor channel length  $L_{eq}$  and the Early Voltage  $V_A$  increase proportionally to  $k$ ; however, the equivalent transistor total area and input capacitance also increase accordingly.

By using the UICM (Unified Current Control Model) all-region transistor model [23] approximation to the weak inversion transistor operation, the transistor drain current  $I_D$  can be calculated as follows:

$$I_D \approx 2 \cdot I_S \cdot \left( e^{\frac{V_{GB}-V_T-nV_{SB}+1}{n\phi_t}} - e^{\frac{V_{GB}-V_T-nV_{DB}+1}{n\phi_t}} \right) \tag{3}$$

$$I_S = I_{SH} \cdot S = \mu C'_{ox} n \frac{\phi_t^2}{2} \cdot \left( \frac{W}{L} \right) \tag{4}$$

where  $V_{GB}$ ,  $V_{SB}$ , and  $V_{DB}$  are respectively the the gate-to-bulk, source-to-bulk, and drain-to-bulk voltages,  $V_T$  is the threshold voltage,  $n$  is the slope factor,  $\phi_t$  is the thermal voltage,  $I_S$  is the normalization current,  $I_{SH}$  is the sheet normalization current,  $S$  is the transistor aspect ratio,  $\mu$  is the charge mobility, and  $C'_{ox}$  is the gate oxide capacitance per area.

Considering that  $I_D = I_{DN,1} = I_{DN,2}$  and  $V_X = V_{DN,1} = V_{SN,2}$ , that  $M_{N,1}$  operates in the linear region,  $M_{N,2}$  operates in the saturation region, and both transistors operate in weak inversion, the composite transistor drain current  $I_D$  can be calculated as shown in (5) and (6):

$$I_D \approx 2 \cdot I_{SH} \cdot S_{N,1} \cdot e^{\frac{V_G+(n-1)V_{B1}-V_T+1}{n\phi_t}} \cdot \left( 1 - e^{-\frac{V_X}{\phi_t}} \right) \tag{5}$$

$$\approx 2 \cdot I_{SH} \cdot S_{N,2} \cdot e^{\frac{(n-1)\Delta V_B}{n\phi_t}} \cdot e^{\frac{V_G+(n-1)V_{B1}-V_T+1}{n\phi_t}} \cdot e^{-\frac{V_X}{\phi_t}}$$

$$V_X \approx \phi_t \cdot \ln \left[ \frac{S_{N,1} + S_{N,2} \cdot e^{\frac{(n-1)\Delta V_B}{n\phi_t}}}{S_{N,1}} \right] \tag{6}$$

By fixing the size of  $M_{N,1}$ , the drain current  $I_D$  can be changed by varying the width of the transistor  $M_{N,2}$ , and assuming the body-bias of the of the two series transistors  $M_{N,1}$  and  $M_{N,2}$  in Figure 1a tied at the same voltage, so that  $V_G = V_D = V_{B1} = V_{B2} = 0.25$  V, the drain current  $I_D$  of the composite transistor is proportional to the equivalent transistor aspect ratio, as described in (7) and shown in Figure 1b:

$$I_D \approx 2 \cdot I_{SH} \cdot S_{eq} \cdot e^{\frac{V_G+(n-1)V_{B1}-V_T+1}{n\phi_t}} \tag{7}$$

$$\propto S_{eq} = \frac{S_{N,1} \cdot S_{N,2}}{S_{N,1} + S_{N,2}} = \frac{k}{k + 1} \cdot S_{N,1}$$

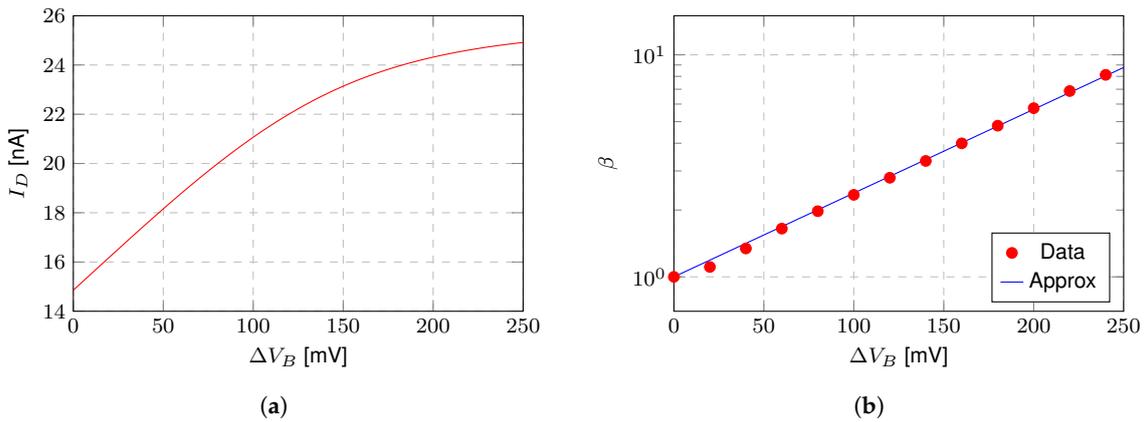
A similar current increase can be reached keeping the size of the two series transistors  $M_{N,2}$  and  $M_{N,1}$  equal ( $k = 1$ ) and biasing the two transistors independently in Figure 1a [22]. Assuming  $V_G = V_D = V_{B1} = 0.25$  V, Figure 2a shows how the drain current  $I_D$  can be increased by means of a difference of the body-bias voltage  $\Delta V_B = V_{B2} - V_{B1}$ . Notice that, in this later case, two series transistors  $M_{N,2}$  and  $M_{N,1}$  in Figure 1a have equal size ( $k = 1$ ) so that the drain current  $I_D$  can be expressed as:

$$I_D \propto \frac{S_{N,1} \cdot \beta S_{N,2}}{S_{N,1} + \beta S_{N,2}} = \frac{\beta}{\beta + 1} \cdot S_{N,1} \tag{8}$$

where

$$\beta \approx e^{\frac{(n-1)\Delta V_B}{n\phi_t}} \tag{9}$$

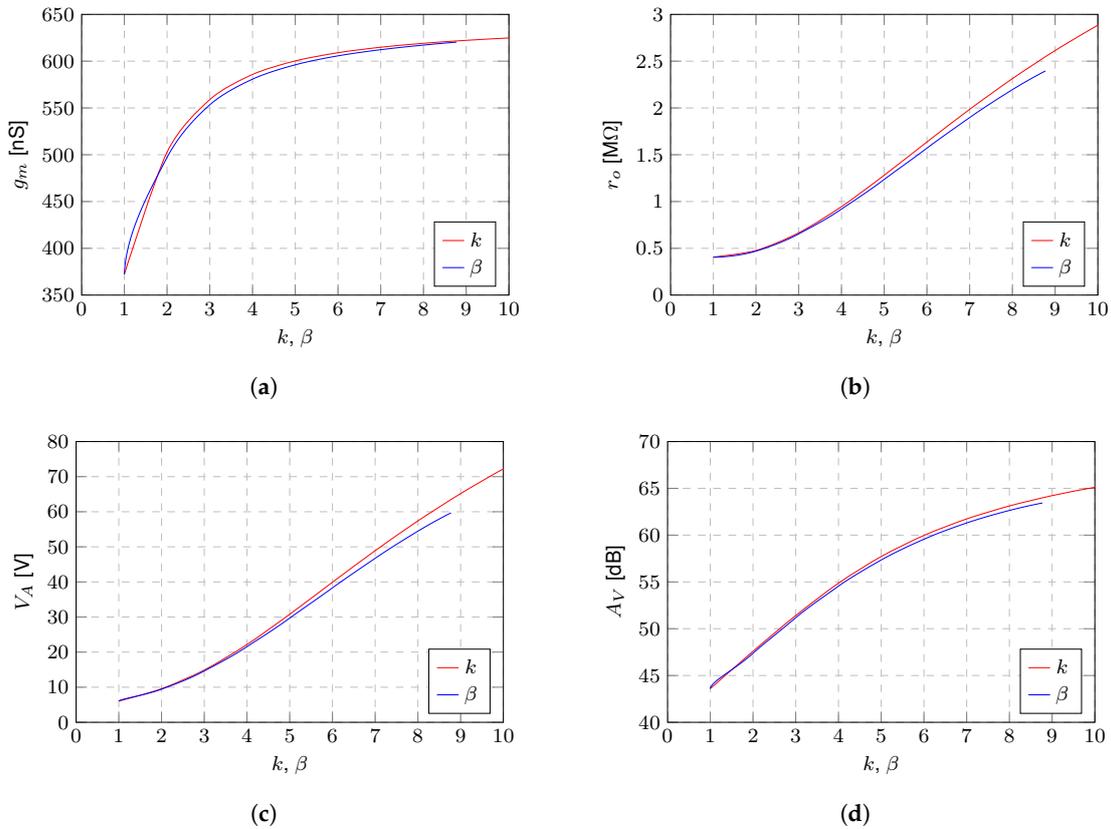
represents a correction factor for the current drain  $I_D$  definition due to the difference between the body-bias of the series transistors  $M_{N,2}$  and  $M_{N,1}$ , assuming the transistors are operating in weak inversion, as can be highlighted comparing (7) with (8). Figure 2b shows how  $\beta$  changes with the difference of the body-bias voltage  $\Delta V_B = V_{B2} - V_{B1}$ , which agrees with the approximation defined by (9) for a slope factor  $n \approx 1.29$  and a thermal voltage  $\phi_t \approx 26$  mV.



**Figure 2.** N-MOS composite transistor: (a) drain current  $I_D$  versus body-bias variation  $\Delta V_B = V_{B2} - V_{B1}$  for equal size of the transistors  $M_{N,2}$  and  $M_{N,1}$  in Figure 1a ( $k = 1$ ); (b) correction factor  $\beta$  versus body-bias variation  $\Delta V_B = V_{B2} - V_{B1}$  for equal size of the transistors  $M_{N,2}$  and  $M_{N,1}$  in Figure 1a ( $k = 1$ ).

Figure 3a shows how the small-signal gate transconductance  $g_m$  changes by varying  $k$  and while keeping  $\Delta V_B = 0$  ( $\beta = 1$ ), and by varying  $\beta$  and keeping  $k = 1$  for  $V_G = V_D = V_{B1} = 0.25$  V. For weak inversion, as expected,  $g_m$  is proportional to  $I_D$ , as

$$g_m \approx \frac{I_D}{n\phi_t} \tag{10}$$



**Figure 3.** Small signal parameters  $k$  and  $\beta$  equivalence: (a) transconductance  $g_m$  (b) output resistance  $r_o$  (c) early voltage  $V_A$  and (d) intrinsic voltage gain ( $A_V$ ).

In addition, the equivalent transistor output resistance  $r_o$ , the inverse of the output conductance  $g_o$ , defined by

$$r_o = \frac{1}{g_o} = \frac{dV_D}{dI_D} = \frac{V_A}{I_D} = \frac{V_E L}{I_D}, \quad (11)$$

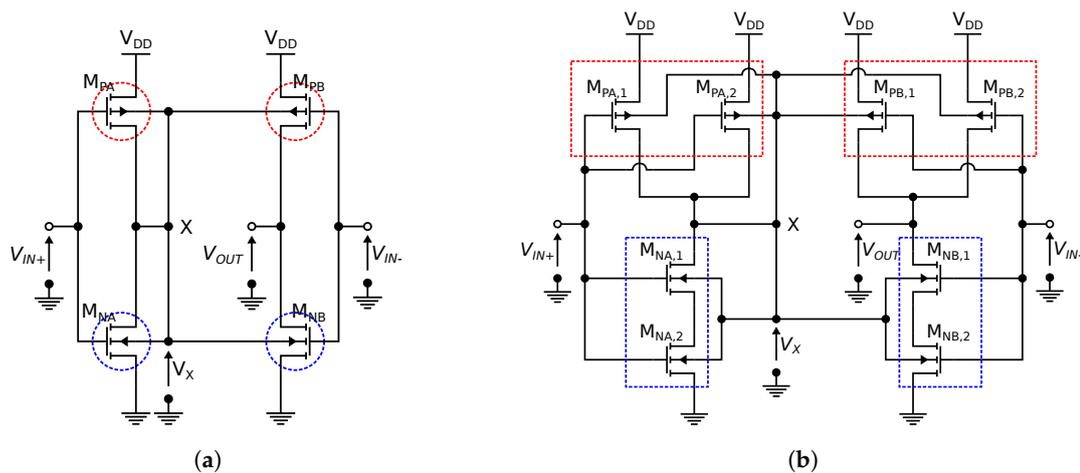
is a function of the Early voltage  $V_A$  and the drain current  $I_D$ , considering that the transistor  $M_{N,2}$  operates in the saturation region. The Early voltage is defined by a technology parameter  $V_E$  and the transistor channel length  $L$ . Figure 3c shows that  $V_A$  increases almost proportionally with  $k$  and  $\beta$ , which means that, by this definition, the equivalent transistor channel length  $L_{eq}$  increases accordingly.

Figure 3d shows the equivalent transistor small-signal intrinsic voltage gain, which is defined as  $A_V = g_m r_o$ . As shown in Figure 3a–d, the small-signal parameters vary almost exactly as a function of  $k$  or  $\beta$ , which proves that an improved composite transistor differential forward-body-bias voltage variation is equivalent to a composite transistor physical parameter variation.

In the next section, the above-mentioned differential forward-body-bias, is applied to two novel inverter-based OTAs with composite transistors.

### 3. Inverter-Based OTAs with an Improved Forward Body-Bias

Figure 4 shows the compact and extended circuit view of the conventional inverter-based, pseudo-differential, single-ended OTA with a forward-body-bias, which is basically the half-circuit of the fully-differential Bulk Nauta OTA proposed in [21].



**Figure 4.** Proposed inverter-based operational transconductance amplifier (OTA) with forward-body-bias common-mode rejection: (a) basic and (b) extended circuit diagram with the respective rectangular transistors highlighted.

In order to compensate the charge mobility difference between PMOS and NMOS transistors, the inverter PMOS aspect ratio  $S_P$  must be greater than the NMOS  $S_N$ . In this particular design,  $S_P$  must be approximately four times greater than  $S_N$ . One way to do that is to keep both PMOS and NMOS transistor lengths  $L$  constant and choose a PMOS width  $W_P$  four times wider than  $W_N$ . In this design, the inverter is made of PMOS parallel transistor arrays and NMOS series transistor arrays, which saves 20% of the total area.

In particular, the equivalent transistors shown in Figure 4a, the PMOS  $M_{PA}$ ,  $M_{PB}$ , and the NMOS  $M_{NA}$ ,  $M_{NB}$  are respectively parallel and series rectangular transistor arrays represented as the single unit transistors in Figure 4b. The red and blue dashed lines highlight such an equivalence.

In the following, all unit transistors that make up the composite transistors have the same aspect ratio  $S_u$ . Assuming that the aspect ratios of  $M_{NA,1}$  and  $M_{NA,2}$  are equal, so that

$$S_{N,1} = S_{N,2} = S_u = \frac{W}{L} \quad (12)$$

the equivalent aspect ratio of the  $N$ -type rectangular transistor array is

$$S_N = \frac{W_N}{L_N} = \frac{W}{2 \cdot L} = \frac{S_u}{2} \quad (13)$$

and its equivalent active area is  $A_{TN} = 2A_u$  where  $A_u$  is the area ( $W \cdot L$ ) of the unit transistor.

Similarly, every  $P$ -type rectangular transistor array  $M_P$  is made of two parallel unit transistors of the same aspect ratio  $S_u$ . Thus, it has an equivalent aspect ratio that is equal to

$$S_P = \frac{W_P}{L_P} = \frac{2 \cdot W}{L} = 2 \cdot S_u \quad (14)$$

and an equivalent active area equal to  $A_{TP} = 2A_u$ .

The two branches of this OTA (named OTA-A in the following) are made of  $P$ -type ( $M_{PA}$ ,  $M_{PB}$ ) and  $N$ -type ( $M_{NA}$ ,  $M_{NB}$ ) transistors whose bulk terminals are all connected to the node  $X$  (see Figure 4a). This way, both the  $P$ - and  $N$ -type transistors  $M_P$  and  $M_N$  bulk terminals of the two branches of the OTA-A are biased at  $V_X \approx V_{DD}/2 = 0.15$  V for typical process parameters.

As the fully differential Bulk Nauta OTA [21], this topology has a limited common-mode rejection and requires additional area required for the guard rings needed to isolate the substrate, so that the overall area is larger than the area of two conventional inverters only. In addition, since the NMOS transistors are independently forward-body-biased, a triple well CMOS process is required.

Based on this topology, a version of the former OTA using improved composite transistors to further increase the voltage gain is proposed, as shown in Figure 5. Similarly to Figure 4a,b, Figure 5a,b represent the compact and extended circuit view of the proposed improved version of the former circuit in Figure 4, where the pull-up and pull-down network are made of improved composite transistors, and each transistor array is equivalently represented by single unit transistors.

In the proposed OTA-B, a modified version of improved composite transistor from [22] is used to independently bias the body of the composite transistors with a differential bulk terminal voltage  $\Delta V_B$ . Instead of being tied to the input nodes of the inverters, as in [22], the bulk terminals of the transistors  $M_{PA-B,2}$  and  $M_{NA-B,2}$  are tied respectively to the diode-connected transistors  $M_{NC}$  and  $M_{PC}$ , so that their voltages are respectively almost equal to zero or to the supply voltage, but the parasitic substrate current is limited [21].

Then, the bulks of the transistors  $M_{PA-B,1}$  and  $M_{NA-B,1}$  are tied to the node  $X$ , which voltage is  $V_X \approx V_{DD}/2 = 0.15$  V.

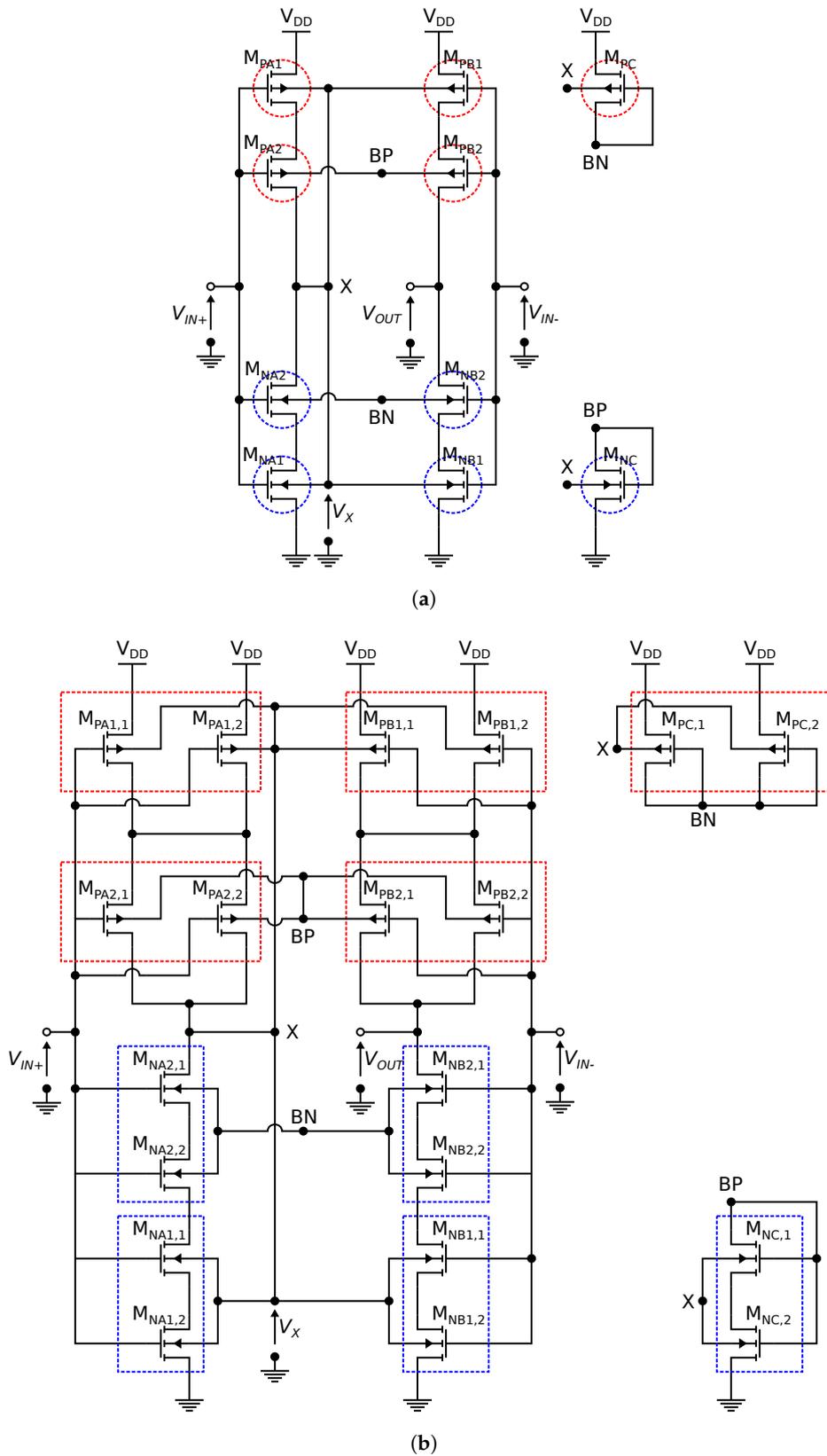
On this basis, each improved composite transistor that defines the pull-up and pull-down network of the OTA-B has a forward-body-bias differential voltage  $\Delta V_B \approx V_{DD}/2 = 0.15$  V, which is the aim of the design.

Notice that these transistors ( $M_{PC}$  and  $M_{NC}$ ) are not required when using a FD-SOI CMOS technology process [24] as this technology offers isolated transistors with a built-in insulator between the substrate and the transistor channel. Moreover, there is no parasitic substrate current by using forward-body-biasing in FD-SOI technologies.

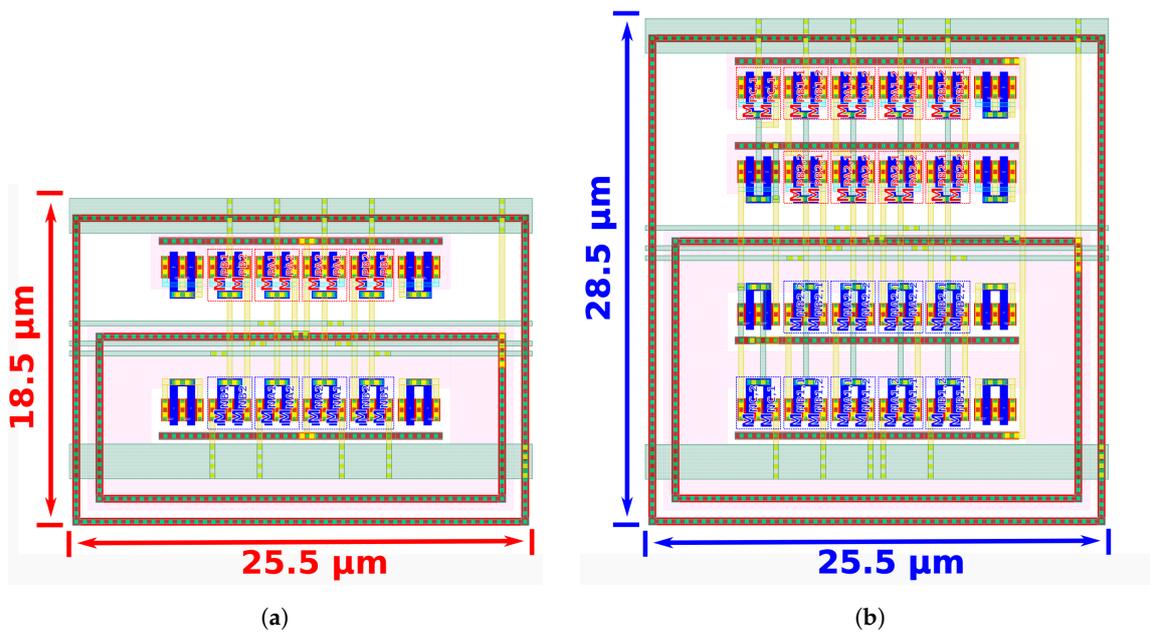
The width  $W$  of each unit transistor, both in the OTA-A and OTA-B, is set on the basis of the minimum sizing requirement of the isolated n-well and p-well. Based on this, all the unit transistors, both PMOS and NMOS, in OTA-A and OTA-B (see Figures 4b and 5b) have an identical aspect ratio equal to

$$\left(\frac{W}{L}\right)_N = \left(\frac{W}{L}\right)_P = \left(\frac{1.26 \mu\text{m}}{0.42 \mu\text{m}}\right) \quad (15)$$

The layouts of the OTA-A and OTA-B are shown in Figure 6a,b, respectively. These figures depict how systematic mismatch reduction layout techniques, such as common centroid and dummy transistors, were employed in both OTAs. The name of the unit transistor are placed on top of each instance in the layout.



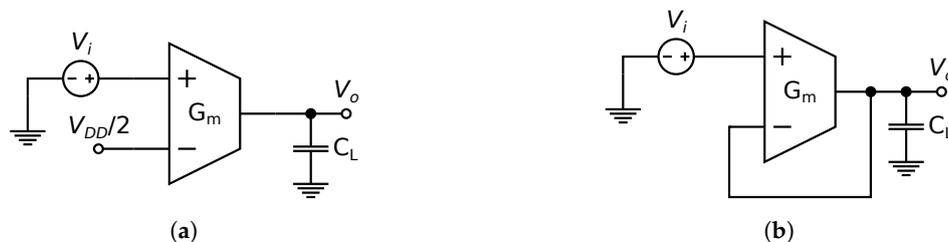
**Figure 5.** Proposed inverter-based OTA with forward-body-bias common-mode rejection and improved composite transistors: (a) compact and (b) extended circuit diagram.



**Figure 6.** Layouts of the proposed inverter-based OTAs with improved forward-body-bias: (a) with single transistors for the pull-down and pull-up network (OTA-A) and (b) with improved composite transistors for the pull-down and pull-up network (OTA-B).

#### 4. Simulation Results

The performance of both OTA-A and OTA-B, designed in TSMC 180 nm CMOS technology, operating at 27 °C, 0.3 V supply voltage, has been validated by using an open-loop and a non-inverting buffer OTA test-bench circuits with a 10 pF capacitive load  $C_L$ . Circuits are respectively shown in Figure 7a,b. These two test-benches are aimed to characterize input and output voltage swings, and output voltage linearity of OTAs.



**Figure 7.** OTAs testbench circuits: (a) Open-Loop (Gm-C Integrator); (b) Non-Inverting Buffer.

Simulations results reported in Sections 4.1 and 4.2 refer respectively to the open-loop and the non-inverting buffer OTA test-bench circuits as shown in Figure 7a,b.

##### 4.1. Open-Loop Analysis

Figure 8 shows how gain and power consumption are affected by the supply voltage variation. It shows how, on the basis of their inverter-based nature, both of the two OTAs are suitable to face voltage/power trade-off as well as operate at the near-threshold voltage. In particular, Figure 8a evince how voltage gains of OTA-A and OTA-B react supply voltage variations from 0.6 V down to 0.2 V. For a supply voltage  $V_{DD}$  equal to 0.2 V, OTA-A and OTA-B have approximately the same voltage gain. As  $V_{DD}$  increases, at a 0.3 V supply voltage, OTA-A and OTA-B have respectively a voltage gains equal to 39 and 51 dB. A further increment of the supply voltage  $V_{DD}$  produce a negligible gain improvement for  $V_{DD}$  higher than 0.4 V. Figure 8b depicts the exponential increment of the current consumption with the voltage supply. Notice that the OTAs are self-biased, thus no extra power consumption related to additional voltage/current reference current has to be considered.

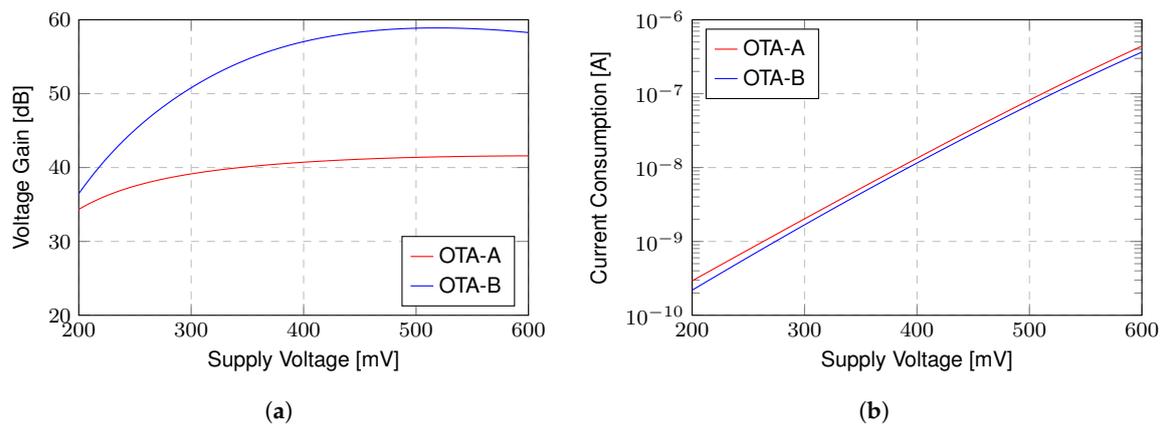


Figure 8. Voltage supply dependence: (a) voltage gain; (b) total current consumption.

The reported results refer to an input voltage equal to  $V_{DD}/2$  where the voltage gain assumes the maximum value. Moreover, the supply voltage affects the OTAs' gains as a consequence of the reverse transistor current and channel length modulation [23]. For these reasons, Figure 9a,b respectively show the proposed OTAs input–output characteristic and the gain of the OTAs versus output voltage for a voltage supply  $V_{DD} = 0.3$  V. Figure 9c,d show the same for  $V_{DD} = 0.6$  V.

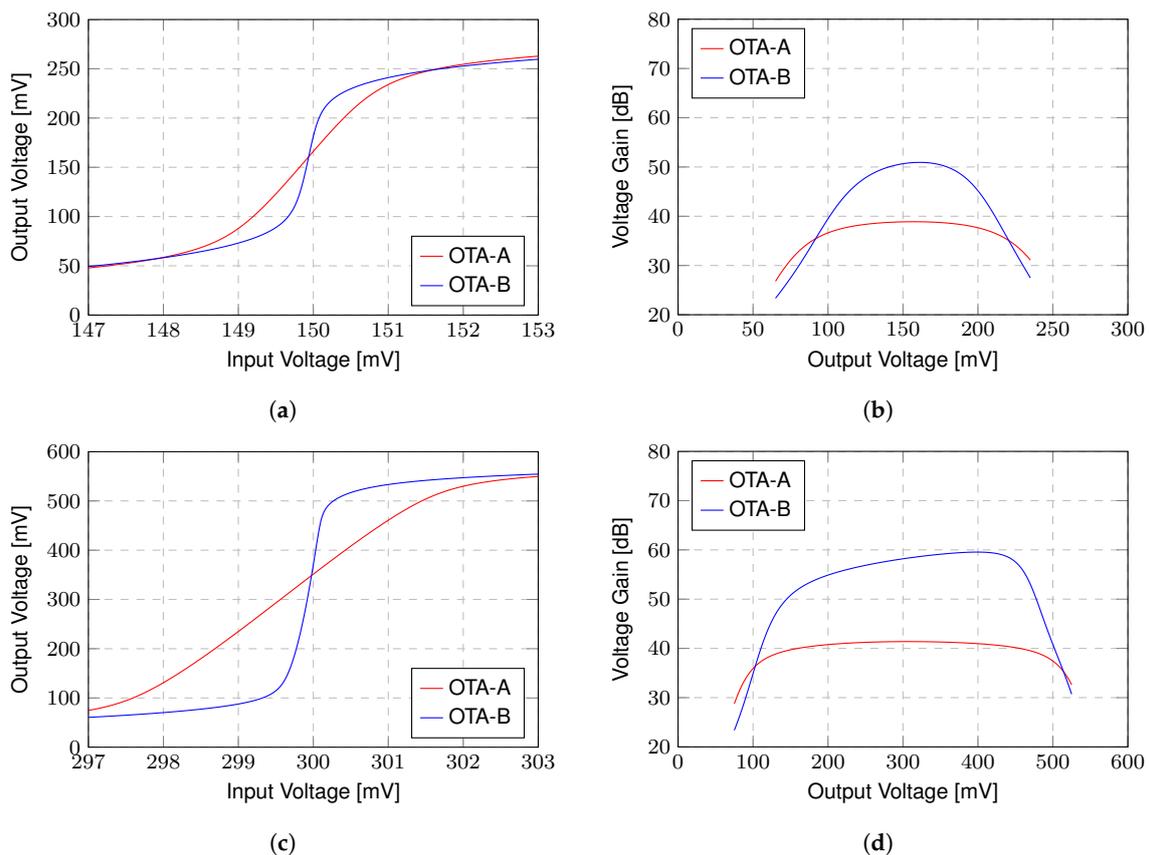


Figure 9. DC open-loop results: (a) input–output characteristic for  $V_{DD} = 0.3$  V; (b) voltage gain for  $V_{DD} = 0.3$  V; (c) input–output characteristic for  $V_{DD} = 0.6$  V; (d) voltage gain for  $V_{DD} = 0.6$  V.

Figure 9b shows output voltage swings from between 100 mV and 200 mV for both OTAs, supplied with  $V_{DD} = 0.3$  V, as either PMOS or NMOS transistors begin to operate in the linear region. Similarly, for a supply voltage  $V_{DD} = 0.6$  V, the valid output voltage swings in the range from 100 mV to 500 mV.

Figure 10a–d show the AC differential voltage gain, CMRR, output phase and PSRR curves, respectively. As expected, OTA-A and OTA-B have similar GBW of 904 and 704 Hz, respectively. As both of the OTAs are single-stage amplifiers, their phase margins are 90°. The common-mode rejection ratios (CMRR) for OTA-A and OTA-B are 30 and 37 dB, and power supply rejection ratios are 33 and 41 dB, respectively.

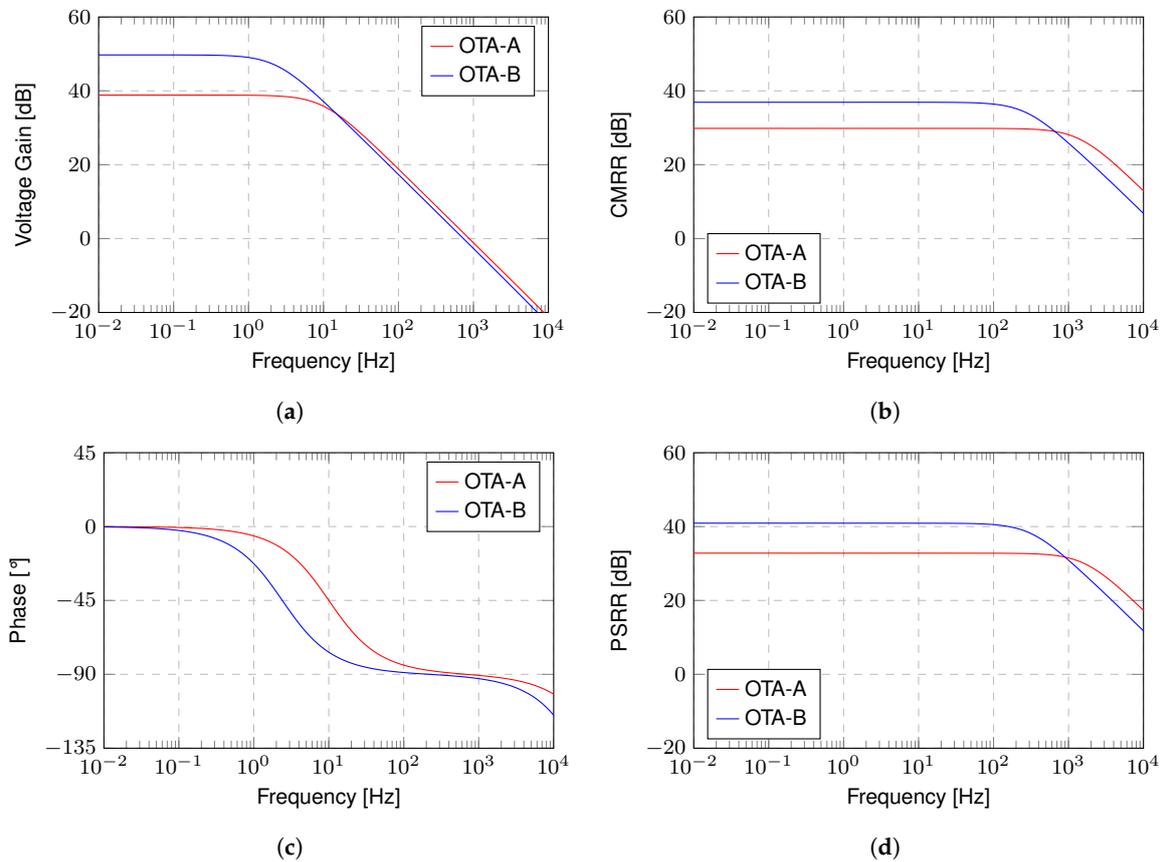


Figure 10. Open-loop AC simulation results: (a) voltage gain; (b) CMRR; (c) phase; (d) PSRR.

Figure 11 shows the equivalent input referred noise for each OTA. OTA-A and OTA-B respectively have equivalent input noises of 784 and 809 nV/√Hz, at 1 kHz. The flicker noise is similar in both OTAs.

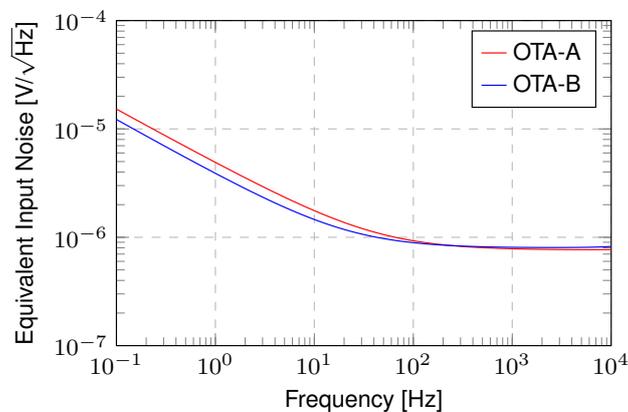


Figure 11. Input referred noise.

### 4.2. Unity-Gain Buffer Analysis

As with the output voltage swing limitations observed in open-loop DC simulations (as in Figure 7a), the non-inverting buffer simulations (as in Figure 7) also reveal the limits of input voltage swing, which are shown in Figure 12.

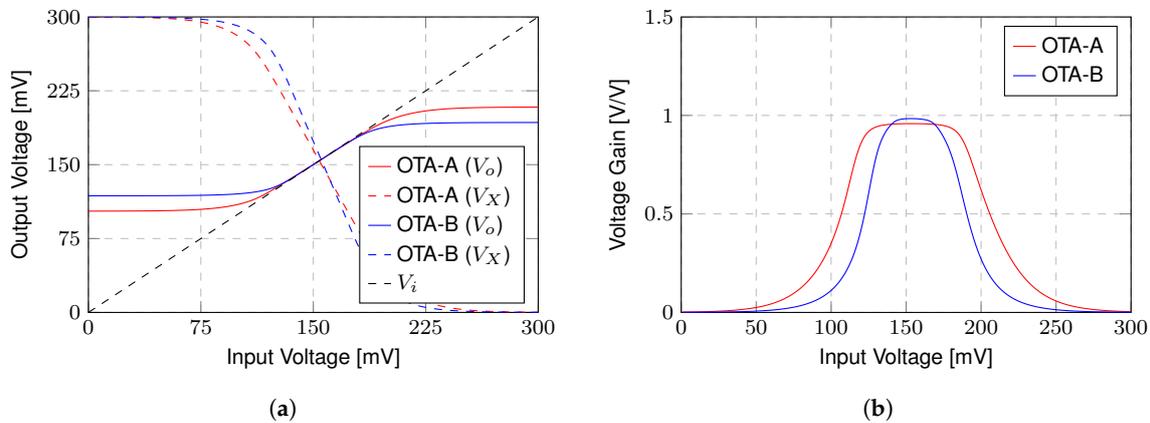


Figure 12. Non-inverting buffer DC simulation results: (a) input–output characteristic and (b) voltage gain.

In particular, Figure 12a shows how the output voltage saturation is a consequence of the voltage gain from the input IN+ to node X. As can be seen,  $V_X \approx -A_{VX}(V_{IN+} - V_{DD}/2) + V_{DD}/2$  and  $A_{VX} \approx 1/(n - 1)$  for OTA-A, where  $A_{VX}$  is the voltage gain between  $V_X$  and  $V_{IN+}$ . This means that the positive input voltage range is limited to approximately  $V_{DD}/2 \pm (n - 1)V_{DD}/2$ . This effect is explained in more detail [21] for the OTA-A fully differential counterpart, the Bulk Nauta OTA. The OTA-B has a slightly shorter input range, since one of the composite transistor bulk terminals are biased by the voltage supply instead of  $V_X$  and does not contribute to common-mode voltage rejection.

The same limitations, from the point of view of time-domain, are shown in Figure 13a for a rail-to-rail input sine-wave. The corresponding total harmonic distortion (THD) is displayed in Figure 13b. A total harmonic distortion of 1% is achieved for input ranges of 70 mV and 35 mV in OTA-A and OTA-B, respectively.

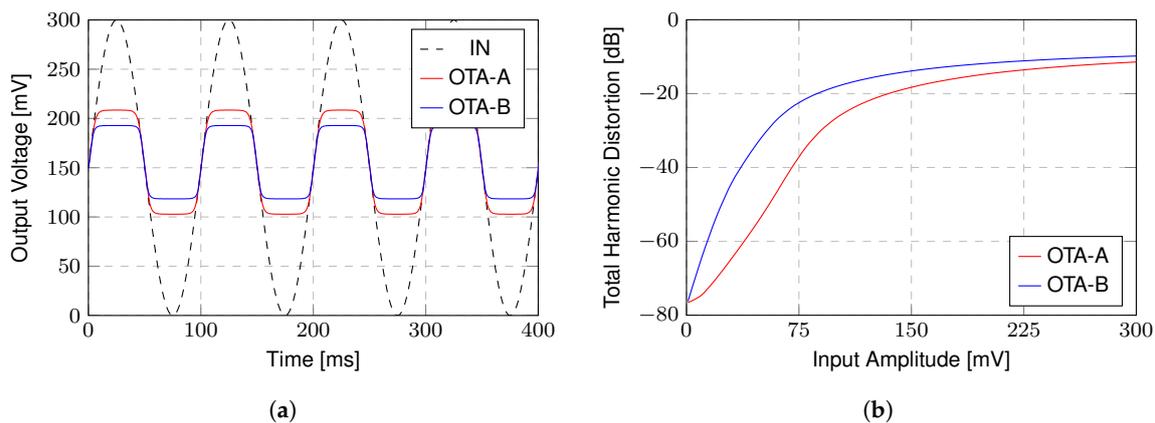


Figure 13. Non-inverting buffer transient simulation results: (a) sine-wave output response; (b) total harmonic distortion.

### 4.3. Monte Carlo Simulation Results

Table 1 summarizes the mean  $\mu$  and the standard variation  $\sigma$  from 1000 Monte Carlo simulation runs. Process and mismatch variations are analyzed individually and combined.

**Table 1.** Monte Carlo results.

		GBW [Hz]		$I_{DD}$ [nA]		FoM [ $V^{-1}$ ]		$A_V$ [dB]		$V_{OS}$ [mV]		Power [pW]	
		$\mu$	$\sigma$	$\mu$	$\sigma$	$\mu$	$\sigma$	$\mu$	$\sigma$	$\mu$	$\sigma$	$\mu$	$\sigma$
Process	OTA-A	947	277	2.1	0.6	447	1	39	0.1	0.2	0.3	635	186
	OTA-B	770	226	1.7	0.5	443	2	51	0.4	0.2	0.4	520	152
Mismatch	OTA-A	905	38	2.0	0.1	447	12	39	0.1	0.1	2.1	607	18
	OTA-B	744	26	1.8	0.0	443	11	51	0.5	0.1	1.8	503	12
All	OTA-A	945	289	2.1	0.6	448	13	39	0.2	0.1	2.1	633	193
	OTA-B	778	778	1.8	0.5	443	11	50	0.7	0.2	1.8	527	154

Results show that gain-bandwidth product GBW, total current  $I_{DD}$ , and power consumption are greatly affected by the process variability. This also results from not using current references for biasing the OTAs. The power efficiency Figure of Merit FoM, defined as  $100 \times (\text{GBW} \cdot C_L)/I_{DD}$ , shows a negligible variation. It is the same for the open-loop voltage gain. As a main drawback, the mismatch variations strongly affect the offset voltage  $V_{OS}$  of both OTAs. The simulations show 6.3 and 5.4 mV input offset voltage for  $3\sigma$  mismatch variation for OTA-A and OTA-B, respectively. Such effect could be compensated by an additional calibration network [25] or by increasing the transistor arrays' sizes [20].

Table 2 summarizes the corner simulation results. As expected, the greatest deviations from typical corner results are GBW and power for SS (Slow-Slow) and FF (Fast-Fast) corners, and the intrinsic input offset voltage for SF (Slow-Fast) and FS (Fast-Slow) corners.

**Table 2.** Corner results.

		GBW [Hz]	$I_{DD}$ [nA]	FoM [ $V^{-1}$ ]	$A_V$ [dB]	$V_{OS}$ [mV]	Power [pW]
TT	OTA-A	904	2.0	447	39	−0.2	607
	OTA-B	743	1.7	443	51	−0.1	503
SS	OTA-A	326	0.7	449	40	0.0	218
	OTA-B	263	0.6	443	50	0.0	178
SF	OTA-A	941	2.1	451	39	−1.7	626
	OTA-B	666	1.4	464	50	−4.3	430
FS	OTA-A	899	2.0	448	39	0.8	603
	OTA-B	735	1.6	448	48	1.1	492
FF	OTA-A	2423	5.4	448	39	−0.3	1624
	OTA-B	1971	4.4	444	51	−0.2	1330

#### 4.4. Performance Comparison

The proposed OTAs are gate input-driven, single-ended, and single-stage and therefore offer compact layouts and power efficiency. The characteristics are summarized and compared with the state of the art in Table 3. The proposed OTA-A is a single-ended version of the fully-differential bulk-nauta OTA presented in [21] that uses conventional composite transistors to increase its voltage gain. Thus, OTA-A would offer similar performance with  $2\times$  less area and power consumption.

Table 3. Performance comparison.

	[8] <sup>+</sup>	[26] <sup>*</sup>	[20] <sup>+</sup>	[25] <sup>*</sup>	[27] <sup>*</sup>	[21] <sup>*</sup>	[8] <sup>+</sup>	[9] <sup>+</sup>	[10] <sup>+</sup>	[11] <sup>*</sup>	[18] <sup>*</sup>	OTA-A <sup>*</sup>	OTA-B <sup>*</sup>	Unit
Technology	180	130	130	180	180	180	180	130	65	65	180	180	180	nm
Input	GD	GD	GD	GD	GD	GD	BD	BD	BD	BD	BD	GD	GD	-
Output	FD	FD	FD	SE	FD	FD	FD	SE	FD	SE	FD	SE	SE	-
N. of Stages	2	2	1	2	1	1	2	2	3	2	2	1	1	-
Die Area	17,000	-	52,000	1426	800	-	26,000	83,000	5000	3000	5000	472	727	μm <sup>2</sup>
VDD	0.5	0.3	0.25	0.3	0.3	0.5	0.5	0.25	0.35	0.3	0.4	0.3	0.3	V
Power	75,000	1800	55	2	10.5	140	17,000	18	17,000	51	300	0.60	0.50	nW
Voltage Gain	62	50	25	35	23	64	52	60	43	60	81	39	51	dB
V. Gain/ N. Stages	31	25	25	18	23	64	26	30	14	30	41	39	51	dB
CMRR	75	-	43	-	-	54	78	-	46	126	126	30	37	dB
PSRR	81	-	47	-	-	51	76	-	35	90	79	33	41	dB
Offset Voltage	6.0	-	-	-	-	-	9.0	8.4	-	7.3	-	6.3	5.4	mV
Input R. Noise	225	38	139	-	-	-	225	3300	-	2820	213	784	809	nV/√Hz
THD	1	-	0.1	3	-	-	1	0.2	0.3	-	-	1	1	%
Input Range	712	-	19	100	-	-	400	150	-	-	-	70	35	mV
GBW	10,000	9100	7.23	0.89	8.0	100	3600	1.88	3600	70	280.4	0.90	0.74	kHz
Phase Margin	60	76	90	76	86	90		53	56	53	59	90	90	°
C <sub>L</sub>	20	2	30	80	10	10	20	15	3	5	5	10	10	pF
FoM	133	303	143	1020	229	370	22	29	22	20	187	447	443	V <sup>-1</sup>

<sup>+</sup> Measured, <sup>\*</sup> Simulated, GD: Gate-Driven, BD: Bulk-Driven, FD: Fully-Differential, SE: Single-Ended.

Bulk-driven OTAs, like those proposed in [8–11,18], are intrinsically more linear and have a larger input voltage range than its gate-driven OTAs counterparts. However, those OTAs deliver a lower transconductance for a given power consumption as can be highlighted from their Figure of Merit (FoM). In addition, bulk-driven OTAs have finite DC input impedance, which could affect previous gain stages. The proposed OTA linearity is limited by the input–voltage excursion, as explained in the previous sections. The THD of both OTA-A and OTA-B are comparable to the other gate-driven inverter-based OTAs shown in the table and their FoMs are the second best after [25], which use extra digital-assisted circuitry.

Multiple-stage OTAs show higher voltage gains at the cost of area and power consumption. Additionally, they need frequency stability circuits to work properly with negative feedback circuits, which costs even more area and power. The OTAs proposed in [9–11,18] are multiple stage OTAs whose first stages are bulk-driven OTAs and the subsequent stages are gate-driven OTAs, which combines the linearity and input range of the bulk-driven OTAs and the voltage gain of gate-driven OTAs. The proposed OTAs have a greater voltage gain than all single-stage OTAs, with the exception of the OTA proposed in [21], which uses larger composite transistors and operates at a higher supply voltage. Most of the presented multiple-stage OTAs have a greater voltage-gain, but their voltage gain over the number of stages are below those of the proposed OTAs.

## 5. Conclusions

This paper introduces two inverter-based OTA topologies to increase the voltage gain without reducing output voltage swing and with a minor linearity degradation for ultra-low-voltage supplies. Proposed OTAs exploit two topological solutions consist of using rectangular arrays for PMOS and NMOS charge mobility balancing and forward-body biasing for common-mode rejection. For analyzing the contribution of each solution individually, OTA-A has been designed as a conventional inverter-based single-end OTA whose equivalent pull-up and pull-down networks are made of rectangular transistor arrays to achieve the smallest area possible. On the other hand, the OTA-B design allies the properties of such rectangular transistors to the improved composite transistor with independent body-bias.

The bulk terminals of the two rectangular transistor arrays which compose the improved composite transistor (pull-up and pull-down network of each branch of the OTA-B) are tied to different voltages. This provides an enhancement of 11 dB on voltage gain for a supply voltage equal to  $V_{DD} = 0.3$  V, which is equivalent to the voltage gain enhancement of a conventional composite transistor with  $2.5\times$  area increase.

Compared with other state-of-art OTAs in similar operation conditions, the proposed OTAs have the largest voltage gain by the number of amplifier gain stages (39 and 51 dB), smallest die-area (472 and  $727\ \mu\text{m}^2$ ), and is among the most power-efficient (447 and  $443\ \text{V}^{-1}$  FoM). The improved self-cascode technique applied to composite transistors can be extended to other inverter-based topologies such as multiple-stage and fully-differential OTAs. Moreover, the same technique can exploit the FD-SOI technologies ability of providing forward-body-bias at higher supply voltages.

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## Abbreviations

The following abbreviations are used in this manuscript:

CMOS	Complementary Metal-Oxide-Semiconductor
CMRR	Common-Mode Rejection Ratio
DP	Differential Pair
FoM	Figure of Merit
GBW	Gain-Bandwidth-Product
NMOS	N-type Metal-Oxide-Semiconductor
OTA	Operational Transconductance Amplifier
PMOS	P-type Metal-Oxide-Semiconductor
PSRR	Power Supply Rejection Ratio
THD	Total Harmonic Distortion
UICM	Unified Current Control Model
ULP	Ultra-Low-Power
ULV	Ultra-Low-Voltage

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