electronics

MDPI

Review

Nonlinear Dynamics, Switching Kinetics and Physical Realization of the Family of Chua Corsage Memristors

Zubaer Ibna Mannan [1] and Hyongsuk Kim [2,*]

[1] Division of Electronics and Information Engineering and Intelligent Robot Research Center, Jeonbuk National University, Jeonju, Jeonbuk 567-54896, Korea; zimannan@gmail.com

[2] Division of Electronics Engineering and Intelligent Robot Research Center, Jeonbuk National University, Jeonju, Jeonbuk 567-54896, Korea

* Correspondence: hskim@jbnu.ac.kr

Received: 31 January 2020; Accepted: 19 February 2020; Published: 21 February 2020

Abstract: This article reviews the nonlinear dynamical attributes, switching kinetics, bifurcation analysis, and physical realization of a family of generic memristors, namely, Chua corsage memristors (*CCM*). *CCM* family contains three 1-st order generic memristor dubbed as 2-lobe, 4-lobe, and 6-lobe Chua corsage memristors and can be distinguished in accordance with their asymptotic stable states. The 2-lobe *CCM* has two asymptotically stable equilibrium states and regarded as a binary memory device. In contrast, the versatile 4-lobe *CCM* and 6-lobe *CCM* are regarded as a multi-bit-per-cell memory device as they exhibit three and four asymptotic stable states, respectively, on their complex and diversified dynamic routes. Due to the diversified dynamic routes, the CC memristors exhibit a highly nonlinear DC *V-I* curve. Unlike most published highly-nonlinear DC *V-I* curves with several disconnected branches, the DC *V-I* curves of *CCMs* are contiguous along with a locally active negative slope region. Moreover, the DC *V-I* curves and parametric representations of the *CCMs* are explicitly analytical. Switching kinetics of the *CCM* family can be demonstrated with universal formulas of exponential state trajectories $x_n(t)$, time period t_{fn}, and applied minimum pulse amplitude V_A and width Δw. These formulas are regarded universal as they can be applied to any piecewise linear dynamic routes for any DC or pulse input and with any number of segments. When local activity, and bifurcation and chaos theorems are employed, CMMs exhibit unique stable limit cycles spawn from a supercritical Hopf bifurcation along with static attractors. In addition, the nonlinear circuit and system theoretic approach is applied to explain the asymptotic stability behavior of *CCMs* and to design real memristor emulators using *off-the-shelf* circuit components.

Keywords: Asymptotical stability; generic memristor; Hopf bifurcation; local activity; memristive system; memory device; nonlinear dynamics; parametric representation; switching kinetics

1. Introduction

Memristor is a nonlinear two-terminal electrical component that completes a theoretical quartet of fundamental electrical components by relating electric charge and magnetic flux linkage. It was postulated by Leon Chua [1] and later generalized to a broader class of dynamical circuit-theoretic concept to a memristive system [2]. Memristor creates immense attention after the seminal paper published by *hp* in 2008, which reveals that the electrical resistance of the device is not constant, but depends on the history of previous inputs [3]. It is considered as one of the most promising element in emerging memory sector [4–6] and neural applications [7,8], due to its propitious attributes under DC or AC excitation and miniature nanoscale physical dimension along with synapse alike operation. Recently, numerous research activities are ongoing on binary and multistate phenomena in generic and extended memristors [9–16] which could lead to another stage of technical innovation

in the memristor area. Nonlinear dynamics theory, and circuit and system theoretic concepts can be devoted to explaining the principle of the multistate memristors [9].

This review paper presents an in-depth and rigorous nonlinear and bifurcation analysis, switching kinetics, and physical realization of the three members of Chua corsage memristor (*CCM*) family. The CC memristors exhibit a highly nonlinear DC *V-I* curves, due to the presence of a higher degree of versatility in its dynamic route map (*DRM*) which has multiple stable equilibrium points. The DC *V-I* curves of *CCMs* are contiguous compared to most published highly-nonlinear DC *V-I* curves which have several *disconnected* branches. The DC *V-I* curves of *CCMs* have an explicit analytical equation with its parametric representation that rarely happens. In addition, each member of *CCM* family exhibits a negative slope region on its DC *V-I* curve which give rise to complexity by exploiting local activity; and *complex phenomenon and information processing* might emerge over the parameter ranges of *CCMs* either operating on or near the neighborhood of its *edge of chaos* domain [12–16].

The locally active *CCM* family exhibit asymptotical stability via the supercritical Hopf bifurcation [13–16]. The state altering of *CCMs* follows the nonlinear dynamic route of a chosen initial state $x_n(0)$ and repeats until the state reaches in a particularly stable state which is termed as an "attractor". The state space of *CCMs* contain various attractors, and each attractor has its own basin of attraction [13–16]. The equilibrium state of these type of memristors moves by the amount of time integral of applied inputs or noises that are applied at a stable equilibrium state. However, the state of *CCMs* returns back to its original equilibrium state (attractor), unless the state moves beyond the boundary of the current basin of attraction [13–16]. Therefore, it can be utilized as a robust bistable or multistate memory device. However, the CC memristors lost a part of previous programming history in this procedure, where such a phenomenon is known as "local fading memory" in bistable and multistate memory devices [10,11].

Another feature of the multistate *CCMs* is the alteration of stable equilibria which requires an input pulse, either a sufficiently large amplitude with a short pulse width or a minimum pulse amplitude with lengthy pulse width. When input pulse is applied, the corsage memristors switch from one stable equilibrium state to another stable state by converging into the basin of the new stable attractor. The resistances or conductances of each attractor, i.e., stable equilibrium states, are distinguishably different from each other [12–16]. The successful alteration of the stable equilibria of *CCMs* is dependent on applied input pulse amplitude and width along with the initial condition. Trajectory movement of the altering equilibria can be demonstrated by computing the time-dependent exponential state trajectories $x_n(t)$ for an individual straight-line segment of PWL *DRM* where time $t = t_{fn}$ is required for the trajectory of $x_n(t)$ to move from any initial point to the end point of that particular segment.

In spite of theoretical insights, concepts from circuit and system theory, and techniques from nonlinear dynamics theory are devoted in this review to investigate the physical realization of the real emulator circuits for *CCM* family. To design a physical emulator circuit for *CCMs*, at least a passive nonlinear-resistive two-port along with a dynamic first-order one-port is required [10–12]. The passive nonlinear-resistive two-port is designed with two parallel connected Graetz bridges [17]. In contrast, the dynamic first-order one-port is designed with a capacitor in parallel with an *active and locally active* resistor where the resistor must exhibit the behavioral attributes of piecewise linear *CCMs*.

Rest of the article is organized as follows: Introduction of *CCM* family and their nonlinear dynamical attributes are presented in Section 2, followed by memory state switching kinetics in Section 3. Local activity and Hopf bifurcation are analyzed in Section 4, and the physical realization of *CCM* emulator is demonstrated in Section 5. Section 6 contains the concluding remarks.

2. *CCM* Family and their Nonlinear Dynamical Attributes

The versatile *CCM* family has three types of generic memristors, namely, 2-lobe *CCM*, 4-lobe *CCM*, and 6-lobe *CCM*. The state-dependent Ohm's law and the piecewise linear state equations of the *CCMs* are defined as

State–Dependent Ohm's Law:

$$i = G(x)\, v, \tag{1}$$

where

$$G(x) = G_0\, x^2, \tag{2}$$

and

State Equation:

$$dx/dt = f_m(x) + v, \tag{3}$$

where x, v, and I denote the memristor state, voltage, and current, respectively. The intrinsic memductance scale of the memristor is fitted with scaling constant G_0 and choose such a way so that the parameters of small-signal equivalent circuit or the current of *CCMs* will not be excessive. For simplicity in this review article, we choose $G_0 = 1$. The state function $f_m(x)$ ("m = {2, 4, 6}" in Equation (3) represents the lobe number of the *CCM*s and determines one of the member of *CCM* family.) of the three types of *CCM* are different from each other and defined as

$$\mathbf{2-lobe\ CCM}:\ f_2(x) = 30 - x + |x-20| - |x-40|, \tag{4}$$

$$\mathbf{4-lobe\ CCM}:\ f_4(x) = 59 - x + |x-20| - |x-40| + |x-65| - |x-95|, \tag{5}$$

and

$$\mathbf{6-lobe\ CCM}:\ f_6(x) = 33 - x + |x-6| - |x-12| + |x-20| - |x-30| + |x-42| - |x-56|. \tag{6}$$

The CCM family exhibits several interesting nonlinear dynamical attributes. Among them, this section analyzes the dynamic route map (*DRM*), power-off plot (*POP*), multivalued DC *V-I* curves and its explicit parametric representation.

2.1. Dynamic Route Map (DRM) and Power-off Plot (POP)

Any curve *f(x, v)* plotted in the phase plane, *dx/dt* vs. *x* plane, along with the *direction of motion* from the representative points is called a *dynamic route* in nonlinear circuit theory. It prescribes the dynamics of defining scalar nonlinear differential equation [18,19]. The *dynamic route map (DRM)* is the most powerful tool for analyzing the dynamics of any first-order differential equation $dx/dt = f(x, v)$ despite its simplicity. It predicts the evolution of any initial state with increasing time [20]. However, the short-circuited ($v = 0$) dynamic route is known as the *Power-off-Plot (POP)* and defined as

$$dx/dt\big|_{v=0} = \hat{f_m}(x,\ \mathbf{0}), \tag{7}$$

where

$$\hat{f_m}(x, \mathbf{0}) = f_m(x). \tag{8}$$

The power-off plot of *CCM* family is shown in Figure 1a–c. Observe from Figure 1a–c that any initial state $x(0)$ on the *upper half* of the *POP*, where $dx/dt > 0$, the state variable $x(t)$ must move to the *right* as x(t) increases with time. Contrarily, any initial state $x(0)$ on the *lower half* of the *POP*, where $dx/dt < 0$, the state variable $x(t)$ decreases with time and must move to the left. The stationary points, where $dx/dt = 0$ (i.e., $\hat{f_m}(x)$ intersects the *x-axis*), are known as *equilibrium points* in the theory of *nonlinear dynamics* [21]. According to nonlinear dynamics theory, the 2-lobe *CCM* has *three* equilibrium points (shown in Figure 1a), whereas, 4-lobe and 6-lobe *CCMs* contains *five* (shown in Figure 1b) and *seven* (shown in Figure 1c) equilibrium points, respectively. Equilibrium points Q_1 ($x = X_{Q1} = 3$), Q_3 ($x = X_{Q3} = 15$), Q_5 ($x = X_{Q5} = 35$), and Q_7 ($x = X_{Q7} = 63$), in Figure 1c, are stable, whereas, Q_2 ($x = X_{Q2} = 9$), Q_4 ($x = X_{Q4} = 25$), and Q_6 ($x = X_{Q6} = 49$) are unstable equilibrium points because the state variable $x(t)$ diverges away from Q_2, Q_4, and Q_6. Similarly, equilibrium point Q_2 ($x = X_{Q2} = 30$) in 2-lobe *CCM*, and the equilibrium points Q_1 ($x = X_{Q1} = 31$) and Q_3 ($x = X_{Q3} = 81$)

in 4-lobe *CCM* are unstable equilibrium points, as shown in Figure 1a and b, respectively. Moreover, the equilibrium points Q_1, Q_3, Q_5, and Q_7 of 6-lobe *CCM* (in Figure 1c), Q_0, Q_2, Q_4 of 4-lobe *CCM* (in Figure 1b), and Q_0, Q_1 of 2-lobe *CCM* (in Figure 1a) are stable as the corresponding eigenvalues of those equilibrium points of the *CCMs* are negative real numbers. In contrast, the unstable equilibrium points have positive real eigenvalues [22].

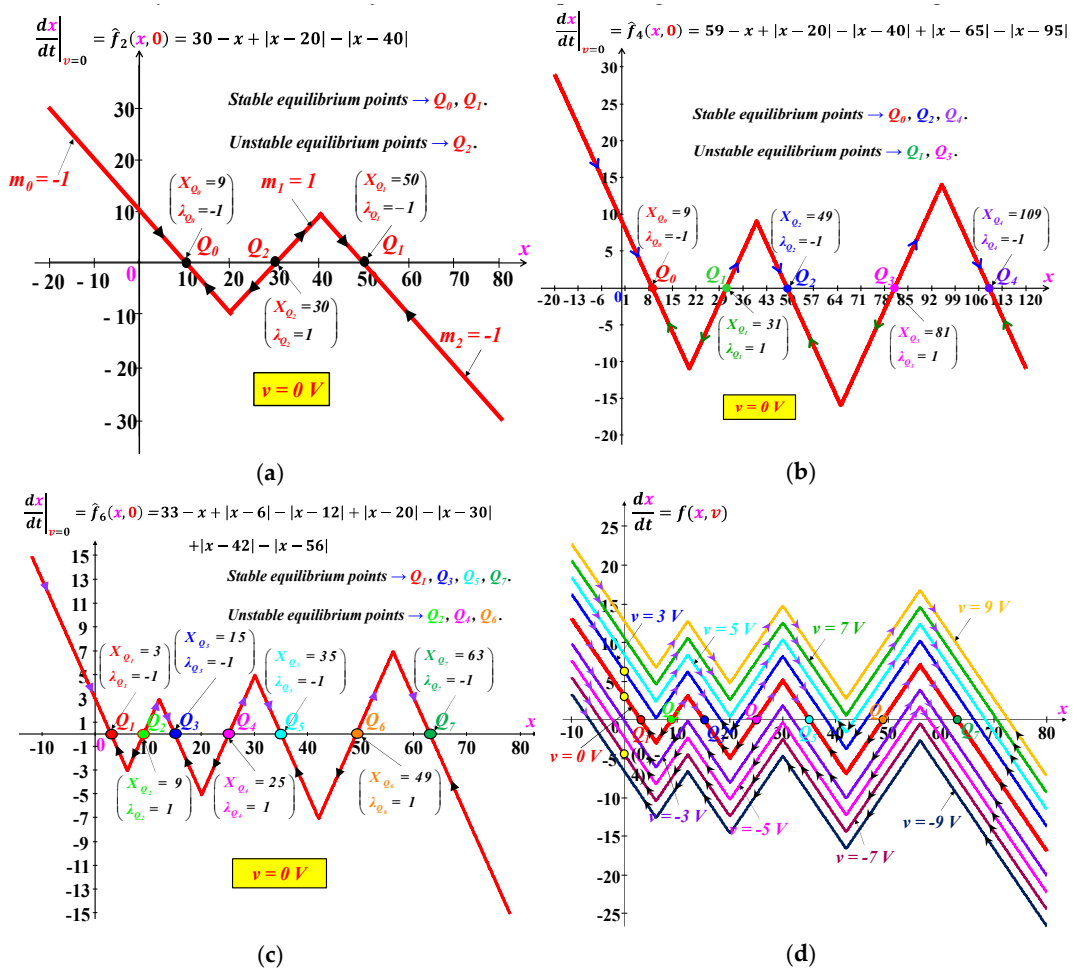

Figure 1. Dynamic route map (*DRM*) and power-off plot (*POP*) of Chua corsage memristors (*CCMs*). *POP* of (**a**) 2-lobe *CCM*, (**b**) 4-lobe *CCM*, (**c**) 6-lobe *CCM*, and (**d**) *DRM* of 6-lobe *CCM*.

The dynamic route map of the 6-lobe *CCM* is shown in Figure 1d for input voltages $v = V = \{-9\ V, -7\ V, -5\ V, -3\ V, 0\ V, 3\ V, 5\ V, 7\ V, 9\ V\}$. Figure 1d shows that for any applied non-zero positive voltage ($v = +V_A$), the red curve $f(x, 0)$ is translated upward by V_A units. For example, for $v = +3\ V$, the corresponding *DRM* $f(x, 3)$ (blue curve) is obtained by translating the red curve (parametrized by $v = 0$) upwards by 3 units. In contrast, for any non-zero negative voltage ($v = -V_A$), the red curve $f(x, 0)$ is translated downwards by V_A units, as the *DRM* for $f(x, -7)$ (burgundy curve) is obtained by translating the red curve ($f(x, 0)$) downward by 7 units for an input voltage $v = -7\ V$, as shown in Figure 1d.

2.2. DC V-I Curve of CCM

DC *V-I* loci of the voltage-controlled *CCMs* are determined through circuit theoretic approach. For each value of voltage V, *all* equilibria ("k" represents the number of equilibrium points of a *CCM*.) $x = X_k$ of the *CCMs* are calculated using state equation (3) where $dx/dt = 0$ and defined as

$$f_m(x) = -V. \tag{9}$$

Then, the DC current $i = I$ of the *CCMs* are determined at each corresponding equilibrium points as

$$I = G(x)\ V = -G_0 X^2 f_m(x) \tag{10}$$

The DC *V-I* curves of *CCM* family are drawn in Figure 2 by plotting the coordinates (*V, I*) computed from Equations (9) and (10) for each value of *X*. The solid curves, in Figure 2, correspond to stable equilibrium states, and the dash curves correspond to unstable equilibrium states. Since the DC *V-I* curve, in Figure 2a, contains two contiguous lobes; hence, the *V-I* curve is called "*two lobes corsage V-I curve*" and the generic memristor is named as 2-lobe *CCM*. Similarly, the DC *V-I* curves in Figure 2b,c contain *four* and *six* contiguous lobes and known as "*four lobes corsage V-I curve*" and "*six lobes corsage V-I curve*", respectively, and the generic memristors are named as 4-lobe *CCM* and 6-lobe *CCM*.

The *five* different colored DC *V-I* branches in Figure 2b represent the equilibrium points of corresponding colors in Figure 1b. The state variables at $v = 0$ *V* are $x = 9$ (red DC *V-I* curve Q_0), $x = 31$ (green DC *V-I* curve Q_1), $x = 49$ (blue DC *V-I* curve Q_2), $x = 81$ (magenta DC *V-I* curve Q_3), and $x = 109$ (purple DC *V-I* curve Q_4) which reveals that the slopes (i.e., conductances $G(x) = G_0\ x^2$) at origin are different and eventually indicates the presence of multiple states. The tabulated upper left inset of Figure 2b shows that the red DC *V-I* curve represents the lowest conductance state (resp., highest resistance state), whereas, the purple DC *V-I* curve represents the highest conductance state (resp., lowest resistance state). Similar to 4-lobe *CCM*, 6-lobe and 2-lobe *CCM* also exhibit the presence of multistate as shown in Figure 2c, and Figure 2a, respectively. However, the unstable dotted *V-I* curves correspond to unstable equilibrium points are going to converge either to the upper stable solid *V-I* curves (for any disturbance $\delta x > X_{Qn}$ or $\delta v > V_{Qn}$) or lowering stable *V-I* curves (for $\delta x < X_{Qn}$ or $\delta v < V_{Qn}$), where *n* determines the number of unstable equilibrium points. This affirms that the 2-lobe *CCM* has *two* stable states, whereas, 4-lobe and 6-lobe *CCMs* have *three* and *four* stable states. These stable equilibrium states can be utilized as memory states in a binary or multi-bit-per-cell memory device [12–16].

Moreover, Figure 2a and the lower right inset of Figure 2b and c show that each member of *CCM* family contain a *negative-slope region* on its DC *V-I* curves which reveals that the CC memristors are locally-active over its corresponding negative slope region as $Re\ Z(i\omega) < 0$ for DC input voltage ($\omega = 0$) [14]. The locally-active negative slope region of Chua corsage memristors are significant in circuit theory as they might give rise to complexity through which *complex phenomenon and information processing* might emerge [23,24].

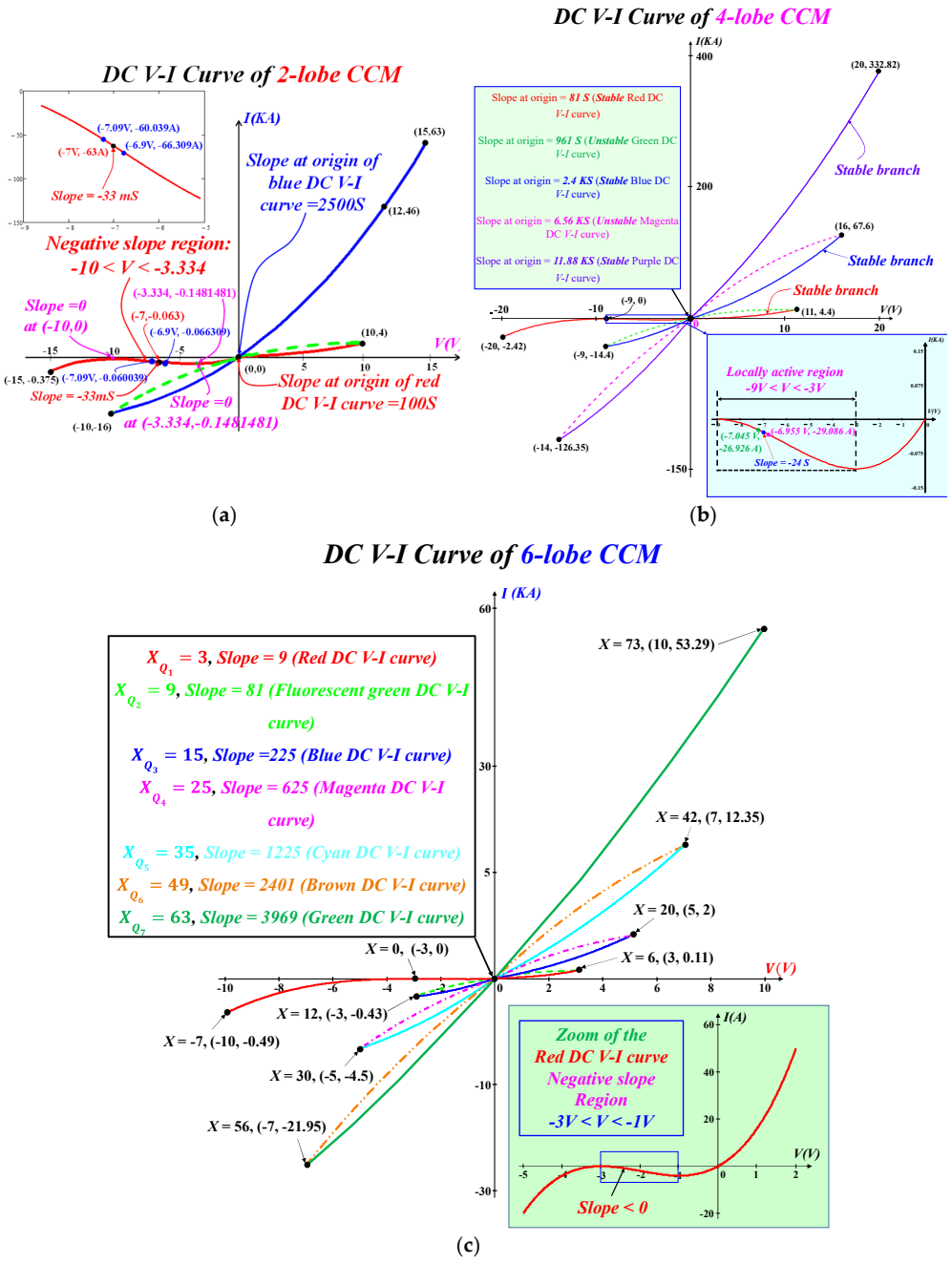

Figure 2. DC *V-I* curves of (**a**) 2-lobe *CCM*, (b) 4-lobe *CCM*, and (c) 6-lobe *CCM*. The lower right insets of figure (**b**) and (**c**) show the zoomed portion of red DC V-I curves and the upper left insets show the slope and state variable X values at $V = 0$ V, respectively.

2.3. Explicit Parametric Representation of CCM

In contrast to DC *V-I* analysis, the parametric representation of *CCMs* can be derived for each DC voltage $v = V$ at the DC equilibrium state $x = X$, namely, $\frac{dx}{dt}\Big|_{(v=V,\ x=X)} = f_m(x) + v = 0$. In particular, substituting $v = V$, $x = X$, and $dx/dt = 0$ in (3), and solving for V, one can obtain

$$V = -f_m(x) \triangleq \hat{v}(X). \tag{11}$$

The parametric representation of the DC curreIt $i = I$ of the *CCMs* can be derived by substituting V given by (11) for $v = V$ in (1); namely,

$$I = G(x)\ V = -G_0 X^2 f_m(x) \triangleq \hat{i}(X). \tag{12}$$

The parametric representations of 6-lobe *CCM* (Due to the page limit we only analyze the parameter representation of the 6-lobe *CCM*.) are shown in Figure 3. Figure 3a, and b show the loci of parametric representation of $V = \hat{v}(x)$ *vs.* X, and $I = \hat{i}(x)$ *vs.* X, respectively, and the loci of parametrically represented $V = \hat{v}(x)$ *vs.* $I = \hat{i}(x)$ is shown in Figure 3c.

Observe from Figure 3a,b that the equilibrium state X spans the entire horizontal axis, namely, $-\infty < X < \infty$. For any value $X \in (-\infty, \infty)$, one can calculate the corresponding DC voltage V, and DC current I using the *exact* formulas in Equations (11) and (12), respectively. Each point on the DC *V-I* curve, shown in Figure 3c, corresponds to an *equilibrium* state X, which may be *stable* (solid line), or *unstable* (dotted line). Since, for voltage $-7\ V \le V \le 7\ V$, the DC *V-I* curve exhibits multiple values, due to corresponding equilibrium states, hence, known as multivalued DC *V-I* curve.

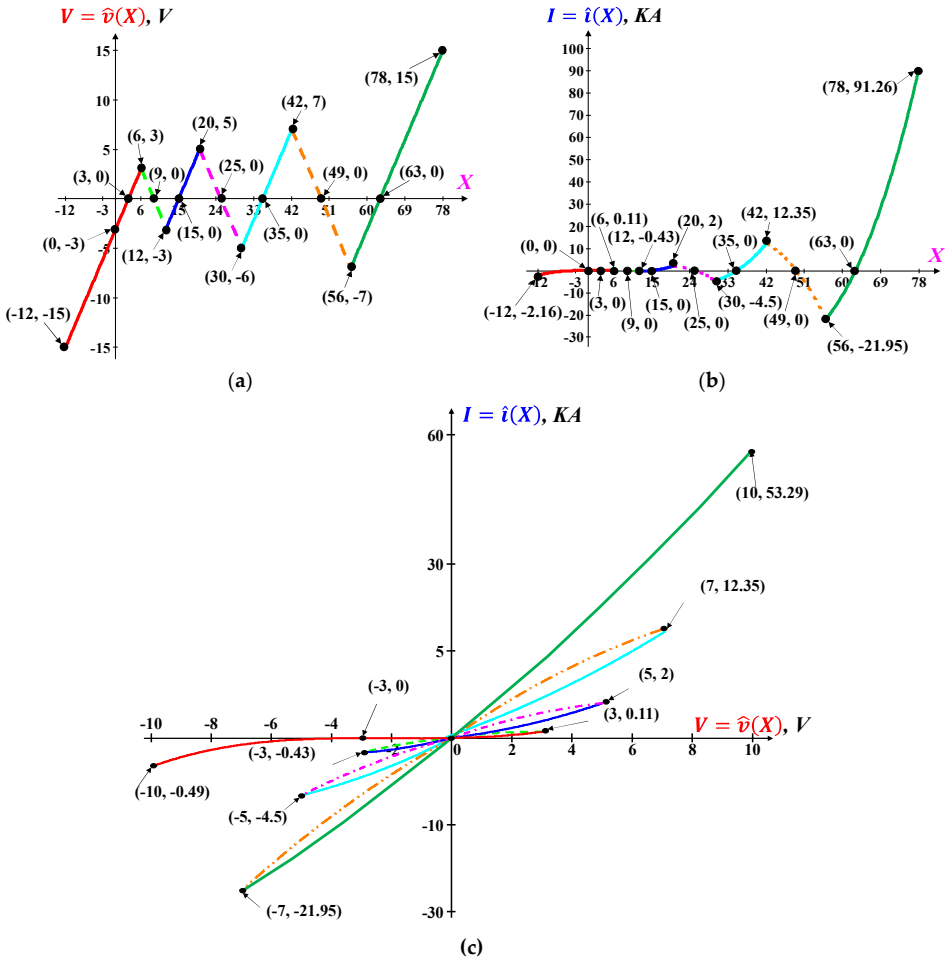

Figure 3. Parametric representation of the 6-lobe *CCM*. (**a**) Voltage $V = \hat{v}(X)$ vs. state variable X, and (**b**) current $I = \hat{i}(x)$ vs. state variable X. (**c**) DC V-I plot, where the coordinates (V, I) of each point are extracted from (a) and (b).

It is important to note that the DC *V-I* curve in Figure 3c is obtained without solving any algebraic, or differential equations. Indeed, it is obtained by substituting any desired value of X, where $-\infty < X < \infty$, into the *explicit analytical* equations (11) for $V = \hat{v}(x)$ and (12) for $I = \hat{i}(x)$. This derivation of *CCMs*

DC V-I curve by direct substitution into the explicit state-dependent Ohm's law, and state equation is a truly remarkable example for future researchers.

In addition, one of the most important features of *CCMs* is that the DC *V-I* curve is contiguous, which is different from many other published nonlinear DC *V-I* curves which exhibit several *disconnected* branches [18]. Another impressive feature is that the parametric representation and DC *V-I* curve of the *CCMs* have an explicit analytical equation, which rarely happens.

3. Switching Kinetics of *CCM* Family

DC *V-I* analysis, in Figure 3, and *power-off-plot*, in Figure 2, explicitly indicate that the Chua corsage memristors can be used as a binary and multistate memory device at $v = 0\ V$. Conceptually, the simplest way to switch the memory states of a memory device is to apply a pulse input with an appropriate pulse amplitude V_A, and pulse width Δw. For successful switching between the memory states of *CCM*, the square pulse should have a minimum pulse width Δw for appropriate pulse amplitude, V_A. Any square pulse with less than the minimum pulse width results in switching failure. The switching kinetics of *CCMs* can be represented through its *dynamic route map* where the solution of each straight-line segments of *DRM* is an exponential function of state variable $x_n(t)$. The complete solution of time-dependent $\boldsymbol{x(t)}$ is made of a sequence of the exponential waveforms joined at the various breakpoints in the dynamic routes [12]. Due to complex and diversified dynamic routes with *multiple* asymptotically stable equilibrium points, 6-lobe *CCM* is chosen to illustrate the successful switching from lower conductance state (resp., higher resistance state) to higher conductance state (resp., lower resistance state) or vice-versa along with switching failure.

Example 1. *Successful switching from lower conductance state* Q_1 *to higher conductance state* Q_5.

The dynamic route map, in Figure 4a, shows the example of a successful switching of the 6-lobe *CCM* from low conductance state Q_1 to high conductance state Q_5 when a pulse input with an amplitude $V_A = 5.5\ V$, and width $\Delta w = 7.48$ s is applied. According to Sect. II-A, the applied pulse with $V_A = 5.5\ V$ is equivalent to translating the red curve $f(x, 0)$ upwards by 5.5 units, as shown by the blue curve $f(x, 5.5)$. The dynamic route starting from low conductance state Q_1 ($x = 3$) at $t = 0^-$ would jump abruptly from Q_1 on red curve to a point directly above Q_1 on the blue curve (yellow circle) at $t = 0^+$ (shown with upward green arrow) as the pulse input increases from 0 V to 5.5 V. Since the blue curve is located above the x-axis (where $dx/dt > 0$), its motion can only move to the right until time $t = \Delta w$. At $t = \Delta w$, the square pulse returns to zero and the point $x_{\Delta w}(t = \Delta w) = 26.5$ (shown with green circle) on the blue curve ($f(x, 5.5)$) reverts back abruptly to the same point on the red curve (shown with light cyan circle followed by a downward green arrowhead). On red curve ($f(x, 0)$), state variable $x(t) = x_{\Delta w}(t)$ diverges away from unstable equilibrium point Q_4 ($x = 25$) and must continue to move rightward along the dynamical movement of *DRM* (i.e., $dx/dt > 0$) until it converges to the low-resistance memory state Q_5 ($x = 35$), as indicated with black arrowheads in Figure 4a.

The exponential trajectories of $x_n(t)$ related to the individual piecewise linear segments are shown in Figure 4b. The total time period needed for the $x(t)$ ($\boldsymbol{x}(t)$ is the collective trajectory of all exponential trajectories $x_n(t)$ that originated from each straight-line segments of *DRM* between Q_1 and Q_5.) trajectory to reach to Q_5 from Q_1 is $t_{fp} = 17.2$ s, although the applied pulse is removed at t = Δw = 7.48 s. This phenomenon illustrates the local fading memory attributes of 6-lobe *CCM*, but reveals the opportunity of utilizing it as a multistate memory device.

Example 2. *Successful switching from higher conductance state* Q_5 *to lower conductance state* Q_1.

To switch from high conductance state Q_5 to low conductance state Q_1 of the 6-lobe *CCM*, a negative pulse with amplitude $V_A = -5.5\ V$ and width $\Delta w_b = 7.684\ s$ is applied. The dynamic route and the state trajectories *x(t)* of switching kinetics from Q_5 to Q_1 are shown in Figure 4c,d, respectively. Figure 4c shows that the dynamic route starting from Q_5 ($x = 35$) on red curve jumps abruptly downward by −5.5 units at $t = 0^+$, as shown with blue curve $f(x, -5.5)$. The state variable $x(t)$ then

moves towards the lower conductance state Q_1 as $dx/dt < 0$. At $t_b = \Delta w_b$, when the negative input is removed, state variable $x_{\Delta wb}$ $(t_b = \Delta w_b) = 8.9$ on blue curve returns to the exact same position on the red curve and continues to move towards Q_1 $(x = 3)$ as $dx/dt < 0$. The exponential trajectories of x_n(t) from memory state Q_5 to Q_1 is shown in Figure 4d where the x_n(t) decreases as the time increases and converges to $x(t_{f1b}) = 3$ which is regarded as the Q_1 memory state. The 6-lobe *CCM* exhibits dissimilar switching time in spite of similar pulse amplitude and greater pulse width as the switching time from higher to lower conductance states, $t_{fpb} = 20.701$ s, is greater than $t_f = 17.2$ s. This reveals that the *CCM* exhibits similar anti-symmetrical switching complication like as other memristive multistate memory devices.

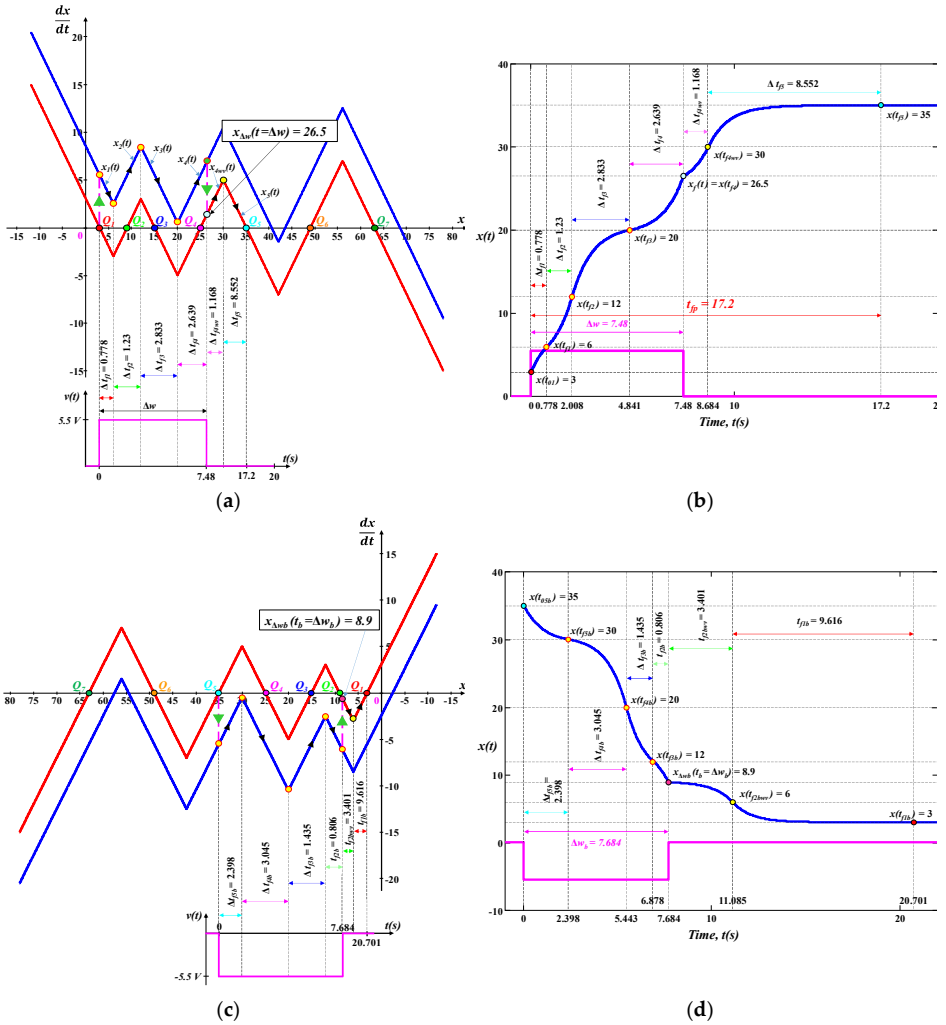

Figure 4. Memory states switching kinetics of the 6-lobe *CCM*. (**a**) Successful switching from lower conductance state Q_1 to higher conductance state Q_5 and (**b**) movement of the exponential trajectories of $x_n(t)$ with respect to time, t, for an input square pulse $V_A = 5.5$ V and $\Delta w = 7.48$ s. (**c**) Successful switching from higher conductance state Q_5 to lower conductance state Q_1 and (**d**) movement of the exponential trajectories of $x_n(t)$ with respect to time, t, for an input square pulse $V_A = -5.5$ V and $\Delta w_b = 7.684$ s.

Example 3. *Switching failure from lower conductance state* Q_1 *to higher conductance state* Q_5.

Amplitude V_A and pulse width Δw of an applied input pulse plays a crucial role in the switching kinetics of memory states of the 6-lobe *CCM*. An inappropriate pulse amplitude or pulse width may result in switching failures which illustrated in Figure 5. An appropriate pulse amplitude $V_A = 5.5$

V with a pulse width Δw = 7 s is applied to the 6-lobe *CCM* to switch the memory state from Q_1 to Q_5. Figure 5 shows that the exponential trajectories are converging to memory state Q_3 (x = 15) rather than converging to memory state Q_5 (x = 35). This switching failure happens as the state variable $x(t)$ fails to cover the distance of $x(t) > X_{Q4}$ = 25 with a pulse width Δw = 7 s. Before the removal of input, the trajectories of state variable $x(t)$ reaches to a point $x_{\Delta w}(t = \Delta w)$ = 23.812 which lies in the left-hand side of Q_4 (x = 25), as shown in Figure 5a. According to Section 2.1, any point lies in the left-side of Q_4 (x = 25) should follow the dynamic route $dx/dt < 0$ (as shown with black arrowhead in Figure 2) and converges to equilibrium state Q_3 and in this case, the state variable $x(t)$ follows the same route $dx/dt <$ 0 and converges to Q_3 (x = 15) rather converging to memory state Q_5 (x = 35), as shown in Figure 5b.

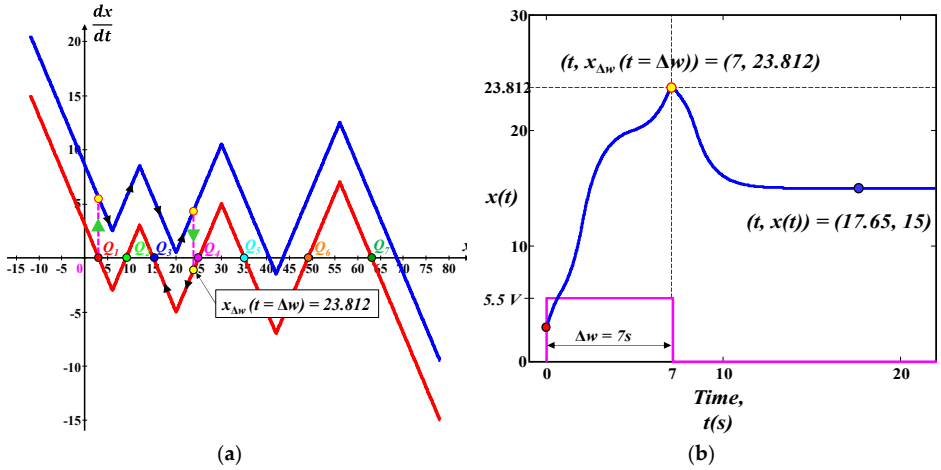

Figure 5. Switching failures of the 6-lobe corsage memristor from Q_1 to Q_5 for a pulse amplitude V_A = 5.5 V and pulse width Δw = 7 s. (**a**) Dynamic routes of the switching kinetics, (**b**) movement of the exponential trajectories of $x_n(t)$ with respect to time, t. The switching failure happens due to insufficient pulse width.

To overcome the switching failure problem, this review article includes the universal formulas (For detail derivation and explanation regarding the universal formulas please refer to ref. [12] and its supplementary materials.) that is required to determine the appropriate pulse amplitude V_A and pulse width Δw. To do so, the exponential trajectories of state variable $x_n(t)$ and the time t_{fn} that required for the trajectorial movement from any initial point $x(t_{in})$ to the end of straight-line segment of *DRM* are computed. The exponential trajectory of state variable x_n(t) of a straight-line segment of the *DRM* at an equilibrium point Q_n is determined as

$$x_n(t) = Q_n - mv(t)\left(1 - e^{m(t-t_{in})}\right) - (Q_n - x(t_{in}))e^{m(t-t_{in})}, \tag{13}$$

where, n represents the number of equilibrium points and m represents the sign value of the straight-line slope,

$$m = sgn\left(\frac{\frac{dx}{dt}\Big|_{start} - \frac{dx}{dt}\Big|_{end}}{x_{start} - x_{end}}\right), \tag{14}$$

and t_{in} is the initial time of the straight-line segment; whereas, $x(t_{in})$ represents the initial state at t_{in}. The time (t_{fn}), that required for the trajectory of $x_n(t)$ to move from any initial point $x(t_{in})$ to the end of the straight-line segment of *DRM*, can be defined as

$$t_{fn} = t_{in} + \underbrace{\frac{1}{m} ln\left[\left|\frac{Q_n - mv(t) - x\left(t_{fn}\right)}{Q_n - mv(t) - x(t_{in})}\right|\right]}_{\Delta t_{fn}}. \tag{15}$$

The complete movement of the exponential trajectories of state variable $x_n(t)$ can be determined by accumulating all the individual exponential trajectories of the straight-line segments of *DRM*,

$$x(t) = \sum_{n=1}^{p} x_n(t) \ (t_{in} \le t < t_{fn}), \tag{16}$$

where there trajectories of $x_n(t)$ only valid over $t_{in} \le t < t_{fn}$ and p represent the total number of *PWL* segments of the *DRM* between initial point $x(t_{in})$and final converged equilibrium point Q_n.

The appropriate pulse amplitude V_A is determined as

$$V_A > \ Q_{(n-1)} - \ x\left(t_{0(n-1)}\right), \tag{17}$$

where $Q_{(n-1)}$ and $x(t_{0(n-1)})$ represent the immediate before equilibrium point and the initial state of the resultant memory state Q_n.

The pulse width Δw is defined as

$$\Delta w = \sum_{n=0}^{q} t_{fn} \ (x(t_{in}) \le x(t) \le \ x_{\Delta w}(t = \ \Delta w))), \tag{18}$$

where q represents the number of straight-line segments of the *DRM* over $x(t_{in}) \le x(t) \le x_{\Delta w}$ $(t = \Delta w)$ and $x_{\Delta w}$ is the user-defined state where the applied input is removed. The value of user-defined $x_{\Delta w}$ determines whether the alteration of memory states is going to be successful or not. For example, in spite choosing $x_{\Delta w}$ $(t = \Delta w) > X = 25(Q_4)$ in Figure 4a, any user-define state value $x_{\Delta w}$ $(t = \Delta w) \le X = 25(Q_4)$ results in unsuccessful switching between Q_1 and Q_5 and the resultant exponential trajectory converges to Q_3 memory state, as shown in Figure 5.

These formulas (Equations (13)–(18)) are universal as they can be applicable to any piecewise linear dynamic routes for any DC or pulse input and with any number of segments. Moreover, the universal formulas in Equations (17) and (18) compute the minimum pulse amplitude and width, which can be used to solve the anti-symmetrical switching complications, in Example 2. Unlike other memristive multistate memory devices which require empirical approach, the CC memristors are defined by universal analytical formulas to determine the appropriate pulse amplitude and width for successful switching from lower conductance state to higher conductance state or vice-versa.

4. Local Activity and Bifurcation Analysis

Local activity principle predicts the presence of *complex phenomena* in a nonlinear dynamical system [23]. Particularly it affirms that a nonlinear circuit made of 2-terminal circuit elements, and/or more complicated 2-terminal devices, can exhibit complex *bifurcation* phenomena, such as *oscillation* and *chaos, if and only if* the circuit contains at least one nonlinear locally-active element. The fundamental deep mathematical theorem given in [23] allows testing the *locally active* phenomenon of a device about some *equilibrium points*, i.e., DC operating points.

According to the theorem presented in [23], 2-lobe, 4-lobe and 6-lobe *CCMs* are locally active over the interval $-10\ V < V < -3.334\ V$ (in Figure 2a), $-9\ V < V < -3\ V$ (in Figure 2b), and $-3\ V < V < -1\ V$ (Figure 2c), respectively, as the slope at any point Q over these intervals is negative, i.e., *Re* $[Y(i\omega)] < 0$ at Q and $\omega = 0$ (DC input), which satisfies the locally active criterion of Re $[Z(i\omega)] < 0$, or Re $[Y(i\omega)] < 0$, for at least one frequency ω [13–16]. Moreover, all the members of the *CCM* family exhibit an *edge of chaos domains* (*Edge of Chaos* is a relatively small subclass of *local activity* [16]. For details regarding *local activity* and *edge of chaos* please refer to ref. [23]) over the same voltage interval as that of local activities [13–16].

Nonlinear dynamical systems satisfying the *edge of chaos criterion* can exhibit bifurcation from a stable equilibrium point regime to a *chaotic* regime by forced excitation [25]. In a local bifurcation, called the *Hopf bifurcation*, an equilibrium point of the system's differential equations loses its stability as a pair of complex conjugate eigenvalues, or equivalently poles of its associated admittance $Y(s, V)$ or impedance $Z(s, I)$, cross the imaginary axis of the complex plane at some critical parameter value

μ_c [26]. Hopf bifurcation theorem asserts that under a relatively general situation, a small-amplitude sinusoidal oscillation will emerge for the control parameter $\mu > \mu_c$, and whose amplitude A increases proportional to $\sqrt{\mu - \mu_c}$, for μ close to μ_c [26,27]. The oscillators made from Chua corsage memristors exhibits *Hopf bifurcation* as it is endowed with a pair of complex conjugate poles on the imaginary axis (known as *Hopf bifurcation points*) of the complex plane [13–16].

The Hopf bifurcation exhibited in the *CCM oscillator circuits* (The *CCM* oscillator circuits are designed by connecting the corsage memristors in series with an external inductor and a battery [13–16].) are classified as *supercritical* because the typical supercritical amplitude $A_v(V) = \sqrt{\bar{x}^2 + \bar{i}_L^2}$ at *Hopf bifurcation points*, shown in Figure 6a,b, is quite similar to the curve computed from the analytical formulas (To avoid the emergence of complex number, the absolute value of $(\mu - \mu_c)$ is used in the analytical formulas. The critical parameters are $\mu_{c1} = -2.25\ V$ and $\mu_{c2} = -1.75\ V$ for 6-lobe *CCM* and constants $k_1 = 2.65$ and $k_2 = 8.75$ are determined empirically for 6-lobe *CCM* oscillator circuit [16].) $A_{m1}(V) = k_1\left[\sqrt{|V + \mu_{c1}|}\right]$ and $A_{m2}(V) = k_2\left[\sqrt{|V + \mu_{c2}|}\right]$ with control parameter $\mu = V$ and critical parameter μ_{c1} and μ_{c2} [16]. In this review article, the supercritical Hopf bifurcation theorem is analyzed using 6-lobe *CCM* oscillator circuit. However, the same bifurcation analogies and amplitude equations hold for 2-lobe and 4-lobe *CCM* oscillator circuits except for the critical parameter of μ_{c1} and μ_{c2}, and constants k_1 and k_2.

According to the supercritical Hopf bifurcation theorem [26,27], the 6-lobe *CCM oscillator circuit* must exhibit a small stable near-sinusoidal oscillation, i.e., a *limit cycle*, over a small range of V beyond the critical parameter value (For better understanding about the choice of critical parameters $\mu_{c1} = -2.25\ V$ and $\mu_{c2} = -1.75\ V$ please refer to Sect. 4.3 and Figure 13 of ref. [16]) $\mu_{c1} = V = -2.25\ V$. Figure 7a and d show that the transient waveforms converge to 2 asymptotically stable equilibrium points $Q_0^1(0.7,\ -1.127)$ for the parameter value $V = -2.3\ V$, (which is near, but to the left of the first Hopf bifurcation point $\mu_{c1} = V = -2.25\ V$ (see inset of Figure 13 in ref. [16])), and $Q_0^2(1.3,\ -2.873)$ for $V = -1.7\ V$ (which is near, but to the left of the second Hopf bifurcation point $\mu_{c2} = V = -1.75\ V$), respectively. However, the transient waveforms generated by 6-lobe *CCM* from two different initial states ($x(0) = 0.95$, $i_L\ (0) = -2.031$) and ($x(0) = 0.8$, $i_L\ (0) = -1.43$) in Figure 7b converge to the yellow stable limit cycle for $V = -2.23\ V$ (which is near, but to the right of the first Hopf bifurcation point $\mu_{c1} = V = -2.25\ V$). Moreover, transient waveforms generated from two different initial states ($x(0) = 1.1$, $i_L\ (0) = -2.431$) and ($x(0) = 1.2$, $i_L\ (0) = -3.53$) for $V = -1.77$ (which is near, but to the right of the second Hopf bifurcation point $\mu_{c2} = V = -1.75\ V$ (see inset of Figure 13 in ref. [16])) converge to a larger yellow limit cycle shown in Figure 7c. The numerical simulation results shown in Figure 7 affirm that the 6-lobe *CCM oscillator circuit* exhibits a stable limit cycle when the bifurcation parameter $\mu = V$ is chosen between the Hopf bifurcation points at $\mu_{c1} = V = -2.25\ V$ and $\mu_{c1} = V = -1.75\ V$, as predicted by the supercritical Hopf bifurcation theorem [16]. Similar supercritical Hopf bifurcation analogies also exhibits in 2-lobe and 4-lobe *CCM* oscillator circuits [13–15].

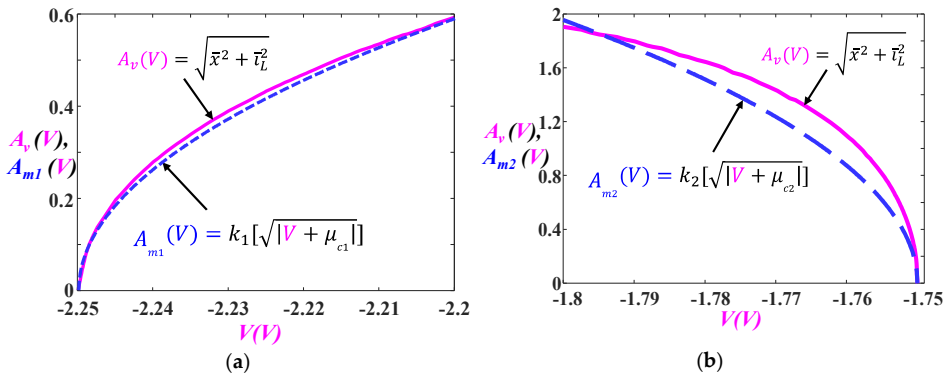

Figure 6. Numerical verification of supercritical Hopf bifurcation of the 6-lobe *CCM* oscillator circuit.

Verification of supercritical Hopf bifurcation as a parameter $\mu = V$ near (**a**) first Hopf bifurcation point $\mu_{c1} = V = -2.25$ V, and (**b**) second Hopf bifurcation point $\mu_{c2} = V = -1.75$ V where $k_1 = 2.65$ and $k_2 = 8.75$ obtained empirically [16].

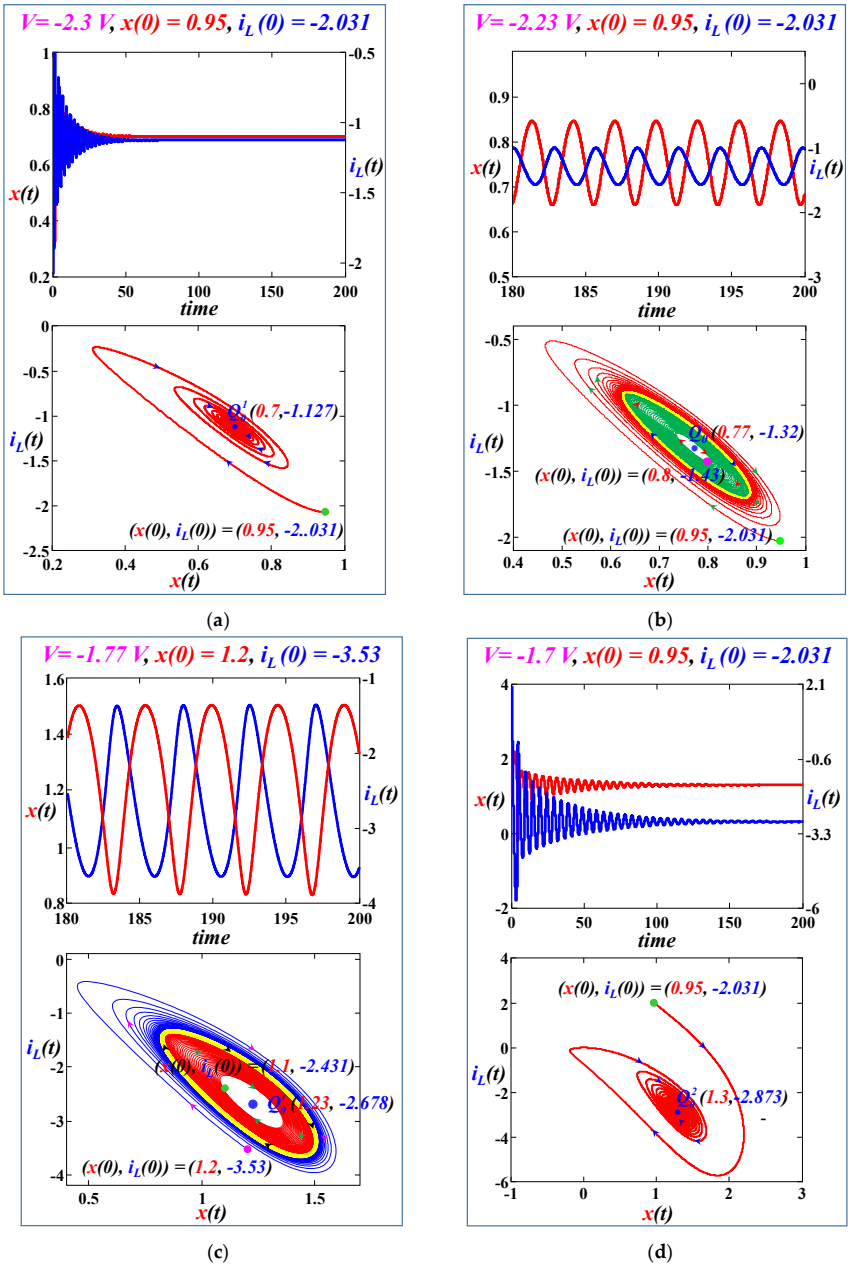

Figure 7. Numerical simulation results of supercritical Hopf bifurcation theorem *of 6-lobe CCM oscillator circuit* with *external inductor* L* = 355.5 mH. (**a**) Transient waveform converges to Q_0^1(0.7, −1.127) for V = −2.3 V with initial condition ($x(0)$, $i_L(0)$) = (0.95, −2.031), (**b**) Transient waveforms generated from two different initial states ($x(0)$, $i_L(0)$) = (0.95, −2.031) and ($x(0)$, i_L (0)) = (0.8, −1.43) converge to a yellow limit cycle for V = −2.23 V, (**c**) Transient waveforms generated from two different initial states ($x(0)$, $i_L(0)$) = (1.1, −2.431) and ($x(0)$, $i_L(0)$) = (1.2, −3.53) converge to a large yellow limit cycle for V = −1.77 V, and (**d**) Transient waveform converges to Q_0^2(1.3, −2.873) for V = −1.7V with initial condition ($x(0)$, $i_L(0)$) = (0.95, −2.031).

5. Physical Realization of *CCM* Family

Chua corsage memristors, shown in Figure 8a, can be physically realized in circuit by including the switching kinetics closer to the behavioral attributes of each segment of PWL dynamic route map. A passive nonlinear-resistive two-port and a dynamic first-order one-port are cascaded to design an emulator circuit for *CCM* memristor [10], as shown in Figure 8b. The passive nonlinear-resistive two-port is composed of parallel connected Graetz bridges [17] with anti-serial diodes and the dynamic first-order one-port is made up of a *C*-*R* parallel circuit. Two set of Graetz bridge are used to supply double amount of input current to the dynamic first-order one-port, i.e., *C*-*R* parallel circuit, for faster switching of memory states.

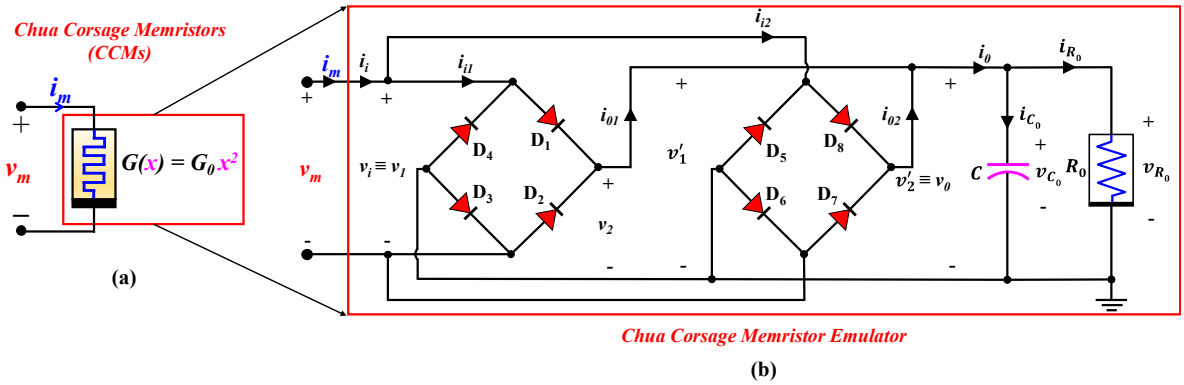

Figure 8. Circuit diagram of (**a**) Chua corsage memristors and (**b**) Chua corsage memristor emulators with bi-stability or multi-stability input dynamics.

The DC *V*-*I* curve of active and locally active resistor R_0 in dynamic one-port, in Figure 8b, should exhibit the same number of contiguous breakpoints to that of the DC *V*-*I* curves of *CCMs*. For example, the DC *V*-*I* curve of R_0 for 2-lobe *CCM* emulator must have *two* breakpoints, whereas, for 4-lobe and 6-lobe emulator the DC *V*-*I* curve of R_0 should exhibit *four* and *six* contiguous breakpoints, respectively.

To design the nonlinear resistor R_0 for *CCM emulators*, circuit theoretic analysis is conducted on opamps to obtain the desired DC *V*-*I* breakpoints at specific voltages to that of *CC memristors*. The driving point characteristic of a single positive and negative feedback op-amp circuit provides *two* breakpoints on its piecewise linear DC *V*-*I* curve [28]. Therefore, only a single positive and negative feedback op-amp circuit is sufficient to design an active and locally active R_0 for 2-lobe *CCM* emulator, as shown in Figure 9a. However, two and three parallel-connected opamp circuits are required to design a *four* and *six* breakpoint piecewise linear DC *V*-*I* curves for 4-lobe and 6-lobe *CCMs*, respectively, as shown in Figure 9b,c. The circuit theoretic analysis for designing the *CCM* emulator circuit is conducted on 6-lobe *CC memristor*, as it has the highest number of breakpoints on its contiguous *six lobes corsage DC V-I curve*.

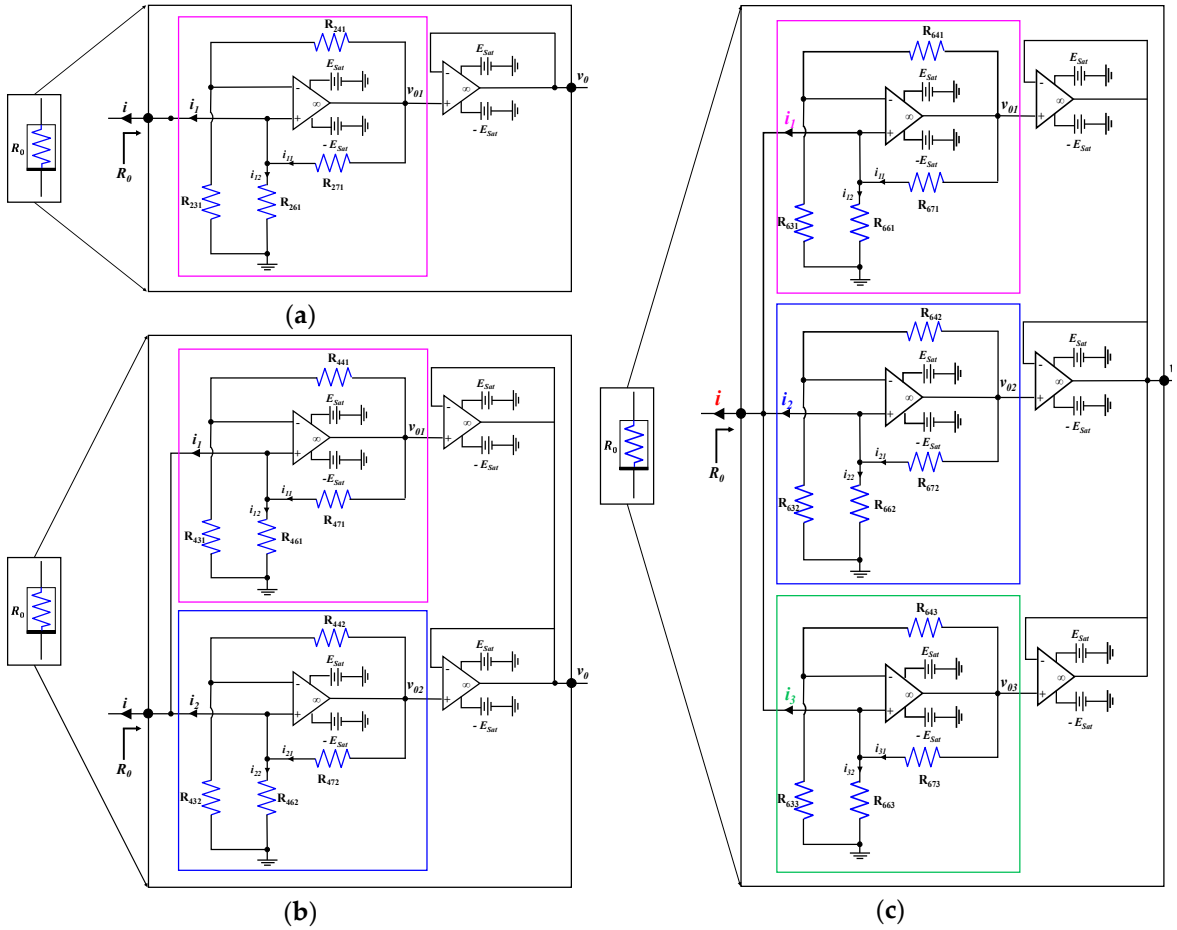

Figure 9. Circuit diagram of the active and locally active nonlinear resistor R_0 for (**a**) 2-lobe *CCM*, (**b**) 4-lobe CCM, and (**c**) 6-lobe CCM.

The circuit components and parameters of the parallel-connected opamps, in Figure 9c, are exactly same except the negative feedback resistances (R_{641}, R_{642}, and R_{643}). The effective saturation voltage (βE_{sat}) of an individual op-amp circuit is determine by the negative feedback resistance which plays a crucial role to achieve the desired *V-I* breakpoints at specified voltages, such as V= ±3 V, V= ±5 V, and V= ±7 V (The 6-lobe *CCM* has six breakpoints on its DC *V-I* curve at V = {±3 V, ±5 V, ±7 V} as shown in Figure 2c). However, the positive feedback path of the op-amp circuits might arise difficulties with the driving-point and transfer function. Such complication can be resolved by replacing the op-amp circuit with three ideal models, such as "***– Saturation region***", "***Linear region***", and "***+ Saturation region***". According to the circuit theoretic approach presented in [12], the three ideal models generate the following combine current (i_n) of an individual opamp circuit for an input voltage v,

$$i_n = \underbrace{\left[\frac{1}{R_{67n}}\left[v\left(1+\frac{R_{67n}}{R_{67n}}\right)+E_{sat}\right]\right]}_{-Saturation\ Region\ (v\le -\beta E_{sat})} + \underbrace{\left[\frac{1}{R_{67n}}\left[v\left(1+\frac{R_{67n}}{R_{67n}}\right)-v_{on}\right]\right]}_{Linear\ Region\ (-\beta E_{sat}\le v\le \beta E_{sat})} + \underbrace{\left[\frac{1}{R_{67n}}\left[v\left(1+\frac{R_{67n}}{R_{67n}}\right)-E_{sat}\right]\right]}_{+Saturation\ Region\ (v\ge \beta E_{sat})} \quad (19)$$

where n = {1, 2, and 3} denotes the operating opamp circuit. Figure 10a shows the mathematically computed *V*-i_n plots of the individual currents of opamp circuits. Observe that each *V-I* curves has two breakpoints at specific voltage at V = ± 2.82 V, V = ± 4.95 V, and V = ± 6.99 V. The value of the breakpoints are a bit dissimilar to that of 6-lobe *CCM* (V = {±3 V, ±5 V, ±7 V}) as the measured resistive

parameters ($R_{631} = R_{632} = R_{633} = 0.985K$, $R_{661} = R_{662} = R_{663} = 100.5K$, $R_{671} = R_{672} = R_{673} = 1.001K$, $R_{641} = 3.888K$, $R_{642} = 1.797K$, $R_{643} = 0.987K$) are used in simulation.

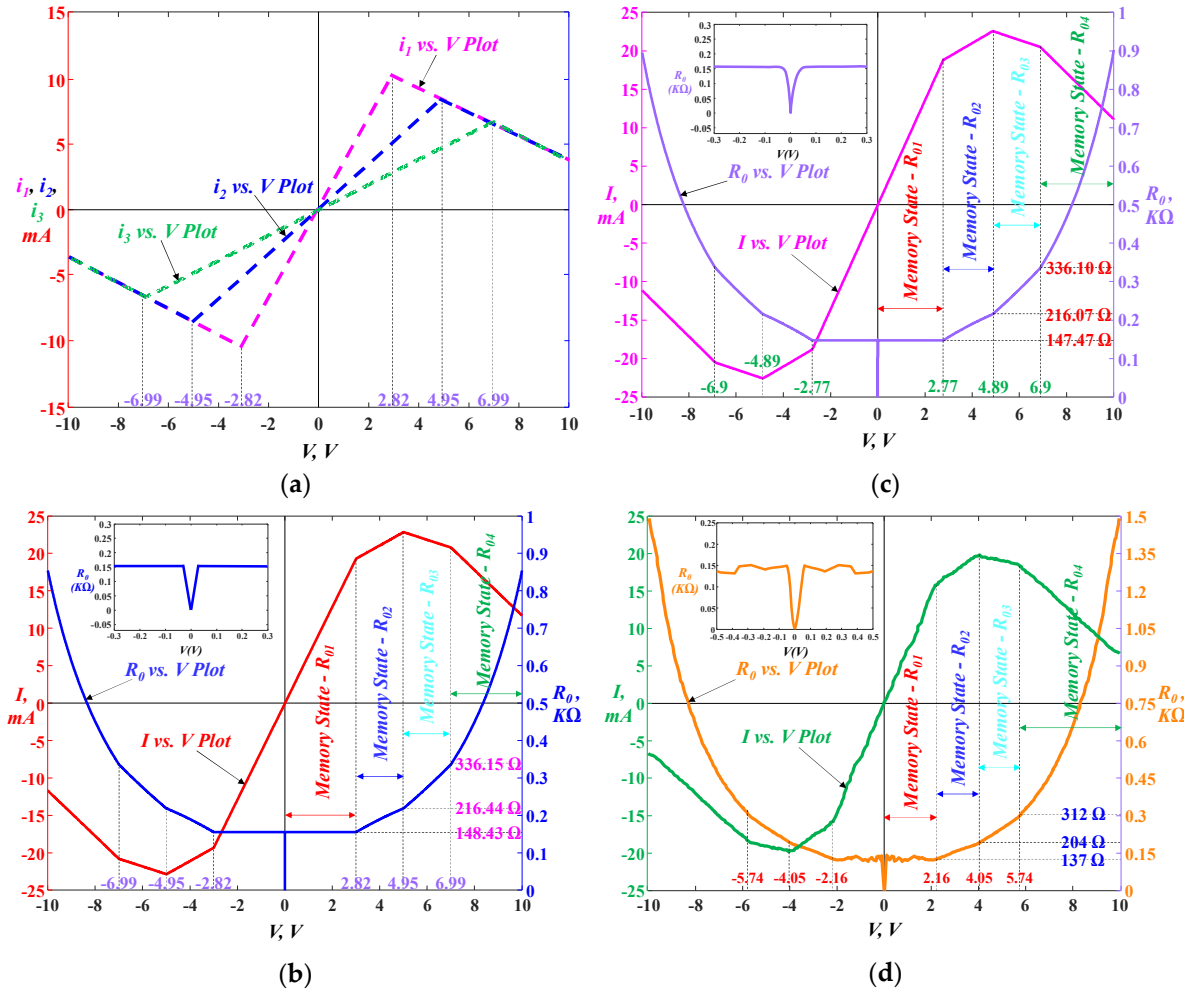

Figure 10. (**a**) DC voltage V vs. current i_1, i_2, and i_3 diagram, (**b**) I vs. V and R_0 vs. V plot of mathematical model, (**c**) I vs. V and R_0 vs. V plot of spice circuit simulation, and (**d**) I vs. V and R_0 vs. V plot of the actual circuit implementation of the active and locally active resistor of the 6-lobe *CCM* emulator.

The total current of parallel-connected opamp circuit is equal to the summation of all individual opamp currents, $i = \sum_{n=1}^{3} i_n$. The mathematical simulation of *V-I* curve and the resistance of active and locally active R_0 ($R_0 = V/I$) are shown in Figure 10b, whereas, the SPICE simulation and circuit implementation waveforms are shown in Figure 10c, and d, respectively. Observe from circuit implementation waveforms, in Figure 10d, that the locally active R_0 remains almost constant at R_{01} = 137Ω over an input voltage range $-2.16\ V < V < 2.16\ V$, except for a tiny interval at the origin. For $\pm 2.16\ V < V < \pm\ 4.05\ V$, $\pm 4.05\ V < V < \pm 5.74\ V$, and $V > \pm 5.74\ V$, R_0 increase from 137 Ω to 204 Ω, 204 Ω to 312 Ω, and 312 Ω *to* R_{max} (very large resistance value), respectively. However, the increment rate of R_0 is dissimilar for each voltage range which reveals that the slope is constant in a particular voltage range, but inconstant for different voltage ranges. This suggests that the active and locally active R_0 exhibits four distinct memory states, namely, R_{01}, R_{02}, R_{03}, and R_{04} as shown in Figure 10b–d.

The numerical values of DC *V-I* breakpoints and the resistance ranges of nonlinear resistor R_0 (in Figure 10b–d) for mathematical modeling, *SPICE* simulation, and circuit implementation are unequal. The reason behind such inequality is the non-ideal circuit components of the *SPICE* module and

the non-ideal characteristic of the implemented opamps along with noise induction from DC power supply and oscilloscope probe. Although the breakpoints of DC *V-I* curves in Figures 2c and 10b–d are quantitatively different, but qualitatively same. This reveals that the DC *V-I* curve of any real nonlinear resistor can be converted into a memristor by applying the basic method explained in [10–12] and [18].

However, unlike a passive nonlinear-resistive two-port emulator circuit, the bi-stability and multi-stability phenomena of Chua Corsage Memristors can be realized by a single device as demonstrated in recent literature [29–31]. The NbO_2 Mott memristor [29,30] exhibits an analogous dynamic route to that of 2-lobe *CCM* which has two stable and one unstable equilibrium points on its dynamic route map (dT/dt vs. T (Figure 1 [29])). The state switching attributes of NbO_2 memristor are identical to 2-lobe *CCM* and regarded as bi-stable device. The universal formulas of switching kinetics (in Section 3) can be applicable to NbO_2 Mott memristor as the PWL dynamic route, and switching kinetics are explicitly similar to 2-lobe *CCM*. In addition, HfOx/AlOy-based homeothermic memristor [31] has a similar number of stable equilibrium states (i.e., four temperature-dependent equilibrium states corresponding to its four dynamic conductances (Figure 3 in [31])) to that of 6-lobe *CCM*. When driven by DC input, the homeothermic memristor exhibits four distinct DC *V-I* curves corresponding to its four temperature-dependent dynamic conductances (Figure 3e and f in [31]) which is identical to 6-lobe *CCM* (shown in Figures 2c and 10). In spite of the quantitative dissimilarities, the NbO_2 Mott memristor and homeothermic memristor qualitative exhibit the bi-stability and multi-stability phenomena of CC memristors.

6. Concluding Remarks

This review article presents an in-depth and rigorous analysis of the nonlinear dynamical attributes, switching kinetics, and physical realization of Chua corsage memristors (*CCMs*). The versatile *CCMs* exhibit multiple stable equilibria on their complex and diversified, dynamic route map (*DRM*) and power-off plot (*POP*). Due to the presence of a higher degree of versatility in *DRM*, the *CC* memristors have a variety of dynamic paths in response to different initial conditions which reveals a highly nonlinear DC *V-I* curves. Unlike most published highly-nonlinear DC *V-I* curves which have several *disconnected* branches, the DC *V-I* curves of *CCMs* are contiguous. Moreover, the parametric representation and DC *V-I* curves of *CCMs* have an explicit analytical equation, which rarely happens.

The multiple stable equilibria on the *DRM* of *CCMs* reveal that it can be utilized as binary and multistate memory device whose exponential state trajectories for a particular linear piecewise segment, time period that required for the state trajectorial movement of the particular PWL segment, and the appropriate pulse amplitude and width that required for successful memory state switching can easily be determined from the universal formulas presented in Sect. 3. These universal formulas are applicable to any PWL *DRM* curves with any number of segments for any DC or pulse input.

Another impressive feature of *CCMs* is the locally active negative slope region of the DC *V-I* curves which gives rise to *complex phenomenon*, such as oscillation, by exploiting the *edge of chaos* and supercritical Hopf bifurcation theorem.

Last, but not least, the *off-the-shelf* active and locally active resistor (R_0) in *CCM* emulators (designed with opamp or parallel-connected opamp circuits) is capable of emulating the attributes of the *CCM* DC *V-I* curves and proved that a memristor could be implemented using any real nonlinear resistor. Moreover, NbO_2 Mott memristor and HfO_x/AlO_y-based homeothermic memristor reveals that the bi-stability and multi-stability phenomena of Chua corsage memristors can also be realized with a single physical device.

Author Contributions: Conceptualization, Z.I.M. and H.K.; methodology, Z.I.M. and H.K.; software, Z.I.M.; validation, Z.I.M. and H.K.; formal analysis, Z.I.M.; investigation, Z.I.M.; resources, Z.I.M. and H.K.; data curation, Z.I.M. and H.K.; writing—original draft preparation, Z.I.M.; writing—review and editing, Z.I.M. and H.K.; visualization, Z.I.M.; supervision, Z.I.M. and H.K.; project administration, H.K.; funding acquisition, H.K. All authors have read and agreed to the published version of the manuscript.

Funding: This work was supported in part by the Basic Science Research Program through the National Research Foundation of Korea (NRF) funded by the Ministry of Education (NRF-2019R1A6A1A09031717 and NRF-2019R1A2C1011297), and the US Air Force Office of Scientific Research under Grant no. FA9550-18-1-0016.

Conflicts of Interest: There is no conflict of interest.

References

1. Chua, L.O. Memristor-the missing circuit element. *IEEE Trans. Circuit Theory* **1971**, *18*, 507–519. [CrossRef]
2. Chua, L.O.; Kang, S.M. Memristive devices and systems. *Proc. IEEE* **1976**, *64*, 209–223. [CrossRef]
3. Strukov, G.; Snider, S.; Stewart, D.R.; Williams, R.S. The missing memristor found. *Nature* **2008**, *453*, 80–83. [CrossRef] [PubMed]
4. Kim, S.; Jung, S.; Kim, M.; Chen, Y.; Chang, Y.; Ryoo, K.; Cho, S.; Lee, J.; Park, B. Scaling effect on silicon nitride memristor with highly doped si substrate. *Small* **2018**, *14*, 1704062. [CrossRef]
5. Chang, Y.; Zhou, F.; Fowler, B.W.; Chen, Y.; Hsieh, C.; Guckert, L.; Swartzlander, E.E.; Lee, J.C. Memcomputing (memristor + computing) in intrinsic SiOx-based resistive switching memory: Arithmetic operations for logic applications. *IEEE Trans. Electron Devices* **2017**, *64*, 2977–2983. [CrossRef]
6. Zhou, F.; Guckert, L.; Chang, Y.; Swartzlander, E.E.; Lee, J.C. Bidirectional voltage biased implication operations using SiOx based unipolar memristors. *Appl. Phys. Lett.* **2015**, *107*, 183501. [CrossRef]
7. Kim, S.; Kim, H.; Hwang, S.; Kim, M.; Chang, Y.; Park, B. Analog synaptic behavior of a silicon nitride memristor. *ACS Appl. Mater. Interfaces* **2017**, *9*, 40420–40427. [CrossRef]
8. Mannan, Z.I.; Adhikari, S.P.; Yang, C.; Budhathoki, R.K.; Kim, H.; Chua, L. Memristive imitation of synaptic transmission and plasticity. *IEEE Trans. Neural Netw. Learn. Syst.* **2019**, *30*, 3458–3470. [CrossRef]
9. Stathopoulos, A.; Khiat, A.; Trapatseli, M.; Cortese, S.; Serb, A.; Valvo, I.; Prodromakis, T. Multibit memory operation of metal-oxide bi-layer memristors. *Sci. Rep.* **2017**, *7*, 17532. [CrossRef]
10. Ascoli, A.; Tetzlaff, R.; Chua, L.O. The First Ever Real Bistable Memristors—Part I: Theoretical Insights on Local Fading Memory. *IEEE Trans. Circuits Syst. II* **2016**, *63*, 1091–1095. [CrossRef]
11. Ascoli, A.; Tetzlaff, R.; Chua, L.O. The First Ever Real Bistable Memristors— Part II: Analysis of a Local Fading Memory. *IEEE Trans. Circuits Syst. II* **2016**, *63*, 1096–1100. [CrossRef]
12. Mannan, Z.I.; Yang, C.; Adhikari, S.P.; Kim, H. Exact analysis and physical realization of the 6-lobe Chua Corsage Memristor. *Complexity* **2018**, *2018*, 8405978. [CrossRef]
13. Mannan, Z.I.; Yang, C.; Kim, H. Oscillation with 4-lobe Chua corsage memristor. *IEEE Circuit Syst. Mag.* **2018**, *18*, 14–27. [CrossRef]
14. Mannan, Z.I.; Choi, H.; Kim, H. Chua Corsage Memristor Oscillator via Hopf Bifurcation. *Int. J. Bifurc. Chaos* **2016**, *26*, 1630009–1-28. [CrossRef]
15. Mannan, Z.I.; Choi, H.; Rajamani, V.; Kim, H.; Chua, L. Chua corsage memristor: Phase portraits, basin of attraction, and coexisting pinched hysteresis loops. *Int. J. Bifurc. Chaos* **2017**, *27*, 173001–1–36. [CrossRef]
16. Mannan, Z.I.; Adhikari, S.P.; Kim, H.; Chua, L. Global dynamics of Chua Corsage Memristor circuit family: Fixed-point loci, Hopf bifurcation, and co-existing dynamic attractors. *Nonlinear Dyn.* **2019**, in press. [CrossRef]
17. Strzelecki, R.; Zinoviev, G.S. Overview of power converters and controls. In *Power Electronics in Smart Electrical Energy Networks*; Springer Limited: London, UK, 2008; Chapter 3, Section 3.1; p. 57.
18. Chua, L. If it's pinched it's a memristor. *Semicond. Sci. Technol.* **2014**, *29*, 104001–1-42. [CrossRef]
19. Chua, L. Everything you wish to know about memristors but are afraid to ask. *Radio Eng.* **2015**, *24*, 319–368. [CrossRef]
20. Chua, L. Five non-volatile memristor enigmas solved. *Appl. Phys. A* **2018**, *124*, 1–43. [CrossRef]
21. Chua, L.O. *Introduction to Nonlinear Network Theory*; McGraw-Hill: New York, NY, USA, 1969.
22. Slotine, J.J.E.; Li, W. Advanced Stability Theory. In *Applied Nonlinear Control*; Prentice-Hall, Inc.: Englewood Cliffs, NJ, USA, 1991.
23. Mainzer, K.; Chua, L. *Local Activity Principle: The Cause of Complexity and Symmetry Breaking*; Imperial College Press: London, UK, 2013.
24. Sah, M.P.; Mannan, Z.I.; Kim, H.; Chua, L. Oscillator made of only one memristor and one battery. *Int. J. Bifurc. Chaos* **2015**, *25*, 1530010. [CrossRef]

25. Itoh, M.; Chua, L. Chaotic oscillation via edge of chaos criteria. *Int. J. Bifurc. Chaos* **2017**, *27*, 1730035. [CrossRef]
26. Kuznetsov, Y.A. Andronov: Hopf bifurcation. *Scholarpedia* **2006**, *1*, 1858. [CrossRef]
27. Strogatz, S.H. *Nonlinear Dynamics and Chaos*, 2nd ed.; Perseus Books Publishing L. L. C.: New York, NY, USA, 1994.
28. Chua, L.O.; Desoer, C.A.; Kuh, E.A. Operational-amplifier circuits. In *Linear and Nonlinear Circuits*; McGraw Hill: New York, NY, USA, 1985; Chapter 4, Section 3; pp. 187–212.
29. Kumar, S.; Strachan, J.; Williams, R. Chaotic dynamics in nanoscale NbO_2 Mott memristors for analogue computing. *Nature* **2017**, *548*, 318–321. [CrossRef]
30. Kumar, S.; Wang, Z.; Davila, N. Physical origins of current and temperature controlled negative differential resistances in NbO_2. *Nat. Commun.* **2017**, *8*, 658. [CrossRef]
31. Kim, S.; Chen, J.; Chen, Y.; Jung, S.; Kim, M.; Kim, H.; Kwon, M.; Hwang, S.; Ismail, M.; Li, Y.; et al. Neuronal dynamics in HfO_x/AlO_y-based homeothermic synaptic memristors with low-power and homogeneous resistive switching. *Nanoscale* **2019**, *11*, 237–245. [CrossRef]