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Direct Space Vector Modulation with Novel DC-Link Voltage Balancing Algorithm for Easy Software Implementation of Three-Phase Three-Level Converter

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Abstract: The present paper proposes a direct space vector modulation and novel balance algorithm for easy software application of three-level converters which operate in three-phase. In the case of the conventional space vector modulation, to get the on-state times of the switches, the dwell times of the three nearest stationary vectors, which are obtained after sector and region selection algorithms, should be rearranged. These processes, therefore, contain diverse conditional statements and complicated calculations such as inverse trigonometric functions and square roots. However, the burden of the software application of the proposed algorithm is greatly reduced by not using the sector selection algorithm, the region selection algorithm, and the on-state time allocation process as the proposed modulation can directly control the switch on-state time. In a three-level topology, it is required to balance top and bottom capacitor voltages because the DC-link voltage is composed of two capacitor voltages; the unbalanced voltage of each DC-link capacitor causes the overvoltage of the switching devices. Thus, the DC-link voltage balancing algorithm is proposed, and it is also very simple and effective without additional circuits because it controls the switch on-state time directly as well. The 5-kW prototype proved the validity of the proposed algorithm with its feasibility.

Keywords: multilevel converter; power conversion; T-type; high efficient; converter

1. Introduction

For three-phase control, space vector modulation (SVM) control is commonly used [1,2]. The SVM is useful because, at the same carrier frequency, the switching number is about 30% less and the maximum possible output voltage is 15.5% higher than the sinusoidal pulse width modulation method [3]. The current controller in the d–q frame gives the angle of desired vector and magnitude to SVM algorithm; the d–q frame is often used to regulate the reactive power and active power [4,5]. However, in this procedure, the SVM demands complex calculations such as the inverse trigonometric functions and the square root of the microprocessor [6]. Moreover, a three-level converter requires much more complex selection algorithms than a two-level converter to control through the SVM; a three-level converter has at least six sectors, each of which is separated into a chain of regions [7,8]. Furthermore, at the end of the selection algorithm, the dwell time of the vectors should be properly distributed to the switch on-state time [9].

Under the same input/output state with the same filter size, three-level converters have better power conversion efficiency, rated voltage conditions, and current total harmonic distortion (THD) compared to two-level converters [10]. However, three-level converters require two DC-link capacitors

linked in series to produce different voltage levels, unlike conventional two-level converters. Therefore, the DC-link voltage could be unbalanced, which causes overvoltage of the switching device and high THD of the grid current, so the two DC-link voltages should be controlled to be the same [11,12]. While additional circuits may solve this balancing problem, this solution increases power loss, cost, and complexity of the circuit [13–15].

In this study, the proposed algorithm and DC-link voltage balancing algorithm were validated through the T-type topology which represents the three-level converter. The proposed direct space vector modulation (DSVM) controls the switch on-state time directly without complicated calculations such as sector and region selection algorithms and on-state time allocation procedure on the software. In addition, the balancing algorithm that uses DSVM not only reduces the load of the software, but also eliminates the need for additional circuit configuration; its principle includes the direction of neutral current and its magnitude. The DC-link voltage comes into a balanced state by controlling the neutral-point-current, so the concerns about overvoltage on switching devices are reduced. The final switch on-state time is the sum of the compensated on-state time and on-state time, which is calculated from DSVM. This paper carries out the analysis of the conventional SVM and the theoretical analysis of the proposed DSVM and DC-link voltage balancing algorithms. Then, the experimental results of the 5-kW T-type topology prototype are provided to verify the validity of the proposed algorithm with its feasibility.

2. Algorithm Analysis

As shown in Figure 1, the grid voltages are e_a, e_b, and e_c; the grid currents are i_a, i_b, and i_c; and the branch voltages are v_{an}, v_{bn}, and v_{cn}. In the stationary, a–b–c frame, the voltage equations are as follows:

$$e_a = E\cos\omega t = -L\frac{di_a}{dt} + v_{an}$$
$$e_b = E\cos\left(\omega t - \frac{2}{3}\pi\right) = -L\frac{di_b}{dt} + v_{bn} \tag{1}$$
$$e_c = E\cos\left(\omega t - \frac{4}{3}\pi\right) = -L\frac{di_c}{dt} + v_{cn},$$

where E and ω are the grid voltage amplitude and the angular frequency of the grid voltage. L_a, L_b, and L_c, which are filter inductors, have the same value of inductance L. The voltage equations in (1) are transformed from a–b–c frame to d–q frame as

$$e_d = E = -L\frac{di_d}{dt} + \omega L i_q + v_d$$
$$e_q = 0 = -L\frac{di_q}{dt} - \omega L i_d + v_q, \tag{2}$$

where d-axis grid voltage and current are e_d and i_d; q-axis grid voltage and current are e_q and i_q; d-axis branch voltages is v_d; and q-axis branch voltages is v_q. By using (2), the active power P which is supplied to the grid is

$$P = \frac{3}{2}(e_d i_d + e_q i_q) = \frac{3}{2}E i_d. \tag{3}$$

i_q cannot affect the active power P of (3) because e_q is 0 in (2). Therefore, the q-axis reference grid current i_q^* should be 0 for the zero reactive power and unity power factor.

For linear control, the following equations should be satisfied:

$$v_d = E - \omega L i_q + \Delta v_d$$
$$v_q = \omega L i_d + \Delta v_q, \tag{4}$$

where the variation of *d*-axis branch voltage is Δv_d and the variation of *q*-axis branch voltage is Δv_q. They can be controlled as

$$\Delta v_d = k_{pd}(i_d^* - i_d) + k_{id}\int(i_d^* - i_d)dt$$

$$\Delta v_q = k_{pq}(i_q^* - i_q) + k_{iq}\int(i_q^* - i_q)dt, \tag{5}$$

where the proportional control gains of Δv_d is k_{pd}; the proportional control gains of Δv_q is k_{pq}; the integral control gains of Δv_d is k_{id}; and the integral control gains of Δv_q is k_{iq}. Since the current controller provides the branch voltages as (4), Equation (2) is easy to control as below:

$$-L\frac{di_d}{dt} + \Delta v_d = 0$$

$$-L\frac{di_q}{dt} + \Delta v_q = 0. \tag{6}$$

This directly controls the grid current and could improve the power quality with simple control.
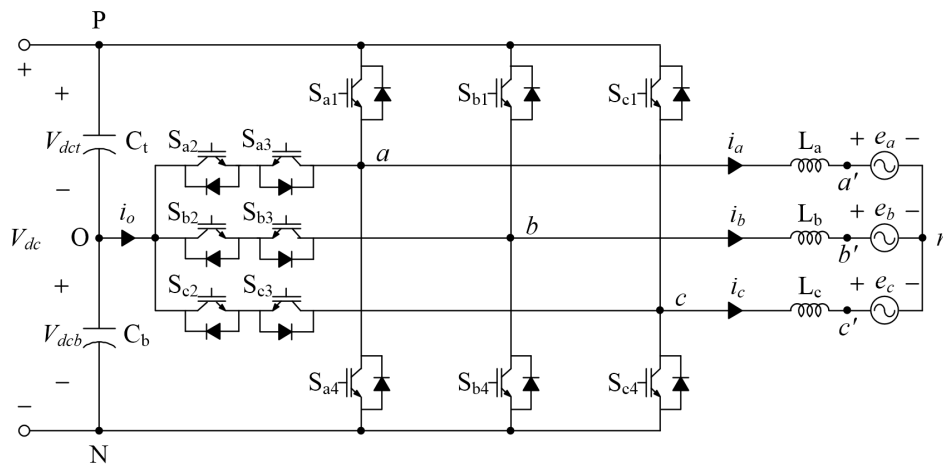

Figure 1. T-type three-phase three-level topology.

2.1. The Conventional SVM Algorithm

The conventional SVM is a switching modulation technique for the three-phase current control of converters. In this modulation, the branch voltages of (4) are considered as the desired voltage. A three-level cell has three switching states, as presented in Table 1, because S_{x2} and S_{x4} (x = a, b, c) operate in complementary relations similar to S_{x1} and S_{x3}. Thus, the three-level converter which operates in three-phase has 27 (= 3 × 3 × 3) switching states because of the three legs configuration.

Table 1. The three-level converter switching states of one leg.

Switching State	Switch Status (x = a, b, c)				Terminal Voltage (v_{xO})
	S_{x1}	S_{x2}	S_{x3}	S_{x4}	
(P)	ON	ON	OFF	OFF	$+V_{dc}/2$
(O)	OFF	ON	ON	OFF	0
(N)	OFF	OFF	ON	ON	$-V_{dc}/2$

In a complex plane, v_{an}, v_{bn}, and v_{cn}, which are three branch voltages, can be represented as a single variable by utilizing the space vector transformation. The space vector $\vec{u}(t)$ in complex plane can be expressed as

$$\vec{u}(t) = \frac{2}{3}\left(u_a(t) + u_b(t)e^{j\frac{2}{3}\pi} + u_c(t)e^{-j\frac{2}{3}\pi}\right), \tag{7}$$

where a scaling factor is $\frac{2}{3}$. Any three of time functions which fulfill $u_a(t) + u_b(t) + u_c(t) = 0$ could be expressed in two-dimensional space. Thus, 27 space vectors with 19 values of vectors ($\vec{V}_0 \sim \vec{V}_{18}$) could be drawn in complex planes, as shown in Figure 2a, and the 27 space vectors are classified into four groups: small, medium, large, and zero. In addition, in accordance with Figure 2b, the vector space can be six triangular sectors (I–VI); each triangular sector can be further divided into four triangular regions (1–4). The reference space vector $\vec{V}_{ref}$ of Figure 2b is provided from (4), and this reference space vector $\vec{V}_{ref}$ can be redefined by the three nearest stationary vectors. For example, if $\vec{V}_{ref}$ is in Region 4 of SECTOR I as in Figure 2b, $\vec{V}_2$, $\vec{V}_7$, and $\vec{V}_{14}$ are the three nearest stationary vectors:

$$\vec{V}_2 T_{nv1} + \vec{V}_7 T_{nv2} + \vec{V}_{14} T_{nv3} = \vec{V}_{ref} T_s \tag{8}$$

$$T_{nv1} + T_{nv2} + T_{nv3} = T_s, \tag{9}$$

where, in this case, the dwell times of $\vec{V}_2$, $\vec{V}_7$, and $\vec{V}_{14}$ are T_{nv1}, T_{nv2}, and T_{nv3}, respectively. The switching period is T_s. In addition, the three nearest stationary vectors $\vec{V}_2$, $\vec{V}_7$, and $\vec{V}_{14}$ are represented as

$$\vec{V}_2 = \frac{1}{3}V_{dc}e^{j\frac{1}{3}\pi} \qquad \vec{V}_7 = \frac{\sqrt{3}}{3}V_{dc}e^{j\frac{1}{6}\pi}$$

$$\vec{V}_{14} = \frac{2}{3}V_{dc}e^{j\frac{1}{3}\pi} \qquad \vec{V}_{ref} = V_{ref}e^{j\theta}, \tag{10}$$

where

$$V_{ref} = \sqrt{v_d^2 + v_q^2}, \qquad \theta = \omega t + tan^{-1}\frac{v_q}{v_d}. \tag{11}$$

After putting (10) into (8), the equation could be split into the real part and the imaginary part. Then, by utilizing (9), the dwell times are obtained as

$$T_{nv1} = T_s\left[2 - 2m_a sin\left(\frac{\pi}{3} + \theta\right)\right]$$

$$T_{nv2} = T_s\left[2m_a sin\left(\frac{\pi}{3} - \theta\right)\right] \tag{12}$$

$$T_{nv3} = T_s[2m_a sin\theta - 1],$$

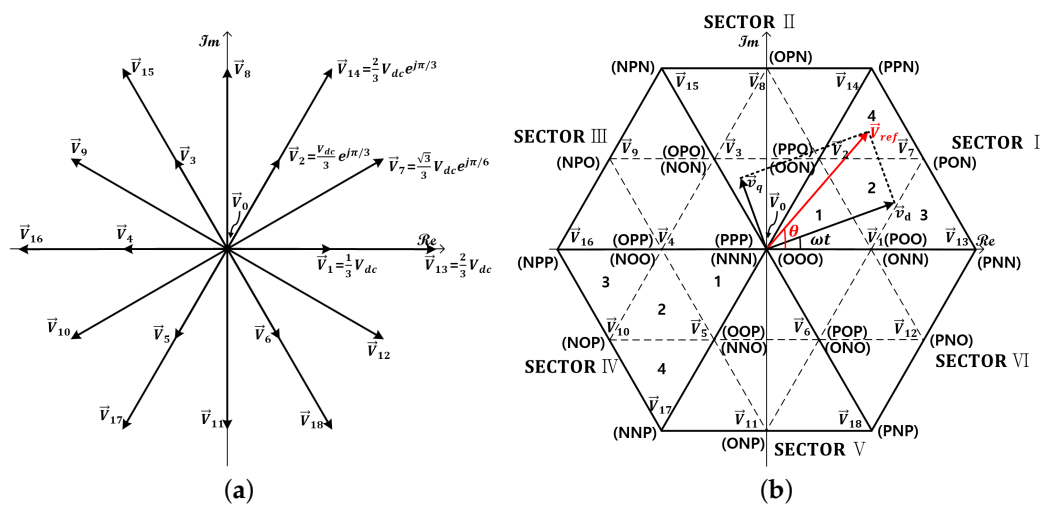where the modulation index is m_a, which is defined as

$$m_a = \sqrt{3}\frac{V_{ref}}{V_{dc}} \qquad 0 \leq m_a \leq 1. \tag{13}$$

The above processes could be repeated for each region. Consequently, Table 2 is the calculation results of the space vector dwell times for the $\vec{V}_{ref}$ in SECTOR I. For the other sectors (II–VI) of dwell times for $\vec{V}_{ref}$, the results of Table 2 can be utilized; if the integer multiple of $\pi/3$ is taken from the actual angular displacement θ, the calculation results are available because the changed angle is in between 0 and $\pi/3$.

Table 2. Space vector dwell times about $\vec{V}_{ref}$ in SECTOR I.

Region	T_{nv1}/T_s	T_{nv2}/T_s	T_{nv3}/T_s
1	$\vec{V}_0 : 1 - 2m_a sin\left(\frac{\pi}{3} + \theta\right)$	$\vec{V}_1 : 2m_a sin\left(\frac{\pi}{3} - \theta\right)$	$\vec{V}_2 : 2m_a sin\theta$
2	$\vec{V}_1 : 1 - 2m_a sin\theta$	$\vec{V}_2 : 1 - 2m_a sin\left(\frac{\pi}{3} - \theta\right)$	$\vec{V}_7 : 2m_a sin\left(\frac{\pi}{3} + \theta\right) - 1$
3	$\vec{V}_1 : 2 - 2m_a sin\left(\frac{\pi}{3} + \theta\right)$	$\vec{V}_7 : 2m_a sin\theta$	$\vec{V}_{13} : 2m_a sin\left(\frac{\pi}{3} - \theta\right) - 1$
4	$\vec{V}_2 : 2 - 2m_a sin\left(\frac{\pi}{3} + \theta\right)$	$\vec{V}_7 : 2m_a sin\left(\frac{\pi}{3} - \theta\right)$	$\vec{V}_{14} : 2m_a sin\theta - 1$

Figure 2. Vector space for the three-level converters which operate in three-phase: (**a**) space vector diagram; and (**b**) divided sectors and regions.

2.2. The Proposed DSVM Algorithm

Because S_{x2} and S_{x4} operate in complementary relations, as indicated in Section 2.1, the S_{x4} on-state time can be represented as $T_s - T_{sx2}$ where T_{sx2} is the on-state time of S_{x2} and T_{sx4} is the on-state time of S_{x4} (x = a, b, c). Thus, v_{aO}, v_{bO}, and v_{cO}, which are the terminal voltages, are represented as

$$v_{aO} = \frac{T_{sa1}}{T_s}\left(\frac{V_{dc}}{2}\right) + \frac{T_s - T_{sa2}}{T_s}\left(-\frac{V_{dc}}{2}\right)$$
$$v_{bO} = \frac{T_{sb1}}{T_s}\left(\frac{V_{dc}}{2}\right) + \frac{T_s - T_{sb2}}{T_s}\left(-\frac{V_{dc}}{2}\right) \tag{14}$$
$$v_{cO} = \frac{T_{sc1}}{T_s}\left(\frac{V_{dc}}{2}\right) + \frac{T_s - T_{sc2}}{T_s}\left(-\frac{V_{dc}}{2}\right).$$

In addition, they can be represented as

$$v_{aO} = v_{an} + v_{nO}$$
$$v_{bO} = v_{bn} + v_{nO} \tag{15}$$
$$v_{cO} = v_{cn} + v_{nO}.$$

From (15), v_{nO} is given as

$$v_{aO} + v_{bO} + v_{cO} = v_{an} + v_{bn} + v_{cn} + 3v_{nO} \tag{16}$$

$$v_{nO} = \frac{v_{aO} + v_{bO} + v_{cO}}{3} \quad (\because v_{an} + v_{bn} + v_{cn} = 0). \tag{17}$$

Therefore, from (14), (15), and (17), v_{an}, v_{bn}, and v_{cn} are arranged as

$$v_{an} = \frac{V_{dc}}{6T_s}[2(T_{sa1}+T_{sa2})-(T_{sb1}+T_{sb2})-(T_{sc1}+T_{sc2})]$$

$$v_{bn} = \frac{V_{dc}}{6T_s}[-(T_{sa1}+T_{sa2})+2(T_{sb1}+T_{sb2})-(T_{sc1}+T_{sc2})] \tag{18}$$

$$v_{cn} = \frac{V_{dc}}{6T_s}[-(T_{sa1}+T_{sa2})-(T_{sb1}+T_{sb2})+2(T_{sc1}+T_{sc2})].$$

In matrix form, (18) is arranged as

$$\begin{bmatrix} v_{an} \\ v_{bn} \\ v_{cn} \end{bmatrix} = \frac{V_{dc}}{6T_s} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \begin{bmatrix} T_{sa1} + T_{sa2} \\ T_{sb1} + T_{sb2} \\ T_{sc1} + T_{sc2} \end{bmatrix}. \tag{19}$$

As shown in Figure 2b, if $\vec{V}_{ref}$ is in Region 4, which is in SECTOR I, the three nearest vectors are $\vec{V}_2$, $\vec{V}_7$, and $\vec{V}_{14}$. In addition, because small vectors have P- and N-type, ($\vec{V}_{2P}$, $\vec{V}_7$, and $\vec{V}_{14}$), ($\vec{V}_{2N}$, $\vec{V}_7$, and $\vec{V}_{14}$), or ($\vec{V}_{2P}$, $\vec{V}_{2N}$, $\vec{V}_7$, and $\vec{V}_{14}$) can be utilized for $\vec{V}_{ref}$. If $\vec{V}_{ref}$ is computed by a P-type space vector $\vec{V}_{2P}$(PPO) with $\vec{V}_7$(PON) and $\vec{V}_{14}$(PPN), the switch on-state time and the space vector dwell time are represented as

$$\begin{bmatrix} T_{sa1} \\ T_{sa2} \\ T_{sb1} \\ T_{sb2} \\ T_{sc1} \\ T_{sc2} \end{bmatrix} = \begin{bmatrix} T_{nv1} \\ T_{nv1} \\ T_{nv1} \\ T_{nv1} \\ 0 \\ T_{nv1} \end{bmatrix} + \begin{bmatrix} T_{nv2} \\ T_{nv2} \\ 0 \\ T_{nv2} \\ 0 \\ 0 \end{bmatrix} + \begin{bmatrix} T_{nv3} \\ T_{nv3} \\ T_{nv3} \\ T_{nv3} \\ 0 \\ 0 \end{bmatrix}. \tag{20}$$

Because of $T_{sa1} = T_{sa2} = T_s$, v_{aO} is $V_{dc}/2$ from (9), (14), and (20). Therefore, from (14), $T_{sa1} + T_{sa2}$, $T_{sb1} + T_{sb2}$, $T_{sc1} + T_{sc2}$ are obtained as

$$\begin{bmatrix} T_{sa1} + T_{sa2} \\ T_{sb1} + T_{sb2} \\ T_{sc1} + T_{sc2} \end{bmatrix} = 2\begin{bmatrix} T_s \\ T_s \\ T_s \end{bmatrix} - \frac{2T_s}{V_{dc}} \begin{bmatrix} V_{dc}/2 - v_{aO} \\ V_{dc}/2 - v_{bO} \\ V_{dc}/2 - v_{cO} \end{bmatrix} \tag{21}$$

$$= 2\begin{bmatrix} T_s \\ T_s \\ T_s \end{bmatrix} - \frac{2T_s}{V_{dc}} \begin{bmatrix} v_{aO} - v_{aO} \\ v_{aO} - v_{bO} \\ v_{aO} - v_{cO} \end{bmatrix} \tag{22}$$

$$= 2\begin{bmatrix} T_s \\ T_s \\ T_s \end{bmatrix} - \frac{2T_s}{V_{dc}} \begin{bmatrix} v_{an} - v_{an} \\ v_{an} - v_{bn} \\ v_{an} - v_{cn} \end{bmatrix} \tag{23}$$

$$= 2\begin{bmatrix} T_s \\ T_s \\ T_s \end{bmatrix} - \frac{2T_s}{V_{dc}} \begin{bmatrix} v_{max} - v_{an} \\ v_{max} - v_{bn} \\ v_{max} - v_{cn} \end{bmatrix}, \tag{24}$$

where $v_{max}(=\max(v_{an}, v_{bn}, v_{cn}))$ is the maximum branch voltage; the branch voltage can be maximized by the maximum value of $T_{sx1} + T_{sx2}$ (x = a, b, c) because of (19). Thus, because of $T_{sa1} = T_{sa2} = T_s$ from (9) and (20), v_{an} is v_{max}.

If $\vec{V}_{ref}$ is computed by the N-type space vector $\vec{V}_{2N}$(OON) with $\vec{V}_7$(PON) and $\vec{V}_{14}$(PPN) instead of $\vec{V}_{2P}$(PPO), the switch on-state times and the space vector dwell time is obtained as

$$\begin{bmatrix} T_{sa1} \\ T_{sa2} \\ T_{sb1} \\ T_{sb2} \\ T_{sc1} \\ T_{sc2} \end{bmatrix} = \begin{bmatrix} 0 \\ T_{nv1} \\ 0 \\ T_{nv1} \\ 0 \\ 0 \end{bmatrix} + \begin{bmatrix} T_{nv2} \\ T_{nv2} \\ 0 \\ T_{nv2} \\ 0 \\ 0 \end{bmatrix} + \begin{bmatrix} T_{nv3} \\ T_{nv3} \\ T_{nv3} \\ T_{nv3} \\ 0 \\ 0 \end{bmatrix}. \tag{25}$$

Because of $T_{sc1} = T_{sc2} = 0$, $-V_{dc}/2$ is v_{cO} from (14) and (25). Therefore, after the same process as the above procedures of (21)–(24), $T_{sa1} + T_{sa2}$, $T_{sb1} + T_{sb2}$, and $T_{sc1} + T_{sc2}$ are represented as

$$\begin{bmatrix} T_{sa1} + T_{sa2} \\ T_{sb1} + T_{sb2} \\ T_{sc1} + T_{sc2} \end{bmatrix} = \frac{2T_s}{V_{dc}} \begin{bmatrix} v_{aO} + V_{dc}/2 \\ v_{bO} + V_{dc}/2 \\ v_{cO} + V_{dc}/2 \end{bmatrix} \tag{26}$$

$$= \frac{2T_s}{V_{dc}} \begin{bmatrix} v_{an} - v_{min} \\ v_{bn} - v_{min} \\ v_{cn} - v_{min} \end{bmatrix}, \tag{27}$$

where $v_{min}(=\min(v_{an}, v_{bn}, v_{cn}))$ is the minimum branch voltage. For the minimum deviation of the DC-link voltages, the P-type state and the N-type state in the dwell time of $\vec{V}_2$ should be equal during T_s ideally. Therefore, from (20) and (25), if $\vec{V}_{2P}$ and $\vec{V}_{2N}$ are utilized equally during T_s, the space vector dwell time and the switch on-state time are obtained as

$$\begin{bmatrix} T_{sa1} \\ T_{sa2} \\ T_{sb1} \\ T_{sb2} \\ T_{sc1} \\ T_{sc2} \end{bmatrix} = \begin{bmatrix} T_{nv1}/2 \\ T_{nv1} \\ T_{nv1}/2 \\ T_{nv1} \\ 0 \\ T_{nv1}/2 \end{bmatrix} + \begin{bmatrix} T_{nv2} \\ T_{nv2} \\ 0 \\ T_{nv2} \\ 0 \\ 0 \end{bmatrix} + \begin{bmatrix} T_{nv3} \\ T_{nv3} \\ T_{nv3} \\ T_{nv3} \\ 0 \\ 0 \end{bmatrix}. \tag{28}$$

$T_{sa1}+T_{sa2}$, $T_{sb1}+T_{sb2}$, and $T_{sc1}+T_{sc2}$, from (24) and (27), are represented as

$$\begin{bmatrix} T_{sa1} + T_{sa2} \\ T_{sb1} + T_{sb2} \\ T_{sc1} + T_{sc2} \end{bmatrix} = \begin{bmatrix} T_s \\ T_s \\ T_s \end{bmatrix} + \frac{T_s}{V_{dc}} \begin{bmatrix} v_{an} - v_{min} \\ v_{bn} - v_{min} \\ v_{cn} - v_{min} \end{bmatrix} - \frac{T_s}{V_{dc}} \begin{bmatrix} v_{max} - v_{an} \\ v_{max} - v_{bn} \\ v_{max} - v_{cn} \end{bmatrix}. \tag{29}$$

The switch on-state times are calculated as represented in Table 3 thanks to the switching characteristics of three-level in [16]. Therefore, the proposed DSVM directly provides the switch on-state times from (29) without complicated computations, i.e. square root, inverse trigonometric function, sector and region selection algorithms, and on-time allocation process. As shown in Figure 3, DSVM takes the switch on-state time more easily through the greatly simplified procedures than the conventional SVM; DSVM needs just one generalized equations, whereas many conditional statements should be included in each block diagram of the conventional SVM in Figure 3. In accordance with Table 4, there are huge differences in complexity of switching sequences for DSVM compared to other methods. Even if, in [11], the number of switching sequence is zero, each sectors has the different equations for the switch on-state time. However, in DSVM, only one generalized equation covers all

sectors, and the proposed DSVM can calculate the switch on-state time without considering of the switching sequence, sectors, and regions.

Table 3. The switch on-state time regulation.

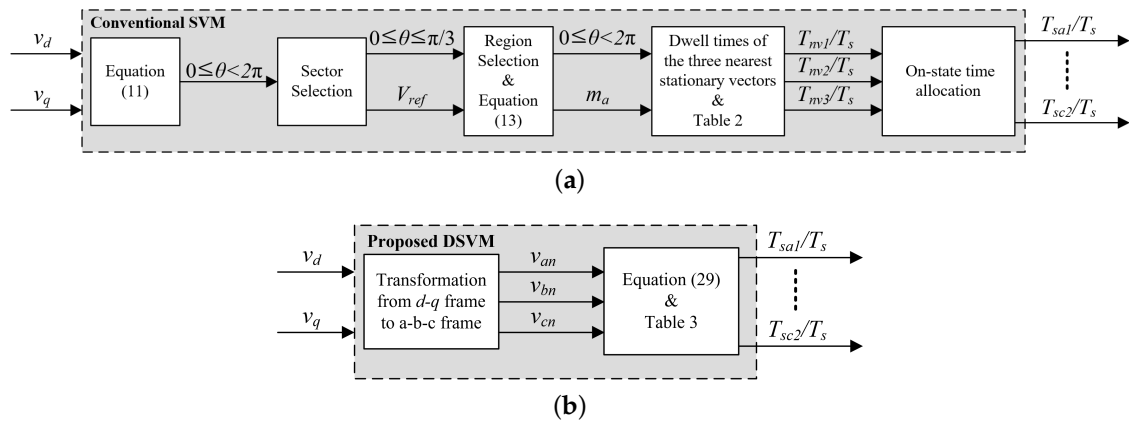| Condition | On-State Times (x = a, b, c) | |
	T_{sx1}	T_{sx2}
$T_{sx1} + T_{sx2} > T_s$	$T_{sx1} + T_{sx2} - T_s$	T_s
$T_{sx1} + T_{sx2} < T_s$	0	$T_{sx1} + T_{sx2}$

(a)

(b)

Figure 3. The block diagram after Equation (4): (**a**) the conventional SVM; and (**b**) the proposed DSVM.

Table 4. Comparison with the existing schemes and the proposed DSVM.

Ref.	The Number of Switching Sequence	The Number of Total Regions	Generalized Equations for Gate Signal
[11]	Not required	12	Each sector has different equations
[17]	25	18	Not provided
[18]	12	6	Not provided
[19]	36	36	Not provided
[20]	24	12	Not provided
[21]	36	36	Not provided
SSVM	Not required	Not required	Only one generalized equation

2.3. The Proposed Balancing Algorithm of the DC-Link Voltage

A seven-segment switching sequence is used for the three-level converter which operates in three-phase after DSVM. Its characteristics could be summarized as follows: A) T_s is composed of seven segments of the dwell times for the three stationary space vectors which are the nearest to the reference. B) The three space vectors have four switching states since the P-type state and the N-type state in the dwell time of small vectors should be equal during T_s for the minimum deviation of the DC-link voltages. C) The change to the another segment is only one leg switching state. The change in Figure 4, for example, from the (PPN) to the (PPO) is conducted by altering the *c*-terminal side leg switching state from (N) to (O). D) For the grid current THD, the segment sequences are center-aligned

and symmetric. E) The center segment, which is the P-type vector switching state, and the edge segments,, which are the N-type vector switching state, have the same dwell time.

The switching state sequence based on A)–E) for $\vec{V}_{ref}$ is shown in Figure 4. As referred to C) and E), the movement from the edge to the center make the switching states of all three legs change. Therefore, In Table 3 and Figure 4, if S_{x1} (or S_{x2}) is 1 or 0 continuously during T_s, the other switch S_{x2} (or S_{x1}) is one of T_{max}, T_{mid}, and T_{min}; T_{max} is the five centered segments period; T_{mid} is the three centered segments period; and T_{min} is the centered segment period. Thus, by utilizing E),

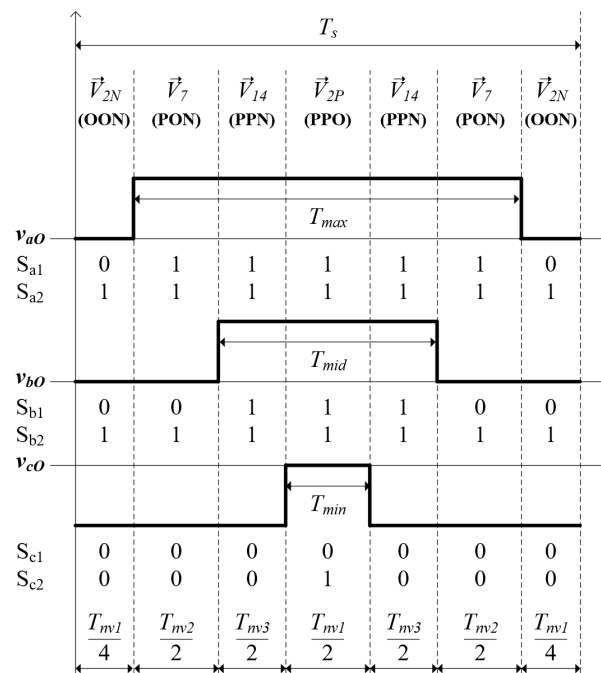$$T_s = T_{max} + T_{min}. \tag{30}$$

Figure 4. The switching state sequences of $\vec{V}_{ref}$, where 1 is the switch on-state and 0 is the switch off-state.

As shown in Figure 5, the five states of the space vectors are (PPP) of a zero vector, (POO) and (ONN) of two small vectors, (PON) of a medium vector, and (PNN) of a large vector. Although Figure 5 represents only the state of (PPP), the converter operates in zero vector $\vec{V}_0$ with (PPP), (NNN), and (OOO). In the state of (PPP), as shown in Figure 5a, the *a*, *b*, and *c* terminals are linked to the positive node of the DC-source because the all of S_{x1} and S_{x2} in three legs are turned on (x = *a*, *b*, *c*). Thus, the voltage difference between the top capacitor and the bottom capacitor maintains constant since the capacitors are linked only to the DC-source. The same is true for (OOO) and (NNN). Figure 5b shows the circuit diagram of small vector $\vec{V}_{1P}$(POO); the top capacitor voltage V_{dct} is decreased since the neutral current i_O flows in the negative direction. On the other hand, as shown in Figure 5c, the bottom capacitor voltage V_{dcb} is decreased since i_O flows out in a positive direction during (ONN) state. In other words, V_{dct} is elevated relatively if i_O flows in the positive direction, while V_{dcb} is increased relatively if i_O flows in the negative direction. Therefore, in the case of the medium vector $\vec{V}_7$(PON) in Figure 5d, the voltage variation of the DC-link capacitors depends on the direction of i_O. Since the current amount which flows through the DC-link capacitors is the same, the large vector $\vec{V}_{13}$(PNN) shown in Figure 5e does not affect voltage difference between the top capacitor and the bottom capacitor.
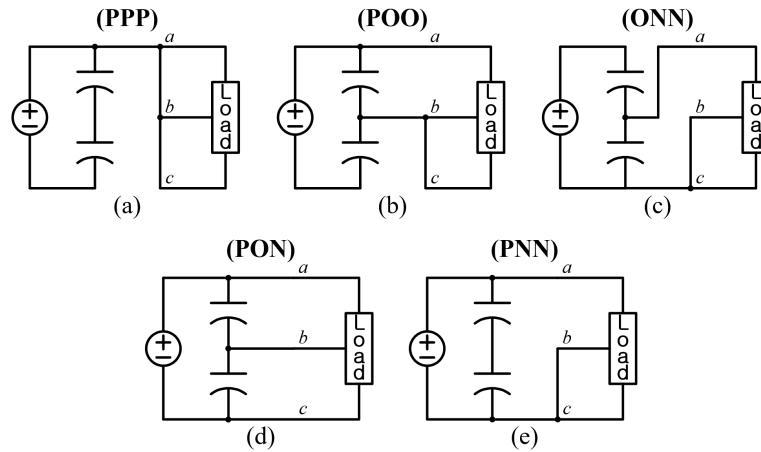
Figure 5. The switching states: (**a**) (PPP); (**b**) (POO); (**c**) (ONN); (**d**) (PON); and (**e**) (PNN).

It can be assumed that the grid current is constant during T_s because the switching frequency is far higher than the grid frequency. Therefore, $i_{O,1s} = -i_{O,4s} = i_{O,7s}$, $i_{O,3s} = i_{O,5s}$, and $i_{O,2s} = i_{O,6s}$, where the neutral current i_O of each segment sequence is sorted by $i_{O,1s}$–$i_{O,7s}$; for example, $i_{O,3s}$ is the neutral current in the third segment of the seven segments. Thus, through utilization of (30), i_O is represented as

$$i_O = \frac{i_{O,1s}(T_s - T_{max}) + i_{O,2s}(T_{max} - T_{mid})}{T_s} + \frac{i_{O,3s}(T_{mid} - T_{min}) + i_{O,4s}T_{min}}{T_s} \tag{31}$$

$$= \frac{i_{O,2s}(T_{max} - T_{mid}) + i_{O,3s}(T_{mid} - T_{min})}{T_s}. \tag{32}$$

By using Figure 4, T_{max}, T_{mid}, and T_{min} can be obtained as

$$T_{max} = T_{sa1}$$
$$T_{mid} = T_{sb1} \tag{33}$$
$$T_{min} = T_{sc2} = T_s - T_{sa1}.$$

Thus, by utilizing (32) and (33),

$$i_O = \frac{i_{O,2s}(T_{sa1} - T_{sb1})}{T_s} \neq 0, \tag{34}$$

where $i_{O,3s}$=0 because i_O is zero in Figure 5e. Thus, the compensated dwell time T_{comp} for the balancing control can be expressed as

$$T_{comp} = kV_{error} + \alpha \quad (\text{, where } V_{error} = V_{dct} - V_{dcb}), \tag{35}$$

where the proportional gain is $k(> 0)$ and the compensation value is α. If T_{comp} compensates T_{max}, T_{mid}, and T_{min} equally, (31) is reorganized as below

$$i_{O,comp} = \frac{i_{O,1s}(T_s - (T_{max} + T_{comp}))}{T_s} + \frac{i_{O,2s}((T_{max} + T_{comp}) - (T_{mid} + T_{comp}))}{T_s}$$
$$+ \frac{i_{O,3s}(T_{mid} + T_{comp}) - (T_{min} + T_{comp}))}{T_s} + \frac{i_{O,4s}(T_{min} + T_{comp})}{T_s} \tag{36}$$
$$= i_O + \frac{2i_{O,4s}T_{comp}}{T_s}.$$

To eliminate i_O term, α can be expressed as:

$$\alpha = -\frac{i_O}{2i_{O,4s}}T_s.$$ (37)

Thus, from (35)–(37), the compensated neutral current $i_{O,comp}$ is expressed as:

$$i_{O,comp} = k'V_{error},$$ (38)

where $2i_{O,4s}k/T_s$ is $k'(<0)$ and $i_{O,4s} < 0$ since the centered segment is the P-type small vector switching state from E). If, in DC-link unbalanced condition, V_{dcb} is lower than V_{dct} ($V_{error} > 0$), $i_{O,comp}$ in (38) has a negative value. Thus, since $i_{O,comp}$ has a negative value, the bottom capacitor voltage V_{dcb} relatively increases for the balance. On the other hand, if V_{dcb} is higher than V_{dct} ($V_{error} < 0$), $i_{O,comp}$ in (38) has a positive value. Therefore, the bottom capacitor voltage V_{dcb} relatively decreases for the balance DC-link condition. Consequently, the final switch on-state time is rearranged by adding T_{comp} to the existing switch on-state time as below

$$\begin{aligned} T_{min,comp} &= T_{min} + T_{comp} \\ T_{mid,comp} &= T_{mid} + T_{comp} \\ T_{max,comp} &= T_{max} + T_{comp}. \end{aligned}$$ (39)

3. Experimental Result

To demonstrate the validity of DSVM and its feasibility, grid-connected experiments were conducted using the prototype for the proposed converter in Figure 1. The parts and component values of the prototype, as shown in Figure 1, are as follows: a-, b-, and c-phase T-type module, 4MBI300VG-120R-50; current sensor, LA 55-P; capacitance of C_t and C_b, 2200 μF; and inductance of L_a, L_b, and L_c, 1 mH. The DC-link voltage V_{dc} is 360 V; the line voltage $v_{a'b'}$ is 220 V_{rms}; the grid frequency f_g is 60 Hz; and the rated power P_o is 5 kW.

Figure 6 shows the experimental results of T-type converter which operates in three-phase and utilizes the proposed control algorithms. i_a, i_b, and i_c, which are the grid currents in Figure 6a, show sinusoidal wave form with the phase difference of 120°. In addition, they provides the desired rated power of 5 kW. Each of the grid currents is controlled very well as the sinusoidal form in Figure 6a. Furthermore, to check the response time in transient condition, load variation was conducted (Figure 6b). In this experiment, the grid currents i_a, i_b and i_c were changed smoothly and quickly from 5 to 2.5 kW. As a result, those experiments completely demonstrated the validity of the proposed control algorithm and its feasibility. As represented in Figure 6c, the three-level voltage v_{ab} has five voltage levels, and the line voltage $v_{a'b'}$ is the 220 V_{rms} sine wave. To verify the proposed DC-link voltage balancing algorithm, the initial unbalancing experiment was conducted, as presented in Figure 6d, which shows the voltage of the top capacitor V_{dct} and the voltage of the bottom capacitor V_{dcb}. The V_{dct} initial condition is 240 V and the V_{dcb} initial condition is 120 V. To make the initial unbalanced DC-link state, the register linked to the circuit breaker, as shown in Figure 7b, is temporarily utilized before the operation. As shown in Figure 6d, after starting the operation of the converter, which conducts the proposed algorithm, the difference between V_{dct} and V_{dcb} has become zero. It proves that the proposed balancing algorithm gives equal distribution of two DC-link capacitor voltages. Thus, the proposed DSVM and the balancing algorithm for the three-level converter which operates in three-phase permit giving precise current control and the DC-link capacitor voltages balancing.

Pictures of experiment environment are shown in Figure 7. The prototype is evenly arranged, as represented in Figure 7a, and a plate also acts as the heatsink and support at the same time. In addition, the power circuit and control board are insulated. As shown in Figure 7b, DC power supply gives the power for the prototype, and the prototype transfers the power to the three-phase grid. To create an

initial DC-link unbalance condition, the register linked to the circuit breaker in Figure 7b is utilized temporarily before the converter operation, as shown in Figure 6d.
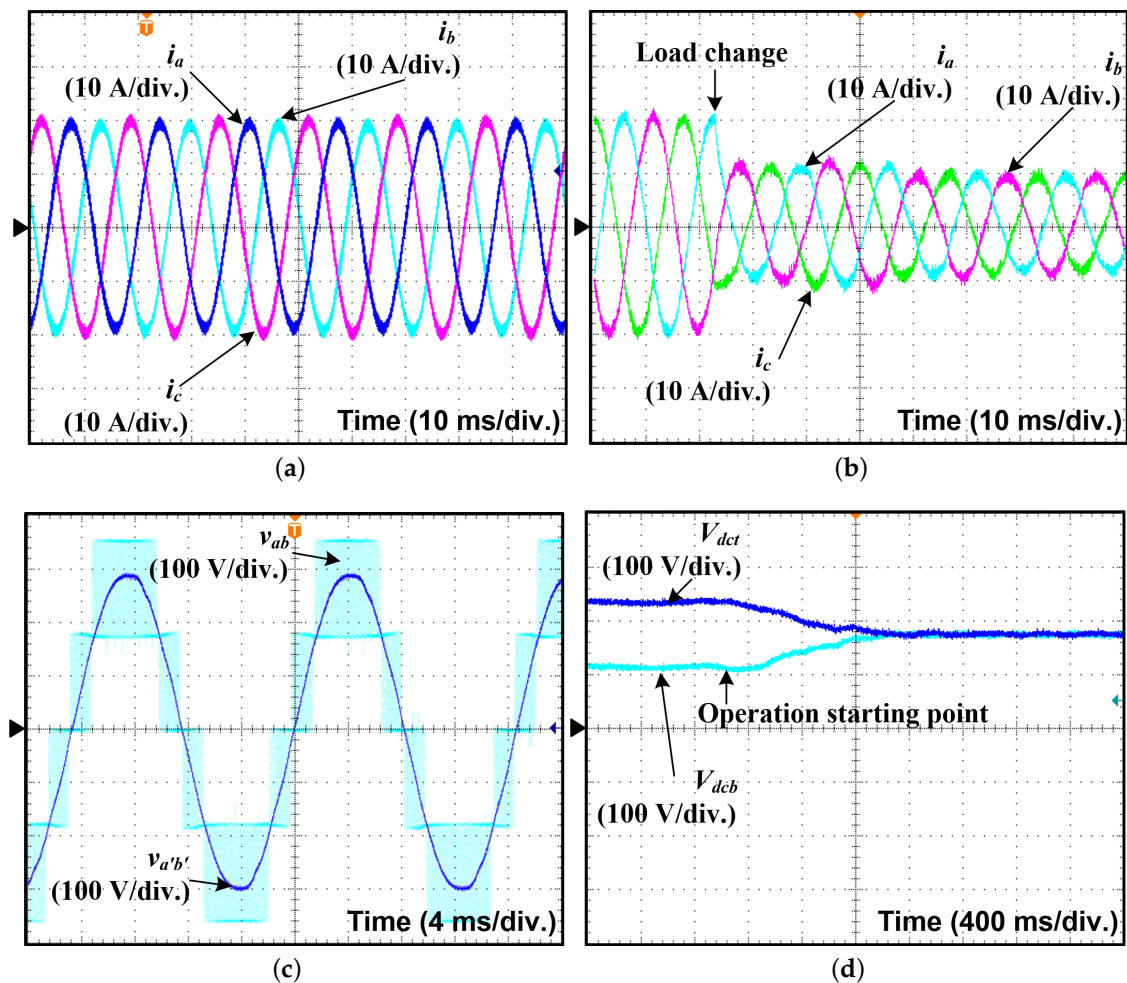

Figure 6. Experimental results: (**a**) The rated 5-kW load condition for the three grid currents i_a, i_b, and i_c; (**b**) the load changes from 5 to 2.5kW for the three grid currents i_a, i_b, and i_c; (**c**) the three-level voltage v_{ab} and the a-phase line to b-phase line voltage $v_{a'b'}$; and (**d**) the balancing algorithm operation with initial unbalanced condition.
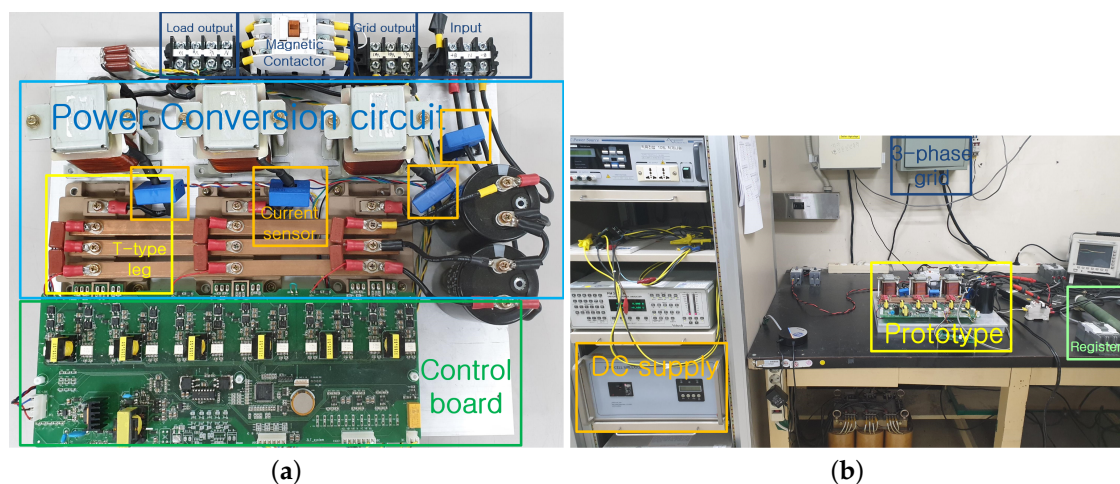

Figure 7. The pictures of experiment environment: (**a**) the prototype shown in Figure 1; and (**b**) experiment environment.

4. Conclusions

This paper proposes a direct space vector modulation and a novel DC-link voltage balance algorithm for easy software application of three-level converters which operate in three-phase. The proposed DSVM directly gives the switch on-state time without complicated computations, which are the on-state time allocation process and sector and region selection algorithms. Due to DSVM, a novel DC-link voltage balancing algorithm is also developed. The three-level converters have two divided DC-link capacitors which are linked in series. Then, it can generate the unbalanced voltages of the DC-link capacitors which is causing raised concerns about overvoltage on switching devices. In addition, the equal voltages of the DC-link capacitors linked in series can improve the current quality of the three-level converters. The proposed balancing algorithm with DSVM simply controls the DC-link voltages in equality by adjusting the neutral current and provides an effective balance control without the additional hardware and complex calculations. Therefore, the proposed DSVM and the balancing algorithm are simple to apply to three-level converters which operate in three-phase, and the experimental results thoroughly represent the validity, effectiveness, and feasibility of the proposed algorithms.

Author Contributions: J.-S.K. performed the experiments, analyzed the data, and mainly wrote the manuscript; J.-M.K. managed the project and edited the manuscript. Both the authors have read and agreed to the published version of the manuscript.

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