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An Ultra-Low Quiescent Current Under-Voltage Lockout Circuit for a High-Voltage Gate Driver IC

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Abstract: An ultra-low quiescent current under-voltage lockout (UVLO) circuit for a high-voltage gate driver integrated circuit (HVIC) is described for application in portable devices. The UVLO circuit consumes the static current in the high-side circuitry and the resistive divider used to detect the supply-voltage was the major consumer of power in the circuit. Hence, a supply-voltage sensor based on a diode-connected metal–oxide–semiconductor field-effect transistor (MOSFET) with a voltage limiter design is proposed to ensure low power consumption. Unlike the conventional UVLO design, where a resistive divider is used, the proposed structure dissipates the negligible current at a low supply-voltage and significantly reduces the static current at the nominal and high supply-voltage. The high-side quiescent current using the proposed design and the conventional designs at various supply-voltage levels are analyzed. In the proposed structure, the size of the voltage sensor is considerably smaller when compared with those in conventional designs.

Keywords: high-voltage gate driver; HVIC; supply-voltage sensing; under-voltage lockout circuit; UVLO; voltage limiter

1. Introduction

The high-voltage gate driver integrated circuits (HVICs) are gaining popularity because of the fast-growing demand for portable home appliances and tablet computers. Portable devices are powered by batteries. The boost converter generates a high-voltage signal from these batteries such as signals with voltages of 50–200 V (Figure 1). An HVIC is used to switch high-voltage signals and drive the coil or specific load conditions [1–4]. In such applications, the driver spends majority of the time in the sleep mode and wakes up occasionally for switching operations. The average power consumption of the HVICs is determined based on the sleep mode operation, which should consume very low power to achieve long battery lifetimes.

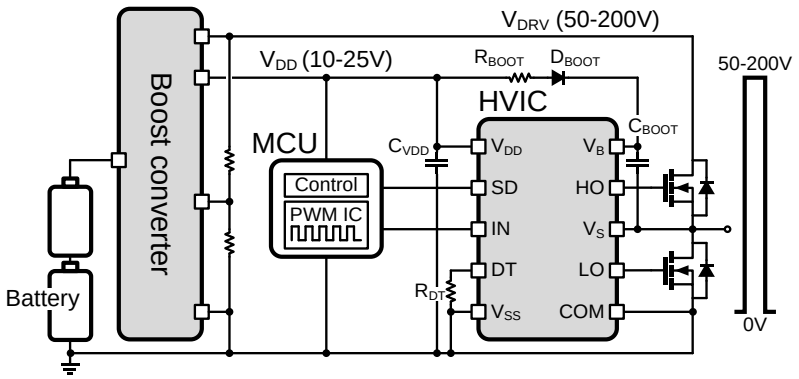


Figure 1. System block diagram of the high-voltage gate driver.

The HVIC consists of high-side circuitry, low-side circuitry, and a high-voltage level shifter (Figure 2a). To reduce the power consumption of the HVICs, a shut-down (SD) pin is added to indicate the sleep mode of an HVIC. Although the SD signal can reduce the power consumption of the low-side circuitry and high-voltage level shifter [4–7], the power consumption of the high-side circuitry cannot be decreased because the high-side region is isolated from the low-side region. Furthermore, an additional high-voltage level shifter is required to send the SD signal to the high-side region, which is undesirable from the cost perspective.

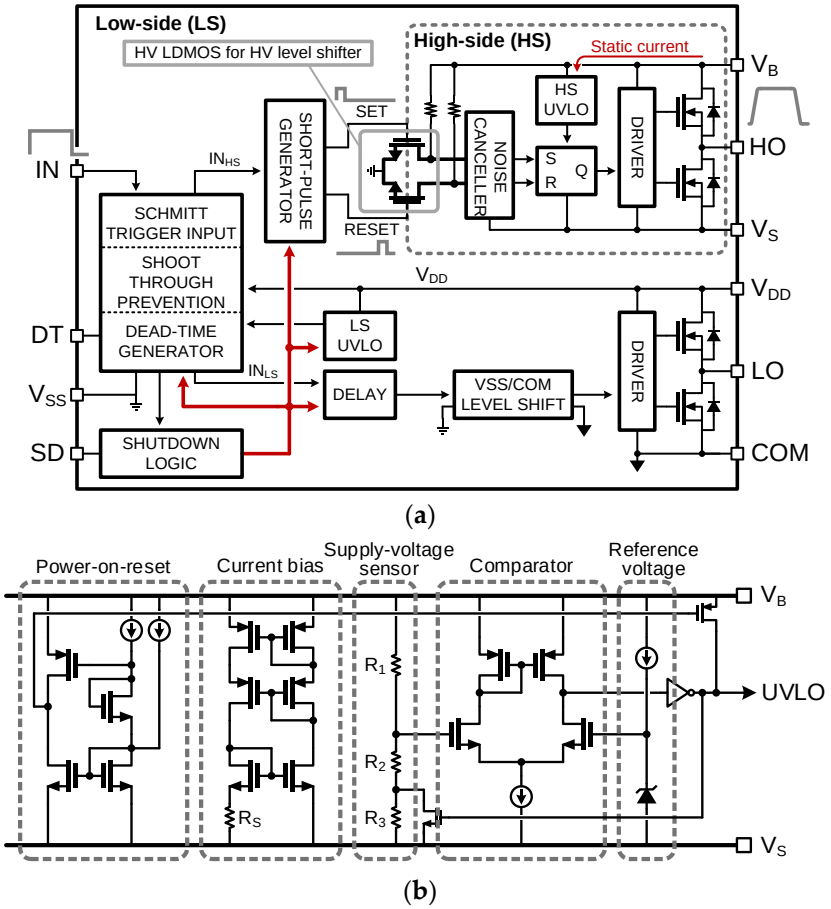


Figure 2. High-voltage gate driver. (**a**) Full block diagram. (**b**) Conventional high-side under-voltage lockout circuit.

The under-voltage lockout (UVLO) protection is an essential part of the HVIC to disable the driver at low supply-voltage and protect the device from damage [8–11]. The UVLO circuits are required for the low-side and high-side region separately since the supply-voltages of both sides are isolated from each other. Although a low-side UVLO can be fully turned off by the SD signal, a high-side UVLO still consumes the quiescent current which is a majority of the quiescent current in the high-side region [10,11]. Therefore, minimizing the power consumption of the UVLO in the high-side region is an important approach to improve the battery lifetime. Figure 2b shows the conventional UVLO structure. The power-on-reset (POR) circuit can be reconfigured as a coarse UVLO to reduce the power consumption of the UVLO [10]. The supply-voltage sensor is disconnected from the supply-voltage when the output of the POR circuit is high. Thus, the static current at a low supply-voltage can be eliminated while dissipating the same current at a nominal supply-voltage. The power consumption of the UVLO can also be reduced using a slope-based POR circuit [11]. Although the current consumption can be reduced by removing the static current in the POR circuit, only a minor improvement can be observed because the POR circuit is not a major factor associated with the UVLO power consumption.

In this paper, a low quiescent current UVLO circuit is described that can reduce the power consumption of the HVIC in the sleep mode and enhance the battery lifetime. The proposed supply-voltage sensor dissipates the negligible current at a low supply-voltage and significantly reduces the static current at the nominal and high supply-voltage. In addition, the size of the UVLO can be considerably reduced by preventing the resistive divider from detecting the supply-voltage level.

This paper is organized as follows. Section 2 describes the architecture of HVIC. Section 3 introduces the proposed low-quiescent current UVLO structure. Section 4 describes the simulation results and the conclusion follows in Section 5.

2. High-Voltage Gate Driver IC

2.1. Architecture

Figure 2a shows the full block diagram of a half-bridge type HVIC comprising a high-side and low-side gate driver. The input signal is received through the Schmitt trigger block, and the dead-time generator generates input signals for both high-side and low-side drivers with the dead-time to prevent shoot-through current between V_B and COM in the output stage [4,12]. A short-pulse generator is used to drive the high-voltage laterally diffused MOSFET (LDMOS) in the high-voltage level shifter to reduce the power consumption at the level shifter. The short-pulse generator generates the SET and RESET short pulses synchronized at the rising and falling edges of the IN_{HS} signal, respectively. The input signal can be restored from these short pulses using the SR latch in the high-side region [13–19]. However, the parasitic capacitance of the LDMOS and dV/dt arises from V_B rising, which will introduce common-mode noise in the level shifter. This noise may lead the incorrect pulses into the SR latch. Therefore, a noise canceller can be employed to remove the common-mode noise during transitions [14]. In addition, the low-side and high-side circuitries contain UVLO protection circuits to perform the switching operation at a sufficiently high supply-voltage.

2.2. Under-Voltage Lockout Circuit

In case of the high-side circuitry, the static current only flows through the high-side UVLO protection circuit. Figure 2b describes the circuit diagram of the conventional high-side UVLO [10,11]. The reference current independent of the supply-voltage (V_{BS}) is generated by the current bias circuit, and the POR circuit generates the reset pulse to prevent any latch-on state during power-up. The comparator compares the V_{BS} level with the reference voltage to ensure that the V_{BS} level is greater than the minimum operating voltage. The V_{BS} level is detected using the resistive divider and the Zener diode generates the reference voltage. The hysteresis can be added by controlling the ratio of the resistive divider. When the supply-voltage is rising, R_1 and R_2 sense the supply-voltage, while R_3 is added if the supply-voltage is falling. Hence, the positive and negative UVLO levels can be determined as follows:

$$V_{UVLO+} = V_{REF}\frac{R_1 + R_2}{R_2} \tag{1}$$

$$V_{UVLO-} = V_{REF}\frac{R_1 + R_2 + R_3}{R_2 + R_3} \tag{2}$$

where V_{REF} is the reference voltage generated by the Zener diode.

In the conventional UVLO circuit, the resistive divider always draws the static current, which is proportional to the supply-voltage. Furthermore, it is the dominant quiescent current source, especially at a high supply-voltage. The current can be reduced by increasing the size of the resistor. However, this requires a large area and increases the cost.

3. Low-Quiescent Current High-Side UVLO

An active resistor using the diode-connected MOSFET (MOS-diode) can be employed for implementing a supply-voltage sensor to reduce the current at the resistive divider (Figure 3a). The resistance of the MOS-diode can be represented as follows:

$$R_{diode} = \frac{1}{g_m} = \sqrt{\frac{1}{2k'}\frac{L}{W}I_D} \tag{3}$$

where k' is the process transconductance parameter. The resistance of the MOS-diode is controlled by adjusting the aspect ratio (W/L). Because the resistance of the smaller-sized MOS-diode is considerably greater than that of the general-purpose poly or diffusion resistor, exploiting the MOS-diode can reduce both the current consumption and size associated with the supply-voltage sensor.

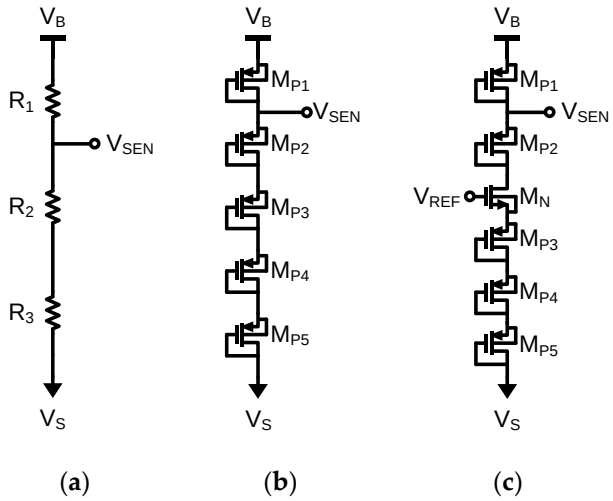


Figure 3. Supply-voltage sensor. (**a**) Resistive divider. (**b**) MOS-diode divider. (**c**) Proposed MOS-diode divider with a voltage limiter.

Figure 3b shows the supply-voltage sensor based on the MOS-diode. By assuming that same sized MOSFETs are used to implement the MOS-diode, the supply-voltage (V_{BS}) can be expressed as follows:

$$V_{BS} = nV_{GS} = n(V_T + V_{ov}) \tag{4}$$

where n is the number of stacked MOS-diode, and V_T and V_{OV} are the threshold and overdrive voltage of the MOSFET, respectively. Therefore, the current at the MOS-diode divider can be expressed as follows:

$$I_D = \frac{k'W}{2L}\left(\frac{V_{BS}}{n} - V_T\right)^2 \tag{5}$$

Unlike the typical resistive divider, the current consumption of the MOS-diode divider is proportional to the square of supply-voltage. Hence, the static current can be significantly reduced at a low supply-voltage. However, this can also result in considerably high current consumption at a high supply-voltage.

To reduce the current of the supply-voltage sensor at a high supply-voltage, a MOS-diode divider with a voltage limiter is proposed (Figure 3c). The voltage limiter is implemented by introducing an additional NMOS transistor (M_N) observed under one MOS-diode below the V_{SEN} node, and the gate voltage is connected to V_{REF}. When V_{SEN} is less than V_{REF}, M_N is fully turned on which is at the triode region and the proposed structure works the same as the MOS-diode divider structure. The resistance of M_N increases if the supply-voltage increases and $V_{GS.MN}$ decreases. Once V_{SEN} becomes greater than $V_{REF} - V_{SG.MP2} + V_{GS.MN}$, M_N enters the saturation region and limits the source

voltage of M_N. $V_{GS.MN}$ should be higher than $V_{SG.MP2}$ to ensure that M_N can limit the voltage when V_{SEN} becomes greater than V_{REF}. Even though the supply-voltage is increasing, the source voltage of M_N is maintained as $V_{SEN} - V_{GS.MN}$, and a constant current is dissipated by the supply-voltage sensor. Therefore, the proposed structure can not only reduce the current at a low supply-voltage but also prevent high current consumption at a high supply-voltage.

Figure 4 shows the proposed high-side UVLO circuit using the MOS-diode divider with a voltage limiter. The hysteresis comparator is employed to ensure the stable switching operation instead of controlling the number of MOS-diode devices in the supply-voltage sensor. Thus, the same static current can be maintained with respect to the supply-voltage sensor when V_{BS} is increased to trigger V_{UVLO+} and V_{BS} is decreased to trigger V_{UVLO-}.

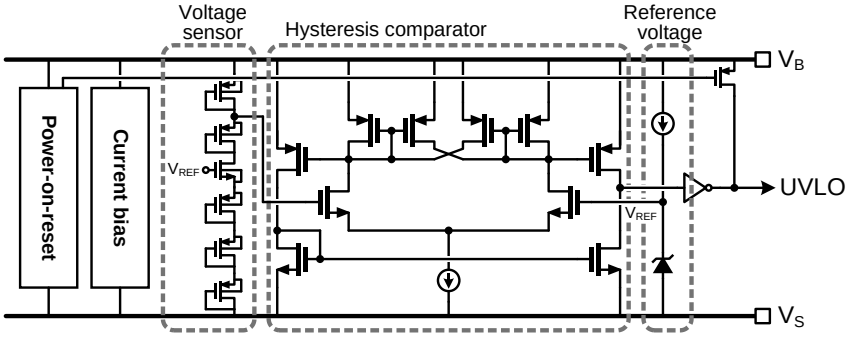


Figure 4. Proposed high-side under-voltage lockout circuit.

4. Simulation Results

A proposed UVLO is designed in 3.8 µm 25 V CMOS devices to provide the V_{BS} level up to 25 V. Cadence Spectre tool is used for the simulation. Figure 5 shows the simulated current consumption of different types of voltage sensors in high-side UVLO. The total resistance of the resistive divider is set to 650 kΩ (R_1 = 100 kΩ, R_2 = 400 kΩ, and R_3 = 150 kΩ), which is a practical value obtained by considering the tradeoff between the size and current consumption. A MOS-diode divider is designed to dissipate 1 µA at a supply-voltage of 8 V that is sufficiently fast to detect the supply-voltage through the MOS-diode structure. Although the current of the MOS-diode divider is considerably smaller than that of the resistive divider, especially at low and nominal supply-voltages, high current is consumed at a high supply-voltage because the current is proportional to the square of the supply-voltage. However, even at a high supply-voltage, the MOS-diode divider with a voltage limiter can maintain very low current consumption because the current is limited when V_{SEN} is greater than $V_{REF} - V_{SG.MP2} + V_{GS.MN}$.

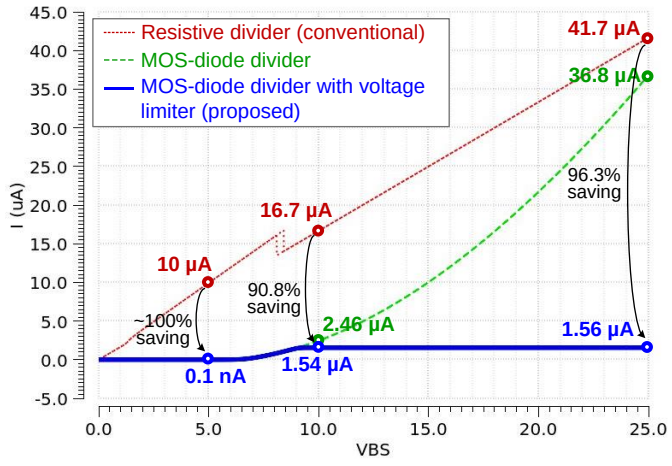


Figure 5. Current consumption of different types of supply-voltage sensors.

The size of the resistive divider is 5136 μm^2 (L = 44.9 μm, W = 4.4 μm, and mul = 26) for a given technology. The MOS-diode divider which uses 3.8 μm 25 V CMOS devices can be implemented with a size of 170 μm^2 (L × W), which is 30 times smaller than the resistive divider.

Figure 6 shows the transient response of the proposed UVLO circuit at different temperatures. The V_{UVLO+}/V_{UVLO-} levels are 8.38/7.82, 8.64/8.08, and 9.03/8.43 V at −40, 25, and 125 °C, respectively. The temperature variation is mainly caused by the reference voltage level variation from the Zener diode.

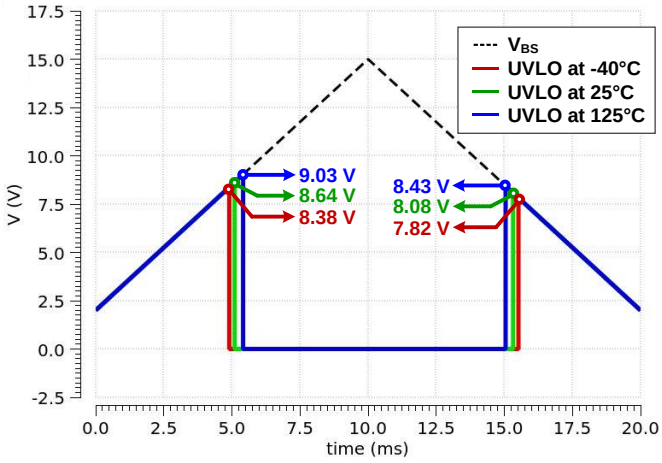
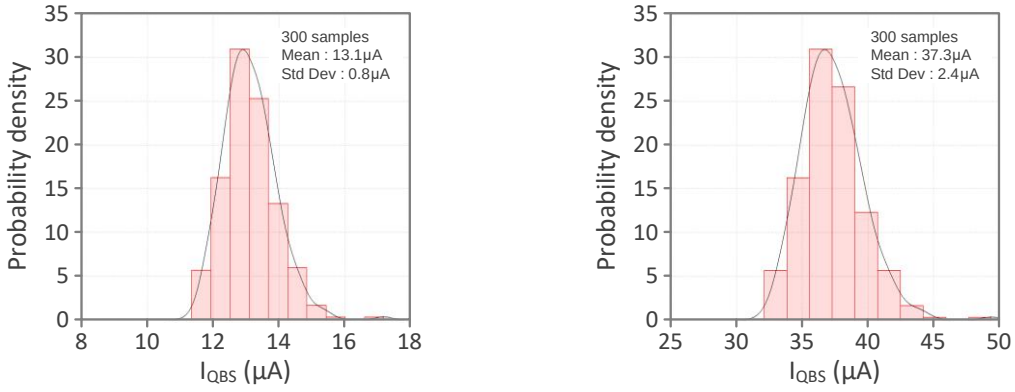


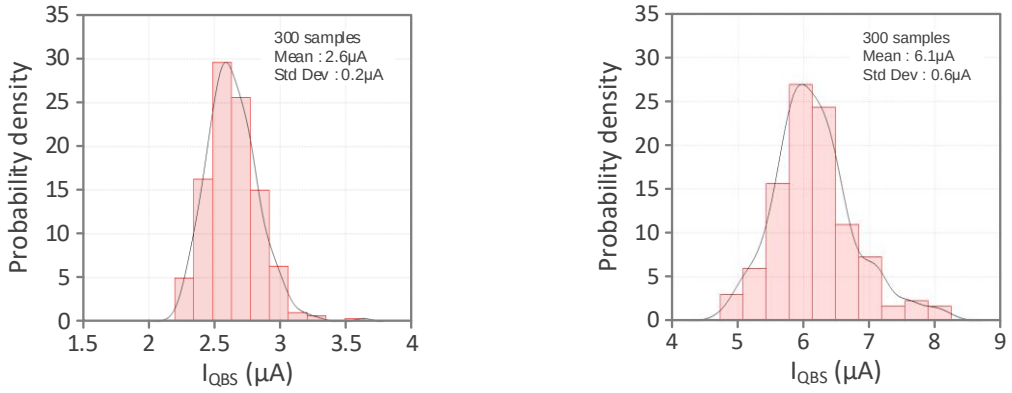
Figure 6. Proposed under-voltage lockout (UVLO) operation at different temperatures.

Figures 7 and 8 show the Monte-Carlo simulation results of the quiescent current consumption of the conventional high-side UVLO and proposed high-side UVLO, respectively. The conventional UVLO design consumes 13.1 and 37.3 μA at V_{BS} of 5 and 20 V, while the proposed UVLO design consumes 2.6 and 6.1 μA at V_{BS} of 5 and 20 V, respectively. The quiescent current can be reduced by 80.2% and 83.6% at V_{BS} of 5 and 20 V, respectively, by employing the proposed design.



(**a**) (**b**)

Figure 7. Monte-Carlo simulation results of the quiescent current consumption of conventional high-side UVLO based on the resistive divider (Figure 2b). (**a**) V_{BS} = 5 V. (**b**) V_{BS} = 20 V.



(**a**) (**b**)

Figure 8. Monte-Carlo simulation results of the quiescent current consumption of proposed high-side UVLO based on the MOS-diode divider with a voltage limiter (Figure 4). (**a**) V_{BS} = 5 V. (**b**) V_{BS} = 20 V.

Figure 9 shows the quiescent current of the high-side UVLO circuits at different supply-voltage levels for different types of supply-voltage sensors. The quiescent current consumption can be significantly reduced at low as well as high supply-voltages because of the quiescent current of the supply-voltage sensor is significantly reduced over the entire supply-voltage range by employing the proposed design.

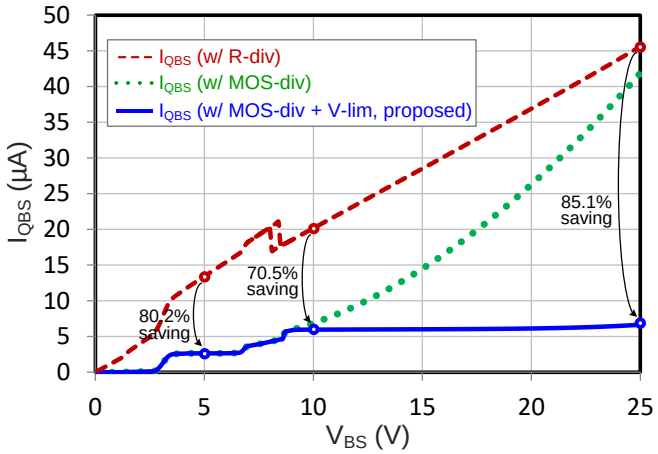


Figure 9. Quiescent current consumption of high-side UVLO circuits.

Figure 10 shows the quiescent current of the proposed structure by varying the temperature from −40 to 125 °C at V_{BS} of 5 and 20 V. Although the quiescent current of the proposed supply-voltage sensor is increased when the temperature rises, the increased amount is sufficiently small compared to total quiescent current. Moreover, the temperature coefficient of the bias current is second order compensated by applying the appropriate temperature coefficient at R_S in the current bias circuit (Figure 2b). The temperature coefficient of R_S can be adjusted by combining diffusion resistors and poly resistors that have a positive temperature coefficient and a complementary temperature coefficient, respectively. Hence the quiescent current of the proposed structure shows an almost constant value over the temperature variation.

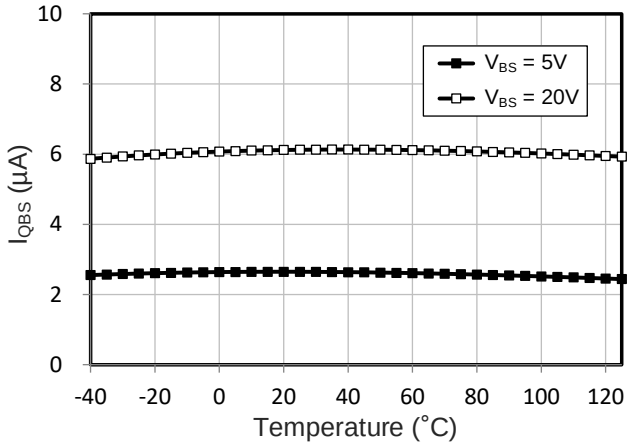


Figure 10. Quiescent current consumption of proposed high-side UVLO circuit at temperature variation.

The quiescent current of the high-side circuitry without UVLO consumes approximately 1 nA [10], which is negligible when compared with that consumed by the circuitry with UVLO. Therefore, the quiescent current of high-side UVLO can be considered as the quiescent current of high-side circuitry. Table 1 summarizes the quiescent current of proposed structure and provides a comparison with prior works that contain the high-side UVLO circuit. A considerably low quiescent current consumption can be achieved using the proposed structure by preventing the resistive divider from detecting the supply-voltage in the high-side UVLO circuit.

Table 1. Performance comparison of high-side quiescent current.

V_{BS}	[11]	[5]	[6]	[7]	This Work	
					Conventional Resistive Divider	**Proposed MOS-Diode Divider with Voltage-Limiter**
5 V	20 μA	N/A	N/A	N/A	13 μA	2.6 μA
20 V	30 μA	50 μA	80 μA	35 μA	37 μA	6.1 μA

5. Conclusions

An ultra-low quiescent current UVLO for the HVIC is described for portable devices. The proposed supply-voltage sensor based on the MOS-diode divider with a voltage limiter consumes negligible current at a low supply-voltage and significantly reduces the static current at the nominal and high supply-voltage. Therefore, the quiescent current of the proposed UVLO can be reduced over the entire supply-voltage range compared to the conventional UVLO design, where the resistive divider is used. Furthermore, the proposed structure significantly reduces the sensor size by avoiding the usage of a resistive divider.

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Conflicts of Interest: The authors declare no conflict of interest.

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