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A PWM Scheme for Five-Level H-Bridge T-Type Inverter with Switching Loss Reduction

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Abstract: In this paper, a new pulse width modulation (PWM) scheme using an offset function to reduce switching loss in the five-level H-bridge T-type inverter (5L-HBT²I) is proposed. The proposed modulation technique is implemented with a third harmonic offset voltage function. A new control voltage, that is adding the offset voltage into the initial control, is shifted to the top or bottom position of the carrier, simultaneously—where the absolute value of its load current is high or medium in comparison to other phase load currents. Due to reducing the intersection between a control voltage and the carriers, the number of switch commutations of the inverter is reduced. As a result of reducing the number of commutation count with a high current at the non-switching position, the switching losses of the inverter are decreased. Analysis and comparison of switching losses on the two-level and three-level inverters, which are components of 5L-HBT²I are presented. The power loss analysis on the 5L-HBT²I is performed. The proposed technique implements the switching loss reduction strategy based on setting the operation of the two-level inverter in six-step mode. PSIM software is used to clarify the proposed technique. The simulation results show that the total switching losses of the proposed technique in 5L-HBT²I reduce in comparison to the conventional sine PWM technique. A prototype is built to validate the proposed scheme. Simulation and experimental results match the analysis.

Keywords: carrier-based pulse width modulation; offset function; switching loss reduction; H-bridge five-level inverter; multilevel inverter

1. Introduction

Five-level inverters are power electronic converters that play important roles in applications of mechanical-electrical systems, transportation, power quality management, renewable energy conversion system, and motor drives [1–4]. In the design of five-level inverters, different topologies have been evolved, including the diode-clamped [5–9], flying capacitor [10–13], cascaded H bridge [14–16], and T type topologies [17–20]. A new single-phase five-level T-type inverter can reduce the harmonic components compared with that of the traditional full-bridge three-level PWM inverter under the same conditions of DC voltage source and switching frequency [18]. In [19] the DC-DC boost converter is connected to a five-level inverter and PI control is used, to control the inverter with much less total harmonic distortion (THD) and near unity power factor. To enhance the input voltage, three PV strings in cascade and parallel configurations with the five-level inverter are found in [19]. To maintain the power factor at near unity, the inverters in [19] and [20] use a proportional–integral (PI) current control scheme. The main solutions for the small-scale rooftop PV applications are proposed in [20]. That paper presents a comparison of four multilevel converters based on the T-type topology.

The switching loss is very important to evaluate the performance of the inverter, especially when multilevel inverter operates at a high frequency. Several studies on switching loss reduction have been introduced in recent years [21–26]. The complete analytical calculation of the switching loss is proposed in [23] for the basic inverters. The switching losses of the IGBT depend on switching frequency, load current, input DC voltage, and characteristics of switches are presented in [24]. The paper [24] shows that the total switching losses of the inverter on a control voltage period are proportional to switching frequency, load current, and DC voltage supply. The switching frequency depends on the carrier frequency and the modulation method. Note that the switching frequency is opposite to the total harmonic distortion (THD) of the output voltage. So that, lower carrier frequencies based switching loss reduction can increase THD value. Therefore, a new technique for switching loss reduction without THD increment is needed to be solved. As a result, the switching energy of the switches when the switches operate is turned on ($E_{c(on)}$) or turned off ($E_{c(off)}$) mode, are determined by current and voltage across the switch (I_C and V_{CE}) [25].

The average switching loss in the switch (P_S) during each period T_s is calculated as Equation (1) [25].

$$P_S = \frac{1}{6} \left(V_{CE} I_s \frac{t_{c(on)} + t_{c(off)}}{T_s} \right) - \frac{1}{3} \left(V_{on} I_s \frac{t_{c(on)} + t_{c(off)}}{T_s} \right) \quad (1)$$

where:

f_s —switching frequency

V_{CE} —voltage across the switch when the switch is turned off

V_{on} —voltage across the switch when the switch is turned on

I_s —current through the switch when the switch is turned on

$t_{c(on)}$ —turn-on cross-over interval

$t_{c(off)}$ —turn-off cross-over interval

From Equation (1), it can be seen that to reduce switching losses it needs to reduce switching frequency (f_s). Or for reduction switching loss, it needs to choose a switching state based on I_C and V_{CE} of phase to have the smallest value in the three-phase. As a result, f_s , I_C and V_{CE} are three basic elements that affect to reduce switching loss. A new space vector modulation strategy with two PI regulators is used in both DC voltage and load voltage sides for controlling the PWM parameters. So, the non-switching state can be controlled by these parameters to generate pulses as found in [26]. The switching losses are reduced by reducing either switching frequency or instantaneous current and voltage values at the time of switching in [26]. Since using two PI regulators, the control technique is very complex and hard to control for the system.

A reduced switching loss PWM strategy to eliminate common mode voltage in multilevel inverters is presented in [27]. This PWM method has increased switching times for the phase with the smallest load current by comparing the three-phase load current to eliminate common mode voltage. Simulation and experimental results in [27] are performed based on the standard models with the collector-emitter voltage of the IGBTs equaled. Therefore, for application to other models, which the voltage crossed IGBTs is not the same, as if the 5L-HBT²I, its effect of loss reduction may not be very high. The two modified space vector modulation strategies were proposed in [28] for the reduction of the qZSI number of switch commutations at high current level with shorter periods during the fundamental cycle, i.e., reducing the switching loss, simplifying the generation of the gate signals by utilizing only three reference signals, and achieving a single switch commutation at a time were also presented in [28].

This paper proposes a new modulation technique to reduce the number of switch commutations for switching losses reduction. There is no switching on the phase which the control voltage has the smallest displacement to top or bottom of the carrier, and the absolute of the load current being the first or second large. In addition, reducing turn on and off the switch that has a large across voltage, will be done to reduce switching losses. The paper is organized as follows: in Section 2, the topology,

operating principles, and circuit analysis of the three-phase 5L-HBT²I are presented. Section 3 presents switching loss calculation for 5L-HBT²I. Section 4 presents the proposed PWM scheme. Simulation and experimental results are shown in Section 5. Finally, the result is summarized in Section 6.

2. Three-Phase Five-Level H-Bridge T-Type Inverter Topology

Figure 1 shows the three-phase 5L-HBT²I. As shown in Figure 1a, the 5L-HBT²I consists of three DC sources (U_a, U_b, U_c), six capacitors ($C_{a1}, C_{b1}, C_{c1}, C_{a2}, C_{b2},$ and C_{c2}), and three T-type H-bridge circuits.

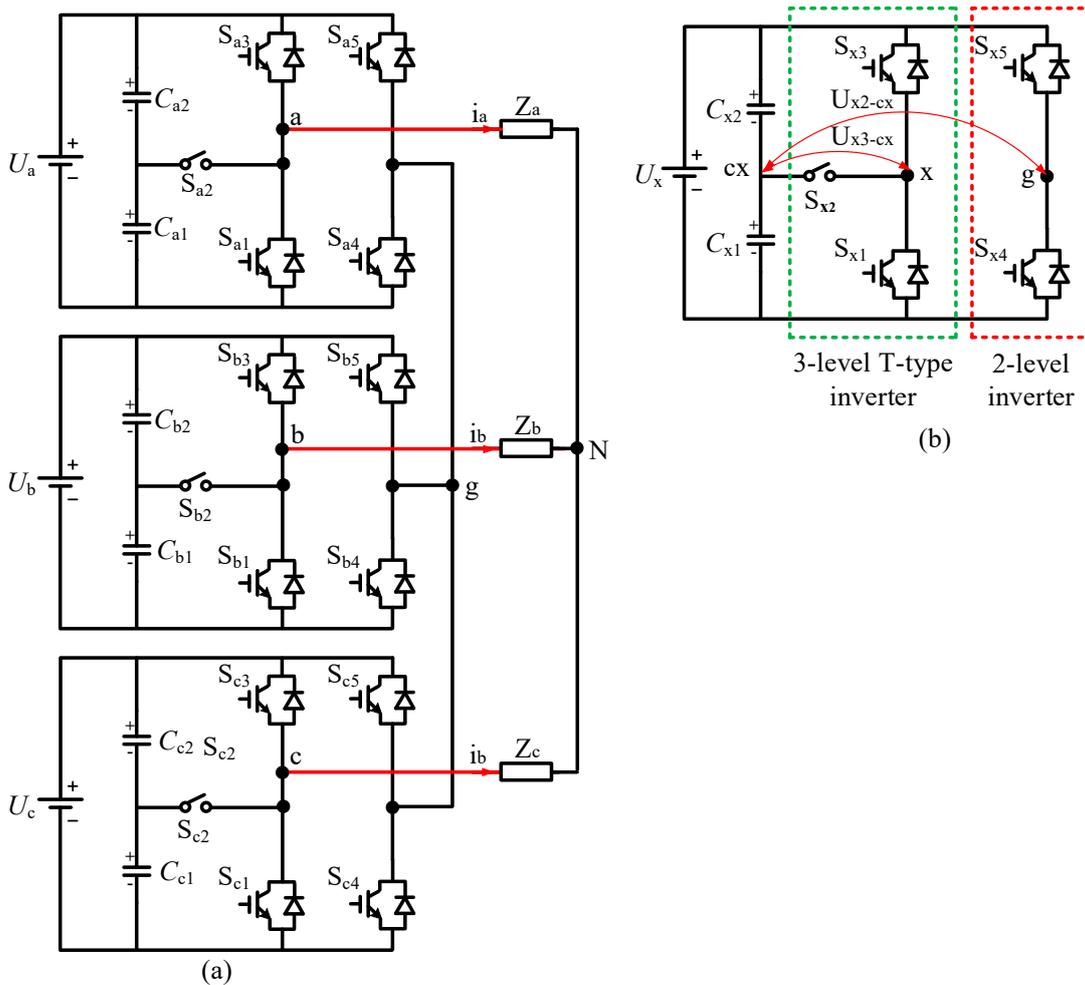


Figure 1. Five-level T-type H-bridge inverter topologies. (a) Three-phase inverter and (b) One phase module.

Define T_{Sxi} is status of the i th switch on phase x ($x = a, b, c$); where i is the index of switches (1 to 5), with conditions:

$$T_{Sxi} = \begin{cases} 0 & \text{if } S_{xi} \text{ off} \\ 1 & \text{if } S_{xi} \text{ on} \end{cases} \quad (2)$$

$$T_{Sx5} + T_{Sx4} = 1 \quad (3)$$

$$T_{Sx1} + T_{Sx2} + T_{Sx3} = 1 \quad (4)$$

Figure 1b shows a structure of phase x , where a leg of 5L-HBT²I is built from two single-phase inverters: two-level and three-level T-type.

From Equations (3) and (4), the pole voltage of two-level (U_{x2-cx}) and three-level T type inverter (U_{x3-cx}) are determined:

$$U_{x2-cx} = (2T_{Sx5} - 1) \frac{V_{dc}}{2} \tag{5}$$

$$U_{x3-cx} = (2T_{Sx3} + T_{Sx2} - 1) \frac{V_{dc}}{2} \tag{6}$$

Hence, the voltage from phase to pole (U_{xg}) is determined as

$$V_{xg} = U_{x3-cx} - U_{x2-cx} = (2T_{Sx3} + T_{Sx2} - 2T_{Sx5}) \frac{V_{dc}}{2} \tag{7}$$

Set T_{Sx} is status of phase x :

$$T_{Sx} = 2T_{Sx3} + T_{Sx2} - 2T_{Sx5} \tag{8}$$

So, the phase to pole voltages is given as Equation (9).

$$\begin{bmatrix} V_{ag} \\ V_{bg} \\ V_{cg} \end{bmatrix} = \frac{V_{dc}}{2} \begin{bmatrix} T_{Sa} \\ T_{Sb} \\ T_{Sc} \end{bmatrix} \tag{9}$$

The output phase and line-to-line voltages of this inverter is given as Equations (10) and (11).

$$\begin{bmatrix} V_{an} \\ V_{bn} \\ V_{cn} \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \begin{bmatrix} V_{ag} \\ V_{bg} \\ V_{cg} \end{bmatrix} \tag{10}$$

$$\begin{bmatrix} V_{ab} \\ V_{bc} \\ V_{ca} \end{bmatrix} = \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix} \begin{bmatrix} V_{an} \\ V_{bn} \\ V_{cn} \end{bmatrix} \tag{11}$$

As a result, the third order harmonic does not appear in the output phase voltage (V_{xn}), while it appears in both pole voltage (V_{xg}) and line-to-line voltage. Therefore, the proposed algorithm has offset the function at the third order harmonic, which will not affect the third order harmonic magnitude of the load. From Equation (8) to Equation (11), the values of V_{xg} can be determined in Table 1. As shown in Table 1, the pole voltage V_{xg} has five levels including two positive, two negative, and one zero.

Table 1. Switching state of five-level H-bridge T-type inverter (5L-HBT²I) for phase- x index.

State	T_{Sx3}	T_{Sx2}	T_{Sx1}	T_{Sx5}	T_{Sx}	V_{xg}
1	0	0	1	0	0	0
2	0	1	0	0	1	$\frac{V_{dc}}{2}$
3	1	0	0	0	2	$2\frac{V_{dc}}{2}$
4	0	0	1	1	-2	$-2\frac{V_{dc}}{2}$
5	0	1	0	1	-1	$-\frac{V_{dc}}{2}$
6	1	0	0	1	0	0

3. Switching Loss Calculation for 5L-HBT²I

The switching loss depends on the load current and collector-emitter voltage of the power switches and the number of commutations during the entire fundamental cycle [24,25]. Therefore, the switching losses of the 5L-HBT²I will be calculated based on the switching losses of the power switches of each phase, where phase x consists of five switches: S_{x1} - S_{x5} , $x = a, b, c$.

Figure 1b and Table 1 can be seen that

$$V_{CE1} = V_{CE2} = V_{CE3} = V_{CE4}/2 = V_{CE5}/2 = V_{dc}/2 \quad (12)$$

where $V_{CE,i}$ is the voltage across switch S_{xi} when S_{xi} is turned-off ($i = 1, 2, 3, 4, 5$).

And the current through switches, i_s is determined as

$$i_{si} = |i_{Lx}(\theta)| \quad \text{where } \theta \text{ is phase angle, } x = a, b, c \quad (13)$$

In Equation (13), i_{Si} and i_{Lx} are current through switch S_{xi} when S_{xi} is turned-on ($i = 1, 2, 3, 4, 5$) and the load current over phase x ($x = a, b, c$), respectively.

Hence, the average value of the local (per control voltage cycle) switching loss over switches S_{x1} – S_{x5} (for instance, for phase-a) can be calculated as [27]

$$P_{S1} = \frac{1}{2\pi}(t_{c(on)} + t_{c(off)}) \int_0^{2\pi} \left(\frac{V_{CE1}}{6} - \frac{V_{on}}{3}\right) i_{s1} d\theta = \frac{1}{2\pi}(t_{c(on)} + t_{c(off)}) \left(\frac{V_{dc}}{12} - \frac{V_{on}}{3}\right) \int_0^{2\pi} i_{s1} d\theta \quad (14)$$

Similarly, we have

$$P_{S2} = \frac{1}{2\pi}(t_{c(on)} + t_{c(off)}) \left(\frac{V_{dc}}{12} - \frac{V_{on}}{3}\right) \int_0^{2\pi} i_{s2} d\theta \quad (15)$$

$$P_{S3} = \frac{1}{2\pi}(t_{c(on)} + t_{c(off)}) \left(\frac{V_{dc}}{12} - \frac{V_{on}}{3}\right) \int_0^{2\pi} i_{s3} d\theta \quad (16)$$

$$P_{S4} = \frac{1}{2\pi}(t_{c(on)} + t_{c(off)}) \left(\frac{V_{dc}}{6} - \frac{V_{on}}{3}\right) \int_0^{2\pi} i_{s4} d\theta \quad (17)$$

$$P_{S5} = \frac{1}{2\pi}(t_{c(on)} + t_{c(off)}) \left(\frac{V_{dc}}{6} - \frac{V_{on}}{3}\right) \int_0^{2\pi} i_{s5} d\theta \quad (18)$$

where P_{Si} is an average value of the local (per carrier cycle) switching loss over the switch ($i = 1, 2, 3, 4, 5$). $V_{on,i}$ is voltage across switch S_{xi} in turned-on state.

Equations (14)–(18) can show that switching loss decreases if the switching is on the phase, which has a small load current. Due to the decrement of the number of commutations on two-level inverter switches (S_{x5} or S_{x4}), the switching loss will be smaller when compared with three-level T-type inverter switches (S_{x1} or S_{x2} or S_{x3}).

As a result, the proposed technique helps to reduce the switching loss by reducing the number of commutations on the phase, which has the absolute of the load current are first or second large in three-phase and by reducing the number of commutations on two level inverter.

4. Proposed Algorithm

4.1. Principle of the Proposed Algorithm

The switching loss depends on the current through power switches, the voltage across the switch, and the number of commutations in the period of control voltage is shown in Equations (14)–(18). Since the switching loss can be decreased by reducing switching frequency of S_{x5} and S_{x4} and reducing the number of commutations on the phase, which has the absolute of the load current is high or medium in comparison to another phase. Therefore, in the first stage, the new control voltages are determined with a non-switching state on the phase, which has the smallest displacement to top or bottom peak (of the carrier) and the absolute of the load current being the first or second largest. In addition, in the second stage, the control voltages that have been determined in the previous stage, are divided into the control voltage for the two-level inverter and three-level T-type inverter for reducing switch turn-on/turn-off on the two-level inverter.

The first stage:

It is defined that v_x is the initial control voltage phase x ($x = a, b, c$) and v_{rx} is control voltage that it is determined as the new control voltage by adding v_{offset} into v_x from first stage of proposed algorithm. The maximum amplitude of carrier is selected by 1. Due to the 5-level inverter, threshold comparison of the carrier is 0, 1, 2, 3 and 4. The initial control voltage of phase v_x is determined as Equation (19).

$$v_x = m \frac{4}{\sqrt{3}} \cos(\omega t + \theta_{0x}) + 2 \quad (19)$$

where v_x , m , ω and θ_{0x} are the initial control voltage of phase x , modulation index, angular velocity, and initial phase angle, respectively.

The error of v_x and L_x are determined:

$$L_x = \begin{cases} \text{int}(v_x) & \text{if } \text{int}(v_x) < 4 \\ \text{int}(v_x - 1) & \text{else} \end{cases}; H_x = L_x + 1 \quad (20)$$

$$e_x = v_x - L_x \quad (21)$$

Call I_{xABS} is the absolute of current across phase x , then

$$i_{xABS} = |i_{Lx}(\theta)| \quad (22)$$

where θ is phase angle, I_{Lx} is the load current of phase x ($x = a, b, c$).

The maximum, minimum, medium of error (e_{max} , e_{min} , e_{med}) and the maximum and medium of absolute of load current (I_{max} , I_{med}) are defined:

$$e_{max} = \max(e_a, e_b, e_c), e_{min} = \min(e_a, e_b, e_c), e_{med} = \text{med}(e_a, e_b, e_c) \quad (23)$$

$$i_{max} = \max(i_{aABS}, i_{bABS}, i_{cABS}), i_{med} = \text{med}(i_{aABS}, i_{bABS}, i_{cABS}) \quad (24)$$

Case 1: When the i_{xABS} is the largest and ($e_x = e_{min}$) or ($e_x = e_{max}$), the none switching phase is x and the offset voltage (v_{offset}) is determined through the value e_x as Equation (25)

$$v_{offset} = \begin{cases} -e_x & \text{if } e_x = e_{min} \\ 1 - e_x & \text{if } e_x = e_{max} \end{cases} \quad (25)$$

Case 2: When i_{aABS} is the largest and e_a equal the e_{med} , for reducing error of output voltages, the offset voltage will be not equal to e_a . In this case, another phase has the absolute of the load current as medium (assuming it is phase b) and the error (e_b) of v_b and L_b fix the maximum or minimum. Then, the offset voltage is calculated following i_{bABS} and e_b as Equation (26)

$$v_{offset} = \begin{cases} 1 - e_b & \text{if } (e_b = e_{max}) \text{ and } (i_{bABS} = i_{med}) \\ -e_b & \text{if } (e_b = e_{min}) \text{ and } (i_{bABS} = i_{med}) \end{cases} \quad (26)$$

Thus, the offset values can be determined as i_{xABS} and e_x in Table 2.

Table 2. The offset voltage of the 5L-HBT²I.

i_{aABS}	i_{bABS}	i_{cABS}	e_a	e_b	e_c	v_{offset}	Figure
i_{max}	NA	NA	e_{min}	NA	NA	$-e_{min}$	2a
i_{max}	NA	NA	e_{max}	NA	NA	$1 - e_{max}$	2b
i_{max}	i_{med}	NA	e_{med}	e_{min}	NA	$-e_{min}$	2c
i_{max}	i_{med}	NA	e_{med}	e_{max}	NA	$1 - e_{max}$	2d
i_{max}	NA	i_{med}	e_{med}	NA	e_{min}	$-e_{min}$	-
i_{max}	NA	i_{med}	e_{med}	NA	e_{max}	$1 - e_{max}$	-

NA: Not applicable.

If the matrixes from Equation (27) to Equation (31) are defined, the offset voltage will be calculated as Equation (32).

$$\begin{cases} [I_{max}] = [a_{max}, b_{max}, c_{max}] \\ x_{max} = \begin{cases} 1 & \text{if } i_{xABS} = i_{max} \\ 0 & \text{else} \end{cases} \end{cases} \quad (27)$$

$$\begin{cases} [I_{med}] = [a_{med}, b_{med}, c_{med}] \\ x_{med} = \begin{cases} 1 & \text{if } i_{xABS} = i_{med} \\ 0 & \text{else} \end{cases} \end{cases} \quad (28)$$

$$\begin{cases} [E_{max}] = [e_{amax}, e_{bmax}, e_{cmax}] \\ e_{xmax} = \begin{cases} 1 & \text{if } e_x = e_{max} \\ 0 & \text{else} \end{cases} \end{cases} \quad (29)$$

$$\begin{cases} [E_{med}] = [e_{amed}, e_{bmed}, e_{cmed}] \\ e_{xmed} = \begin{cases} 1 & \text{if } e_x = e_{med} \\ 0 & \text{else} \end{cases} \end{cases} \quad (30)$$

$$\begin{cases} [E_{min}] = [e_{amin}, e_{bmin}, e_{cmin}] \\ e_{xmin} = \begin{cases} 1 & \text{if } e_x = e_{min} \\ 0 & \text{else} \end{cases} \end{cases} \quad (31)$$

$$v_{offset} = \begin{cases} [I_{max}][E_{max}]^T(1 - e_{max}) - [I_{max}][E_{min}]^T e_{min} & \text{if } [I_{max}][E_{med}]^T = 0 \\ [I_{med}][E_{max}]^T(1 - e_{max}) - [I_{med}][E_{min}]^T e_{min} & \text{else} \end{cases} \quad (32)$$

The new control voltage v_{rx} is determined

$$v_{rx} = v_x + v_{offset} \quad (33)$$

Since matrixes $[I_{max}]$, $[I_{med}]$, $[E_{max}]$, $[E_{med}]$ and $[E_{min}]$ have “0” and “1” values, which can be determined by simple comparison commands lead to the calculation of the offset voltage easy and quick. The new control voltage (v_{rx}) is the old control voltage (v_x) add the offset voltage. The new control voltages (v_{rx}) on the phase which the absolute of the load current are first or the second large in three-phase and e_x equal e_{max} or e_{min} will be shifted to the top or bottom peak of the carrier.

Figure 2 shows the shift of the control voltages according to the conditions of the proposed algorithm. As shown in Figure 2a, when ($i_{aABS} = i_{max}$) and ($e_a = e_{min}$), the offset voltage is $-e_a$. This offset voltage is added to the original control voltages so the new control voltages will shift down to the new positions. The new position of the control voltage of phase-a will be L_a . Therefore, there will be no switching on the phase-a when ($i_{aABS} = i_{max}$) and ($e_a = e_{min}$) as shown in Figure 2b. Similarly, the switching state on the phase-b is off if ($I_{aABS} \geq I_{bABS} \geq I_{cABS}$), ($e_a = e_{med}$) and ($e_b = e_{min}$ or e_{max}), as shown in Figure 2c or 2d.

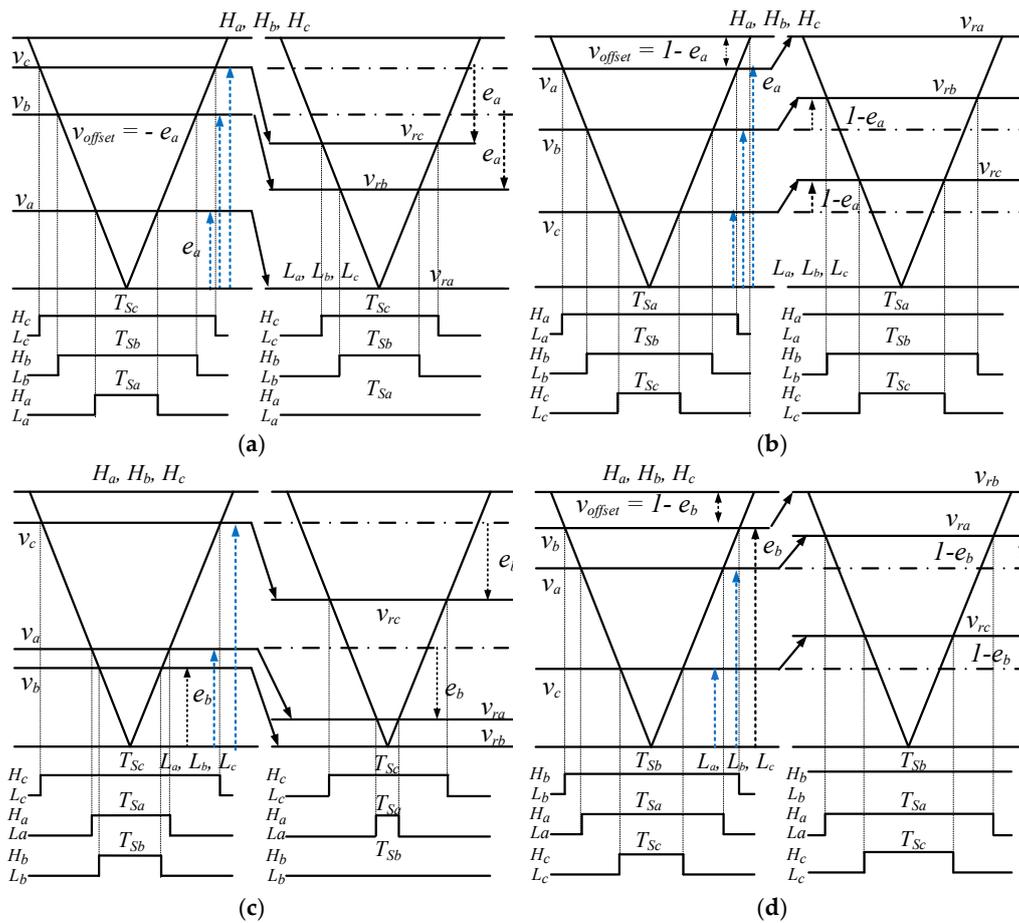


Figure 2. Offset voltages under the proposed algorithm. (a) ($i_{aABS} = i_{max}$) and ($e_a = e_{min}$); (b) ($i_{aABS} = i_{max}$) and ($e_a = e_{max}$); (c) ($i_{aABS} \geq i_{bABS} \geq i_{cABS}$), ($e_a = e_{med}$) and ($e_b = e_{min}$); (d) ($i_{aABS} \geq i_{bABS} \geq i_{cABS}$), ($e_a = e_{med}$) and ($e_b = e_{max}$).

The second stage:

In the second stage, the control voltages that were created in the previous stage will be divided into the control voltage for the two-level inverter and three-level T-type inverter. Since the two-level inverter is operated in six-step mode, its control voltage can be calculated as

$$v_{x,2l} = \begin{cases} 1 & \text{if } v_{rx} \geq 2 \\ 0 & \text{else} \end{cases} \quad (34)$$

In addition, from Equation (7), it is easy to determine the control voltages for three-level T type, which are:

$$v_{x,3l} = v_{rx} - 2v_{x,2l} \quad (35)$$

where v_{rx} is the control voltage, created from first stage; $v_{x,2l}$ and $v_{x,3l}$ are the control voltages for two-level inverter and T-type inverter on phase x .

4.2. Flow Chart

Figure 3 shows a flow chart of the proposed algorithm using simple commands such as subtraction, and comparison on the program. The comparison of the phase currents can be done by comparing hardware circuits that do not require the use of expensive sensors. Thus, calculation time of the algorithm is low and suitable for closed-loop control or other control methods.

For example, assuming that control voltages $v_a, v_b,$ and v_c are 1.12 V, 0.64 V and 3.24 V, respectively, from Equation (22), the error of v_x and L_x are $e_a = 0.12, e_b = 0.64,$ and $e_c = 0.24$. From Equation (24), $e_{min} = 0.12, e_{max} = 0.64, e_{mid} = 0.24$.

Assuming that $I_{aABS} > I_{bABS} > I_{cABS}$, from Equations (27) and (28), $[I_{max}] = [1\ 0\ 0], [I_{mid}] = [0\ 1\ 0]$. From Equations (30)–(32), $[E_{max}] = [0\ 1\ 0], [E_{med}] = [0\ 0\ 1], [E_{min}] = [1\ 0\ 0]$. From Equations (22)–(32), the offset voltage is $v_{offset} = -e_{min} = -0.12$. Then, new control voltages are $v_{ra} = v_a - e_{min} = 1\text{ V}, v_{rb} = v_b - e_{min} = 0.52\text{ V}, v_{rc} = v_c - e_{min} = 3.12\text{ V}$.

When $v_{ra} = 1\text{ V}$, switches $S_1, S_3,$ and S_5 are turned off while switches S_2 and S_4 are turned on. Thus, the phase-a switches will not be switched in one cycle T . Similarly, when $v_{rc} = 3.12\text{ V}$, $S_1, S_3,$ and S_4 are turned off while S_2 and S_5 are switching. As a result, the phase-c switches will be switched in one cycle T . Therefore, the proposed algorithm can reduce the switching times of the switches.

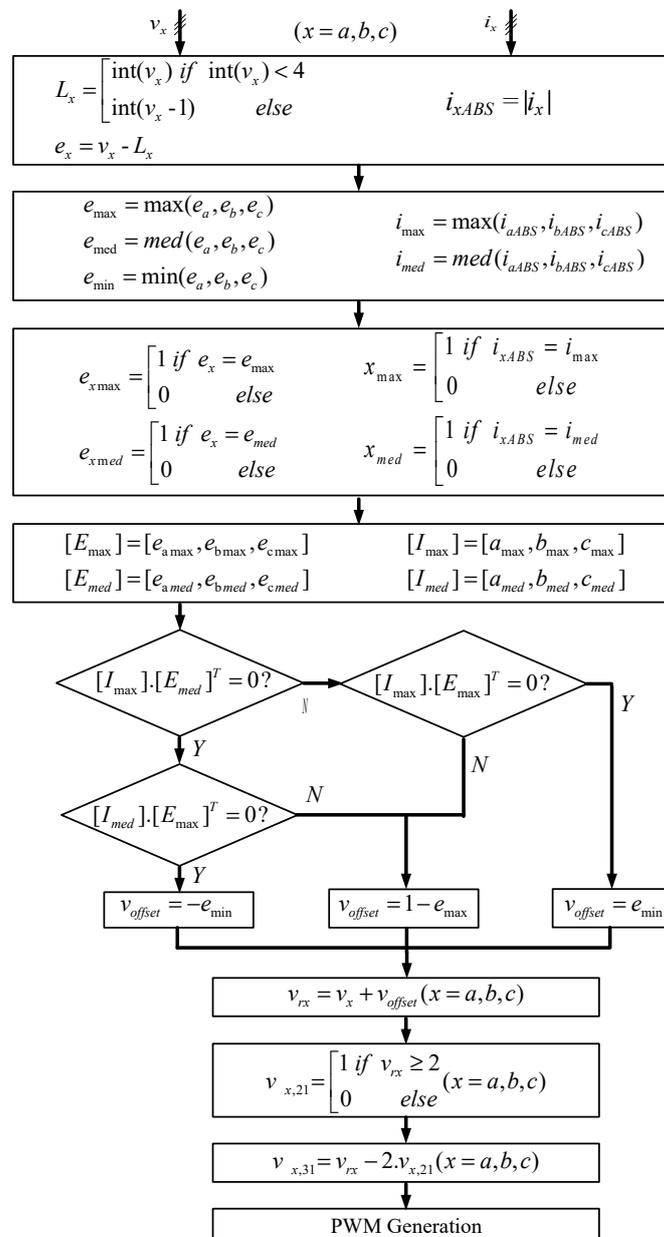


Figure 3. The flow chart of the proposed scheme.

5. Simulation and Experimental Results

5.1. Simulation Results

Parameters used in simulation is shown in Table 3. Figure 4 shows the simulation results of the proposed algorithm when modulation index are 0.4 and 0.9, respectively. The waveforms from top to bottom in Figure 4 are three-phase absolute current, three-phase error (e_a, e_b, e_c), maximum and minimum errors (e_{max} and e_{min}), the initial voltage (v_x) and new control voltage (V_{rx}), control voltage of two-level inverter (v_{a2L}), and control voltage of three-level T-type inverter (v_{a3L}), the next waveforms are gating signals of S_{x1} to S_{x5} and the bottom is the pole voltage output. It can be seen that from t_1 to t_2 , i_{aABS} is maximum and e_a hit maximum (e_{max}), then v_{offset} will be $1 - e_a$ lead to the control voltage of phase a move up to 3V; see Figure 4a and obtain 4V; see Figure 4b. As shown in Figure 4a, during a time interval of $[t_1$ to $t_2]$, the control phase-a voltage is 4 V. As a result, the switching states on phase-a are ($S_{5a} = 0, S_{4a} = 1, S_{3a} = 1, S_{2a} = 0$ and $S_{1a} = 0$) and its phase pole voltage is $V_{ag} = V_{dc} = 100$ V. Similarly, in Figure 4b, the phase-a to pole voltage is $V_{ag} = \frac{V_{dc}}{2} = 50$ V when ($S_{5a} = 0, S_{4a} = 1, S_{3a} = 0, S_{2a} = 1$ and $S_{1a} = 0$). From t_3 to t_4 , i_{bABS} is maximum, the e_b is medium. Simultaneously, the absolute of phase a current load (i_{aABS}) is medium and e_a is e_{min} as analyzed in the above section, the offset voltage is $-e_a$ and the new control voltage of phase a shift down 0 V ($m = 0.9$) and 1 V ($m = 0.4$), so there is no switching in phase-a. Similarly, the phase-b and phase-c in the situation have no switching.

Table 3. Parameters used in simulation.

Parameter/Component		Attributes
Input voltage	V_{dc}	100 V
Output frequency	f_o	50 Hz
Carrier frequency	f_s	5 kHz, 10 kHz, 15 kHz and 20 kHz
Capacitors	$C_1 = C_2$	47,000 μ F/300 V
Three-phase RL load	R_{load} and L_{load}	40 Ω and 10 mH

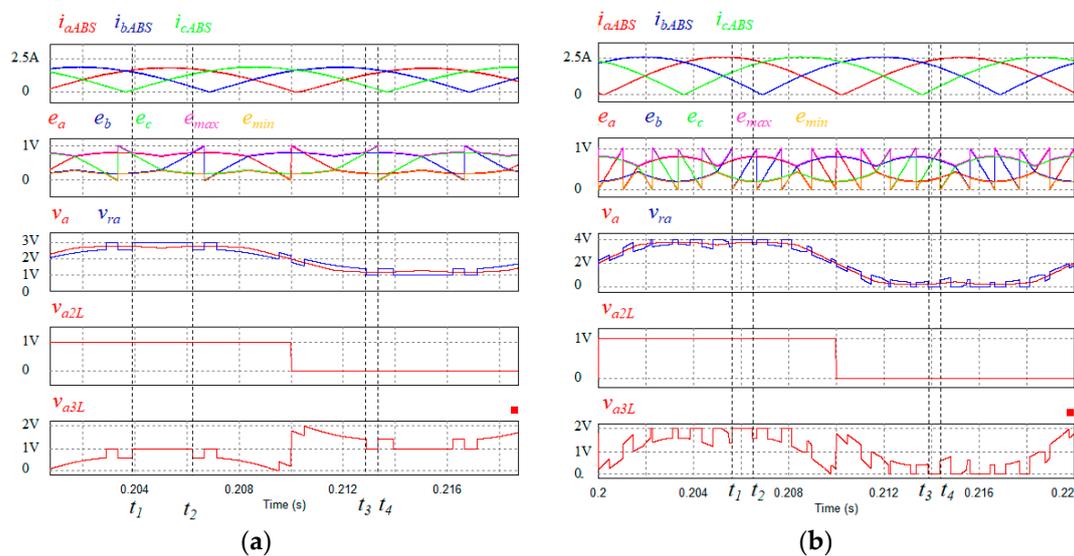


Figure 4. Cont.

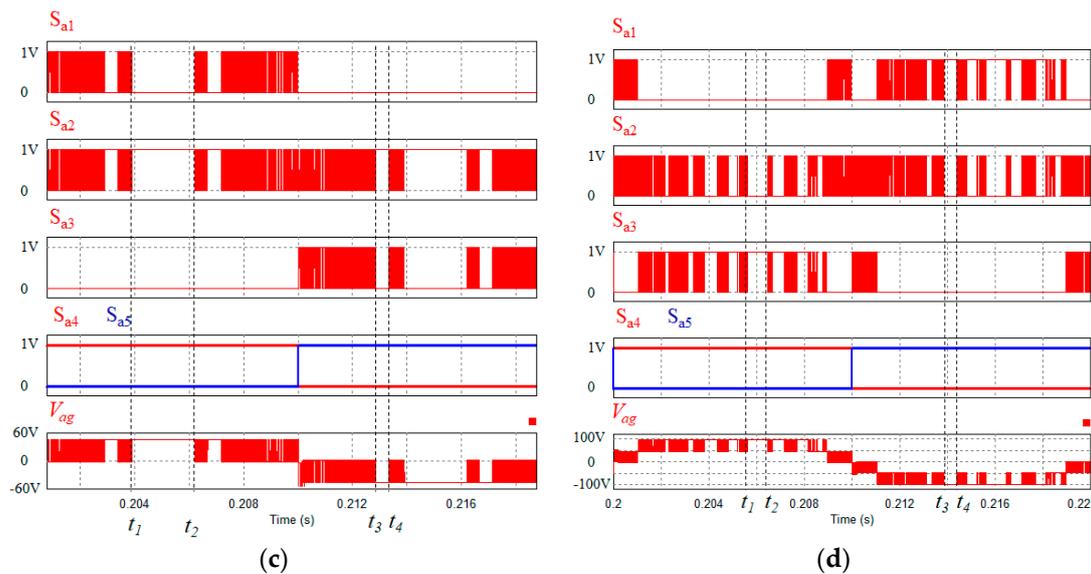


Figure 4. Control voltage generation, gating signals of S_{a1} to S_{a5} and the phase pole voltage in the proposed technique with (a,c) $m = 0.4$ and (b,d) $m = 0.9$.

To evaluate the efficiency of switching loss reduction, IGBT CM1000HA-24H module (Mitsubishi Electric., Tokyo, Japan) in PSIM’s device database is used in the simulation. Figure 5 shows the conduction loss (P_c -sinPWM), switching loss (P_s -sinPWM) using sine PWM algorithm and conduction loss (P_c -proposed), switching loss (P_s -proposed) using the proposed algorithm on a phase on changing carrier frequency. As a result, the proposed technique can reduce switching losses. The switching loss reduction value is maximized when $m = 0.5$, equivalent to 78% reduction. There is no significant difference in conduction loss (P_c) between the proposed algorithm and sinPWM algorithm, especially at low carrier frequencies. The difference in conduction loss is due to the difference in the high harmonic amplitude between the proposed algorithm and sinPWM algorithm. When the carrier frequency is not high enough (e.g., at $f_c = 5$ kHz), the load phase voltage that applies the proposed technique has the high harmonic amplitude at some modulation index values. Therefore, the conduction loss in this case is greater than that in the sinPWM method as in Figure 5c,d. The harmonics spectrum of the proposed and sinPWM algorithms are presented in Figure 6. The harmonics with a large amplitude in the proposed technique focus around the carrier frequency, while they are around twice the carrier frequency in the sinPWM algorithm. The THD of the phase current in the two algorithms is slightly different, as seen in Figure 7.

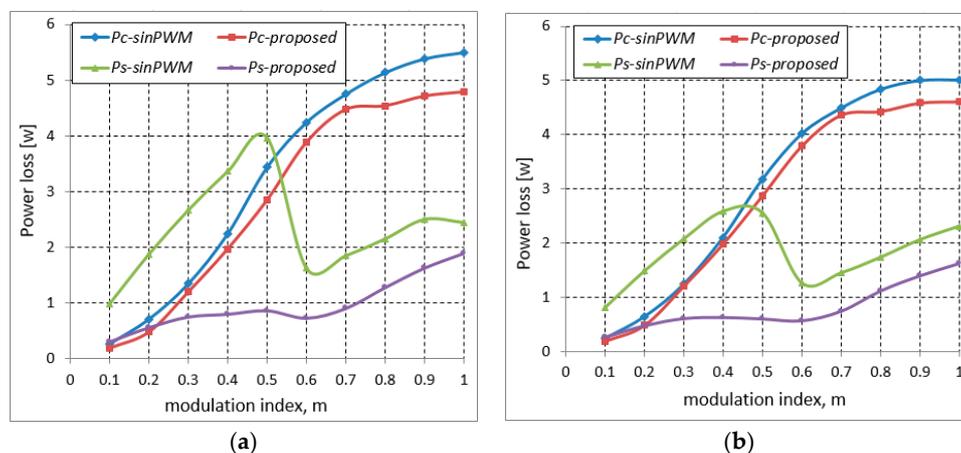


Figure 5. Cont.

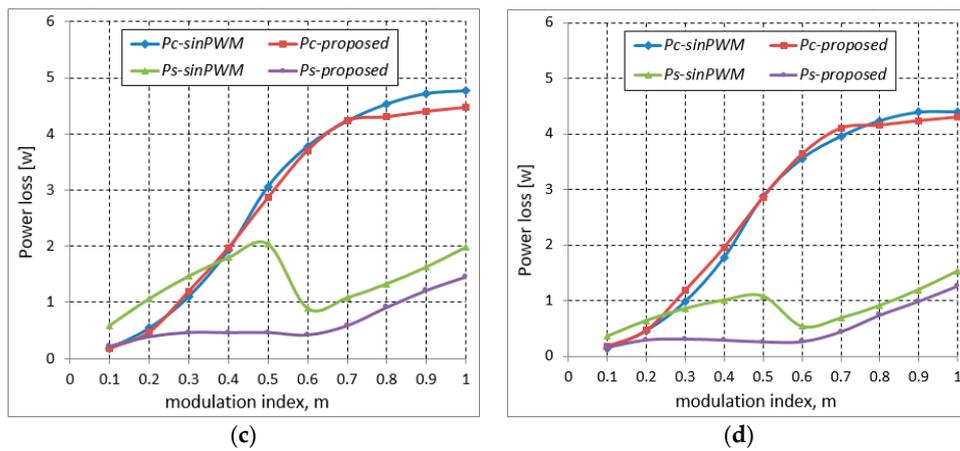


Figure 5. Power loss on a phase under sinPWM method and proposed algorithm at carrier frequency of (a) 20 kHz, (b) 15 kHz, (c) 10 kHz, and (d) 5 kHz.

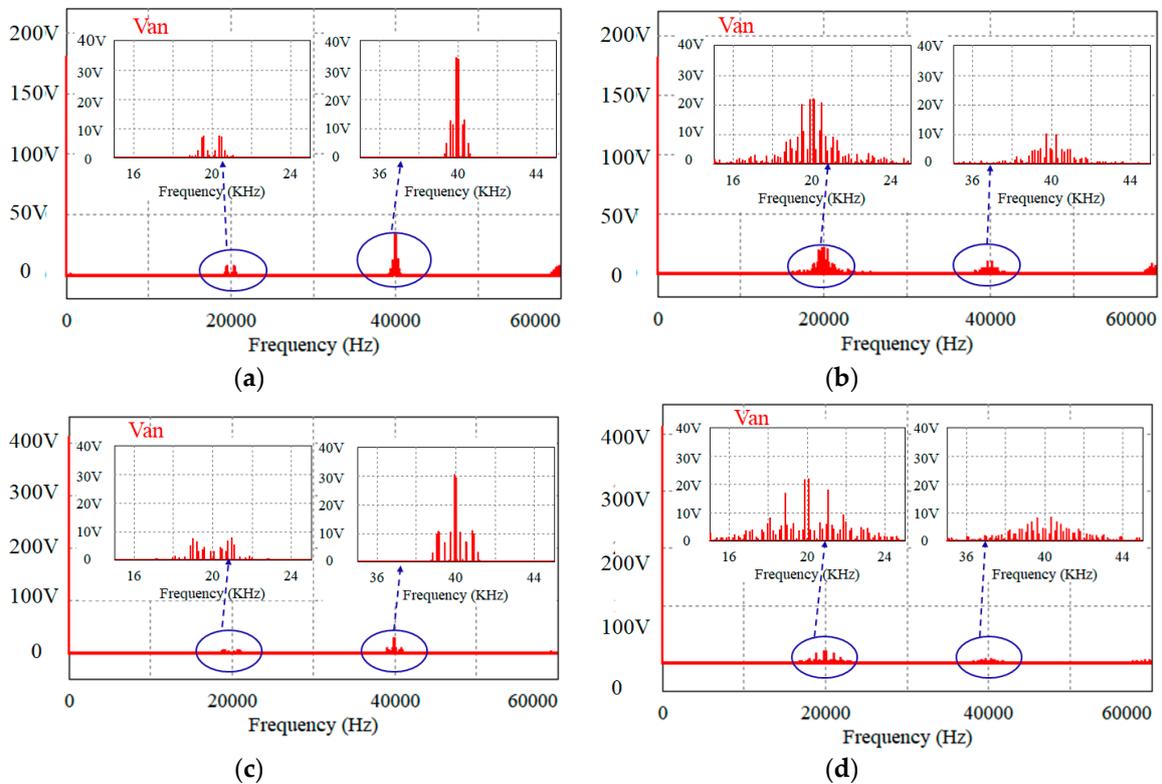


Figure 6. Harmonics spectrum of phase voltage at $f_s = 20$ kHz using (a) sinPWM method with $m = 0.4$, (b) proposed method with $m = 0.4$, (c) sinPWM method with $m = 0.9$, and (d) proposed method with $m = 0.9$.

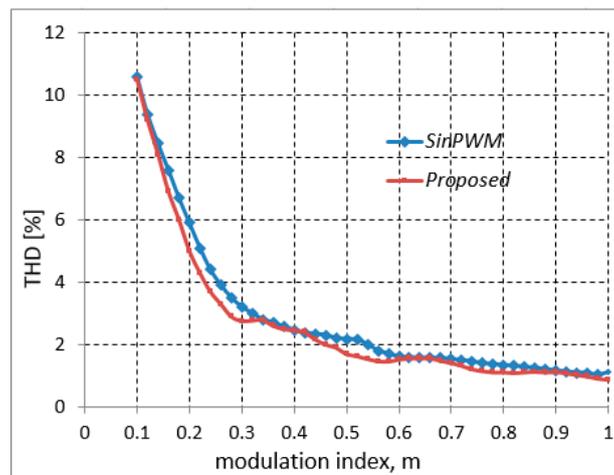


Figure 7. Total harmonic distortion (THD) comparison between sinPWM method and proposed technique at $f_s = 20$ kHz.

Figure 7 shows a comparison of THD values of the phase current between sinPWM method and the proposed technique. As shown in Figure 7, THD value of the phase voltage of 5L-HBT²I under the proposed algorithm is smaller than that with the sinPWM method at $f_c = 20$ kHz. This can explain that the two-level inverter only operates in a six-step mode with rarely rapid changes of phase voltage on this inverter. As a result, the output harmonics have a small amplitude and conductive losses are also lower than sinPWM techniques, as shown in Figure 5.

Under the load of 40Ω and 10 mH at the output frequency of 50 Hz, the calculated load power factor is 0.997 . Table 4 shows the power factor (PF) and the power factor displacement (PFD) in simulation. As shown in Table 4, the simulated power factor of the inverter is lower than the calculated load power factor of 0.997 . This is due to the harmonics distortion of load current and voltage.

Table 4. Simulated power factor and power factor displacement.

m	THDi	THDu	PFDi	PFDu	PF
0.4	2.45%	40%	0.997	0.928	0.9264
0.9	1.12%	17%	0.999	0.986	0.9826

5.2. Experimental Results

An experimental model based on the DSP TMS320F28335 microcontroller (Texas Instruments, Dallas, TX, US) is built in the laboratory to verify the effectiveness of the proposed control technique with the elements in Table 5. Figure 8 shows a laboratory prototype. The input voltage is 100 V. The output frequency is 50 Hz, while the switching frequency of the inverter circuit is 5 kHz. A three-phase inductive load of 40Ω and 10 mH is used in the experiment.

Table 5. Elements used in experiment.

Elements	Type
IGBT	FGL40N150D
Current sensor	LEM-LA 25-P
Microcontroller	DSP TMS320F28335
Tektronix oscilloscope	MSO 2024B

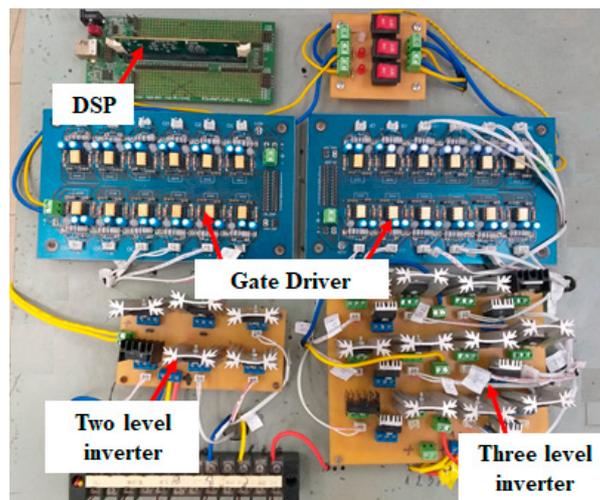


Figure 8. Experimental setup of the prototype.

Figure 9 shows the experimental result of the proposed algorithm when $m = 0.9$ and $m = 0.4$. In Figure 9, the waveforms from the top to the bottom are the gating control signals of the power switches S_{A5} , S_{A3} , S_{A2} and S_{A1} , the pole voltage (V_{ag}), the phase voltage that its harmonic spectrum is in Figure 10. The experimental result of the proposed algorithm in Figure 9 are under modulation index $m = 0.4$ (Figure 9a) and $m = 0.9$ (Figure 9b).

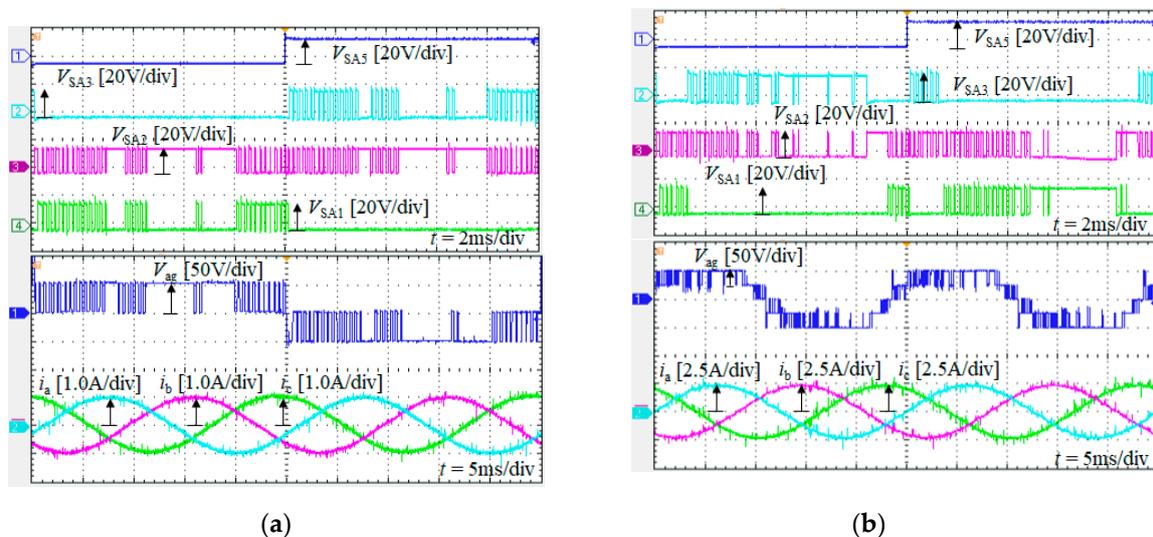


Figure 9. Experimental results at (a) $m = 0.4$ and (b) $m = 0.9$.

The experimental results are close to the simulation results. Figure 9a,b show the position “no switching” in the phase, which has the absolute of its load current hitting maximum or medium in three phases. The gating signal of S_{A5} is similar to that of S_{A4} , that is the switch of the two-level inverter. This is similar to its waveform in the six-steps mode.

Figure 10 shows the experimental results of the load current fast Fourier transform (FFT) and its THD at $m = 0.4$ and 0.9 . The experimental results are close to the simulation results. As shown in Figure 10, the THD of the load current with the proposed algorithm at $m = 0.4$ is bigger it at $m = 0.9$. Since the THD of the load current under the proposed algorithm is smaller than 5%, this complies in the standard IEC61000-4-30 Edition 2 Class A. The experimental results in Figure 10 show that the amplitude of lower harmonics is very small. That is one of the advantages of the proposed technique. The measured THD values in Figure 10 are close to the simulation results shown in Figure 7.

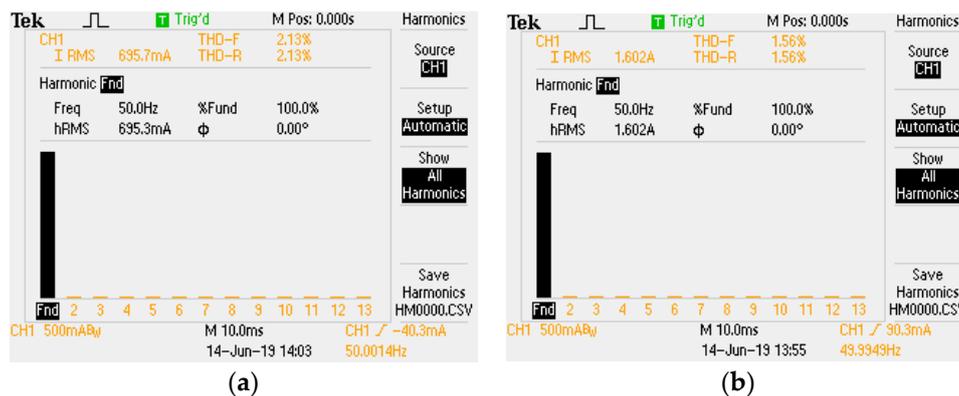


Figure 10. The load current fast Fourier transform (FFT) and its THD. (a) $m = 0.4$ and (b) $m = 0.9$.

6. Conclusions

The paper presents the carrier based PWM algorithm for 5L-HBT²I by using the offset function to reduce the number of commutations on the power switches. Since the phase leg switches are reduced, the number of commutations at maximum phase current are absolute, the two-level inverter in 5L-HBT²I is on six-step mode, and the switching losses of the inverter 5L-HBT²I are reduced under the proposed algorithm. The switching loss reduction value, in the proposed algorithm for 5L-HBT²I, is maximized when $m = 0.5$, that is equivalent to a reduction of 78%. Since there is no increase conductive loss when applying the proposed algorithm on 5L-HBT²I, the power loss of the inverter is also reduced. Due to no increase of THD, this algorithm not only reduces the number of commutations but also hits ME standards as IEC61000-4-30 Edition 2 Class A at small modulation indexes [28].

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Conflicts of Interest: The authors declare no conflict of interest.

Nomenclature

5L-HBT ² I	Five-level H-bridge T-type inverter
f_s	Switching frequency
NA	Not applicable
Pc-sinPWM	Conduction loss using sine PWM
Pc-proposed	Conduction loss using proposed
PI	Proportional integral
Ps-proposed	Switching loss using proposed
Ps-sinPWM	Switching loss using sine PWM
PV	Photovoltaic
PWM	Pulse width modulation

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