electronics

MDPI

Article

Heavy-Ion Induced Single Event Upsets in Advanced 65 nm Radiation Hardened FPGAs

Chang Cai [1,3], Xue Fan [2,*], Jie Liu [1], Dongqing Li [1,3], Tianqi Liu [1,3,*], Lingyun Ke [1,3], Peixiong Zhao [1,3] and Ze He [1,3]

[1] Institute of Modern Physics, Chinese Academy of Sciences, Lanzhou 730000, China; caichang@impcas.ac.cn (C.C.); j.liu@impcas.ac.cn (J.L.); lidongqing@impcas.ac.cn (D.L.); kelingyun@impcas.ac.cn (L.K.); zhaopeix16@impcas.ac.cn (P.Z.); heze17@mails.ucas.ac.cn (Z.H.)

[2] Chengdu Technological University, Chengdu 611730, China

[3] University of Chinese Academy of Sciences, Beijing 100049, China

* Correspondence: x_fan@foxmail.com (X.F.); liutianqi@impcas.ac.cn (T.L.)

Received: 14 January 2019; Accepted: 12 March 2019; Published: 14 March 2019

Abstract: The 65 nm Static Random Access Memory (SRAM) based Field Programmable Gate Array (FPGA) was designed and manufactured, which employed tradeoff radiation hardening techniques in Configuration RAMs (CRAMs), Embedded RAMs (EBRAMs) and flip-flops. This radiation hardened circuits include large-spacing interlock CRAM cells, area saving debugging logics, the redundant flip-flops cells, and error mitigated 6-T EBRAMs. Heavy ion irradiation test result indicates that the hardened CRAMs had a high linear energy transfer threshold of upset ~18 MeV/(mg/cm^2) with an extremely low saturation cross-section of 6.5 $\times$ 10^{-13} cm^2/bit, and 71% of the upsets were single-bit upsets. The combinational use of triple modular redundancy and check code could decline ~86.5% upset errors. Creme tools were used to predict the CRAM upset rate, which was merely 8.46 $\times$ 10^{-15}/bit/day for the worst radiation environment. The effectiveness of radiation tolerance has been verified by the irradiation and prediction results.

Keywords: FPGA; radiation hardening; single event upsets; heavy ions; error rates

1. Introduction

Static Random Access Memory (SRAM) based Field Programmable Gate Array (FPGA) possesses plenty of flexible configuration switches and logics to implement million-gate circuits with a very short development time [1,2], which makes it a valuable Integrated Circuit (IC) for an electronic system. However, the Complementary Metal Oxide Semiconductor (CMOS) based architectures in SRAM-FPGA are very sensitive to radiation effects, which reduces the on-orbit safety and reliability [3–9]. Therefore, it is necessary to evaluate and mitigate the Single Event Effects (SEEs) of SRAM-based FPGAs for potential space applications. Although there have been some radiation hardened SRAM-based FPGAs such as XQVR300 (220 nm) and XQR4VSX55 (90 nm) employed for space mission, a fast system scrubbing is still required to reduce the on-orbit risks [7].

There are several radiation hardening techniques such as Error Correct Code (ECC), Triple Modular Redundancy (TMR) and Dual Interlocked storage Cell (DICE) that can be used in FPGAs, but they are area or power consuming and less effective when the Multiple Bit Upset (MBU) phenomenon occurs frequently [2]. Besides, different circuit blocks in an FPGA have different functions and importance. Hence, hardening technique selection is a tradeoff strategy among function, performance, area and radiation tolerance. For example, errors occurring in Configuration RAMs (CRAMs), which control the routing, the switches and the logic state of an FPGA, have the most critical impact on the FPGA function, and so that the radiation tolerance of CRAMs has to be high, although it costs non-negligible area and

power [8–11]. Other resources, e.g. Embedded RAMs (EBRAMs) and registers, can be hardened with a proper combination of several soft error mitigation methods which cost less area and power.

For planar bulk Si CMOS technologies, the operation voltages decrease and frequencies increase with the feature size scaling down, which make CMOS logic circuits, including FPGAs, more sensitive to SEU [12,13] and contribute more complex and diverse upsets phenomenon happening in cosmic rays and solar flare environments [8,10,11]. In most cases, the complexity of SEUs also affect the effectiveness of hardening designs, especially in million-gate deep submicron FPGA. For commercial FPGAs, in [11–13], the significant SEU sensitivities appear, even under low Linear Energy Transfer (LET) heavy-ion radiation. Therefore, more hardening techniques are applied in the deep submicron FPGAs than the submicron hardened FPGAs. As reported in [8], three reasonable radiation hardened 90 nm Xilinx FPGAs using several radiation hardening techniques presented superior performances and radiation tolerance, which are very representative products for space application. Thus, the implementation of reasonable hardening strategies for advanced FPGAs as well as the calculation of FPGAs' convincible error rates in space are extremely necessary and feasible [11,14].

In this paper, a radiation-hardened SRAM-based FPGA was designed and manufactured on a 65 nm CMOS process as the Device Under Test (DUT). This device employed a preferable tradeoff radiation hardening strategy by realizing an effective combination of direct layout reinforcement and error mitigation oriented bitstream configuration design. The basic information about the DUTs is introduced in Section 2. SEE experiments under heavy-ion irradiation were implemented, and experimental details and results are described in Section 3. In Section 4, an effective forecast of the space upset rates is calculated thoroughly. Finally, a deep discussion based on the design purposes and further prediction analysis is explicated.

2. DUT Introduction

2.1. DUT Parameters

The DUT (die area: 1.8 cm × 1.3 cm) was fabricated with a 65 nm bulk silicon epitaxial CMOS process (as the classical 65 nm commercial foundry) with ten metal layers. It was flip-chip packaged in a Ball Grid Array (BGA) type. The ∼700 µm silicon substrate was thinned down to 40 µm, which is less than the range of each experimental heavy ion.

The picture of the developed device in the 8-inch wafer is shown in Figure 1a and the whole view of chip's layout is shown in Figure 1b. The DUT contained 600 programmable I/O blocks located in banks. The ∼20 Mbit CRAM were used to control the routes and switch boxes. The ∼8 Mbit embedded block memories were organized and distributed in DUT. Besides, The ∼170 Kbit Debugging Logics (DLs) in circuits were also included to test the actual function of devices by capturing read back signals. Apart from the different architecture and resource distributions, the most essential improvement in the DUT is the combined usage of 8-T and DICE structures in the layout design (programmable modules in Figure 1b).

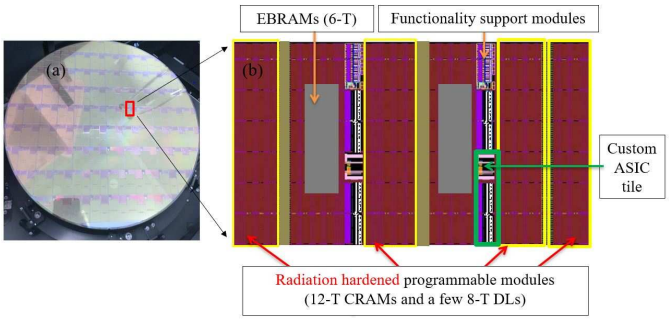

Figure 1. The developed device: (**a**) the 8-inch wafer of designed DUT; and (**b**) the layout and architecture of DUT.

2.2. Radiation Hardening Design

Three kinds of layout hardness techniques were designed in CRAMs, DLs and D flip-flops (DFFs) and the configuration hardness methods were mainly added to EBRAM by Prosice (a self-developed FPGA configuration software). Each DFF was reinforced by double redundant cells. For CRAM, it occupied majority of chip area, and all of them were reinforced by DICE structure (as shown in Figure 2) with large spacing to insulate single-ion charge sharing effect, although the DICE hardened cell had ∼2 times area and power cost. Another 8-T structure (as shown in Figure 3) was designed in DL cells to keep the accuracy of read back signals by adding two more anti-disturbance transistors. 8-T cell, which was used to replace the standard 6-T cell, consumed less area.

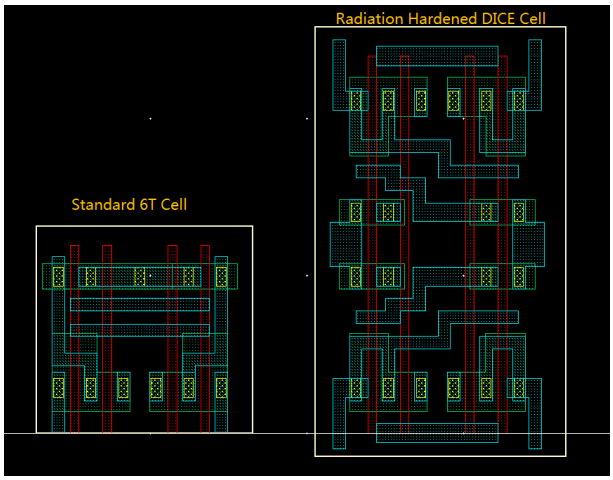

Figure 2. Layout comparison of the DICE hardened cell and standard 6-T cell.

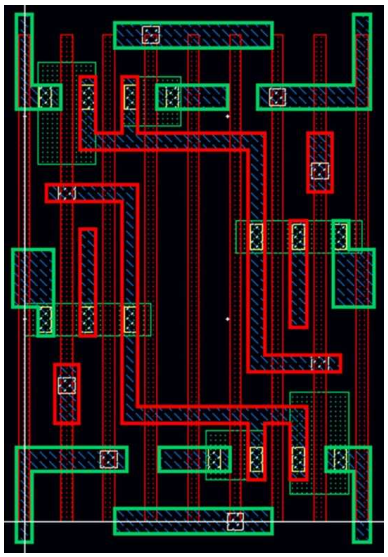

Figure 3. Layout of the 8-T hardened DL.

Configuration hardness techniques such as TMR and ECC created by hardware description language can be employed to verify the effectiveness of error mitigation methods in EBRAM. Thus, four EBRAM modules (Figure 4a) occupying ∼100% resources were configured by FPGA bitstreams and tested synchronously. The key method for TMR is the voter design. For each data line, three AND gates and two OR gates, which are generated by FPGA configuration resources, are the TMR circuits (as shown in Figure 4b). For each bit of the data, there is a TMR module to check. To analyze the worst condition in basic 6-T structure, the adjacent RAM resources were included in the TMR test, which means that an event may disturb more than one cell and make the voter invalid. The ECC logics employ hamming codes

with five more bits for data check [15]. Hence, the ECC encode and decode circuits shown in Figure 4c,d were created. The 8-bit data became 13-bit data due to the 5-bit redundancy check bits. Eventually, the output data could be reconstructed by the ECC decode design to reveal the error information.

Configuration hardness techniques such as TMR and ECC created by Hardware Description Language (HDL) in Prosice can be employed to verify the effectiveness of error mitigation methods in EBRAM. The special bitstreams, including the initialization and configuration of block memory and logical resources, were generated by Prosice with detailed reports for routing and timing conditions. Both the HDL and the tool command languages are supported in Prosice. The resources of device, the HDL input and the constrained conditions are required for each configuration. A compiled visual control and operation interface can be used to control the SEE testing system and it is compatible for Prosice to achieve a series of operation from the FPGA configuration, bitstream selection, and a real-time debugging. Thus, four EBRAM modules (Figure 4a) occupying ∼100% resources were configured by Prosice and tested synchronously. The key method for TMR is the voter design. For each data line, three AND gates and two OR gates, which are generated by FPGA configuration resources, are the TMR circuits (as shown in Figure 4b). For each bit of the data, there is a TMR module to check. To analyze the worst condition in basic 6-T structure, the adjacent RAM resources were included in the TMR test, which means that an event may disturb more than one cell and make the voter invalid. The ECC logics employ hamming codes with five more bits for data check [15]. Hence, the ECC encode and decode circuits shown in Figure 4c,d were created. The 8-bit data became 13-bit data due to the 5-bit redundancy check bits. Eventually, the output data can be reconstructed by the ECC decode design to reveal the error information.

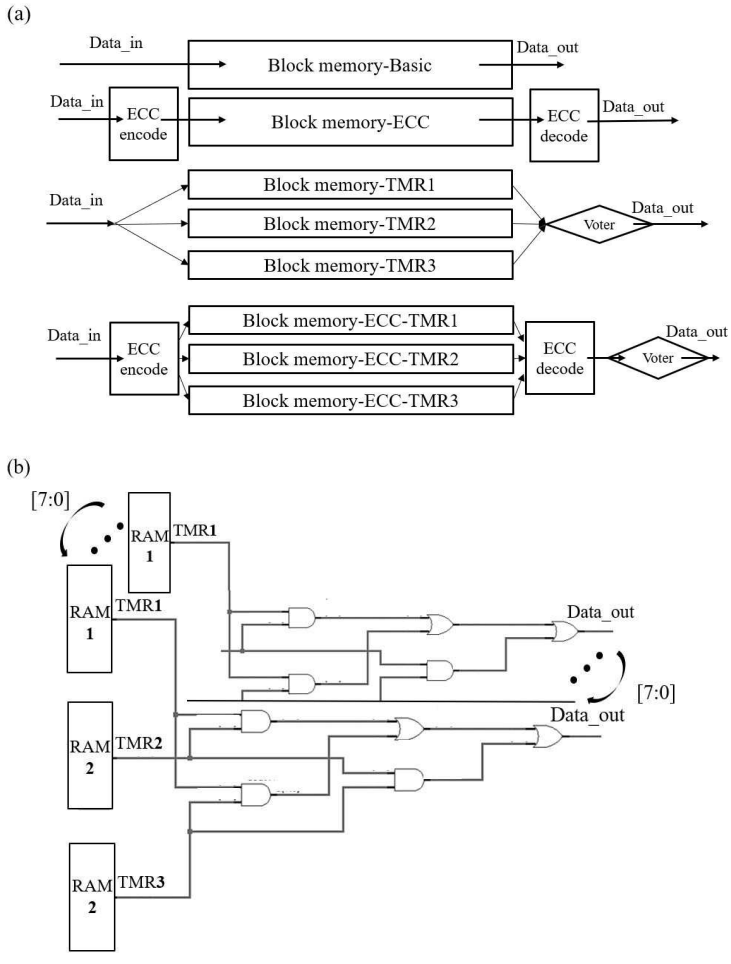

Figure 4. *Cont.*

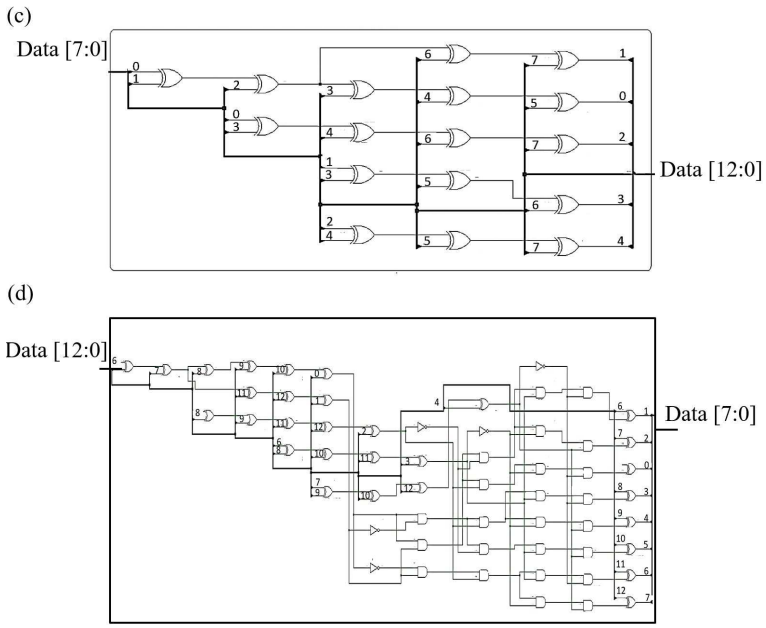

Figure 4. Configured EBRAM: (**a**) the four types of EBRAM; (**b**) the generated 8-channel TMR circuits; (**c**) the generated ECC encode circuits in FPGA; and (**d**) the generated ECC decode circuits in FPGA.

3. Heavy-Ion Test

3.1. Experimental Setup

Heavy ion tests were completed at Heavy Ion Research Facility in Lanzhou (HIRFL) in the Institute of Modern Physics, Chinese Academy of Sciences, and HI-13 Tandem accelerator, China Institute of Atomic Energy. At HIRFL, the tests were carried out in air; and at HI-13 Tandem accelerator, the DUT was located in a vacuum chamber. The type of heavy ions applied for the tests are detailed in Figure 5. To realize a superior accuracy control in LET, for each type of ion, only one energy in high energy region was selected (in the right side of Bragg peak). For each type of heavy ion, its initial energy in DUT surface and the energy in the active layer of DUT (after passing through the thick silicon substrate) are marked in Figure 5. In this study, the LET values in data analysis were all calculated using the ion energy in the active layer.

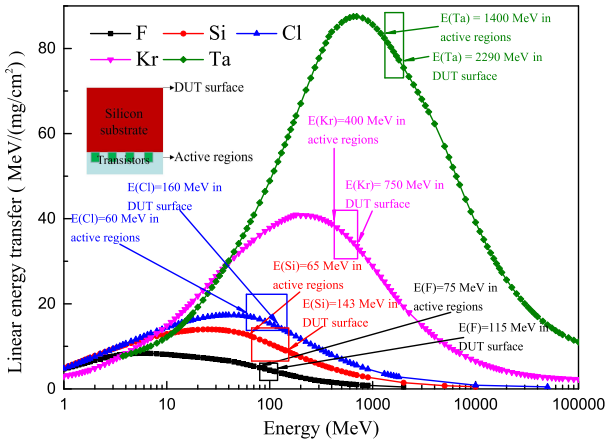

Figure 5. Experimental heavy-ion types and energies.

The DUT was installed on a daughterboard and controlled by a FPGA-based motherboard via digital I/O interface (as shown in Figure 6). The tested resources in DUT, the data configuration, the error data distinction and the communication with Personal Computer (PC) were all completed by the FPGA in the motherboard. During heavy ion irradiation, the upsets (errors) in EBRAM, CRAM, DL and DFF were analyzed automatically by configured FPGA logic and then the error information including the detail of address were recorded and presented on the screen of PC. Besides, the currents in the testing system were monitored and recorded to judge whether there was a latch-up.

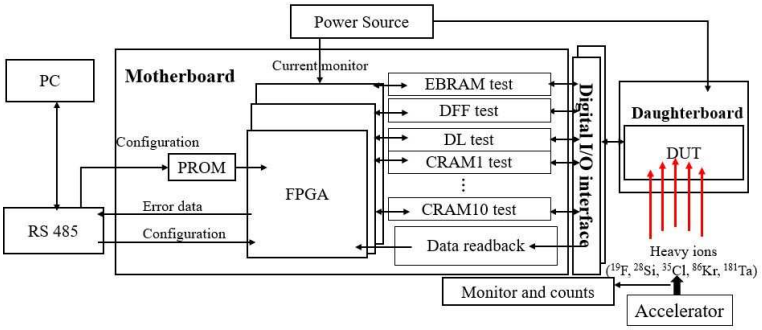

Figure 6. Block diagram of the testing system.

The static mode was employed in tests. The static mode can exclude the influence of the internal address counter SEUs and SET perturbation in peripheral decoding circuit. Considering that the data patterns may influence the SEU cross sections, the checkboard data with "0" and "1" balanced were used in the experiment. For DFFs and EBRAMs, it is easy to design the special bitstream with checkboard data in initialization and then be configured into DUT. However, for configuration modules, plenty of resources have to be used for the whole DUT function, which means the CRAMs cannot be measured at one time. Thus, the CRAMs were divided into ten blocks, with one block for each test to guarantee the function of the DUT.

3.2. Experimental Results

Heavy ion evaluation was focused on the layout hardening and configuration hardening effectiveness. Layout hardening including DICE hardened CRAM, 8-T hardened DL, and double redundant DFF aimed at reducing the SEU sensitivity and system errors, while the configuration hardening was more flexible and applicable to secondarily significant parts such as 6-T EBRAM.

3.2.1. Effectiveness of Layout Hardening

Based on the heavy ion measured upset data, the SEU cross sections could be fitted by Weibull function

$$\sigma_{SEU} = \begin{cases} \sigma_{sat}\left\{1 - exp[-(\frac{LET - LET_{th}}{w})^s]\right\}, & LET \geq LET_{th} \\ 0, & LET \leq LET_{th} \end{cases} \quad (1)$$

where σ_{SEU} (cm^2/bit) indicates the SEU cross-section, σ_{sat} (cm^2/bit) indicates the saturation upset cross-section, LET_th represents the threshold of LET to observe upset errors, s means a dimensionless exponent, and w is a width parameter, as shown in Figure 7. Weibull function is widely used to describe the direct ionization caused by heavy ions, providing great agreement in fitting cross-section thresholds, plateau or limit values. The saturated cross section in EBRAM, DFF, CRAM and DL were 6.2×10^{-8} (cm^2/bit), 8.3×10^{-8} (cm^2/bit), 6.5×10^{-13} (cm^2/bit), and 8.9×10^{-11} (cm^2/bit), respectively, for the diverse layout hardening.

DFFs are radiation sensitive resources in FPGA logical blocks. The cross section results of redundant hardened DFF chains are shown in Figure 7. The tested cross sections were still high (8.3 $\times$ 10^{-8} (cm^2/bit)). SET may affect sensitive parts in peripheral circuits such as the buffers with error transient creation to disturb the initial data in DFF chains. Besides, the checkboard data were used as the input signals of DFF cells in experiments; therefore, one error of the clock path may cause more than one output error of the DFFs, which can increase the cross sections.

The DL module was distinguished from CRAMs that were used in routing and controlling functions. For the DLs, a superior SEU cross section (8.9 $\times$ 10^{-11} (cm^2/bit)) indicates that the 8-T structure with the transient interference excision by two additional transistors (Figure 3) guaranteed its radiation hardening performance. Apparently, the 8-T structure improved its upset threshold and saturated cross section significantly when compared with redundant cell in DFF. More interestingly, the full-DICE protected structure improved CRAM's upset threshold to ~18 MeV/(mg/cm^2). An extremely low SEU saturated cross section at 6.5 $\times$ 10^{-13} (cm^2/bit) was tested by ^{181}Ta irradiation because of the successfully isolated sensitive volumes in CRAM.

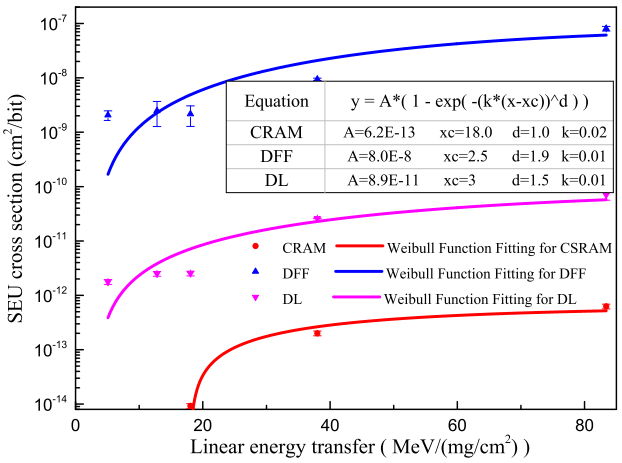

Figure 7. SEU cross section in CRAM, DFF and DL vs. LET.

Additionally, layout hardening declined the Multiple Bits Upset (MBU) significantly. As shown in Figure 8a, Single Bit Upset (SBU) takes high proportion in DICE hardened CRAM. Three-bit or more upsets did not appear during the whole irradiation test. However, in 6-T cell, MBU accounted for a large proportion (54.5%) and four-bit or even five-bit upsets in the unhardened cells were more than 10% (Figure 8b).

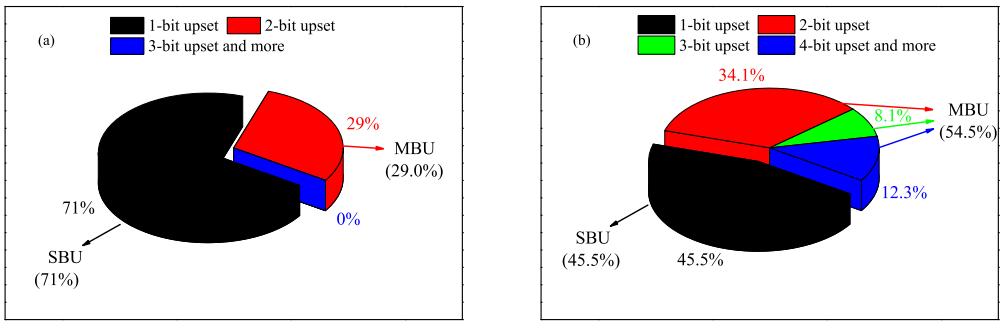

Figure 8. Proportion of SBU and MBU in: (**a**) DICE hardened structure; and (**b**) 6-T structure.

3.2.2. Effectiveness of Configuration Hardening

For the advanced 65 nm CMOS-based EBRAM cells, SEU critical charge declined significantly when compared with sub-micron devices, making the unhardened unit more sensitive to heavy ion irradiation [9,10]. In addition, the carriers created by ionized ions could deposit enough energy in more than one drain regions of off-state MOSFETs in the vicinity, leading to a large MBU rate and high SEU cross section.

Three hardening techniques, namely 8 + 5 ECC codes, TMR and ECC codes plus TMR, were used to evaluate the effectiveness of soft error mitigation. As shown in Figure 9,the ECC codes plus TMR had the lowest upset rates. Even in ^{181}Ta irradiation, the cross section was just 8.5 $\times$ 10^{-9} (cm^2/bit), declined ~86.3% when compared with the unhardened one. Merely ECC or TMR method in EBRAM played a minor role in upset error correction, although they were area and resources consuming. The results matched the high MBU rates in basic 6-T cells presented in Figure 8, leading the separated fault tolerance method (ECC or TMR) becoming invalid.

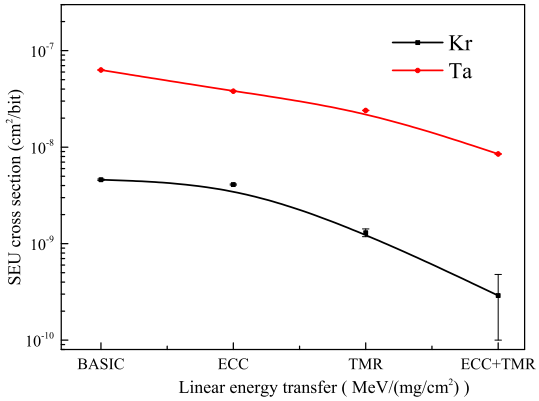

Figure 9. SEU cross section in four kinds of configured EBRAM vs. LET.

4. SEU Rates Prediction

In near-Earth interplanetary or GEO orbit, heavy ions in cosmic ray and solar ray dominate the total SEU rates by direct ionization to produce carriers in the vicinity of transistors' sensitive regions and then lead to SEU phenomenon. The SEU rates induced by heavy-ion direct ionization in space can be calculated by Creme 96 HUP tool [16]. The flux vs. kinetic energy curves of variety of particles under four different radiation environments in GEO were achieved, as shown in Figure 10, through the Creme 96 HUP tool. Then, we obtained the flux distribution vs. LET (Figure 11) with 3 mm aluminum shielding, which is normal for space application. For the calculation of SEU probability (P_{SEU} (/bit/day)), we used P (E_{th}/MeV) to characterize the probability. If the deposited ionization energy of a particle through the track was higher than the energy threshold (E_{th}/MeV) of upset, then an upset was considered to have occurred. For an incident ion, the probability to get an upset is [14,16,17]:

$$P_{SEU} = \frac{1}{\phi_0}\frac{d_\phi}{d(LET)}(LET)\times P(E_{th}) \quad (2)$$

Bradford et al. contributed by expressing the total SEU rates (N) by LET and length, which could also be extended to a statistical result of particle events [18]. Thus, the effective LET spectrum can be integrated with the σ_{SEU} and σ_{sat}. If the surface area S (cm^2) of sensitive volume was determined, a simple formula can be transformed to [14,16,17,19]:

$$N = \frac{s}{4\times\sigma_{sat}}\int_{LET_{min}}^{LET_{max}}\frac{d_\phi}{d(LET)}|_{eff}\sigma_{SEU}\cdot d(LET) \quad (3)$$

where $\frac{d_\phi}{d(LET)}$ is a differential LET spectrum and the LET_max as the maximal LET value of the incident particles is 10^5 MeV/(mg/cm^2), as shown in Figure 11.

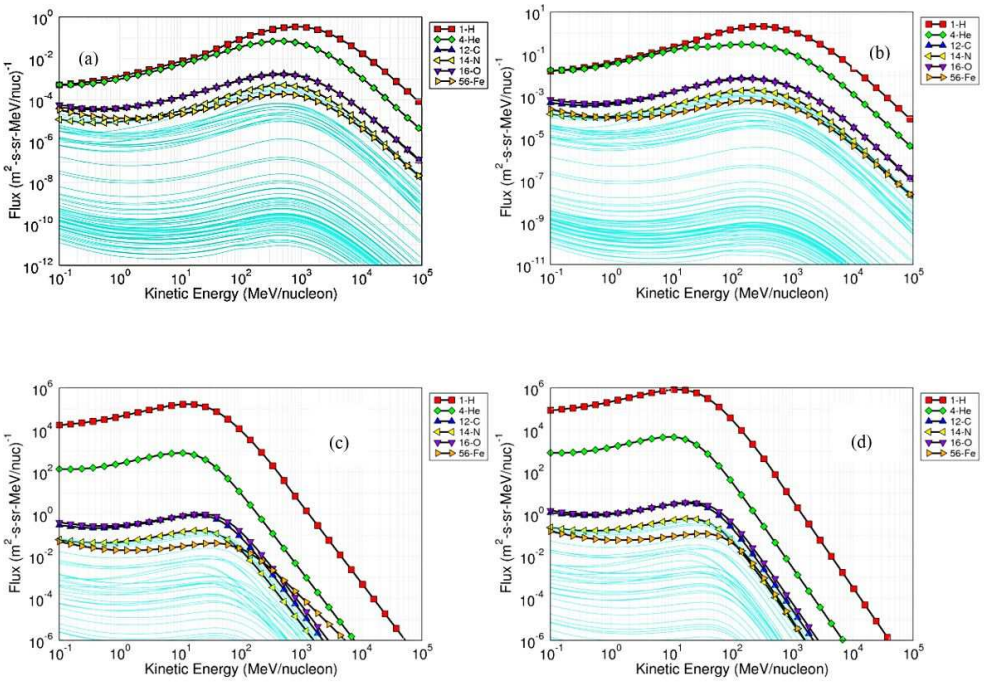

Figure 10. Creme results in GEO: (**a**) cosmic ray min; (**b**) cosmic ray max; (**c**) worst week; and (**d**) worst day.

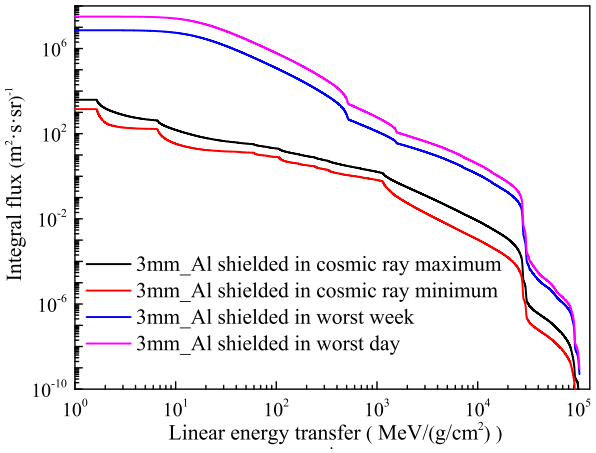

Figure 11. Integral flux behind 3 mm of aluminum in GEO environment.

The SEU rates were calculated and normalized to per bit per day by Creme tools. As shown in Figure 12, CRAM had strong radiation tolerance (8.46×10^{-15}/day/bit) in worst week, even in extremely cruel radiation environments. EBRAM and DFF had upset rates of $\sim 10^{-8}$/bit/day in cosmic ray minimum and maximum periods. Although the rate was many orders of magnitude higher than CRAM, it was still a quite low rate when compared with the results in [7,8]. The calculation results reveal that, even in worst-week radiation condition, only several errors occurred per day per device for EBRAM and lower errors in DFF.

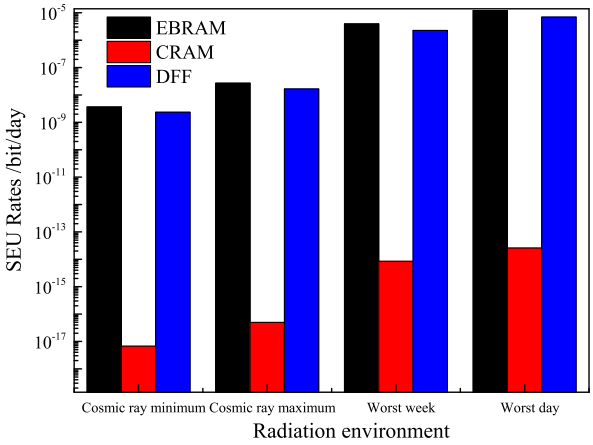

Figure 12. Creme results: SEU rates in isotropic GEO environment behind 3 mm aluminum shielding.

5. Discussion

The special radiation hardening designed circuits in our SRAM-based FPGAs including CRAMs, DLs, EBRAMs and DFFs were manufactured and evaluated. The radiation-hardened DUT and the testing details were all developed to realize the convincible SEU evaluation in large circuit system. All of the hardening information is presented and compared in the previous sections. Next, more details about the purposes of design and the relations between the effectiveness of tradeoff strategy and the actual requirements in space are discussed.

5.1. Radiation Hardening Design

According to the importance on FPGA function, several different hardening techniques are employed in different modules in DUT. The most important part of the FPGA is CRAMs. The upsets in CRAMs contribute the most serious influence to the FPGA system work because routing and logical resources existing in CRAMs are key to FPGA system functions; besides, CRAMs are irradiation sensitive and may cause serious consequent system errors. The errors in CRAMs can be classified into logic block errors and switch box errors. For logic blocks, errors may disturb or change the combinational functions, the multiplexer results, the polarity of reset signal or clock path for DFFs [20]. In switch resources, the open circuit, short circuit or short/open circuit errors may lead to permanent effects with single, multiple or even consequent system errors until the rewritten operation can be carried out. Therefore, the DICE circuit, which costs two times area and power of unhardened CRAM cell, was employed to harden the CRAMs. As shown in Figure 7, the hardened CRAMs had SEU saturation cross section at 6.5×10^{-13} (cm^2/bit). For similar 65 nm space grade SRAM-based FPGA reported in [21], the saturated SEU cross section is $\sim 3 \times 10^{-8}$ (cm^2/bit) for the hardened RAMs. In [7,8], the SEU saturation cross section is only $\sim 6 \times 10^{-8}$ (cm^2/bit) for the configuration cells in 90 nm space grade SRAM-based FPGAs. This means that the SEU data of hardened CRAMs in DUT is 5 orders of magnitude lower than the state-of-the-art space grade SRAM-based FPGAs employing similar CMOS technologies.

Compared with CRAMs, the upset in DFF seems not so critical [8]. For DFFs, not only the heavy ion irradiation but also the CRAM errors or transient pulses can cause upsets. Double redundancy technique was applied for DFF cells and reset control signal ports. The hardened DFFs in DUT had saturation cross section at 8.3×10^{-8} (cm^2/bit), which was almost one order lower than the saturated values at 7.5×10^{-7} (cm^2/bit) and 6.1×10^{-7} (cm^2/bit) of 90 nm radiation hardened FPGAs in [8].

Errors in EBRAM can be mitigated with various methods, which are not suitable for CRAMs and DFFs. EBRAMs are similar to commercial SRAMs, storing the information from users. Thus, some soft error mitigation methods used in general SRAMs such as ECC code and TMR structure with dynamic

scrubbing can be replicated in the case of EBRAM. Besides, some soft error mitigation IPs are provided by Electronic Design Automation (EDA) memory generator tools in FPGA configuration procedure having ECC function with Hamming code in a constrained bit width, which can be used easily to decline upsets in EBRAM. These methods are suitable to be used in memory modules to mitigate upset-induced soft errors, making the additional time and area consuming design in layout seems unnecessary.

Besides, the designed 65 nm SRAM-based FPGA had more sufficient resources than other reported devices. The ∼8 Mbit EBRAMs in DUT were larger than the same module (<∼6.2 Mbi) for FPGAs in [7], which provides more flexible usages and more sufficient data redundancy. The ∼20 Mbit CRAMs in DUT had very high radiation resistance (1.69×10^{-7} upset/device/day in worst-week condition in GEO), while the error rate for similar 90 nm hardened FPGA under typical solar conditions in GEO is only ∼4 upset/device/day [7]. Although higher radiation tolerances were expected, the overall hardened strategies should depend on the device's importance, upset mechanism, area overhead, performance and the actual radiation tolerant needs in on-orbit missions.

5.2. Convincible Prediction and Perspectives

The drains of the off-state transistors were considered to be the sensitive volumes of memory cells [22]. The spacing of sensitive volume was referred to drain to drain distance in the layout of FPGA in order to get credible results. Based on the accurate curve-fitting results in LET thresholds and saturation cross section, the upset rates we predicted are convincible.

The on-orbit SEU rates can affect the operation security in aircraft and spacecraft systems, although high-speed scrubbing is an essential mitigation technique. However, scrubbing is a time and power consuming method and its frequency must depend on the dynamic changed particle flux and the upset cross-section of device, and the particle flux mainly comprised by the continuous changed cosmic-ray and solar wind was hard to ascertain. After the successful use of radiation hardened techniques in DUT, an extremely low event rate under continuous working conditions was obtained, which was more serious than actual intermittent working modes, indicating an excellent hardening result. Furthermore, the reasonable and effective radiation hardened method used in DUT can be further guided to 28 nm or smaller radiation hardened integrated circuit to enrich the family of urgently needed space-grade devices.

6. Conclusions

In this paper, we present a proper utilization of radiation hardened techniques for SRAM-based FPGA with 65 nm CMOS process. The hardening results are characterized by SEUs of CRAMs, DFFs, DLs and EBRAMs. Both layout hardening techniques including DICE, 8-T, double redundancy, and configuration hardening techniques including ECC and TMR are employed for this FPGA. The heavy-ion results indicate satisfying radiation tolerance, especially for the DICE CRAMs. The convincible low SEU rates for each part of DUT in GEO orbit reported above reveal a good result even without further additional reinforcement. Besides, the heavy ion evaluation results will be also useful for the related CMOS-based integrated circuits.

Author Contributions: Conceptualization, C.C.; methodology, C.C., P.Z. and T.L.; software, D.L. and Z.H.; validation, X.F.; writing—original draft preparation, C.C.; writing—review and editing, X.F., T.L. and L.K.; supervision, J.L.; project administration, and X.F., T.L. and J.L.; funding acquisition, J.L.

Funding: This research was funded by the National Natural Science Foundation of China (No. 11690041, No.11805244 and No.11675233) and the APC was funded by 11805244.

Acknowledgments: The authors concentrate on the research of radiation effects and are devoted to the academic contributions. Thus, they thank the related chip research and development institutes in China for the support of information in DUT design. The DUT and the detail information they provide are very helpful for our research.

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Rose, J.; ElGamal, A.; Sangiovanni-Vincentelli, A. Architecture of Field-Programmable Gate Arrays. *Proc. IEEE* **1993**, *81*, 1013–1029. [CrossRef]
2. Stroud, C.; Nall, J.; Lashinsky, M.; Abramovici, M. Bist-based diagnosis of fpga interconnect. In Proceedings of the International Test Conference, Baltimore, MD, USA, 8–10 October 2002; pp. 618–627. [CrossRef]
3. George, J.; Koga, R.; Swift, G.; Allen, G.; Carmichael, C.; Tseng, C.W. Single Event Upsets in Xilinx Virtex-4 FPGA Devices. In Proceedings of the IEEE Radiation Effects Data Workshop (REDW), Ponte Vedra, FL, USA, 17–21 July 2006; pp. 109–114. [CrossRef]
4. Berg, M.; Poivey, C.; Petrick, D.; Espinosa, D.; Lesea, A.; Label, K.A. Effectiveness of internal versus external SEU scrubbing mitigation strategies in a Xilinx FPGA: Design, test, and analysis. *IEEE Trans. Nucl. Sci.* **2008**, *55*, 2259–2266. [CrossRef]
5. Koga, R.; George, J.; Swift, G.; Yui, C.; Edmonds, L.; Carmichael, C.; Langley, T.; Murray, P.; Lanes, K.; Napier, M. Comparison of Xilinx Virtex-II FPGA SEE sensitivities to protons and heavy ions. *IEEE Trans. Nucl. Sci.* **2004**, *51*, 2825–2833. [CrossRef]
6. Graham, P.; Caffrey, M.; Johnson, D.E.; Rollins, N.; Wirthlin, M. SEU mitigation for half-latches in Xilinx Virtex FPGAs. *IEEE Trans. Nucl. Sci.* **2003**, *50*, 2139–2146, doi:10.1109/TNS.2003.820744. [CrossRef]
7. Gregory, A. Virtex-4QV Static SEU Characterization Summary. In *NASA Electronic Parts and Packaging Program Office of Safety and Mission Assurance*; National Aeronautics and Space Administration: Washington, DC, USA, 2008; pp. 1–15.
8. Swift, G.M.; Allen, G.R.; Tseng, C.W.; Carmichael, C.; Miller, G.; George, J.S. Static Upset Characteristics of the 90 nm Virtex-4QV FPGAs. In Proceedings of the IEEE Radiation Effects Data Workshop (REDW), Tucson, AZ, USA, 14–18 July 2008; pp. 98–105. [CrossRef]
9. Chen, W.; Liu, J.; Ma, X.; Guo, G.; Zhao, Y.; Guo, X.; Luo, Y.; Yao, Z.; Ding, L.; Wang, C.; et al. Research progress of radiation effects mechanisms and experimental techniques in nano-devices. *Chin. Sci. Bull.* **2018**, *63*, 1211–1222. [CrossRef]
10. Liu, T.; Liu, J.; Xi, K.; Zhang, Z.; He, D.; Ye, B.; Yin, Y.; Ji, Q.; Wang, B.; Luo, J.; et al. Heavy Ion Radiation Effects on a 130-nm COTS NVSRAM Under Different Measurement Conditions. *IEEE Trans. Nucl. Sci.* **2018**, *65*, 1119–1126. [CrossRef]
11. Maillard, P.; Hart, M.; Barton, J.; Chang, P.; Welter, M.; Le, R.; Ismail, R.; Crabill, E. Single-event upsets characterization evaluation of Xilinx UltraScale Soft Error Mitigation (SEM IP) Tool. In Proceedings of the IEEE Radiation Effects Data Workshop (REDW), Portland, OR, USA, 11–15 July 2016; pp. 1–4. [CrossRef]
12. Tonfat, J.; Kastensmidt, F.L.; Artola, L.; Hubert, G.; Medina, N.H.; Added, N.; Aguiar, V.A.P.; Aguirre, F.; Macchione, E.L.A.; Silveira, M.A.G. Analyzing the Influence of the Angles of Incidence and Rotation on MBU Events Induced by Low LET Heavy Ions in a 28-nm SRAM-based FPGA. *IEEE Trans. Nucl. Sci.* **2017**, *64*, 2161–2168. [CrossRef]
13. Andrew, M.K.; Timothy, A.W.; Kenneth, B.S.; Michael, J.W. Dynamic SEU Sensitivity of Designs on Two 28-nm SRAM-Based FPGA Architectures. *IEEE Trans. Nucl. Sci.* **2018**, *65*, 280–287. [CrossRef]
14. Inguimbert, C.; Duzellier, S.; Ecoffet, R.; Guibert, L.; Barak, J.; Chabot, M. Using a carbon beam as a probe to extract the thickness of sensitive volumes. *IEEE Trans. Nucl. Sci.* **2000**, *47*, 551–558. [CrossRef]
15. Hamming, R.W. Error detecting and error correcting codes. *Bell Syst. Tech. J.* **1950**, *29*, 147–160. [CrossRef]
16. Sierawski, B.D.; Mendenhall, M.H.; Weller, R.A.; Reed, R.A.; Adams, J.H.; Watts, J.W.; Barghouty, A.F. CREME-MC: A Physics-Based Single Event Effects Tool. In Proceedings of the IEEE Nuclear Science Symposium and Medical Imaging Conference (NSS/MIC), Knoxville, TN, USA, 30 October–6 November 2010; pp. 1258–1261. [CrossRef]
17. Weller, R.A.; Mendenhall, M.H.; Reed, R.A.; Schrimpf, R.D.; Warren, K.M.; Sierawski, B.D.; Massengill, L.W. Monte Carlo Simulation of Single Event Effects. *IEEE Trans. Nucl. Sci.* **2010**, *57*, 1726–1746. [CrossRef]
18. Bradford, J. Geometric Analysis of Soft Errors and Oxide Damage Produced by Heavy Cosmic Rays and Alpha Particles. *IEEE Trans. Nucl. Sci.* **1980**, *27*, 941–947. [CrossRef]
19. Mendenhall, M.; Weller, R. A probability-conserving cross-section biasing mechanism for variance reduction in Monte Carlo particle transport calculations. *Nucl. Instrum. Methods Phys. Res. A* **2011**, *667*, 38–43. [CrossRef]

20. Bellato, M.; Bernardi, P.; Bortolato, D.; Candelori, A.; Ceschia, M.; Paccagnella, A.; Rebaudengo, M.; Reorda, M.S.; Violante, M.; Zambolin, P. Evaluating the effects of SEUs affecting the configuration memory of an SRAM-based FPGA. In Proceedings of the Design, Automation and Test in Europe Conference and Exhibition (DATE), Paris, France, 16–20 February 2004; pp. 584–589. [CrossRef]
21. Gregory, A.; Larry, E.; Chen, W.T.; Gary, S.; Carl, C. Error Detect and Correct Enabled Block Random Access Memory (Block RAM) Within the Xilinx XQR5VFX130. *IEEE Trans. Nucl. Sci.* **2010**, *57*, 3426–3431. [CrossRef]
22. Lei, Z.; Zhang, Z.; En, Y.; Huang, Y. Mechanisms of atmospheric neutron-induced single event upsets in nanometric soi and bulk sram devices based on experiment-verified simulation tool. *Chin. Phys. B* **2018**, *27*, 066105. [CrossRef]