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A 5GS/s 8-bit ADC with Self-Calibration in 0.18 µm SiGe BiCMOS Technology

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Abstract: A 5 GS/s 8-bit analog-to-digital converter (ADC) implemented in 0.18 µm SiGe BiCMOS technology has been demonstrated. The proposed ADC is based on two-channel time-interleaved architecture, and each sub-ADC employs a two-stage cascaded folding and interpolating topology of radix-4. An open loop track-and-hold amplifier with enhanced linearity is designed to meet the dynamic performance requirement. The on-chip self-calibration technique is introduced to compensate the interleaving mismatches between two sub-ADCs. Measurement results show that the spurious free dynamic range (SFDR) stays above 44.8 dB with a peak of 53.52 dB, and the effective number of bits (ENOB) is greater than 5.8 bit with a maximum of 6.97 bit up to 2.5 GS/s. The ADC exhibits a differential nonlinearity (DNL) of -0.31/+0.23 LSB (least significant bit) and an integral nonlinearity (INL) of -0.68/+0.68 LSB, respectively. The chip occupies an area of 3.9 × 3.6 mm^2, consumes a total power of 2.8 W, and achieves a figure of merit (FoM) of 10 pJ/conversion step.

Keywords: folding and interpolating; time-interleaved; analog-to-digital converter; SiGe BiCMOS; self-calibration

1. Introduction

High-speed ADCs with moderate resolution are in high demand for applications such as the radar receiver. Although the flash ADC is known as the simplest and fastest architecture, the resolution is limited since the number of comparators increases exponentially with the number of bits, resulting in unacceptable complexity [1–3]. In pipelined ADC, large latency is inevitable because of the multiple pipeline stages, and this is undesirable for swift response situations. As for successive approximation register (SAR) ADC, which has superior energy efficiency, its speed potential usually requires very advanced technology (e.g. 40 nm or even smaller) because of its primarily digital nature [4–6]. Moreover, the sampling rate of a single SAR ADC is still not very high, so the time-interleaved architecture is often preferred for overcoming the speed limitation. Also, the number of interleaving channels is generally large, which requires a complex calibration process. Evolved from flash and two-step topologies, the folding and interpolating (F&I) architecture has low complexity along with the advantage of high speed and low latency by enabling simultaneous operation of the coarse and fine quantization.

In addition to the design topology, the manufacturing process is also an important consideration for the ADC implementation. Currently, ADCs are predominantly designed in a CMOS process. In fact, compared with metal-oxide-semiconductor field-effect transistor (MOSFET), silicon-germanium (SiGe)

heterojunction bipolar transistors (HBT) possess higher transit frequency and superior matching property [7]. In addition, due to its reliability in extreme environmental conditions and inherent tolerance to irradiation effects, it is suitable for special applications such as space exploration [8–10]. With the rapid development of semiconductor integrated circuits, BiCMOS technology can offer the synthesis of low power excellence of CMOS and low distortion capability of HBT [11,12], facilitating the design of high-performance ADCs. Besides, the 0.18 µm SiGe BiCMOS technology is cost efficient and beneficial for special applications in low-volume manufacturing. In general, according to application requirements and cost considerations, the F&I ADC based on SiGe BiCMOS technology is an attractive choice.

In this paper, a prototype of a two-channel time-interleaved 5 GS/s 8-bit F&I ADC fabricated in 0.18 µm SiGe BiCMOS technology has been demonstrated. An open loop track-and-hold amplifier with enhanced linearity is designed to meet the dynamic specifications. The two-stage cascaded folding and interpolating structure of radix-4 is adopted, which makes use of the inherent relationship between folding operation and quantization process to get the most significant bits (MSBs) in parallel with the LSBs digitization, eliminating the traditional coarse quantization stage and requiring less hardware overhead. The self-calibration module is embedded inside the chip and proven to be very effective in reducing the inter-channel mismatches.

The outline of this paper is organized as follows. Section 2 describes the system architecture of the ADC, Section 3 discusses the design details and critical considerations of the key blocks, and Section 4 presents the self-calibration technique. Measurement results are illustrated in Section 5, and the conclusion is drawn in Section 6.

2. Proposed Architecture

The proposed ADC is based on two-channel time-interleaved architecture, and each sub-ADC adopts a two-stage cascaded folding and interpolating topology of radix-4, that is, both the folding factor (FF) and interpolating factor (IF) are equal to 4, as shown in Figure 1.

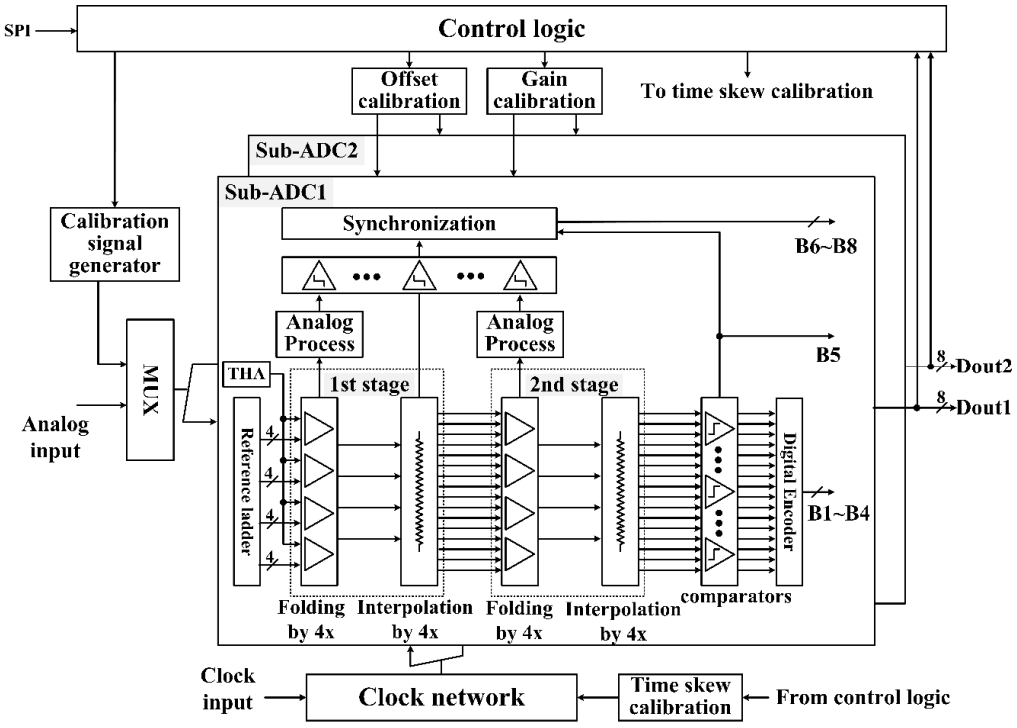


Figure 1. The block diagram of the analog-to-digital converter (ADC).

The ADC supports three operating modes, including a single-channel mode in which two identical sub-ADCs work in an interleaving manner with an equivalent sampling frequency of 5 GS/s, a dual-channel mode with two sub-ADCs that run independently at 2.5 GS/s, and a self-calibration mode for compensating the inter-channel mismatches automatically on-chip.

The control logic module can be accessed through the serial peripheral interface (SPI), offering flexible configurations of ADC operation. The calibration signal generator is integrated into the chip to provide special input signals for calibration purposes, which can effectively reduce the complexity of the calibration algorithm. The input signals or calibration signals can be routed to the ADC by a multiplexer (MUX) as needed.

The radix-4 folding and interpolating curves, as shown in Figure 2, have a natural mapping relationship with the quantization process of ADC, which is essentially binary (that is, radix-2) [13].

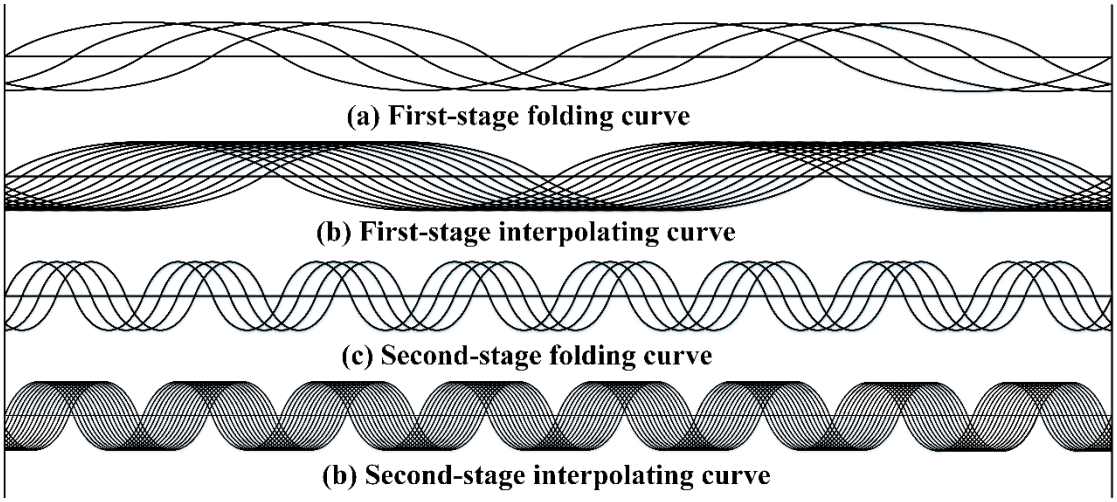


Figure 2. Radix-4 two-stage cascaded folding and interpolating curves.

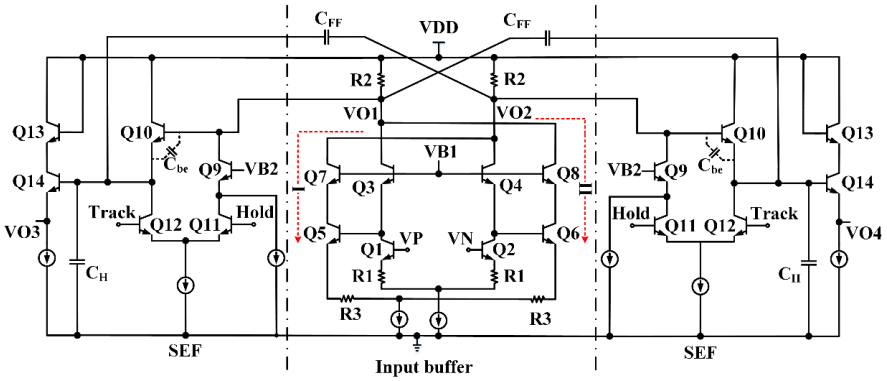
The F&I ADC folds the input signal into several sub-ranges with their zero-crossings corresponding to the reference voltages provided by the reference ladder. In order to reduce the number of folded amplifiers, an interpolating technique is introduced to add new folding curves that are uniformly distributed between adjacent folding curves. After two-stage folding and interpolating, 16 folding curves with FF of 16 are generated, including 256 equally spaced zero-crossings, which actually contain all the information needed for 8-bit quantization.

These 16 folding curves are fed into 16 comparators to translate the analog information into cyclical thermometer codes, which are then converted by the digital encoder to four LSBs (i.e. B1~B4) in binary format. Note that the F&I ADC extracts the information from the location of the comparison thresholds (i.e. zero-crossings) and not from the amplitude of the folding waveform. The quantization curve of the fifth bit resembles the folding curve (FF = 16) generated by the second stage interpolation circuit so that one of the comparison results from the comparators array can be directly used as B5. The situation is the same for B7, whose quantization curve is similar to the folding curve (FF = 4) from the first stage interpolation output. The number of quantization intervals for the eighth and sixth bits is 2 and 8, while the FF of the two-stage radix-4 folding curves is 4 or 16, so there is no direct correspondence between them. Fortunately, they have a common feature that is the power of 2; hence, the intermediate signals produced in the folding and interpolating operation can be transformed by the analog processing units to obtain the desired quantization curves, which are passed through the comparators to get B8 and B6. Besides, B5 is used to synchronize B6~B8. For traditional F&I ADC, the MSBs are resolved using a coarse flash stage in parallel with the LSBs digitization. In this design, the dedicated coarse flash channel is eliminated, and the MSBs are derived from the intermediate signals of the folding process [13].

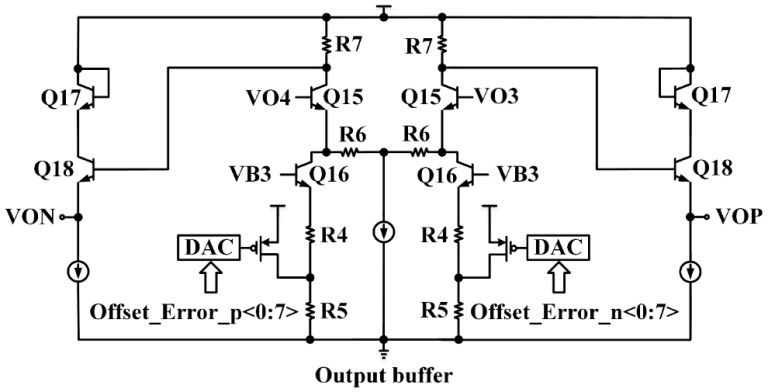
3. Circuit Design

3.1. Track-and-Hold Amplifier

The track-and-hold amplifier (THA) plays an important role in ultra-high-speed F&I ADC, which can alleviate the frequency multiplication effect in the folding process and boost the dynamic performance [14]. The open loop THA consists of an input buffer, switched emitter follower (SEF), and output buffer, as shown in Figure 3.



(**a**)



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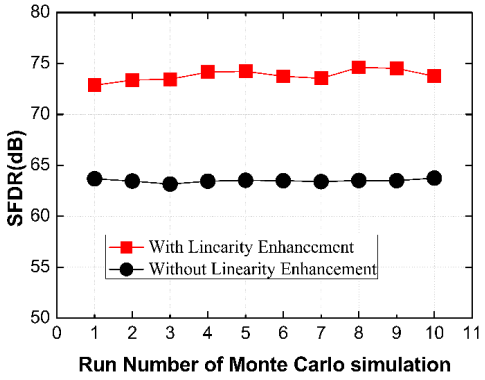


(**c**)

Figure 3. (**a**) Input buffer and switched emitter follower (SEF) in the track-and-hold amplifier (THA); (**b**) Output buffer with offset calibration interface; (**c**) Comparison of linearity enhancement effect.

This input buffer basically behaves as a cascode differential amplifier [15,16], where the emitter degeneration resistor R1 provides local negative feedback to improve linearity. However, the base-emitter voltage V_{be} modulation effect of the input transistors still affects the linearity, so branches I (composed of Q5 and Q7) and II (composed of Q6 and Q8) are added for further linearity compensation. If there are no branches I and II,

$$\begin{array}{c} V_{IN} = VP - VN = 2i \times R_1 + V_{be1} - V_{be1} = 2i \times R_1 + \Delta V_{be} \\ V_{OUT} = VO2 - VO1 = 2i \times R_2 = \frac{R_2}{R_1} \times (V_{IN} - \Delta V_{be}) \end{array} \quad (1)$$

In the above formula, V_{be1} and V_{be2} are the base-emitter voltages of Q1 and Q2, and their difference is ΔV_{be}. The symbol i represents the current variation caused by the change of the input voltage. Evidently, the linearity of V_{OUT} will be degraded by ΔV_{be}. After adding branches I and II, Q5 and Q6 convert ΔV_{be} into relevant current variations, which are superimposed on the output nodes VO1 and VO2 of the input buffer. Taking branch I as an example for analysis:

$$\Delta V_{be} \underset{Q1\ for\ voltage\ amplification}{\rightarrow} -A_V \times \Delta V_{be} \underset{Q5\ for\ current\ conversion}{\rightarrow} -A_V \times \Delta V_{be} \times g_m$$

Herein, A_V represents the voltage amplification factor of Q1, and g_m is the transconductance of Q5, indicating the voltage–current conversion capability.

Branch I converts the ΔV_{be} into current variation, which is equal to -α*ΔV_{be}, where $\alpha = A_V{}^* g_m$. Branch II acts similarly except that its current variation is opposite to that of branch I, that is, $\alpha \times \Delta V_{be}$. Recalculate the output voltage of the input buffer:

$$\begin{array}{l} V_{OUT} = (2i + 2\alpha \times \Delta V_{be}) \times R_2 = \left(\frac{V_{IN} - \Delta V_{be}}{R_1} + 2\alpha \times \Delta V_{be} \right) \times R_2 \\ = \frac{R_2}{R_1} \times V_{IN} + \left(2\alpha - \frac{1}{R_1} \right) \times R_2 \times \Delta V_{be} \end{array} \quad (2)$$

It can be seen that if $2\alpha = 1/R_1$ by appropriate design, the influence of ΔV_{be} on the output linearity can be eliminated. The comparison of the linearity enhancement effect is shown in Figure 3c, and the Monte Carlo simulation results show that the SFDR is improved by about 10 dB with linearity enhancement. Moreover, as a design consideration of the input buffer, some gain is needed to amplify the narrow input swing. In this topology, the output gain is theoretically determined by R2/R1. Compared to the linearity compensation technique with the diode-type load placed in series on the signal path [17], this structure adds two parallel branches to counteract the modulation effect of V_{be} without impairing the signal margin, relaxing the requirements for the power supply voltage.

The SEF is located behind the input buffer and acts as a current switch that controls the current conduction path through the clock signals "Track" and "Hold" to realize signal sampling. The feedforward capacitor C_{FF} is employed to cancel the feed-through effect caused by the parasitic base-emitter junction capacitance C_{be} in the holding phase [18].

The output buffer, as shown in Figure 3b, isolates the sampling capacitor C_H from the subsequent circuits, and also ensures sufficient driving ability and bandwidth. In addition, the calibration ports, named "Offset_Error_p" and "Offset_Error_n" are reserved for adjusting the output of THA to reduce the offset error. The specific calibration method will be described in detail later.

3.2. Folding and Interpolating Circuits

Following the THA, the folding circuits serve to amplify the small voltage difference between the input signal and reference voltages [19] and map the quantization intervals to a segmented folding curve with the reference voltages as zero-crossing points. The first stage folding amplifier incorporates four differential pairs with adjacent collectors connected, as shown in Figure 4.

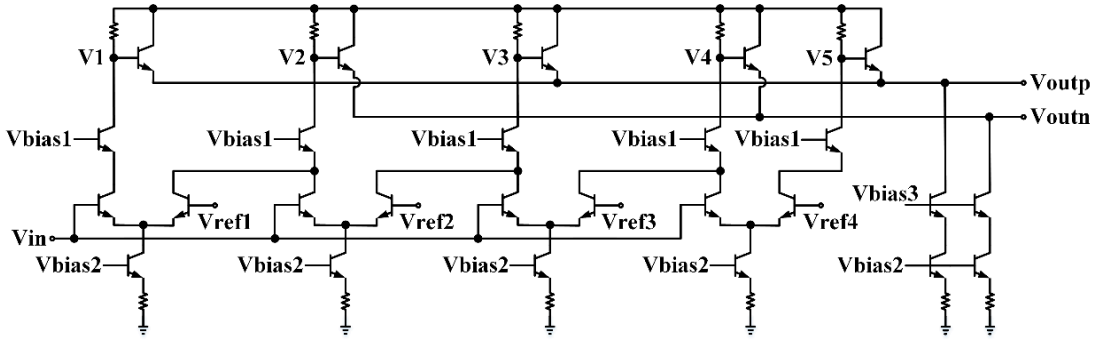
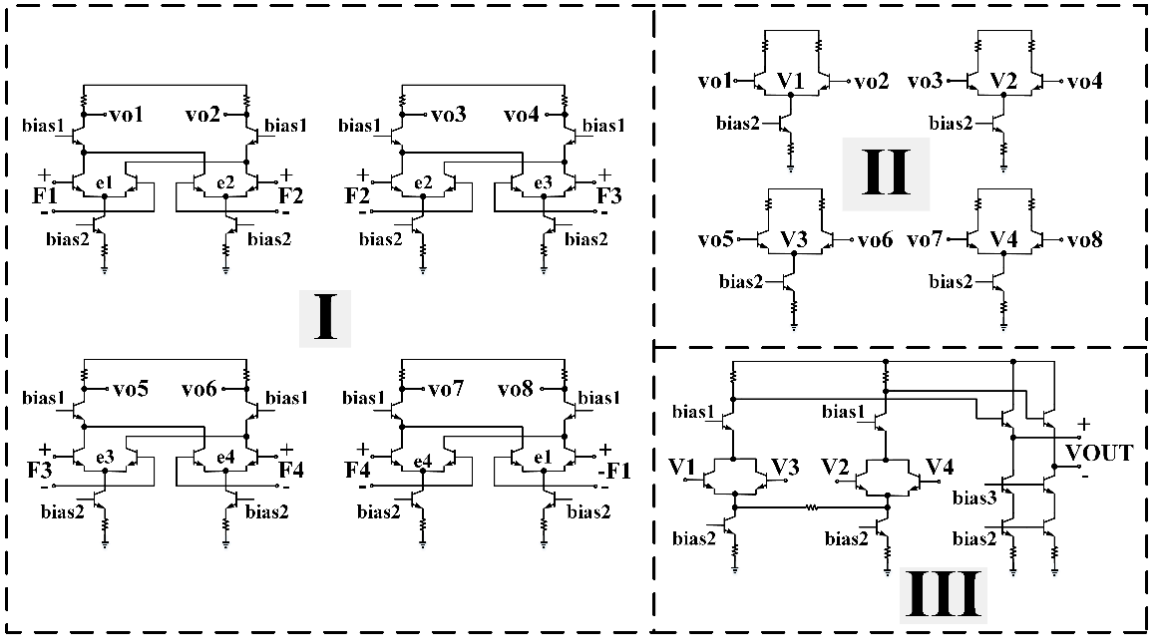


Figure 4. The folding amplifier in the first stage.

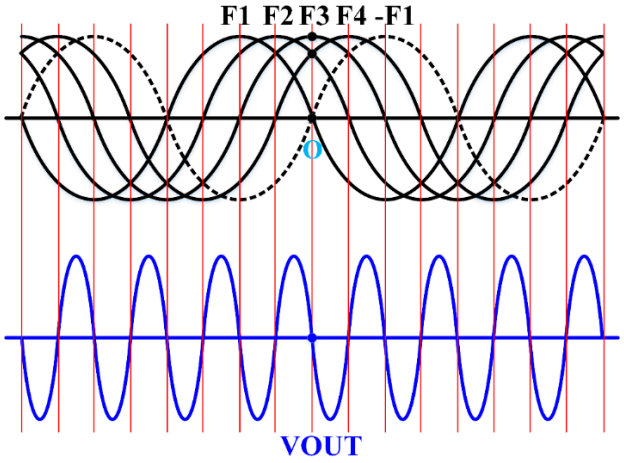
The internal voltages V1, V3, and V5 are combined by emitter followers, which perform analog "wire-OR" function [20,21], and operation is the same for another set of signals V2 and V4. Finally, a differential folding signal with zero-crossings Vref1~Vref4 is obtained. Besides, V1~V5 are preserved as intermediate signals for further processing to get MSBs. Compared to the conventional "wire-AND" topology where all the outputs of differential pairs are alternatively joined together, this kind of folding amplifier has a much wider bandwidth because the collector parasitic capacitors are not accumulated at the output node [22]. The actual first folding stage comprises four such modules, yielding four primary folding curves of FF = 4, as shown in Figure 2a.

The second stage folding amplifier is used to further increase the folding factor, and its circuit is shown in Figure 5a.



(**a**)

Figure 5. *Cont.*



(**b**)

Figure 5. (**a**) The folding amplifier in the second stage; (**b**) The input and output signals.

F1~F4 are folding curves from the first stage, and -F1 is the reverse version of F1. The core of part I is a subtraction circuit for amplifying the difference between adjacent differential signals. Then, the differences are detected by part II with the function of "OR," and all values are combined into a differential output by "NOR" operation in part III. In fact, it is the zero-crossings that carry the quantization information in folding curves, so the focus is on the transformation of zero-crossings proceeding along the signal processing chain. As shown in Figure 5b, a zero-crossing marked as "O" in F1 is taken as a case study. At this point, both F1 and -F1 are zero and F2 = F4. F1-F2 and F4-(-F1) have the same amplitude and opposite phase, so vo1 = vo8 and vo2 = vo7 in part I, making V1 = V4 in part II. Similarly, V2 = V3. Finally, VOUT = 0 in part III, meaning that a zero-crossing of F1 has been transformed into a zero-crossing of the output signal. Likewise, all the zero-crossings of F1~F4 are mapped to the zero-crossings of VOUT one by one, thus realizing the intention of combining the characteristic information of four folding curves into one folding curve. Compared with the solution based on a Gilbert-type multiplier [23,24], this novel structure has fewer transistors stacked on the signal path and larger voltage headroom, beneficial for improving the output voltage swing and optimizing the bias conditions of the transistors. There are four such folding amplifiers in the second stage, absorbing 16 folding curves of FF = 4 from the first stage, and generating four folding curves of FF = 16, as shown in Figure 2c.

Interpolation is used along with folding to generate extra quantization levels between every two neighboring reference voltages, further reducing the number of the folding amplifiers. A resistive interpolation circuit is chosen due to its simplicity and efficiency [25]. The resulting curves from the first and second stage interpolation are shown in Figure 2b,d, respectively.

4. Self-Calibration Technique

Due to the random mismatch, process variation and design deviation, time-interleaved ADC suffers from offset, gain, and time skew errors between sub-channels. Therefore, calibration is necessary to compensate for these interleaving errors. The on-chip self-calibration method is used with the calibration logic built in the chip, and the whole calibration procedure is automatic without the need for externally applied calibration vectors, making the chip application more convenient.

During the calibration process, the ADC outputs are processed in the digital domain, and the error information is extracted based on statistical estimation, then converted to analog signal by digital-to-analog converter (DAC) and fed back to the internal blocks of the ADC to adjust their operation states in the analog domain. This process forms a negative feedback loop to compensate for the errors iteratively, which is repeated until the error value converges to an acceptable range.

Since the offset and gain mismatches are static errors, their corrections are straightforward and simple, and they can be estimated by giving DC reference voltage to the input of the ADC during the calibration period [26]. In contrast, the time skew mismatch is relatively difficult to correct because the skew-induced error is dependent on signal content [6,27].

For the offset calibration, zero voltage is applied to all sub-ADCs [28]. Theoretically, the zero-level input of ADC corresponds to the median of the output digital codes (that is 127.5 for 8-bit ADC). The actual output digital codes of ADC are subtracted by 127.5, and then the difference is accumulated and averaged (ACC&AVG) to obtain the offset error, as indicated in Figure 6. The calculations involved in this error extraction only consist of simple subtraction operations in combination with averaging, enabling a small and efficient on-chip digital calibration engine instead of a complex software approach [29].

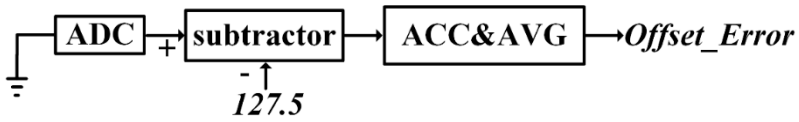


Figure 6. Offset error extraction diagram.

The extracted offset error is converted into an analog signal by an 8-bit current-steering DAC to adjust the bias setting of the THA output buffer, as shown in Figure 3b.

The gain error calibration follows as the offset calibration is completed. A reference voltage V_{gain_cal} with a fixed DC value is applied to all sub-ADCs [28]. In the ideal case without gain error, a deterministic output digital code labeled C_{ref} is generated and stored as a default reference code. In fact, due to the influence of gain error, ADC may produce a different digital code, which is subtracted by C_{ref}. Then, the difference is accumulated and averaged to obtain the gain error, as shown in Figure 7.

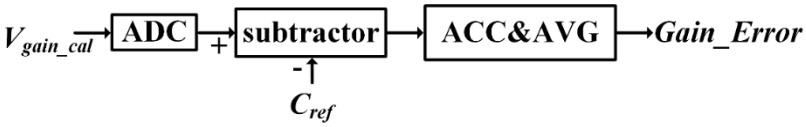


Figure 7. Gain error extraction diagram.

The calibration object for gain error is the resistive reference ladder with an adjustable current source at the bottom [30]. The gain error is fed back and converted into an analog signal by an 8-bit current-steering DAC to regulate the current source and trim the reference voltages, as shown in Figure 8.

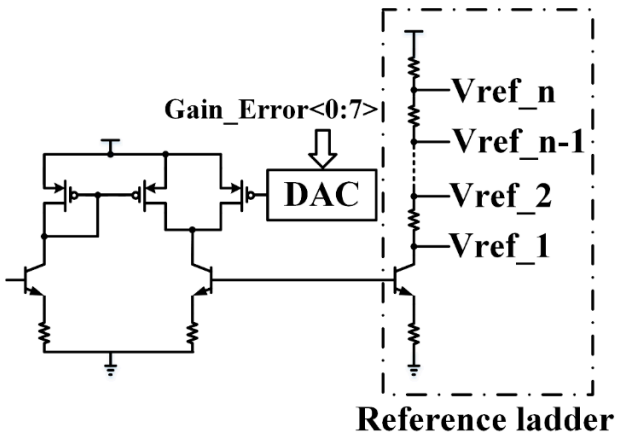


Figure 8. Reference ladder with gain error calibration interface.

The time skew results in the non-uniform sampling of the input signal, which causes sampling errors [31]. The correlation between the quantization results and the sampling time of ADC can be used to estimate the time skew. In the time skew calibration process, a triangular wave serves as the calibration input signal, whose values change linearly with time in the monotonically ascending or descending region. Therefore, the sampling time mismatch can be extracted indirectly based on the statistical information of the quantization results at different sampling instants.

In this design, two sub-ADCs alternately sample the monotonic linear region of the triangular signal in sequence. Assume that the sampling values of sub-ADC1 are S_{t1} and S_{t3}, respectively, corresponding to the sampling instants t1 and t3, while for sub-ADC2, the case is S_{t2} and t2. There are two possibilities for the relationship between sampled values, that is, $S_{t1} < S_{t2} < S_{t3}$ in a monotonically rising region or $S_{t1} > S_{t2} > S_{t3}$ in a monotonically decreasing region, as shown in Figure 9. The sampling time mismatch among channels can be reflected by the difference of $|S_{t3} - S_{t2}|$ and $|S_{t2} - S_{t1}|$. For example, compared with the ideal sampling of $|S_{t2} - S_{t1}| = |S_{t3} - S_{t2}|$, the sampling time of sub-ADC2 is delayed if $|S_{t2} - S_{t1}| > |S_{t3} - S_{t2}|$ or advanced if $|S_{t2} - S_{t1}| < |S_{t3} - S_{t2}|$.

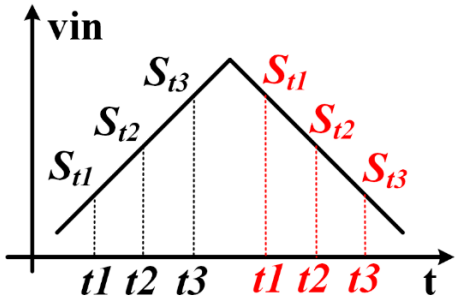


Figure 9. Triangular wave as the calibration input signal.

In the actual calibration process, the output digital codes of the ADC, which are one-to-one mapped with the sampled values, are used as the basis for the time skew information extraction. For example, if sub-ADC2 is taken as the reference channel, the output digital codes of sub-ADC1 minus that of sub-ADC2 and the absolute values of the differences are accumulated and averaged to obtain the time skew between the two channels, as shown in Figure 10.

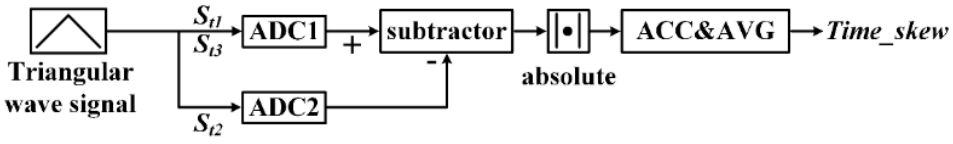
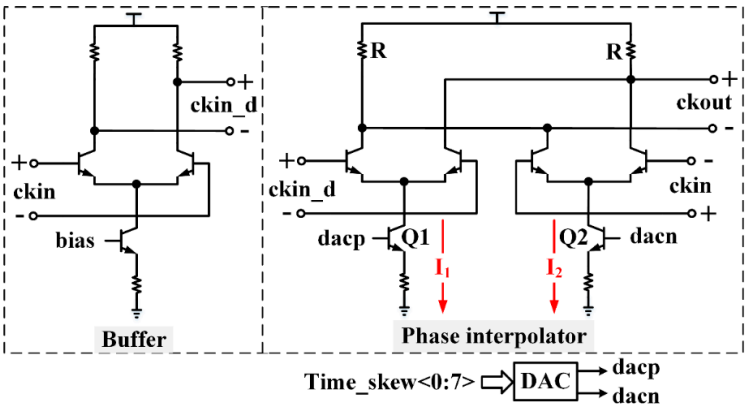
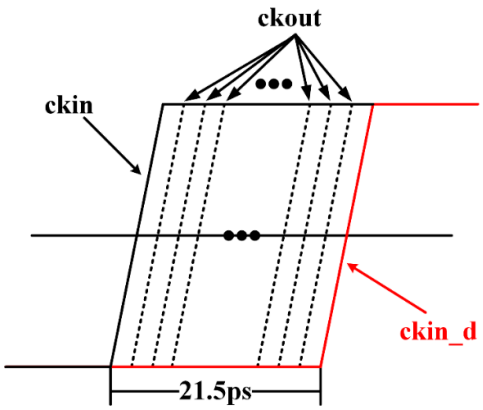


Figure 10. Time skew extraction diagram.

After the time skew is detected, it is converted into analog signals by an 8-bit current-steering DAC, which controls the variable delay cells in the clock network to iteratively adjust the phases of the sampling clocks. The variable delay cell is shown in Figure 11. The sampling clock ckin passes through a buffer to get ckin_d with a relative delay of 21.5 ps, and these two clock signals are input to an analog phase interpolator, which is designed by a pair of differential amplifiers with shared load resistors, acting as a current adder circuit [32]. The delay adjustment is realized by interpolating phase between ckin and ckin_d according to the different weights of the tail currents I1 and I2, which are controlled by an 8-bit current-steering DAC, resulting in a delay adjustment accuracy of $21.5\ \text{ps}/2^8 = 84\ \text{fs/step}$.



(**a**)



(**b**)

Figure 11. (**a**) Variable delay cell for time skew calibration; (**b**) The diagram of phase interpolating.

5. Measured results

The ADC prototype was manufactured in 0.18 µm SiGe BiCMOS technology with a chip size of 3.9 × 3.6 mm^2 (including pads). The micrograph is shown in Figure 12.

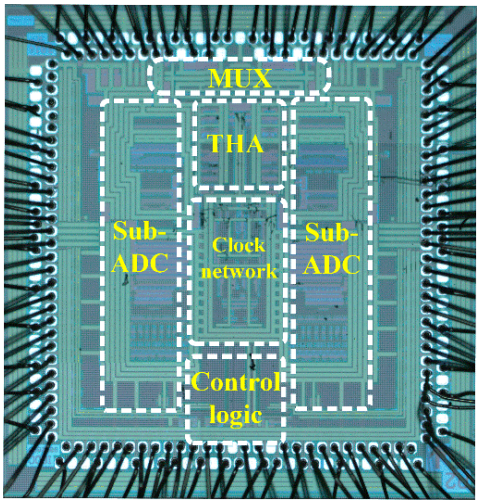


Figure 12. Micrograph of the proposed ADC.

The static performance of DNL and INL is shown in Figure 13. The measured DNL and INL were −0.31/+0.23 LSB and −0.68/+0.68 LSB, respectively.

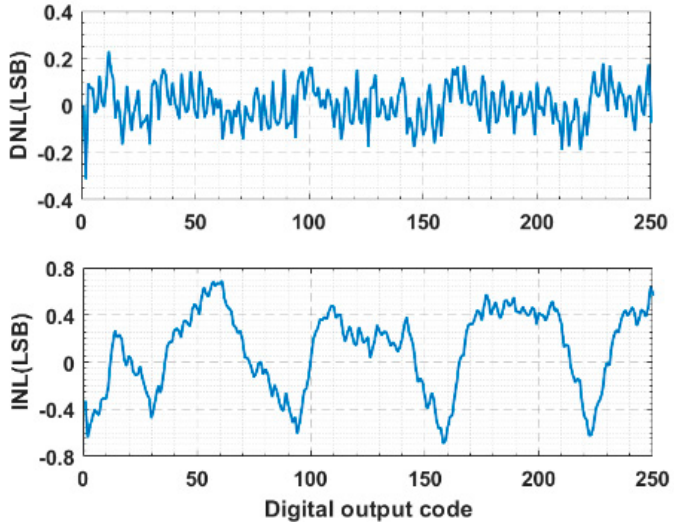
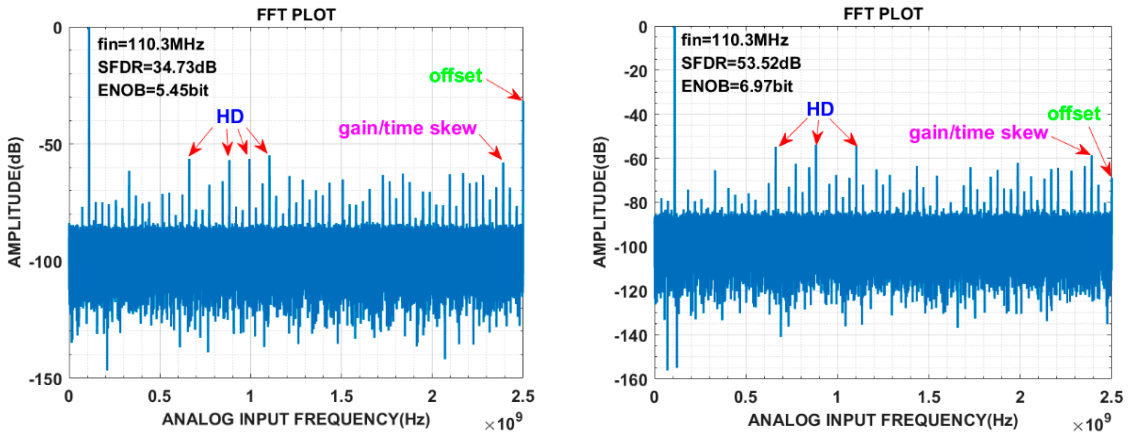


Figure 13. Measured differential nonlinearity (DNL) and integral nonlinearity (INL).

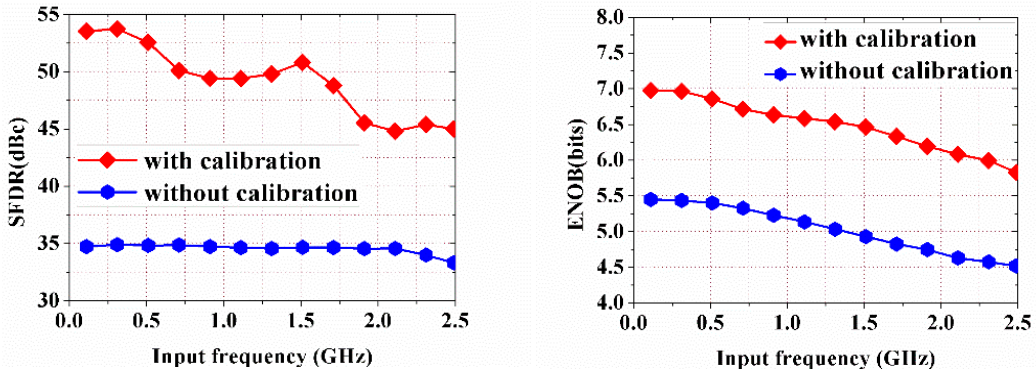
The calibration effectiveness is illustrated in Figure 14, where the output fast Fourier transform (FFT) spectrums before and after calibration at 110.3 MHz input frequency are shown. Before calibration, the ADC performance was limited mainly by the mismatches rather than harmonic distortion (HD). After calibration, the SFDR improved from 34.73 dB to 53.52 dB, and the ENOB from 5.45 bit to 6.97 bit.



(**a**) (**b**)

Figure 14. Output fast Fourier transform (FFT) spectrum (**a**) before calibration; (**b**) after calibration.

Figure 15 shows SFDR and ENOB versus input frequency at 5 GS/s. Without calibration, the ADC performance was not satisfactory. In contrast, the calibrated results reveal that the SFDR improved by more than 10 dB and stayed above 44.8 dB up to 2.5 GHz, and the ENOB improved by at least 1.3 bit and greater than 5.8 bit up to 2.5 GHz.



(**a**) (**b**)

Figure 15. (**a**) Spurious free dynamic range (SFDR) versus input frequency; (**b**) Effective number of bits (ENOB) versus input frequency.

The ADC consumed a total power of 2.8 W and achieved a FoM of 10 pJ/conversion step across the entire first Nyquist zone.

Table 1 gives a performance comparison of ADCs with similar specifications.

Table 1. Comparison of the analog-to-digital converter (ADC) performance.

Parameter	[1]	[8]	[11]	[33]	This work
Technology	0.25 μm SiGe	0.35 μm SiGe	47 GHz SiGe	0.8 μm InP	0.18 μm SiGe
Architecture	F&I	TI F&I	F&I	F&I	TI F&I
Sample frequency (GS/s)	6	4	2	5	5
Resolution (bits)	9.5	8	8	7	8
ENOB (bits) @Nyquist frequency	7.3	5.5	6.2	5.7	5.8
DNL/INL (LSB)	1.2/3.5	0.3/0.8	0.5/1.0	N.A.	0.31/0.68
Core power (W)	10.2	3.0	3	8.4	2.8
FoM (pJ/conv.step) [1]	10.8	16.5	12	32	10
Calibration	no	yes	no	no	yes

[1] FoM = Power/(2^{ENOB} × Sampling frequency).

6. Conclusions

In this paper, a two-channel time-interleaved 5 GS/s 8-bit F&I ADC fabricated in 0.18 μm SiGe BiCMOS technology has been presented. The on-chip self-calibration technique used to reduce the interleaving errors exhibits lower calibration complexity and a good compensation effect. The ADC shows DNL of -0.31/+0.23 LSB and INL of -0.68/+0.68 LSB. The SFDR stays above 44.8 dB with a peak of 53.52 dB, and the ENOB is greater than 5.8 bit with a maximum of 6.97 bit up to Nyquist frequency. The chip consumes 2.8 W, occupies an area of 3.9 × 3.6 mm^2, and realizes a FoM of 10 pJ/conversion step.

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